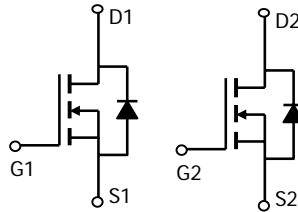
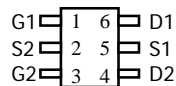



AO6802
Dual N-Channel Enhancement Mode Field Effect Transistor
General Description

The AO6802 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for use as a load switch or in PWM applications. *Standard Product AO6802 is Pb-free (meets ROHS & Sony 259 specifications). AO6802L is a Green Product ordering option. AO6802 and AO6802L are electrically identical.*

Features

$V_{DS} (V) = 30V$
 $I_D = 3.1 A (V_{GS} = 10V)$
 $R_{DS(ON)} < 75m\Omega (V_{GS} = 10V)$
 $R_{DS(ON)} < 115m\Omega (V_{GS} = 4.5V)$

**TSOP6
Top View**

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	$T_A=25^\circ C$	3.1	A
	$T_A=70^\circ C$	2.4	
Pulsed Drain Current ^B	I_{DM}	12	
Power Dissipation ^A	$T_A=25^\circ C$	1.15	W
	$T_A=70^\circ C$	0.73	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics each FET

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	78	110	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	106	
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	64	80	$^\circ C/W$

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	1.9	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	12			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=3.1\text{A}$		54	75	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		78		
		$V_{GS}=4.5\text{V}$, $I_D=2\text{A}$		88	115	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=3.1\text{A}$		4.5		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$		0.79	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		200	240	pF
C_{oss}	Output Capacitance			40		pF
C_{riss}	Reverse Transfer Capacitance			20		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		2.3	3	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $I_D=3.1\text{A}$		6.5	8.5	nC
$Q_g(4.5\text{V})$	Total Gate Charge			3.1	4	nC
Q_{gs}	Gate Source Charge			1.2		nC
Q_{gd}	Gate Drain Charge			1.6		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=15\text{V}$, $R_L=4.7\Omega$, $R_{GEN}=3\Omega$		3.3		ns
t_r	Turn-On Rise Time			2.5		ns
$t_{D(off)}$	Turn-Off DelayTime			13.2		ns
t_f	Turn-Off Fall Time			1.7		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=3.1\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		9.4	12	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=3.1\text{A}$, $di/dt=100\text{A}/\mu\text{s}$		3.5		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

Rev 1 : June 2005

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N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

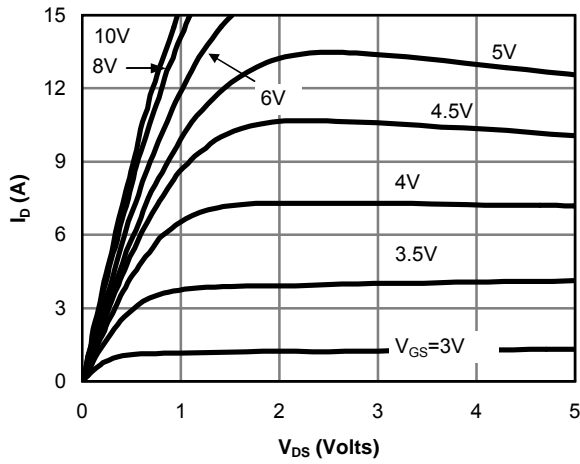


Fig 1: On-Region Characteristics

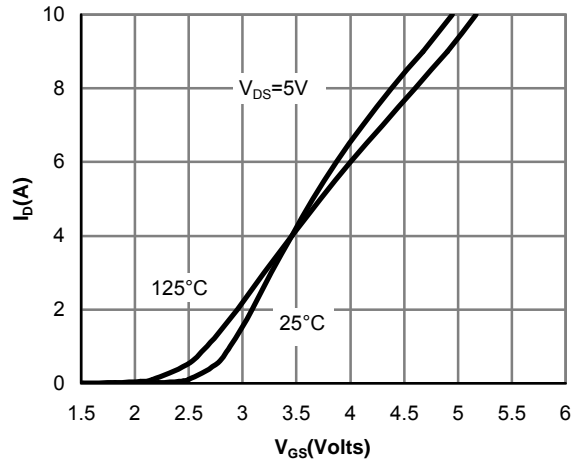


Figure 2: Transfer Characteristics

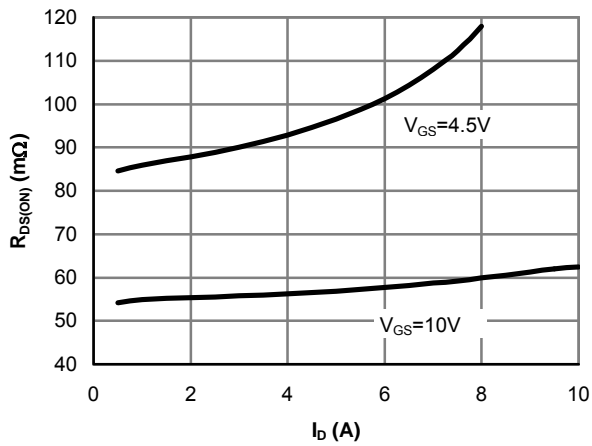


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

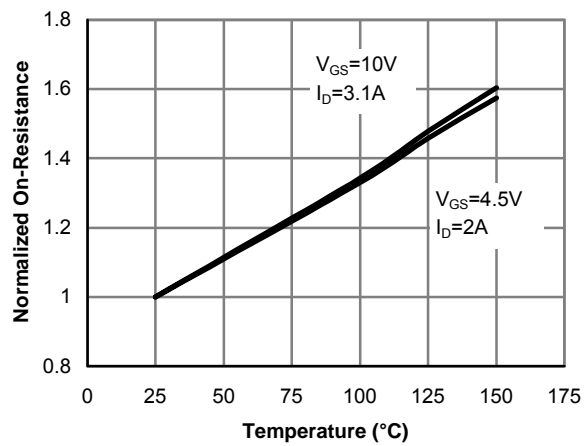


Figure 4: On-Resistance vs. Junction Temperature

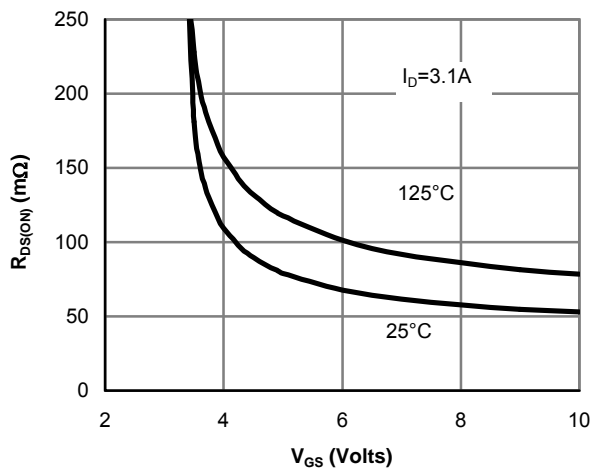


Figure 5: On-Resistance vs. Gate-Source Voltage

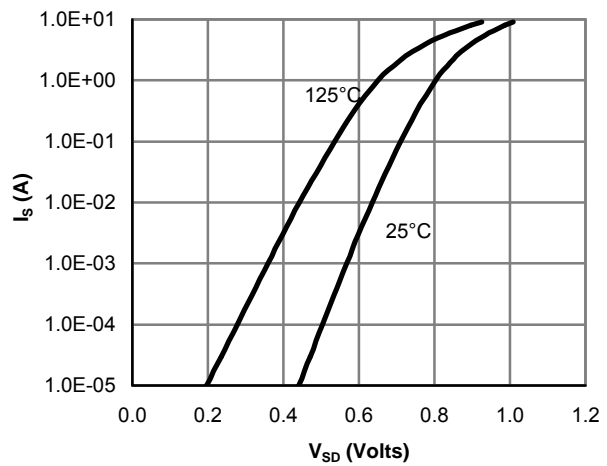


Figure 6: Body-Diode Characteristics

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

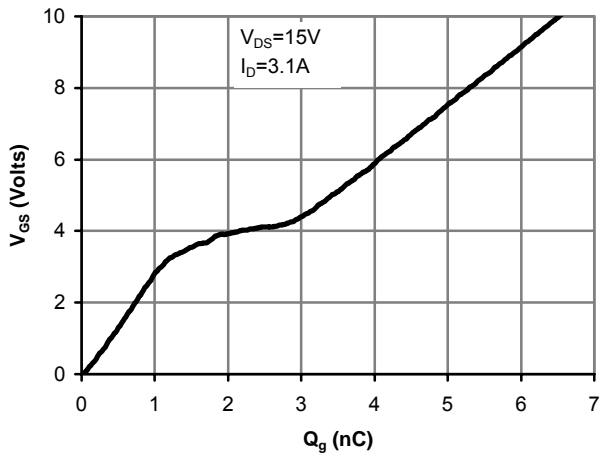


Figure 7: Gate-Charge Characteristics

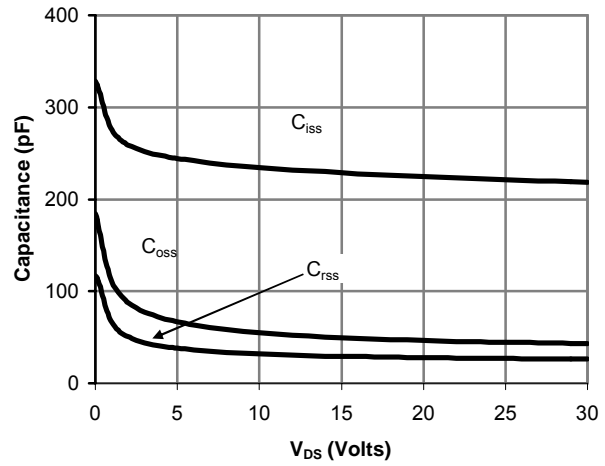


Figure 8: Capacitance Characteristics

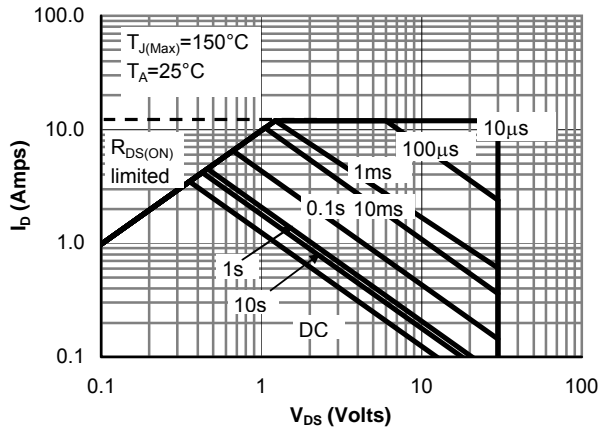


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

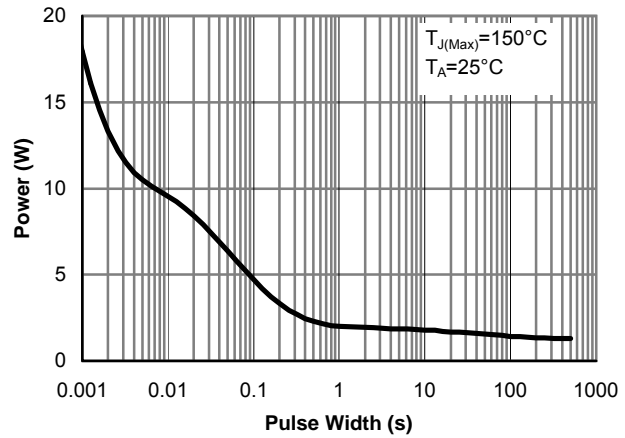


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

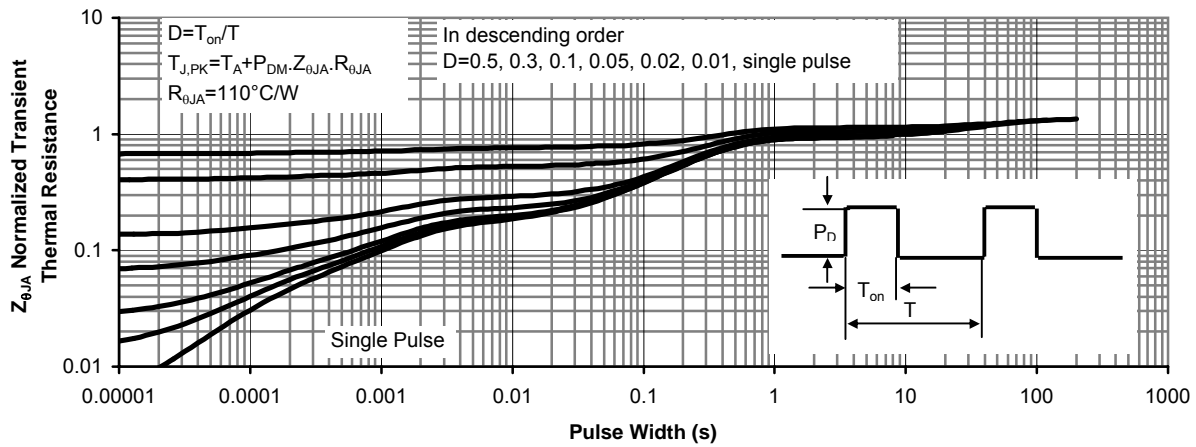


Figure 11: Normalized Maximum Transient Thermal Impedance