

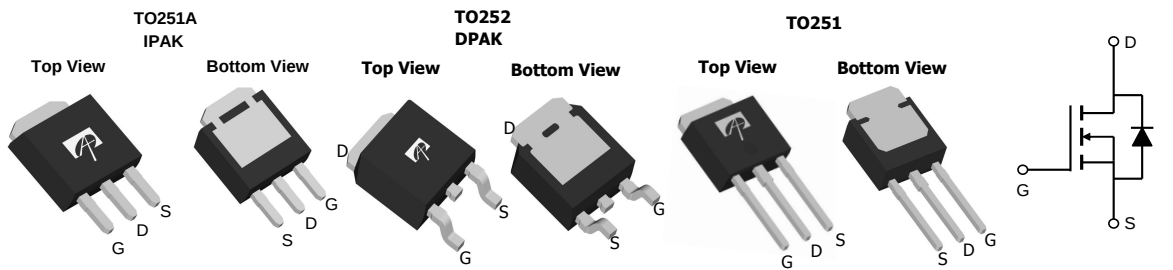
#### General Description

The AOD4144/AOI4144/AOU4144 is fabricated with SDMOS™ trench technology that combines excellent  $R_{DS(ON)}$  with low gate charge and low  $Q_{rr}$ . The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

#### Product Summary

|                                    |        |
|------------------------------------|--------|
| $V_{DS}$                           | 30V    |
| $I_D$ (at $V_{GS}=10V$ )           | 55A    |
| $R_{DS(ON)}$ (at $V_{GS}=10V$ )    | < 8mΩ  |
| $R_{DS(ON)}$ (at $V_{GS} = 4.5V$ ) | < 14mΩ |

100% UIS Tested  
 100%  $R_g$  Tested



#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter                                      | Symbol                  | Maximum    | Units            |
|------------------------------------------------|-------------------------|------------|------------------|
| Drain-Source Voltage                           | $V_{DS}$                | 30         | V                |
| Gate-Source Voltage                            | $V_{GS}$                | $\pm 20$   | V                |
| Continuous Drain Current <sup>G</sup>          | $T_C=25^\circ\text{C}$  | 55         | A                |
|                                                | $T_C=100^\circ\text{C}$ | 42         |                  |
| Pulsed Drain Current <sup>C</sup>              | $I_{DM}$                | 110        |                  |
| Continuous Drain Current                       | $T_A=25^\circ\text{C}$  | 13         | A                |
|                                                | $T_A=70^\circ\text{C}$  | 10         |                  |
| Avalanche Current <sup>C</sup>                 | $I_{AS}, I_{AR}$        | 30         | A                |
| Avalanche energy $L=0.1\text{mH}$ <sup>C</sup> | $E_{AS}, E_{AR}$        | 45         | mJ               |
| Power Dissipation <sup>B</sup>                 | $T_C=25^\circ\text{C}$  | 50         | W                |
|                                                | $T_C=100^\circ\text{C}$ | 25         |                  |
| Power Dissipation <sup>A</sup>                 | $T_A=25^\circ\text{C}$  | 2.3        | W                |
|                                                | $T_A=70^\circ\text{C}$  | 1.4        |                  |
| Junction and Storage Temperature Range         | $T_J, T_{STG}$          | -55 to 175 | $^\circ\text{C}$ |

#### Thermal Characteristics

| Parameter                                   | Symbol          | Typ | Max | Units              |
|---------------------------------------------|-----------------|-----|-----|--------------------|
| Maximum Junction-to-Ambient <sup>A</sup>    | $R_{\theta JA}$ | 18  | 22  | $^\circ\text{C/W}$ |
| Maximum Junction-to-Ambient <sup>A, D</sup> |                 | 44  | 55  | $^\circ\text{C/W}$ |
| Maximum Junction-to-Case                    | $R_{\theta JC}$ | 2.4 | 3   | $^\circ\text{C/W}$ |

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

| Symbol                      | Parameter                                          | Conditions                                                                                 | Min | Typ       | Max      | Units |
|-----------------------------|----------------------------------------------------|--------------------------------------------------------------------------------------------|-----|-----------|----------|-------|
| <b>STATIC PARAMETERS</b>    |                                                    |                                                                                            |     |           |          |       |
| BV <sub>DSS</sub>           | Drain-Source Breakdown Voltage                     | I <sub>D</sub> =250μA, V <sub>GS</sub> =0V                                                 | 30  |           |          | V     |
| I <sub>DSS</sub>            | Zero Gate Voltage Drain Current                    | V <sub>DS</sub> =30V, V <sub>GS</sub> =0V<br>T <sub>J</sub> =55°C                          |     |           | 10<br>50 | μA    |
| I <sub>GSS</sub>            | Gate-Body leakage current                          | V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V                                                |     |           | ±100     | nA    |
| V <sub>GS(th)</sub>         | Gate Threshold Voltage                             | V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA                                   | 1.2 | 1.8       | 2.4      | V     |
| I <sub>D(ON)</sub>          | On state drain current                             | V <sub>GS</sub> =10V, V <sub>DS</sub> =5V                                                  | 110 |           |          | A     |
| R <sub>DS(ON)</sub>         | Static Drain-Source On-Resistance                  | V <sub>GS</sub> =10V, I <sub>D</sub> =20A<br>T <sub>J</sub> =125°C                         |     | 6.7<br>10 | 8<br>12  | mΩ    |
|                             |                                                    | V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A                                                 |     | 11        | 14       | mΩ    |
|                             |                                                    |                                                                                            |     |           |          |       |
| g <sub>FS</sub>             | Forward Transconductance                           | V <sub>DS</sub> =5V, I <sub>D</sub> =20A                                                   |     | 40        |          | S     |
| V <sub>SD</sub>             | Diode Forward Voltage                              | I <sub>S</sub> =1A, V <sub>GS</sub> =0V                                                    |     | 0.7       | 1        | V     |
| I <sub>S</sub>              | Maximum Body-Diode Continuous Current <sup>G</sup> |                                                                                            |     |           | 55       | A     |
| <b>DYNAMIC PARAMETERS</b>   |                                                    |                                                                                            |     |           |          |       |
| C <sub>iss</sub>            | Input Capacitance                                  | V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz                                          | 950 | 1190      | 1430     | pF    |
| C <sub>oss</sub>            | Output Capacitance                                 |                                                                                            | 150 | 220       | 290      | pF    |
| C <sub>rss</sub>            | Reverse Transfer Capacitance                       |                                                                                            | 80  | 130       | 180      | pF    |
| R <sub>g</sub>              | Gate resistance                                    | V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz                                           | 0.4 | 0.9       | 1.4      | Ω     |
| <b>SWITCHING PARAMETERS</b> |                                                    |                                                                                            |     |           |          |       |
| Q <sub>g(10V)</sub>         | Total Gate Charge                                  | V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A                            | 18  | 23        | 28       | nC    |
| Q <sub>g(4.5V)</sub>        | Total Gate Charge                                  |                                                                                            | 9   | 11        | 13       | nC    |
| Q <sub>gs</sub>             | Gate Source Charge                                 |                                                                                            | 2.4 | 3         | 3.6      | nC    |
| Q <sub>gd</sub>             | Gate Drain Charge                                  |                                                                                            | 3.6 | 6         | 8.4      | nC    |
| t <sub>D(on)</sub>          | Turn-On DelayTime                                  | V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω,<br>R <sub>GEN</sub> =3Ω |     | 7         |          | ns    |
| t <sub>r</sub>              | Turn-On Rise Time                                  |                                                                                            |     | 10        |          | ns    |
| t <sub>D(off)</sub>         | Turn-Off DelayTime                                 |                                                                                            |     | 22        |          | ns    |
| t <sub>f</sub>              | Turn-Off Fall Time                                 |                                                                                            |     | 5         |          | ns    |
| t <sub>rr</sub>             | Body Diode Reverse Recovery Time                   | I <sub>F</sub> =20A, dI/dt=500A/μs                                                         | 7.8 | 9.8       | 12       | ns    |
| Q <sub>rr</sub>             | Body Diode Reverse Recovery Charge                 | I <sub>F</sub> =20A, dI/dt=500A/μs                                                         | 14  | 17.6      | 21       | nC    |

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating g.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

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## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

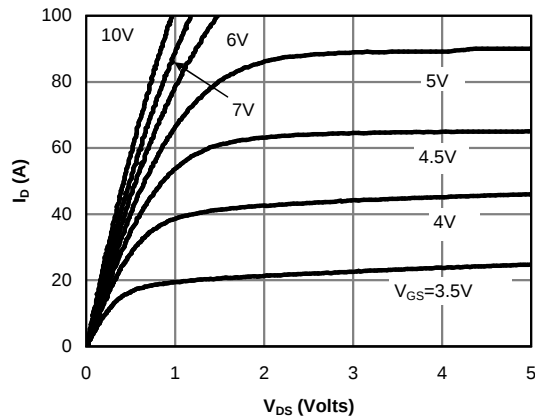


Fig 1: On-Region Characteristics (Note E)

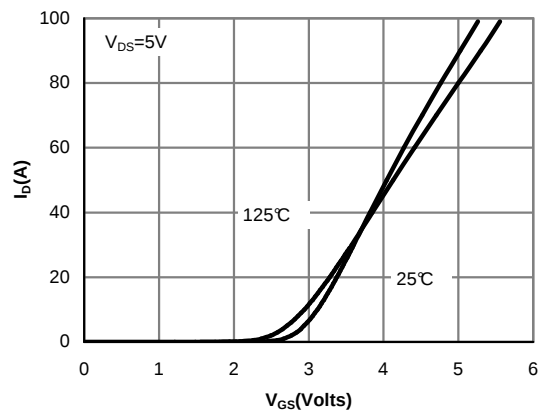


Figure 2: Transfer Characteristics (Note E)

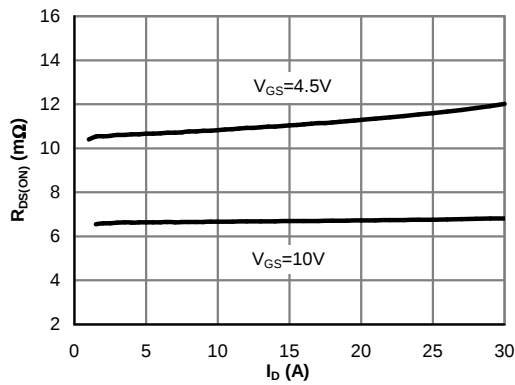


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

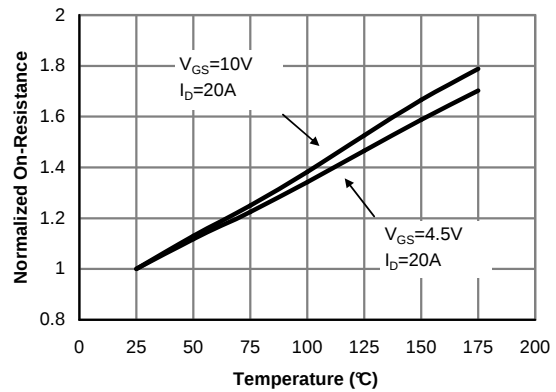


Figure 4: On-Resistance vs. Junction Temperature (Note E)

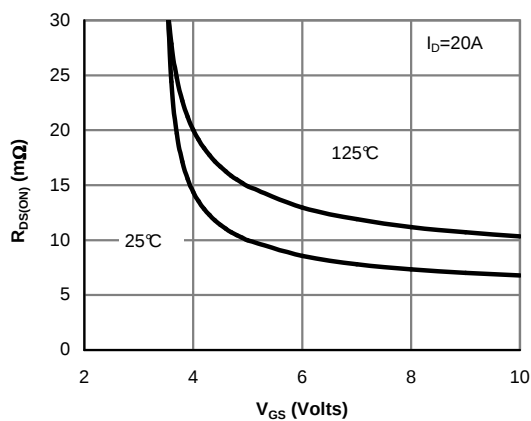


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

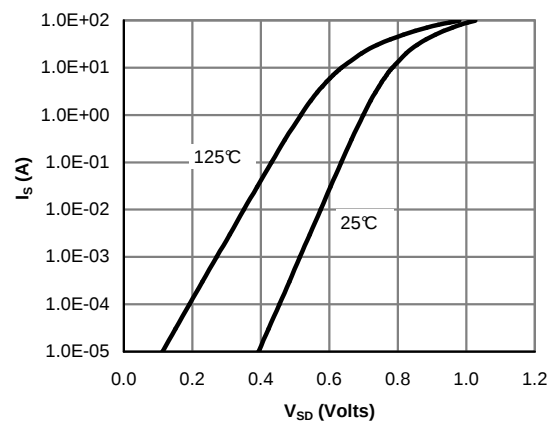
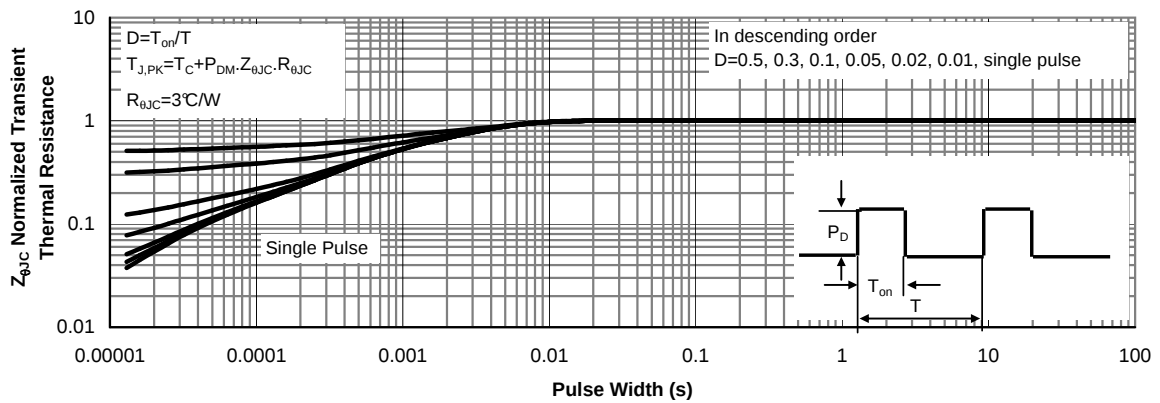
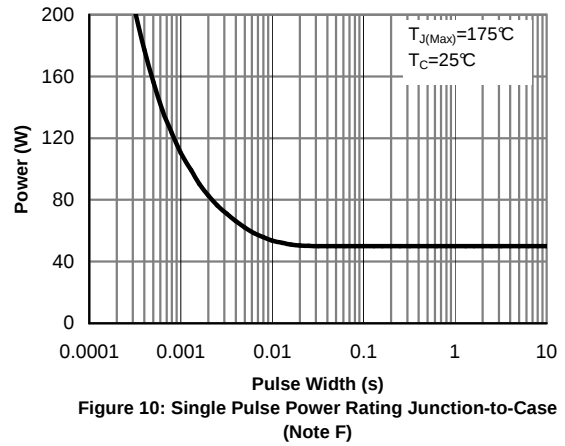
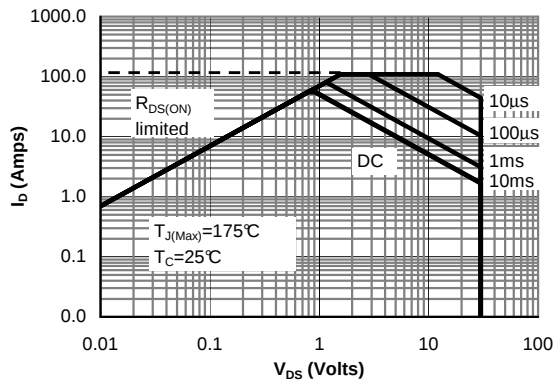
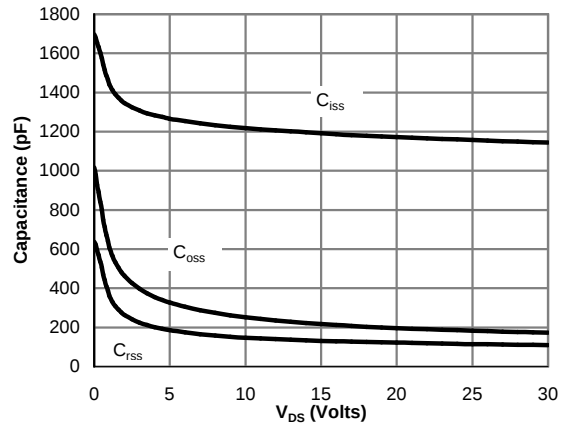
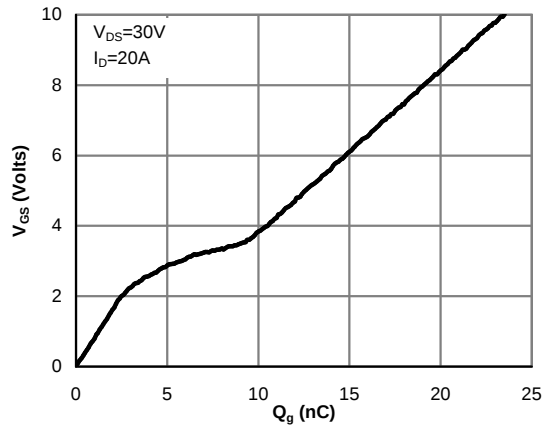


Figure 6: Body-Diode Characteristics (Note E)

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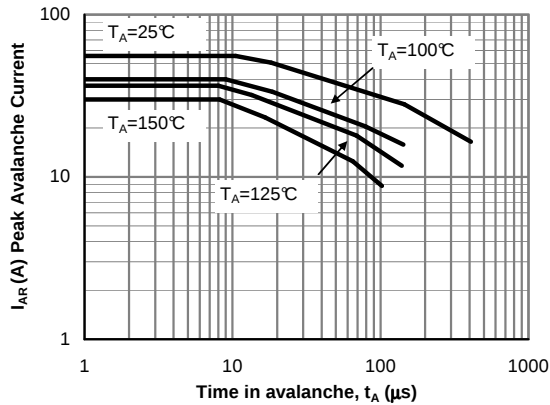


Figure 12: Single Pulse Avalanche capability (Note C)

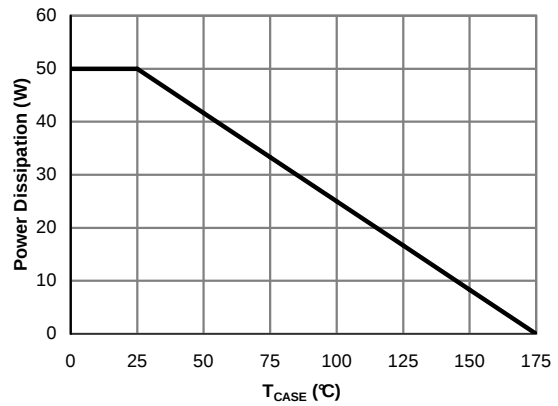


Figure 13: Power De-rating (Note F)

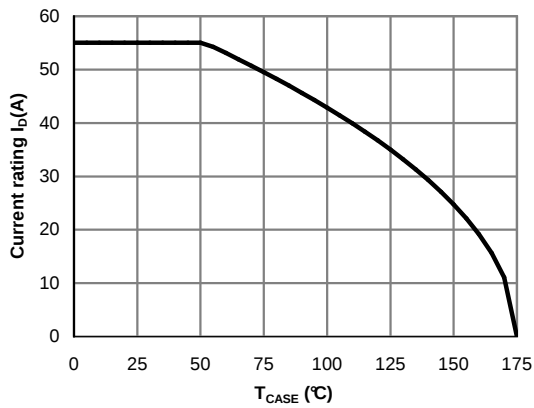


Figure 14: Current De-rating (Note F)

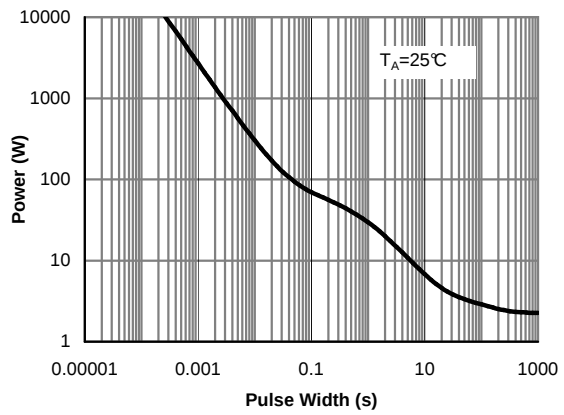


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

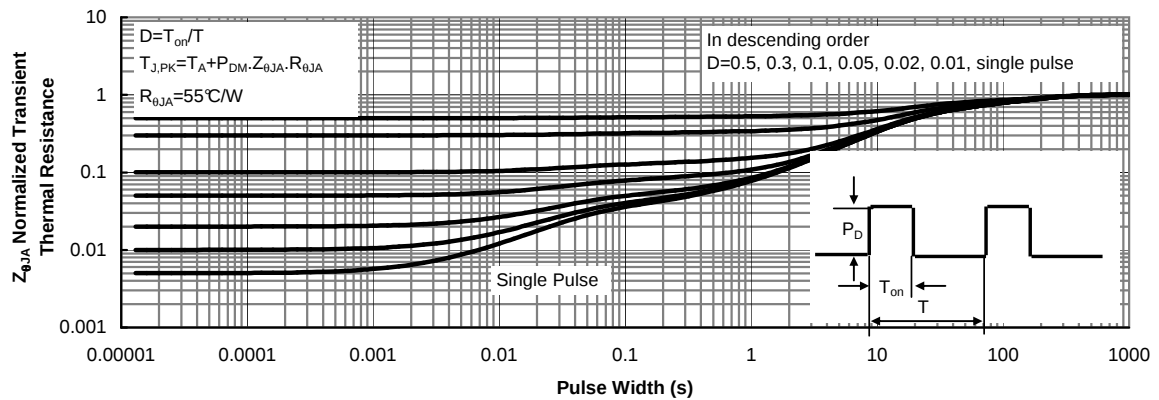


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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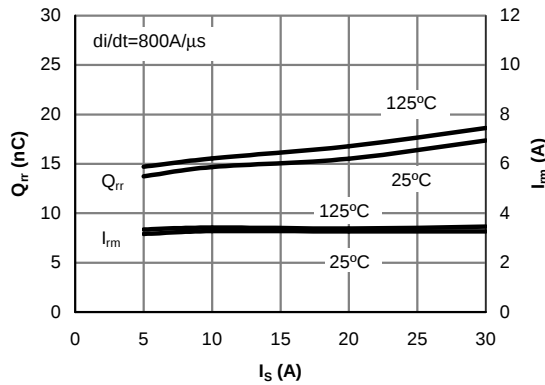


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

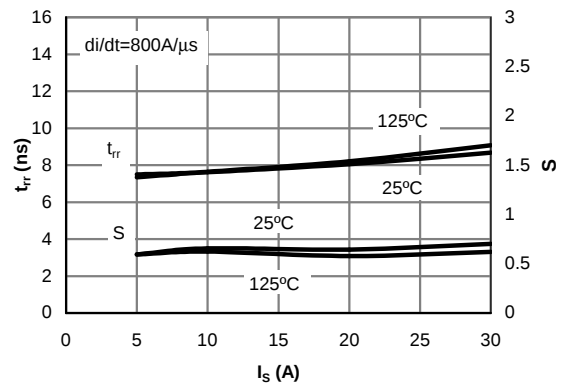


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

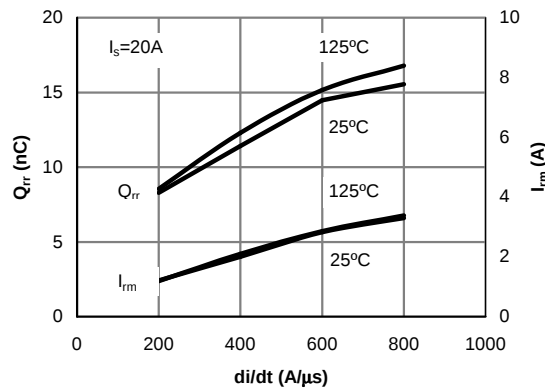


Figure 19: Diode Reverse Recovery Charge and Peak Current vs.  $di/dt$

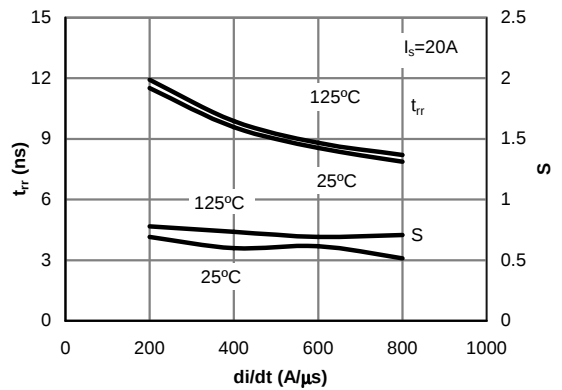
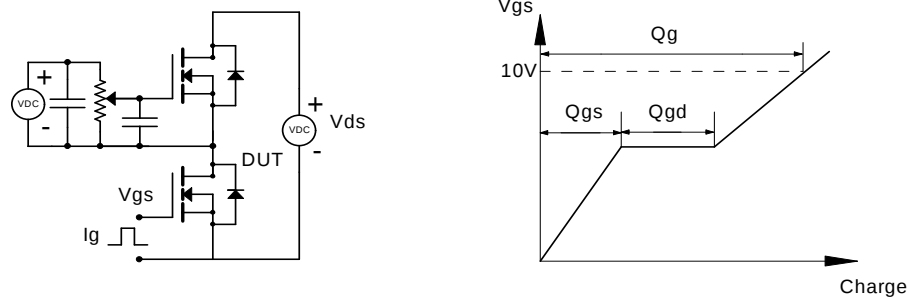
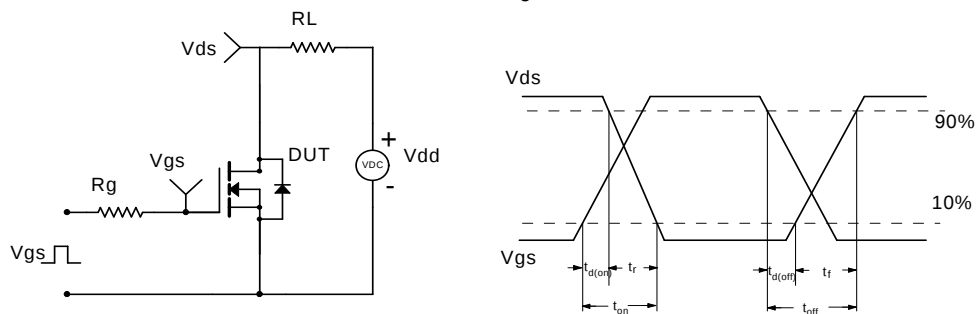


Figure 20: Diode Reverse Recovery Time and Softness Factor vs.  $di/dt$

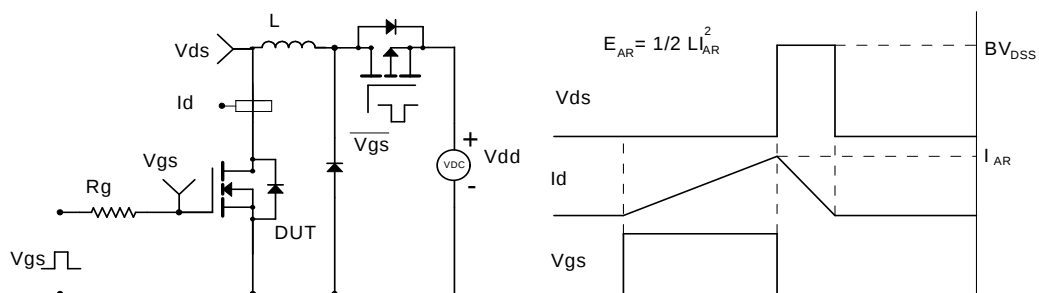
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

