Fast, Voltage-Out DC–440 MHz, 95 dB Logarithmic Amplifier

AD8310

FEATURES

Multistage demodulating logarithmic amplifier
Voltage output, rise time <15 ns
High current capacity: 25 mA into grounded RL
95 dB dynamic range: –91 dBV to +4 dBV
Single supply of 2.7 V min at 8 mA typ
DC–440 MHz operation, ±0.4 dB linearity
Slope of +24 mV/dB, intercept of –108 dBV
Highly stable scaling over temperature
Fully differential dc-coupled signal path
100 ns power-up time, 1 mA sleep current

APPLICATIONS

Conversion of signal level to decibel form
Transmitter antenna power measurement
Receiver signal strength indication (RSSI)
Low cost radar and sonar signal processing
Network and spectrum analyzers
Signal-level determination down to 20 Hz
True-decibel ac mode for multimeters

GENERAL DESCRIPTION

The AD8310 is a complete, dc–440 MHz demodulating logarithmic amplifier (log amp) with a very fast voltage mode output, capable of driving up to 25 mA into a grounded load in under 15 ns. It uses the progressive compression (successive detection) technique to provide a dynamic range of up to 95 dB to ±3 dB law conformance or 90 dB to a ±1 dB error bound up to 100 MHz. It is extremely stable and easy to use, requiring no significant external components. A single-supply voltage of 2.7 V to 5.5 V at 8 mA is needed, corresponding to a power consumption of only 24 mW at 3 V. A fast-acting CMOS-compatible enable pin is provided.

Each of the six cascaded amplifier/limiter cells has a small-signal gain of 14.3 dB, with a –3 dB bandwidth of 900 MHz. A total of nine detector cells are used to provide a dynamic range that extends from –91 dBV (where 0 dBV is defined as the amplitude of a 1 V rms sine wave), an amplitude of about ±40 μV, up to +4 dBV (or ±2.2 V). The demodulated output is accurately scaled, with a log slope of 24 mV/dB and an intercept of –108 dBV. The scaling parameters are supply- and temperature-independent.

FUNCTIONAL BLOCK DIAGRAM

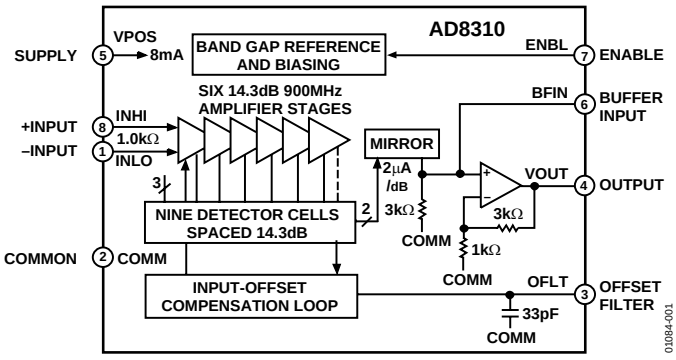


Figure 1.

The fully differential input offers a moderately high impedance (1 kΩ in parallel with about 1 pF). A simple network can match the input to 50 Ω and provide a power sensitivity of –78 dBm to +17 dBm. The logarithmic linearity is typically within ±0.4 dB up to 100 MHz over the central portion of the range, but it is somewhat greater at 440 MHz. There is no minimum frequency limit; the AD8310 can be used down to low audio frequencies. Special filtering features are provided to support this wide range.

The output voltage runs from a noise-limited lower boundary of 400 mV to an upper limit within 200 mV of the supply voltage for light loads. The slope and intercept can be readily altered using external resistors. The output is tolerant of a wide variety of load conditions and is stable with capacitive loads of 100 pF.

The AD8310 provides a unique combination of low cost, small size, low power consumption, high accuracy and stability, high dynamic range, a frequency range encompassing audio to UHF, fast response time, and good load-driving capabilities, making this product useful in numerous applications that require the reduction of a signal to its decibel equivalent.

The AD8310 is available in the industrial temperature range of –40°C to +85°C in an 8-lead MSOP package.

Rev. D
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REVISION HISTORY

10/04—Data Sheet Changed from Rev. C to Rev. D

Format Updated ... Universal
Typical Performance Characteristics Reordered ... 6
Changes to Figures 41 and 42 ... 20

7/03—Data Sheet Changed from Rev. B to Rev. C

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2/03—Data Sheet Changed from Rev. A to Rev. B

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Updated Outline Dimensions ... 16

1/00—Data Sheet Changed from Rev. 0 to Rev. A

10/99—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 5 V, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT STAGE	Inputs INHI, INLO				
Maximum Input[1]	Single-ended, p-p	±2.0	±2.2		V
			4		dBV
Equivalent Power in 50 Ω	Termination resistor of 52.3 Ω		17		dBm
	Differential drive, p-p		20		dBm
Noise Floor	Terminated 50 Ω source		1.28		nV/√Hz
Equivalent Power in 50 Ω	440 MHz bandwidth		−78		dBm
Input Resistance	From INHI to INLO	800	1000	1200	Ω
Input Capacitance	From INHI to INLO		1.4		pF
DC Bias Voltage	Either input		3.2		V
LOGARITHMIC AMPLIFIER	Output VOUT				
±3 dB Error Dynamic Range	From noise floor to maximum input		95		dB
Transfer Slope	10 MHz ≤ f ≤ 200 MHz	22	24	26	mV/dB
	Overtemperature, −40°C < T_A < +85°C	20		26	mV/dB
Intercept (Log Offset)[2]	10 MHz ≤ f ≤ 200 MHz	−115	−108	−99	dBV
	Equivalent dBm (re 50 Ω)	−102	−95	−86	dBm
	Overtemperature, −40°C ≤ T_A ≤ +85°C	−120		−96	dBV
	Equivalent dBm (re 50 Ω)	−107		−83	dBm
	Temperature sensitivity		−0.04		dB/°C
Linearity Error (Ripple)	Input from −88 dBV (−75 dBm) to +2 dBV (+15 dBm)		±0.4		dB
Output Voltage	Input = −91 dBV (−78 dBm)		0.4		V
	Input = 9 dBV (22 dBm)		2.6		V
Minimum Load Resistance, RL			100		Ω
Maximum Sink Current			0.5		mA
Output Resistance			0.05		Ω
Video Bandwidth			25		MHz
Rise Time (10% to 90%)	Input Level = −43 dBV (−30 dBm), RL ≥ 402 Ω, CL ≤ 68 pF		15		ns
	Input Level = −3 dBV (+10 dBm), RL ≥ 402 Ω, CL ≤ 68 pF		20		ns
Fall Time (90% to 10%)	Input Level = −43 dBV (−30 dBm), RL ≥ 402 Ω, CL ≤ 68 pF		30		ns
	Input Level = −3 dBV (+10 dBm), RL ≥ 402 Ω, CL ≤ 68 pF		40		ns
Output Settling Time to 1%	Input Level = −13 dBV (0 dBm), RL ≥ 402 Ω, CL ≤ 68 pF		40		ns
POWER INTERFACES					
Supply Voltage, VPOS		2.7		5.5	V
Quiescent Current	Zero-signal	6.5	8.0	9.5	mA
Overtemperature	−40°C < T_A < +85°C	5.5	8.5	10	mA
Disable Current			0.05		µA
Logic Level to Enable Power	High condition, −40°C < T_A < +85°C		2.3		V
Input Current when High	3 V at ENBL		35		µA
Logic Level to Disable Power	Low condition, −40°C < T_A < +85°C		0.8		V

[1] The input level is specified in dBV, because logarithmic amplifiers respond strictly to voltage, not power. 0 dBV corresponds to a sinusoidal single-frequency input of 1 V rms. A power level of 0 dBm (1 mW) in a 50 Ω termination corresponds to an input of 0.2236 V rms. Therefore, the relationship between dBV and dBm is a fixed offset of 13 dBm in the special case of a 50 Ω termination.

[2] Guaranteed but not tested; limits are specified at six sigma levels.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Value
Supply Voltage, V_S	7.5 V
Input Power (re 50 Ω), Single-Ended	18 dBm
Differential Drive	22 dBm
Internal Power Dissipation	200 mW
θ_{JA}	200°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering 60 s)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

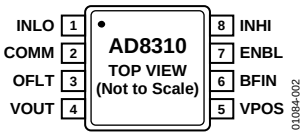


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	INLO	One of Two Balanced Inputs, Biased Roughly to VPOS/2.
2	COMM	Common Pin (Usually Grounded).
3	OFLT	Offset Filter Access, Nominally at about 1.75 V.
4	VOUT	Low Impedance Output Voltage, 25 mA Maximum Load.
5	VPOS	Positive Supply, 2.7 V to 5.5 V at 8 mA Quiescent Current.
6	BFIN	Buffer Input; Used to Lower Postdetection Bandwidth.
7	ENBL	CMOS Compatible Chip Enable (Active when High).
8	INHI	Second of Two Balanced Inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

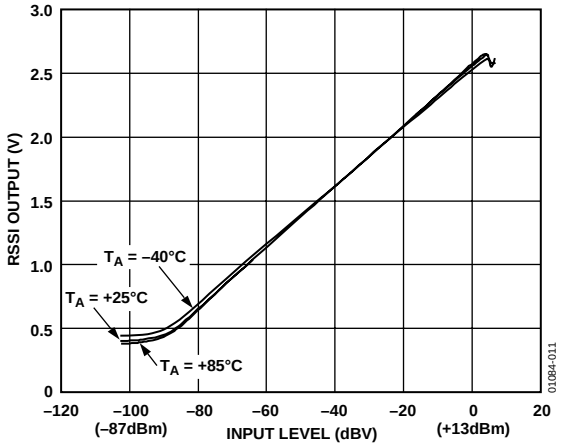


Figure 3. RSSI Output vs. Input Level, 100 MHz Sine Input at T_A = –40°C, +25°C, and +85°C, Single-Ended Input

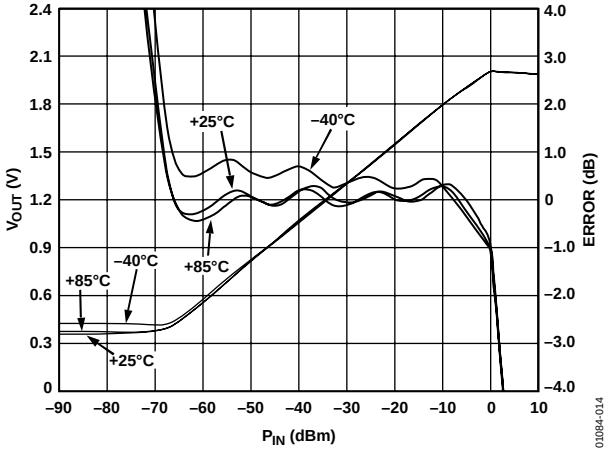


Figure 6. Log Linearity of RSSI Output vs. Input Level, 100 MHz Sine Input at T_A = –40°C, +25°C, and +85°C

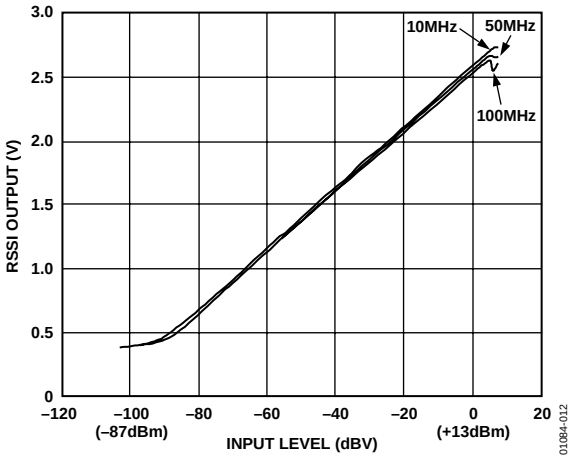


Figure 4. RSSI Output vs. Input Level at T_A = 25°C for Frequencies of 10 MHz, 50 MHz, and 100 MHz

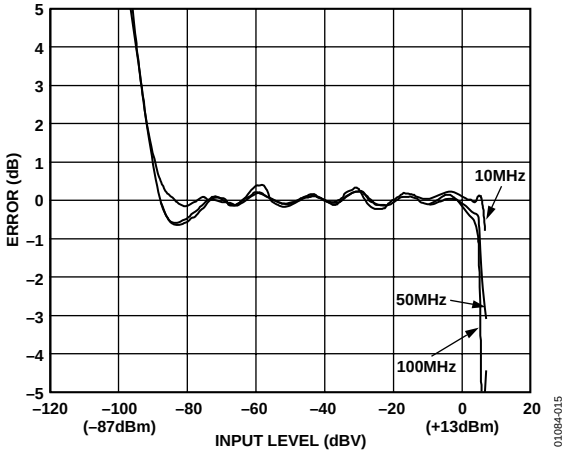


Figure 7. Log Linearity of RSSI Output vs. Input Level, at T_A = 25°C, for Frequencies of 10 MHz, 50 MHz, and 100 MHz

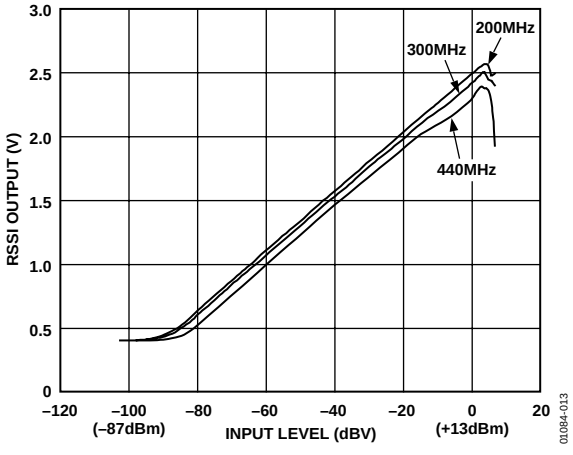


Figure 5. RSSI Output vs. Input Level at T_A = 25°C for Frequencies of 200 MHz, 300 MHz, and 440 MHz

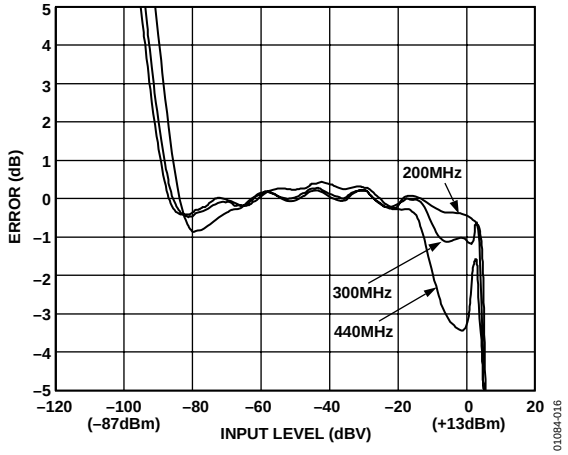


Figure 8. Log Linearity of RSSI Output vs. Input Level at T_A = 25°C for Frequencies of 200 MHz, 300 MHz, and 440 MHz

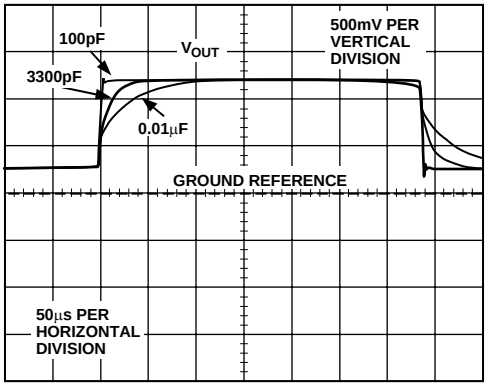


Figure 9. Small-Signal AC Response of RSSI Output with External BFIN Capacitance of 100 pF, 3300 pF, and 0.01 µF

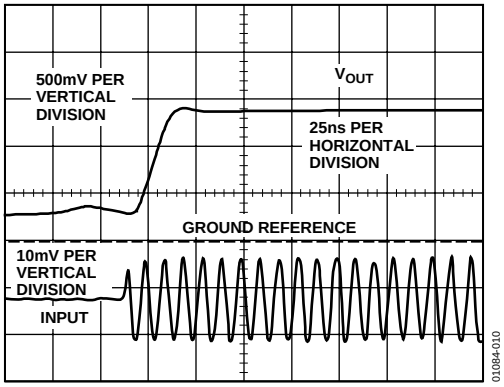


Figure 12. Small-Signal RSSI Pulse Response with R_L = 402 Ω and C_L = 68 pF

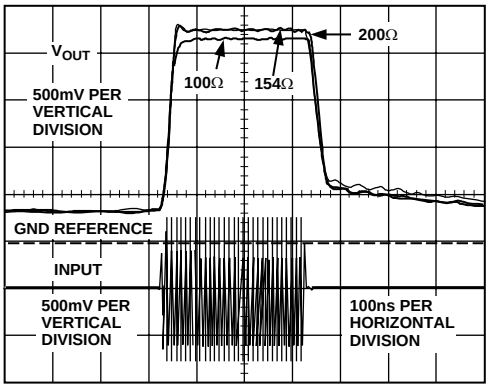


Figure 10. Large-Signal RSSI Pulse Response with C_L = 100 pF and R_L = 100 Ω, 154 Ω, and 200 Ω

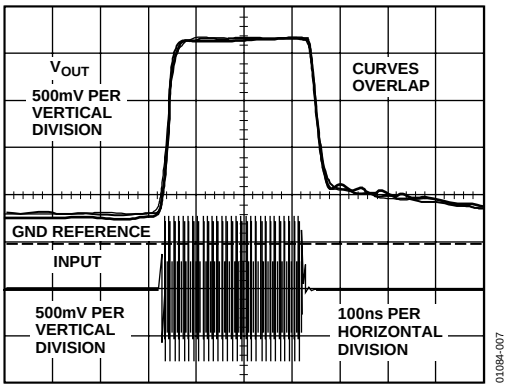


Figure 13. Large-Signal RSSI Pulse Response with R_L = 100 Ω and C_L = 33 pF, 68 pF, and 100 pF

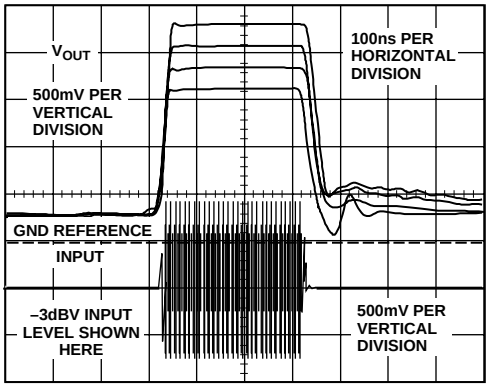


Figure 11. RSSI Pulse Response with R_L = 402 Ω and C_L = 68 pF, for Inputs Stepped from 0 dBV to −33 dBV, −23 dBV, −13 dBV, and −3 dBV

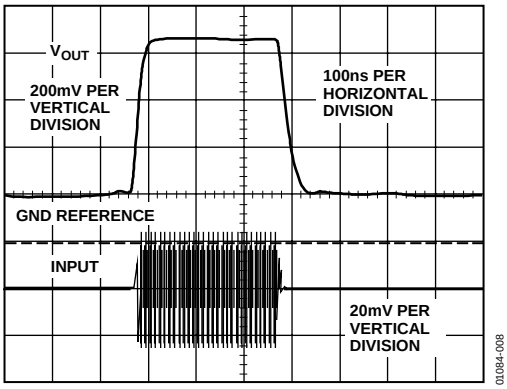


Figure 14. Small-Signal RSSI Pulse Response with R_L = 50 Ω and Back Termination of 50 Ω (Total Load = 100 Ω)

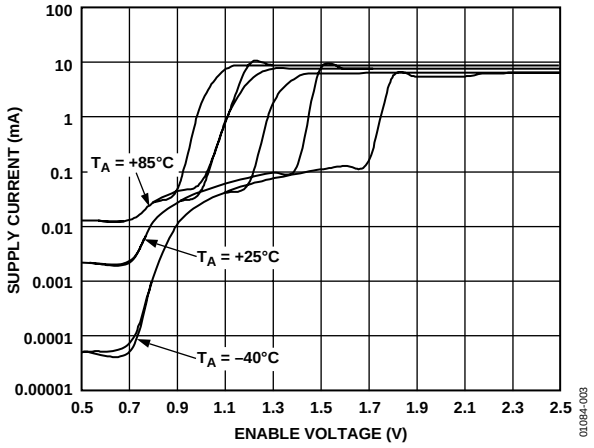


Figure 15. Supply Current vs. Enable Voltage at T_A = –40°C, +25°C, and +85°C

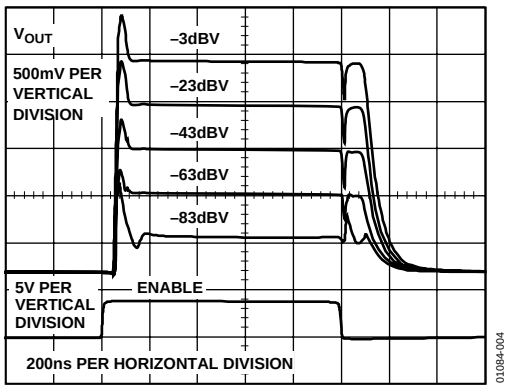


Figure 18. Power-On/Off Response Time with RF Input of –83 dBV to –3 dBV

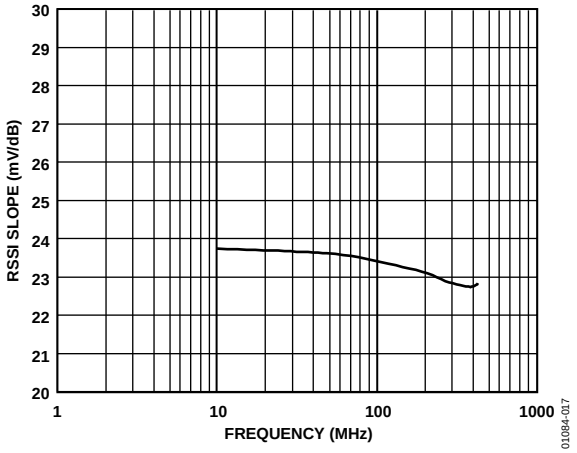


Figure 16. RSSI Slope vs. Frequency

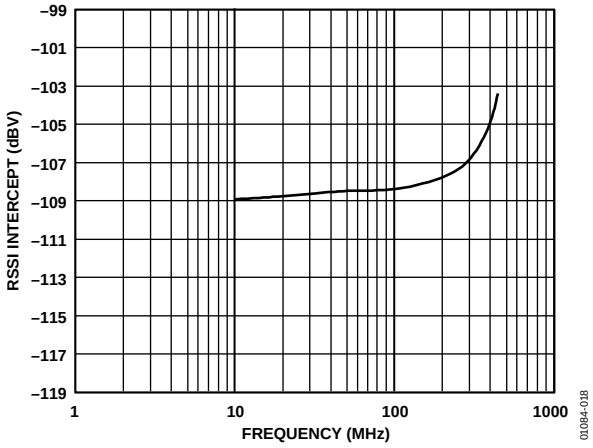


Figure 19. RSSI Intercept vs. Frequency

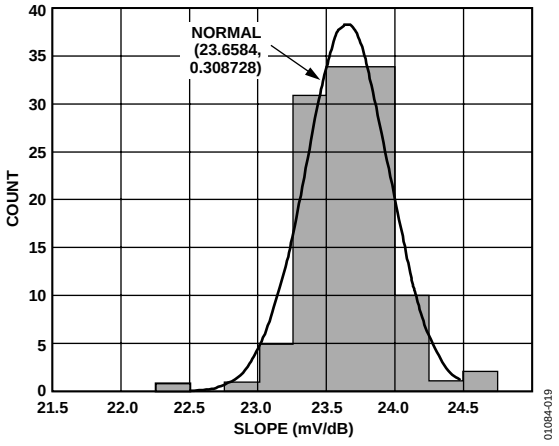


Figure 17. Transfer Slope Distribution, V_S = 5 V, Frequency = 100 MHz, 25°C

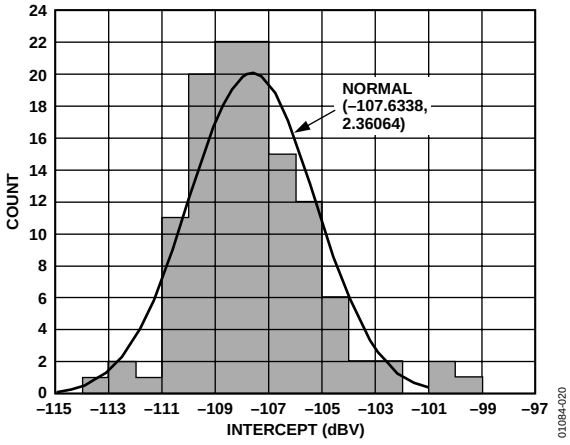


Figure 20. Intercept Distribution V_S = 5 V, Frequency = 100 MHz, 25°C

THEORY OF OPERATION

Logarithmic amplifiers perform a more complex operation than classical linear amplifiers, and their circuitry is significantly different. A good grasp of what log amps do and how they do it can help users avoid many pitfalls in their applications. For a complete discussion of the theory, see the AD8307 data sheet.

The essential purpose of a log amp is not to amplify (though amplification is needed internally), but to compress a signal of wide dynamic range to its decibel equivalent. It is, therefore, a measurement device. An even better term might be logarithmic converter, because the function is to convert a signal from one domain of representation to another via a precise nonlinear transformation:

$$V_{OUT} = V_Y \log\left(\frac{V_{IN}}{V_X}\right) \quad (1)$$

where:

V_{OUT} is the output voltage.
V_Y is the slope voltage. The logarithm is usually taken to base ten, in which case V_Y is also the volts-per-decade.
V_{IN} is the input voltage.
V_X is the intercept voltage.

Log amps implicitly require two references (here V_X and V_Y) that determine the scaling of the circuit. The accuracy of a log amp cannot be any better than the accuracy of its scaling references. In the AD8310, these are provided by a band gap reference.

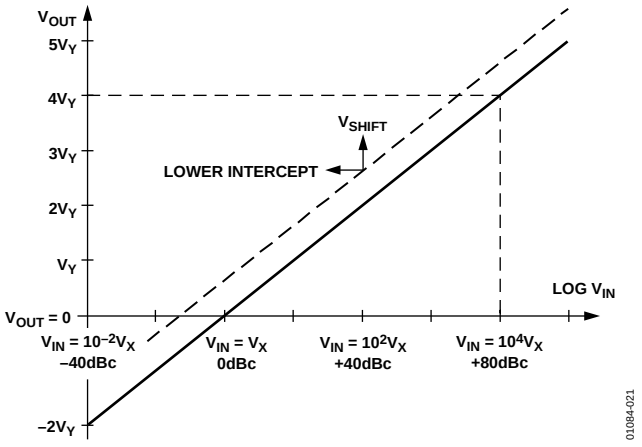


Figure 21. General Form of the Logarithmic Function

While Equation 1, plotted in Figure 21, is fundamentally correct, a different formula is appropriate for specifying the calibration attributes or demodulating log amps like the AD8310, operating in RF applications with a sine wave input.

$$V_{OUT} = V_{SLOPE}\left(P_{IN} - P_O\right) \quad (2)$$

where:

V_{OUT} is the demodulated and filtered baseband (video or RSSI) output.
V_{SLOPE} is the logarithmic slope, now expressed in V/dB (25 mV/dB for the AD8310).
P_{IN} is the input power, expressed in dB relative to some reference power level.
P_O is the logarithmic intercept, expressed in dB relative to the same reference level.

A widely used reference in RF systems is dB above 1 mW in 50 Ω, a level of 0 dBm. Note that the quantity ($P_{IN} – P_O$) is dB. The logarithmic function disappears from the formula, because the conversion has already been implicitly performed in stating the input in decibels. This is strictly a concession to popular convention. Log amps manifestly do not respond to power (tacitly, power absorbed at the input), but rather to input voltage. The input is specified in dBV (decibels with respect to 1 V rms) throughout this data sheet. This is more precise, although still incomplete, because the signal waveform is also involved. Many users specify RF signals in terms of power (usually in dBm/50 Ω) and this convention is used in this data sheet when specifying the performance of the AD8310.

PROGRESSIVE COMPRESSION

High speed, high dynamic-range log amps use a cascade of nonlinear amplifier cells to generate the logarithmic function as a series of contiguous segments, a type of piecewise linear technique. The AD8310 employs six cells in its main signal path, each having a small-signal gain of 14.3 dB (×5.2) and a −3 dB bandwidth of about 900 MHz. The overall gain is about 20,000 (86 dB) and the overall bandwidth of the chain is approximately 500 MHz, resulting in a gain-bandwidth product (GBW) of 10,000 GHz, about a million times that of a typical op amp. This very high GBW is essential to accurate operation under small-signal conditions and at high frequencies. The AD8310 exhibits a logarithmic response down to inputs as small as 40 μV at 440 MHz.

Progressive compression log amps either provide a baseband video response or accept an RF input and demodulate this signal to develop an output that is essentially the envelope of the input represented on a logarithmic or decibel scale. The AD8310 is the latter kind. Demodulation is performed in a total of nine detector cells. Six are associated with the amplifier stages, and three are passive detectors that receive a progressively attenuated fraction of the full input. The maximum signal frequency can be 440 MHz, but, because all the gain stages are dc-coupled, operation at very low frequencies is possible.

SLOPE AND INTERCEPT CALIBRATION

All monolithic log amps from Analog Devices use precision design techniques to control the logarithmic slope and intercept. The primary source of this calibration is a pair of accurate voltage references that provide supply- and temperature-independent scaling. The slope is set to 24 mV/dB by the bias chosen for the detector cells and the subsequent gain of the postdetector output interface. With this slope, the full 95 dB dynamic range can be easily accommodated within the output swing capacity, when operating from a 2.7 V supply. Intercept positioning at−108 dBV (−95 dBm re 50 Ω) has likewise been chosen to provide an output centered in the available voltage range.

Precise control of the slope and intercept results in a log amp with stable scaling parameters, making it a true measurement device as, for example, a calibrated received signal strength indicator (RSSI). In this application, the input waveform is invariably sinusoidal. The input level is correctly specified in dBV. It can alternatively be stated as an equivalent power, in dBm, but in this case, it is necessary to specify the impedance in which this power is presumed to be measured. In RF practice, it is common to assume a reference impedance of 50 Ω, in which 0 dBm (1 mW) corresponds to a sinusoidal amplitude of 316.2 mV (223.6 mV rms). However, the power metric is correct only when the input impedance is lowered to 50 Ω, either by a termination resistor added across INHI and INLO, or by the use of a narrow-band matching network.

Note that log amps do not inherently respond to power, but to the voltage applied to their input. The AD8310 presents a nominal input impedance much higher than 50 Ω (typically 1 kΩ at low frequencies). A simple input matching network can considerably improve the power sensitivity of this type of log amp. This increases the voltage applied to the input and, therefore, alters the intercept. For a 50 Ω reactive match, the voltage gain is about 4.8, and the whole dynamic range moves down by 13.6 dB. The effective intercept is a function of waveform. For example, a square-wave input reads 6 dB higher than a sine wave of the same amplitude, and a Gaussian noise input reads 0.5 dB higher than a sine wave of the same rms value.

OFFSET CONTROL

In a monolithic log amp, direct coupling is used between the stages for several reasons. First, it avoids the need for coupling capacitors, which typically have a chip area at least as large as that of a basic gain cell, considerably increasing die size. Second, the capacitor values predetermine the lowest frequency at which the log amp can operate. For moderate values, this can be as high as 30 MHz, limiting the application range. Third, the parasitic back-plate capacitance lowers the bandwidth of the cell, further limiting the scope of applications.

However, the very high dc gain of a direct-coupled amplifier raises a practical issue. An offset voltage in the early stages of the chain is indistinguishable from a real signal. If it were as high as 400 μV, it would be 18 dB larger than the smallest ac signal (50 μV), potentially reducing the dynamic range by this amount. This problem can be averted by using a global feedback path from the last stage to the first, which corrects this offset in a similar fashion to the dc negative feedback applied around an op amp. The high frequency components of the feedback signal must, of course, be removed to prevent a reduction of the HF gain in the forward path.

An on-chip filter capacitor of 33 pF provides sufficient suppression of HF feedback to allow operation above 1 MHz. The −3 dB point in the high-pass response is at 2 MHz, but the usable range extends well below this frequency. To further lower the frequency range, an external capacitor can be added at OFLT (Pin 3). For example, 300 pF lowers it by a factor of 10.

Operation at low audio frequencies requires a capacitor of about 1 μF. Note that this filter has no effect for input levels well above the offset voltage, where the frequency range would extend down to dc (for a signal applied directly to the input pins). The dc offset can optionally be nulled by adjusting the voltage on the OFLT pin (see the Applications section).

PRODUCT OVERVIEW

The AD8310 has six main amplifier/limiter stages. These six cells and their and associated g_m styled full-wave detectors handle the lower two-thirds of the dynamic range. Three top-end detectors, placed at 14.3 dB taps on a passive attenuator, handle the upper third of the 95 dB range. The first amplifier stage provides a low noise spectral density (1.28 nV/√Hz). Biasing for these cells is provided by two references: one determines their gain, and the other is a band gap circuit that determines the logarithmic slope and stabilizes it against supply and temperature variations. The AD8310 can be enabled or disabled by a CMOS-compatible level at ENBL (Pin 7).

The differential current-mode outputs of the nine detectors are summed and then converted to single-sided form, nominally scaled 2 μA/dB. The output voltage is developed by applying this current to a 3 kΩ load resistor followed by a high speed gain-of-four buffer amplifier, resulting in a logarithmic slope of 24 mV/dB (480 mV/decade) at VOUT (Pin 4). The unbuffered voltage can be accessed at BFIN (Pin 6), allowing certain functional modifications such as the addition of an external postdemodulation filter capacitor and the alteration or adjustment of slope and intercept.

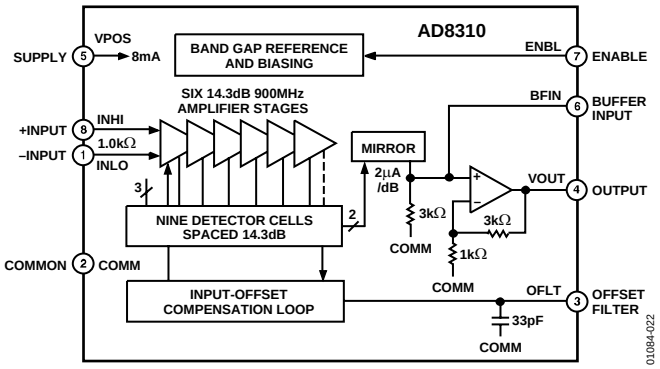


Figure 22. Main Features of the AD8310

The last gain stage also includes an offset-sensing cell. This generates a bipolarity output current, if the main signal path exhibits an imbalance due to accumulated dc offsets. This current is integrated by an on-chip capacitor that can be increased in value by an off-chip component at OFLT (Pin 3). The resulting voltage is used to null the offset at the output of the first stage. Because it does not involve the signal input connections, whose ac-coupling capacitors otherwise introduce a second pole into the feedback path, the stability of the offset correction loop is assured.

The AD8310 is built on an advanced, dielectrically isolated, complementary bipolar process. In the following interface diagrams, resistors labeled as R are thin-film resistors that have a low temperature coefficient of resistance (TCR) and high linearity under large-signal conditions. Their absolute tolerance is typically within ±20%. Similarly, capacitors labeled as C have a typical tolerance of ±15% and essentially zero temperature or voltage sensitivity. Most interfaces have additional small junction capacitances associated with them, due to active devices or ESD protection, which might not be accurate or stable. Component numbering in these interface diagrams is local.

ENABLE INTERFACE

The chip-enable interface is shown in Figure 23. The currents in the diode-connected transistors control the turn-on and turn-off states of the band gap reference and the bias generator. They are a maximum of 100 μA when ENBL is taken to 5 V under worst-case conditions. For voltages below 1 V, the AD8310 is disabled and consumes a sleep current of under 1 μA. When tied to the supply or a voltage above 2 V, it is fully enabled. The internal bias circuitry is very fast (typically <100 ns for either off or on). In practice, however, the latency period before the log amp exhibits its full dynamic range is more likely to be limited by factors relating to the use of ac-coupling at the input or the settling of the offset-control loop (see the following sections).

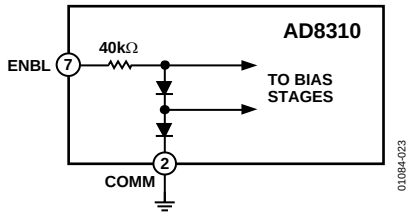


Figure 23. Enable Interface

INPUT INTERFACE

Figure 24 shows the essentials of the input interface. C_P and C_M are parasitic capacitances, and C_D is the differential input capacitance, largely due to Q1 and Q2. In most applications, both input pins are ac-coupled. The S switches close when enable is asserted. When disabled, bias current I_E is shut off and the inputs float; therefore, the coupling capacitors remain charged. If the log amp is disabled for long periods, small leakage currents discharge these capacitors. Then, if they are poorly matched, charging currents at power-up can generate a transient input voltage that can block the lower reaches of the dynamic range until it becomes much less than the signal.

A single-sided signal can be applied via a blocking capacitor to either Pin 1 or Pin 8, with the other pin ac-coupled to ground. Under these conditions, the largest input signal that can be handled is 0 dBV (a sine amplitude of 1.4 V) when using a 3 V supply; a 5 dBV input (2.5 V amplitude) can be handled with a 5 V supply. When using a fully balanced drive, this maximum input level is permissible for supply voltages as low as 2.7 V. Above 10 MHz, this is easily achieved using an LC matching network. Such a network, having an inductor at the input, usefully eliminates the input transient noted above.

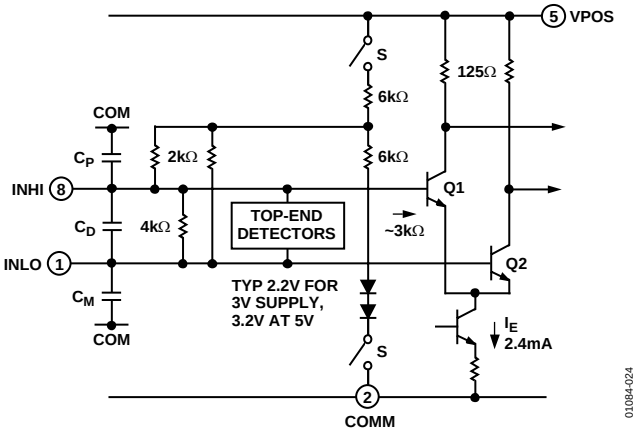


Figure 24. Signal Input Interface

Occasionally, it might be desirable to use the dc-coupled potential of the AD8310 in baseband applications. The main challenge here is to present the signal at the elevated common-mode input level, which might require the use of low noise, low offset buffer amplifiers. In some cases, it might be possible to use dual supplies of ±3 V, which allow the input pins to operate at ground potential. The output, which is internally referenced to the COMM pin (now at −3 V), can be positioned back to ground level, with essentially no sensitivity to the particular value of the negative supply.

OFFSET INTERFACE

The input-referred dc offsets in the signal path are nulled via the interface associated with Pin 3, shown in Figure 25. Q1 and Q2 are the first-stage input transistors, having slightly unbalanced load resistors, resulting in a deliberate offset voltage of about 1.5 mV referred to the input pins. Q3 generates a small current to null this error, dependent on the voltage at the OFLT pin. When Q1 and Q2 are perfectly matched, this voltage is about 1.75 V. In practice, it can range from approximately 1 V to 2.5 V for an input-referred offset of ±1.5 mV.

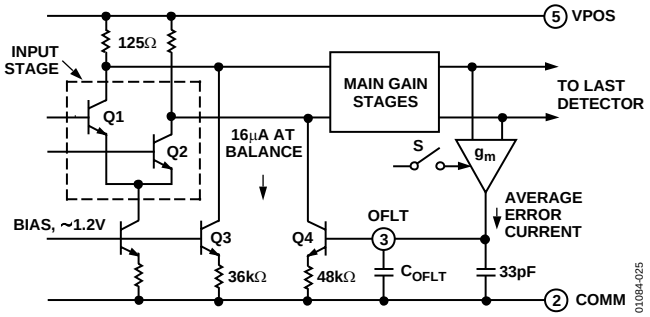


Figure 25. Offset Interface and Offset-Nulling Path

In normal operation using an ac-coupled input signal, the OFLT pin should be left unconnected. The g_m cell, which is gated off when the chip is disabled, converts a residual offset (sensed at a point near the end of the cascade of amplifiers) to a current. This is integrated by the on-chip capacitor, C_{HP}, plus any added external capacitance, C_{OFLT}, to generate the voltage that is applied back to the input stage in the polarity needed to null the output offset. From a small-signal perspective, this feedback alters the response of the amplifier, which exhibits a zero in its ac transfer function, resulting in a closed-loop high-pass −3 dB corner at about 2 MHz. An external capacitor lowers the high-pass corner to arbitrarily low frequencies; using 1 μF, the 3 dB corner is at 60 Hz.

OUTPUT INTERFACE

The nine detectors generate differential currents, having an average value that is dependent on the signal input level, plus a fluctuation at twice the input frequency. These are summed at nodes LGP and LGN in Figure 26. Further currents are added at these nodes to position the intercept by slightly raising the output for zero input and to provide temperature compensation.

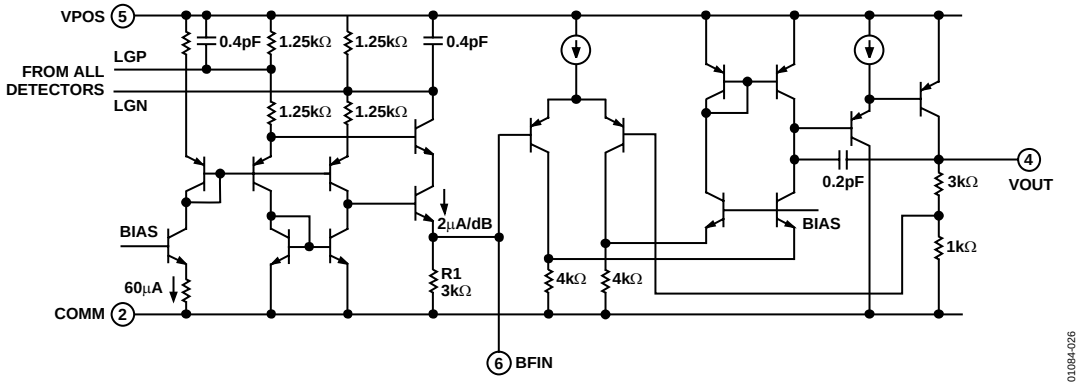


Figure 26. Simplified Output Interface

For zero-signal conditions, all the detector output currents are equal. For a finite input of either polarity, their difference is converted by the output interface to a single-sided unipolar current, nominally scaled 2 μA/dB (40 μA/decade), at the output pin BFIN. An on-chip resistor, R1, of ~3 kΩ converts this current to a voltage of 6 mV/dB. This is then amplified by a factor of 4 in the output buffer, which can drive a current of up to 25 mA in a grounded load resistor. The overall rise time of the AD8310 is under 15 ns. There is also a delay time of about 6 ns when the log amp is driven by an RF burst, starting at zero amplitude.

When driving capacitive loads, it is desirable to add a low value of load resistor to speed up the return to the baseline; the buffer is stable for loads of a least 100 pF. The output bandwidth can be lowered by adding a grounded capacitor at BFIN. The time-constant of the resulting single-pole filter is formed with the 3 kΩ internal load resistor (with a tolerance of 20%). Therefore, to set the –3 dB frequency to 20 kHz, use a capacitor of 2.7 nF. Using 2.7 μF, the filter corner is at 20 Hz.

USING THE AD8310

The AD8310 has very high gain and bandwidth. Consequently, it is susceptible to all signals that appear at the input terminals within a very broad frequency range. Without the benefit of filtering, these are indistinguishable from the desired signal and have the effect of raising the apparent noise floor (that is, lowering the useful dynamic range). For example, while the signal of interest has an IF of 50 MHz, any of the following can easily be larger than the IF signal at the lower extremities of its dynamic range: a few hundred mV of 60 Hz hum picked up due to poor grounding techniques, spurious coupling from a digital clock source on the same PC board, local radio stations, and so on. Careful shielding and supply decoupling is, therefore, essential. A ground plane should be used to provide a low impedance connection to the common pin COMM, for the decoupling capacitor(s) used at VPOS, and for the output ground.

BASIC CONNECTIONS

Figure 27 shows the connections needed for most applications. A supply voltage between 2.7 V and 5.5 V is applied to VPOS and is decoupled using a 0.01 μF capacitor close to the pin. Optionally, a small series resistor can be placed in the power line to give additional filtering of power-supply noise. The ENBL input, which has a threshold of approximately 1.3 V (see Figure 21), should be tied to VPOS when this feature is not needed.

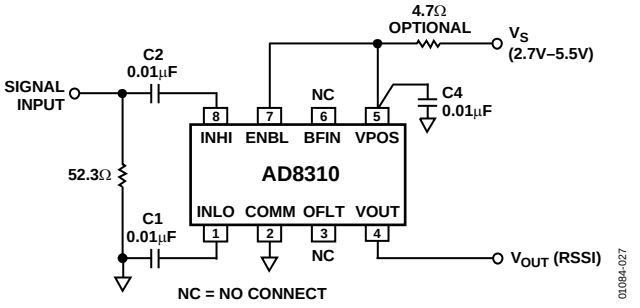


Figure 27. Basic Connections

While the AD8310's input can be driven differentially, the input signal is, in general, single-ended. C1 is tied to ground, and the input signal is coupled in through C2. Capacitors C1 and C2 should have the same value to minimize start-up transients when the enable feature is used; otherwise, their values need not be equal.

The 52.3 Ω resistor combines with the 1.1 kΩ input impedance of the AD8310 to yield a simple broadband 50 Ω input match. An input matching network can also be used (see the Input Matching section).

The coupling time constant, $50 \times C_C/2$, forms a high-pass corner with a 3 dB attenuation at $f_{HP} = 1/(\pi \times 50 \times C_C)$, where C1 = C2 = C_C. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. In low frequency applications, a simple RC network forming a low-pass filter should be added at the input for similar reasons. This should generally be placed at the generator side of the coupling capacitors, thereby lowering the required capacitance value for a given high-pass corner frequency.

For applications in which the ground plane might not be an equipotential (possibly due to noise in the ground plane), the low input of an unbalanced source should generally be ac-coupled through a separate connection of the low associated with the source. Furthermore, it is good practice in such situations to break the ground loop by inserting a small resistance to ground in the low side of the input connector (see Figure 28).

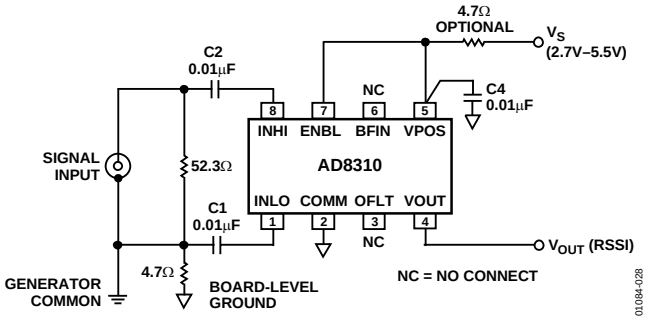


Figure 28. Connections for Isolation of Source Ground from Device Ground

Figure 29 shows the output vs. the input level for sine inputs at 10 MHz, 50 MHz, and 100 MHz. Figure 30 shows the logarithmic conformance under the same conditions.

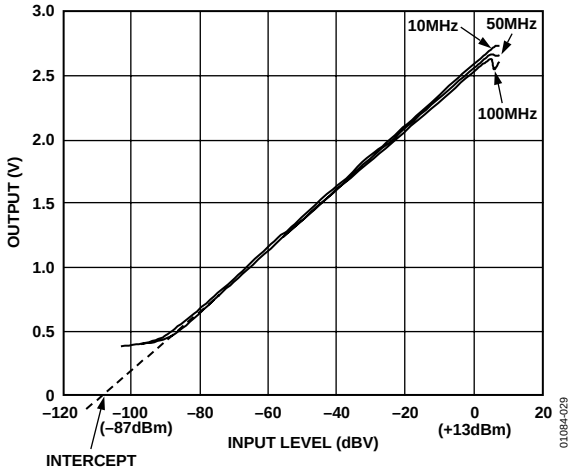


Figure 29. Output vs. Input Level at 10 MHz, 50 MHz, and 100 MHz

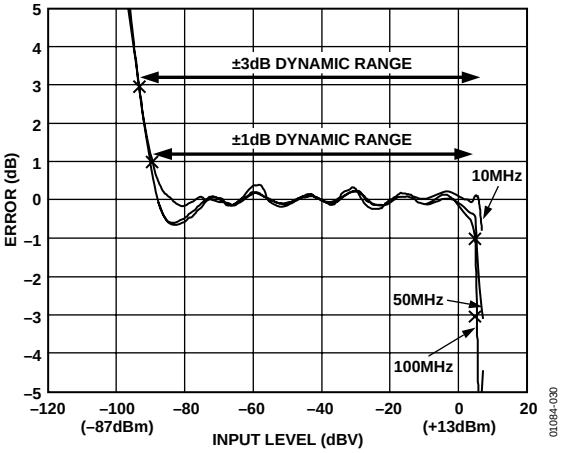


Figure 30. Log Conformance Errors vs. Input Level at 10 MHz, 50 MHz, and 100 MHz

TRANSFER FUNCTION IN TERMS OF SLOPE AND INTERCEPT

The transfer function of the AD8310 is characterized in terms of its slope and intercept. The logarithmic slope is defined as the change in the RSSI output voltage for a 1 dB change at the input. For the AD8310, slope is nominally 24 mV/dB. Therefore, a 10 dB change at the input results in a change at the output of approximately 240 mV. The plot of log conformance shows the range over which the device maintains its constant slope. The dynamic range of the log amp is defined as the range over which the slope remains within a certain error band, usually ±1 dB or ±3 dB. In Figure 30, for example, the ±1 dB dynamic range is approximately 95 dB (from +4 dBV to −91 dBV).

The intercept is the point at which the extrapolated linear response would intersect the horizontal axis (see Figure 29). For the AD8310, the intercept is calibrated to be −108 dBV (−95 dBm). Using the slope and intercept, the output voltage can be calculated for any input level within the specified input range using the following equation:

$$V_{OUT} = V_{SLOPE} \times (P_{IN} - P_O)$$

where:

V_{OUT} is the demodulated and filtered RSSI output.
V_{SLOPE} is the logarithmic slope expressed in V/dB.
P_{IN} is the input signal expressed in dB relative to some reference level (either dBm or dBV in this case).
P_O is the logarithmic intercept expressed in dB relative to the same reference level.

For example, for an input level of −33 dBV (−20 dBm), the output voltage is

$$V_{OUT} = 0.024 \text{ V/dB} \times (-33 \text{ dBV} - (-108 \text{ dBV})) = 1.8 \text{ V}$$

dBV vs. dBm

The most widely used convention in RF systems is to specify power in dBm, decibels above 1 mW in 50 Ω. Specification of the log amp input level in terms of power is strictly a concession to popular convention. As mentioned previously, log amps do *not* respond to power (power absorbed at the input), but to the input voltage. The use of dBV, defined as decibels with respect to a 1 V rms sine wave, is more precise. However, this is still ambiguous, because waveform is also involved in the response of a log amp, which, for a complex input such as a CDMA signal, does not follow the rms value exactly. Because most users specify RF signals in terms of power (more specifically, in dBm/50 Ω) both dBV and dBm are used to specify the performance of the AD8310, showing equivalent dBm levels for the special case of a 50 Ω environment. Values in dBV are converted to dBm re 50 Ω by adding 13 dB.

Table 4. Correction for Signals with Differing Crest Factors

Signal Type	Correction Factor[1] (dB)
Sine wave	0
Square wave or dc	−3.01
Triangular wave	0.9
GSM channel (all time slots on)	0.55
CDMA channel (forward link, nine channels on)	3.55
CDMA channel (reverse link)	0.5
PDC channel (all time slots on)	0.58

[1]Add to the measured input level.

INPUT MATCHING

Where higher sensitivity is required, an input matching network is useful. Using a transformer to achieve the impedance transformation also eliminates the need for coupling capacitors, lowers the offset voltage generated directly at the input, and balances the drive amplitude to INLO and INHI.

The choice of turns ratio depends somewhat on the frequency. At frequencies below 50 MHz, the reactance of the input capacitance is much higher than the real part of the input impedance. In this frequency range, a turns ratio of about 1:4.8 lowers the input impedance to 50 Ω, while raising the input voltage lowers the effect of the short-circuit noise voltage by the same factor. The intercept is also lowered by the turns ratio; for a 50 Ω match, it is reduced by 20 $\log_{10}$ (4.8) or 13.6 dB. The total noise is reduced by a somewhat smaller factor, because there is a small contribution from the input noise current.

NARROW-BAND MATCHING

Transformer coupling is useful in broadband applications. However, a magnetically coupled transformer might not be convenient in some situations. Table 5 lists narrow-band matching values.

Table 5. Narrow-Band Matching Values

F_C (MHz)	Z_{IN} (Ω)	C1 (pF)	C2 (pF)	L_M (nH)	Voltage Gain (dB)
10	45	160	150	3300	13.3
20	44	82	75	1600	13.4
50	46	30	27	680	13.4
100	50	15	13	270	13.4
150	57	10	8.2	220	13.2
200	57	7.5	6.8	150	12.8
250	50	6.2	5.6	100	12.3
500	54	3.9	3.3	39	10.9
10	103	100	91	5600	10.4
20	102	51	43	2700	10.4
50	99	22	18	1000	10.6
100	98	11	9.1	430	10.5
150	101	7.5	6.2	260	10.3
200	95	5.6	4.7	180	10.3
250	92	4.3	3.9	130	9.9
500	114	2.2	2.0	47	6.8

At high frequencies, it is often preferable to use a narrow-band matching network, as shown in Figure 31. This has several advantages. The same voltage gain is achieved, providing increased sensitivity, but a measure of selectivity is also introduced. The component count is low: two capacitors and an inexpensive chip inductor. Additionally, by making these capacitors unequal, the amplitudes at INP and INM can be equalized when driving from a single-sided source, that is, the network also serves as a balun. Figure 32 shows the response for a center frequency of 100 MHz; note the very high attenuation at low frequencies. The high frequency attenuation is due to the input capacitance of the log amp.

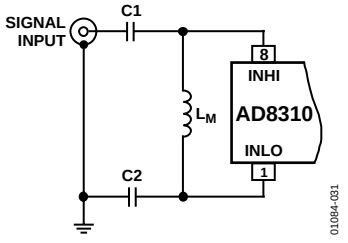


Figure 31. Reactive Matching Network

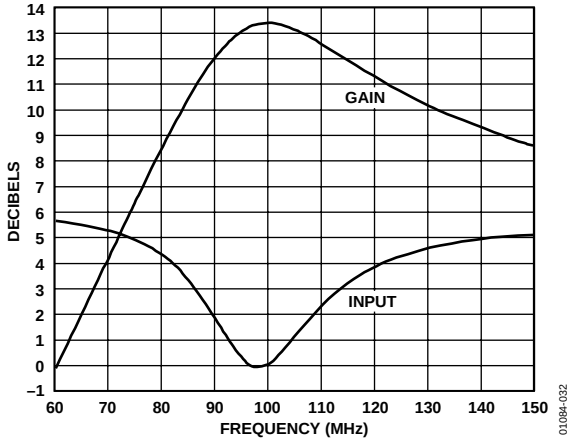


Figure 32. Response of 100 MHz Matching Network

GENERAL MATCHING PROCEDURE

For other center frequencies and source impedances, the following steps can be used to calculate the basic matching parameters.

Step 1: Tune Out C_{IN}

At a center frequency, f_C, the shunt impedance of the input capacitance, C_{IN}, can be made to disappear by resonating with a temporary inductor, L_{IN}, whose value is given by

$$L_{IN} = \frac{1}{\omega^2 C_{IN}}$$

where C_{IN} = 1.4 pF. For example, at f_C = 100 MHz, L_{IN} = 1.8 µH.

Step 2: Calculate C_O and L_O

Now, having a purely resistive input impedance, calculate the nominal coupling elements, C_O and L_O, using

$$C_O = \frac{1}{2\pi f_C \sqrt{R_{IN} R_M}}; \quad L_O = \frac{\sqrt{(R_{IN} R_M)}}{2\pi f_C}$$

For the AD8310, R_{IN} is 1 kΩ. Therefore, if a match to 50 Ω is needed, at f_C = 100 MHz, C_O must be 7.12 pF and L_O must be 356 nH.

Step 3: Split C_O into Two Parts

To provide the desired fully balanced form of the network shown in Figure 31, two capacitors C1 and C2, each of nominally twice C_O, can be used. This requires a value of 14.24 pF in this example. Under these conditions, the voltage amplitudes at INHI and INLO are similar. A somewhat better balance in the two drives can be achieved when C1 is made slightly larger than C2, which also allows a wider range of choices in selecting from standard values.

For example, capacitors of C1 = 15 pF and C2 = 13 pF can be used, making C_O = 6.96 pF.

Step 4: Calculate L_M

The matching inductor required to provide both L_{IN} and L_O is the parallel combination of these.

$$L_M = \frac{L_{IN} L_O}{(L_{IN} + L_O)}$$

With L_{IN} = 1.8 µH and L_O = 356 nH, the value of L_M to complete this example of a match of 50 Ω at 100 MHz is 297.2 nH.

The nearest standard value of 270 nH can be used with only a slight loss of matching accuracy. The voltage gain at resonance depends only on the ratio of impedances, as given by

$$GAIN = 20 \log\left(\sqrt{\frac{R_{IN}}{R_S}}\right) = 10 \log\left(\frac{R_{IN}}{R_S}\right)$$

SLOPE AND INTERCEPT ADJUSTMENTS

Where system (that is, software) calibration is not available, the adjustments shown in Figure 33 can be used, either singly or in combination, to trim the absolute accuracy of the AD8310. The log slope can be raised or lowered by VR1; the values shown provide a calibration range of ±10% (22.6 mV/dB to 27.4 mV/dB), which includes full allowance for the variability in the value of the internal resistances. The adjustment can be made by alternately applying two fixed input levels, provided by an accurate signal generator, spaced over the central portion of the dynamic range, for example, −60 dBV and −20 dBV.

Alternatively, an AM-modulated signal at about the center of the dynamic range can be used. For a modulation depth M, expressed as a fraction, the decibel range between the peaks and troughs over one cycle of the modulation period is given by

$$\Delta\text{dB} = 20 \log_{10} \frac{1+M}{1+M} \quad (3)$$

For example., using a generator output of −40 dBm with a 70% modulation depth (M = 0.7), the decibel range is 15 dB, because the signal varies from −47.5 dBm to −32.5 dBm.

The log intercept is adjustable by VR2 over a −3 dB range with the component values shown. VR2 is adjusted while applying an accurately known CW signal, preferably near the lower end of the dynamic range, to minimize the effect of any residual uncertainty in the slope. For example, to position the intercept to −80 dBm, a test level of −65 dBm can be applied, and VR2 adjusted to produce a dc output of 15 dB above 0 at 24 mV/dB, which is 360 mV.

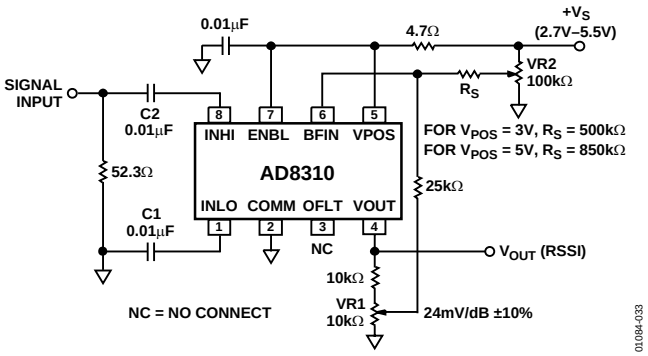


Figure 33. Slope and Intercept Adjustments

INCREASING THE SLOPE TO A FIXED VALUE

It is also possible to increase the slope to a new fixed value and, therefore, to increase the change in output for each decibel of input change. A common example of this is the need to map the output swing of the AD8310 into the input range of an analog-to-digital converter (ADC) with a rail-to-rail input swing. Alternatively, a situation might arise when only a part of the total dynamic range is required—say, just 20 dB—in an application where the nominal input level is more tightly constrained and a higher sensitivity to a change in this level is required. Of course, the maximum output is limited either by the load resistance and the maximum output current rating of 25 mA or by the supply voltage (see the Specifications section).

The slope can easily be raised by adding a resistor from VOUT to BFIN, as shown in Figure 34. This alters the gain of the output buffer, by means of stable positive feedback, from its normal value of 4 to an effective value that can be as high as 16, corresponding to a slope of 100 mV/dB.

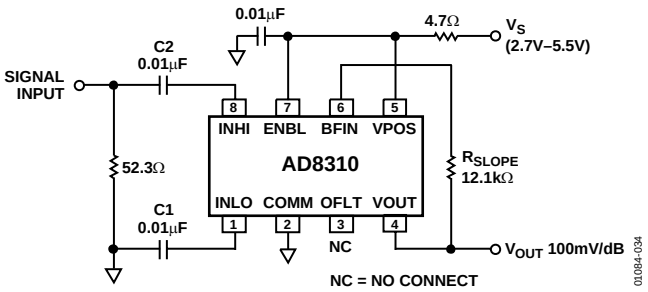


Figure 34. Raising the Slope to 100 mV/dB

The resistor, R_{SLOPE}, is set according to the equation

$$R_{SLOPE} = \frac{9.22\ \text{k}\Omega}{1 + \dfrac{24\ \text{mV/dB}}{Slope}}$$

OUTPUT FILTERING

For applications in which maximum video bandwidth and, consequently, fast rise time are desired, it is essential that the BFIN pin be left unconnected and free of any stray capacitance.

The nominal output video bandwidth of 25 MHz can be reduced by connecting a ground-referenced capacitor (C_{FILT}) to the BFIN pin, as shown in Figure 35. This is generally done to reduce output ripple (at twice the input frequency for a symmetric input waveform such as sinusoidal signals).

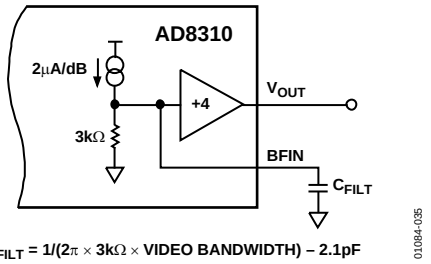


Figure 35. Lowering the Postdemodulation Video Bandwidth

C_{FILT} is selected using the following equation:

$$C_{FILT} = \frac{1}{\left(2\pi \times 3\ \text{k}\Omega \times VideoBandwidth\right)} - 2.1\ \text{pF}$$

The video bandwidth should typically be set at a frequency equal to about one-tenth the minimum input frequency. This ensures that the output ripple of the demodulated log output, which is at twice the input frequency, is well filtered.

In many log amp applications, it might be necessary to lower the corner frequency of the postdemodulation filtering to achieve low output ripple while maintaining a rapid response time to changes in signal level. An example of a 4-pole active filter is shown in the AD8307 data sheet.

LOWERING THE HIGH-PASS CORNER FREQUENCY OF THE OFFSET COMPENSATION LOOP

In normal operation using an ac-coupled input signal, the OFLT pin should be left unconnected. Input-referred dc offsets of about 1.5 mV in the signal path are nulled via an internal offset control loop. This loop has a high-pass −3 dB corner at about 2 MHz. In low frequency ac-coupled applications, it is necessary to lower this corner frequency to prevent input signals from being misinterpreted as offsets. An external capacitor on OFLT lowers the high-pass corner to arbitrarily low frequencies (Figure 36). For example, by using a 1 µF capacitor, the 3 dB corner is reduced to 60 Hz.

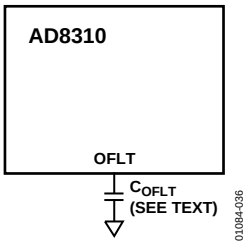


Figure 36. Lowering the High-Pass Corner Frequency of the Offset Control Loop

The corner frequency is set by the following equation:

$$f_{CORNER} = \frac{1}{\left(2\pi \times 2625 \times C_{OFLT}\right)}$$

where C_{OFLT} is the capacitor connected to OFLT.

APPLICATIONS

The AD8310 is highly versatile and easy to use. It needs only a few external components, most of which can be immediately accommodated using the simple connections shown in the Using the AD8310 section.

A few examples of more specialized applications are provided in the following sections. See the AD8307 data sheet for more applications (note the slightly different pin configuration).

CABLE-DRIVING

For a supply voltage of 3 V or greater, the AD8310 can drive a grounded 100 Ω load to 2.5 V. If reverse-termination is required when driving a 50 Ω cable, it should be included in series with the output, as shown in Figure 37. The slope at the load is then 12 mV/dB. In some cases, it might be permissible to operate the cable without a termination at the far end, in which case, the slope is not lowered. Where a further increase in slope is desirable, the scheme shown in Figure 34 can be used.

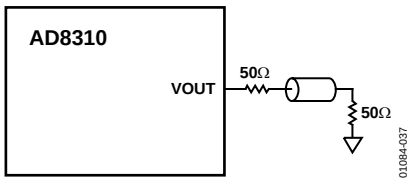


Figure 37. Output Response of Cable-Driver Application

DC-COUPLED INPUT

It might occasionally be necessary to provide response to dc inputs. Because the AD8310 is internally dc-coupled, there is no reason why this cannot be done. However, its differential inputs must be positioned at least 2 V above the COM potential for proper biasing of the first stage. Usually, the source is a single-sided ground-referenced signal, so level-shifting and a single-ended-to-differential conversion must be provided to correctly drive the AD8310's inputs.

Figure 38 shows how a level-shift to midsupply (2.5 V in this example) and a single-ended-to-differential conversion can be accomplished using the AD8138 differential amplifier. The four 499 Ω resistors set up a gain of unity. An output common-mode (or bias) voltage of 2.5 is achieved by applying 2.5 V from a supply-referenced resistive divider to the AD8138's V_{OCM} pin. The differential outputs of the AD8138 directly drive the 1.1 kΩ input impedance of the AD8310.

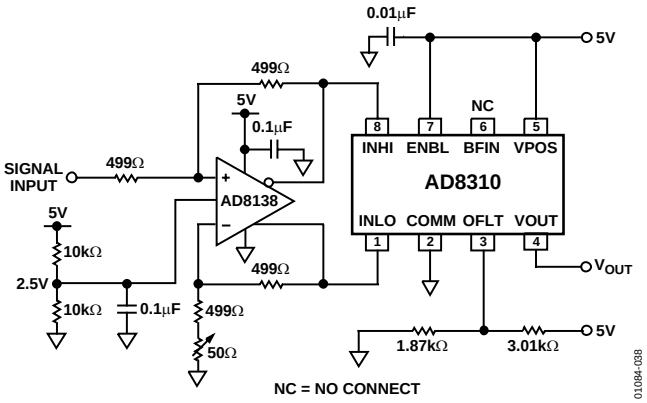


Figure 38. DC-Coupled Log Amp

In this application the offset voltage of the AD8138 must be trimmed. The internal offset compensation circuitry of the AD8310 is disabled by applying a nominal voltage of ~1.9 V to the OFLT pin, so the trim on the AD8138 is effectively trimming both devices' offsets. The trim is done by grounding the circuit's input and slightly varying the gain resistors on the AD8138's inverting input (a 50 Ω potentiometer is used in this example) until the voltage on the AD8310's output reaches a minimum.

After trimming, the lower end of the dynamic range is limited by the broadband noise at the output of the AD8138, which is approximately 425 µV p-p. A differential low-pass filter can be added between the AD8138 and the AD8310 when the very fast pulse response of the circuit is not required.

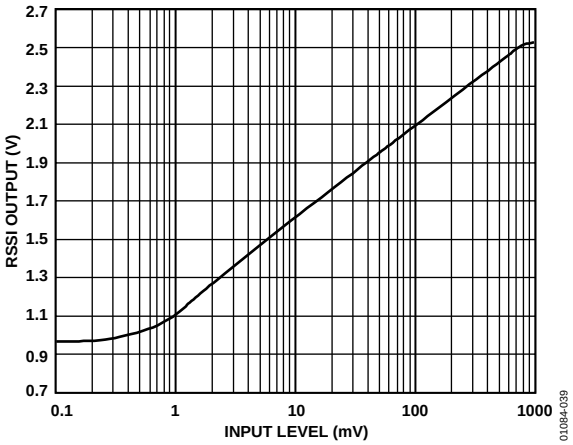


Figure 39. Transfer Function of DC-Coupled Log Amp Application

EVALUATION BOARD

An evaluation board is available, which has been carefully laid out and tested to demonstrate the specified high speed performance of the AD8310. Figure 40 shows the schematic of the evaluation board, which follows the basic connections schematic shown in Figure 27.

Connectors INHI, INLO, and VOUT are of the SMA type. Supply and ground are connected to the TP1 and TP2 vector pins. The layout and silkscreen for the component side of the board are shown in Figure 41 and Figure 42. Switches and component settings for different setups are described in Table 6. For ordering information, see the **Error! Reference source not found.**.

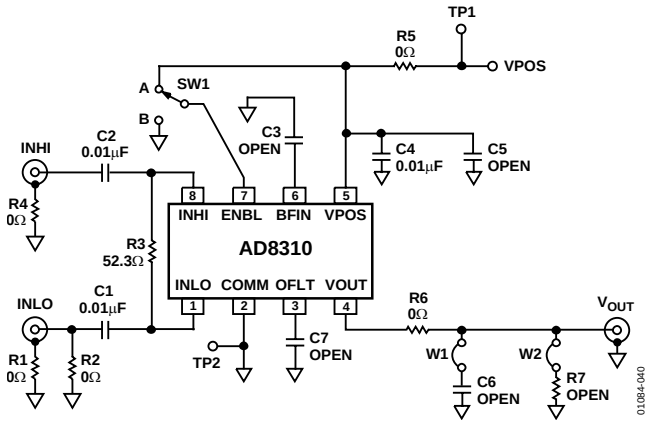


Figure 40. Evaluation Board Schematic

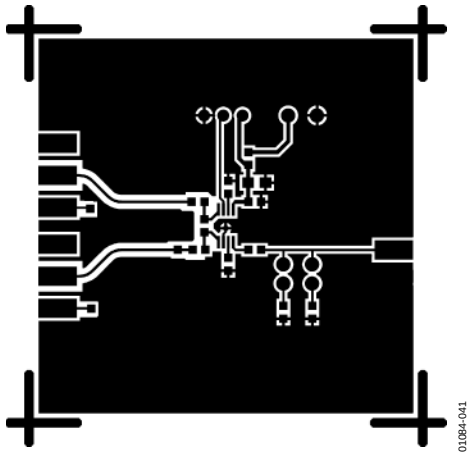


Figure 41. Layout of the Component Side of the Evaluation Board

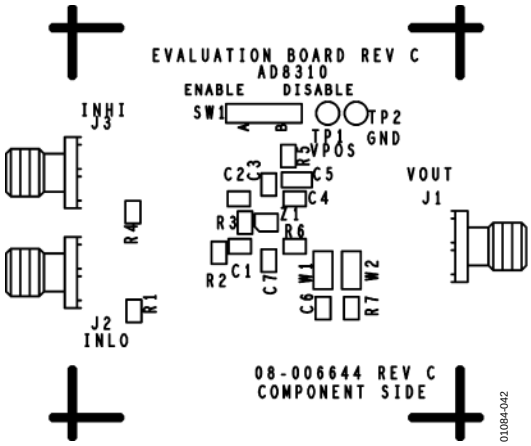


Figure 42. Component Side Silkscreen of the Evaluation Board

Table 6. Evaluation Boards Setup Options

Component	Function	Default Condition
TP1, TP2	Supply and Ground Vector Pins.	Not Applicable
SW1	Device Enable. When in Position A, the ENBL pin is connected to $+V_S$ and the AD8310 is in normal operating mode. In Position B, the ENBL pin is connected to ground, putting the device into sleep mode.	SW1 = A
R1/R4	SMA Connector Grounds.Connects common of INHI and INLO SMA connectors to ground. Can be used to isolate the generator ground from the evaluation board ground (see Figure 28).	R1 = R4 = 0 Ω
C1, C2, R3	Input Interface. R3 (52.3 Ω) combines with the AD8310's 1 kΩ input impedance to give an overall broadband input impedance of 50 Ω. C1, C2, and the AD8310's input impedance combine to set a high-pass input corner of 32 kHz. Alternatively, R3, C1, and C2 can be replaced by an indicator and matching capacitors to form an input matching network. See the Input Matching section for details.	R3 = 52.3 Ω, C1 = C2 = 0.01 µF
C3	RSSI (Video) Bandwidth Adjust. The addition of C3 (farads) lowers the RSSI bandwidth of the VLOG output according to the following equation: $C_{FILT} = 1/(2\pi \times 3\ \text{k}\Omega\ \textit{Video Bandwidth}) - 2.1\ \text{pF}$	C3 = Open
C4, C5, R5	Supply Decoupling. The normal supply decoupling of 0.01 µF (C4) can be augmented by a larger capacitor in C5. An inductor or small resistor can be placed in R5 for additional decoupling.	C4 = 0.01 µF, C5 = Open, R5 = 0
R6	Output Source Impedance. In cable-driving applications, a resistor (typically 50 Ω or 75 Ω) can be placed in R6 to give the circuit a back-terminated output impedance.	R6 = 0 Ω
W1,W2, C6, R7	Output Loading. Resistors and capacitors can be placed in C6 and R7 to load-test VOUT. Jumpers W1 and W2 are used to connect or disconnect the loads.	C6 = R7 = Open, W1 = W2 = Installed
C7	Offset Compensation Loop. A capacitor in C7 reduces the corner frequency of the offset control loop in low frequency applications.	C7 = Open

OUTLINE DIMENSIONS

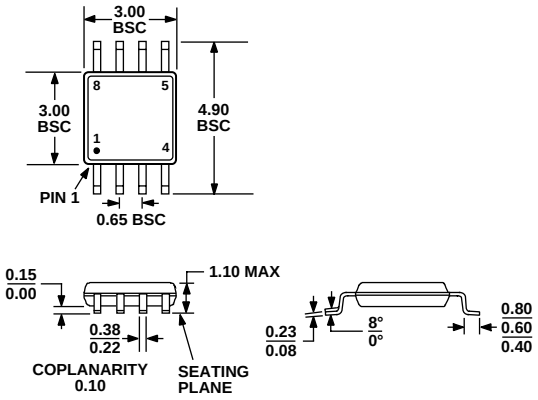


Figure 43. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8310ARM	−40°C to +85°C	8-Lead MSOP, Tube	RM-8	J6A
AD8310ARM-REEL7	−40°C to +85°C	8-Lead MSOP, 7 Tape and Reel	RM-8	J6A
AD8310ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP, 13 Tape and Reel	RM-8	J6A
AD8310ARMZ-REEL7[1]	−40°C to +85°C	8-Lead MSOP, 7 Tape and Reel	RM-8	J6A
AD8310-EVAL		Evaluation Board		

[1] Z = Pb-free part.

NOTES

NOTES

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