

## Multiport Gigabit Ethernet Switches

### GENERAL DESCRIPTION

The Broadcom® BCM53115S is a highly integrated, cost-effective smart-managed Gigabit switch. The switch design is based on the field-proven, industry-leading ROBO architecture. This device combines all the functions of a high-speed switch system including packet buffers, PHY transceivers, media access controllers (MACs), address management, port-based rate control, and a non-blocking switch fabric into a single 65 nm CMOS device. Designed to be fully compliant with the IEEE 802.3™ and IEEE 802.3x specifications, including the MAC-control PAUSE frame, the BCM53115S provides compatibility with all industry-standard Ethernet, Fast Ethernet, and Gigabit Ethernet (GbE) devices.

The BCM53115S has a rich feature set suitable for not only standard GbE connectivity for desktop and laptop PCs, but also for next-generation gaming consoles, set-top boxes, networked DVD players, and home theater receivers. It is also specifically designed for next generation SOHO/SMB routers and gateways.

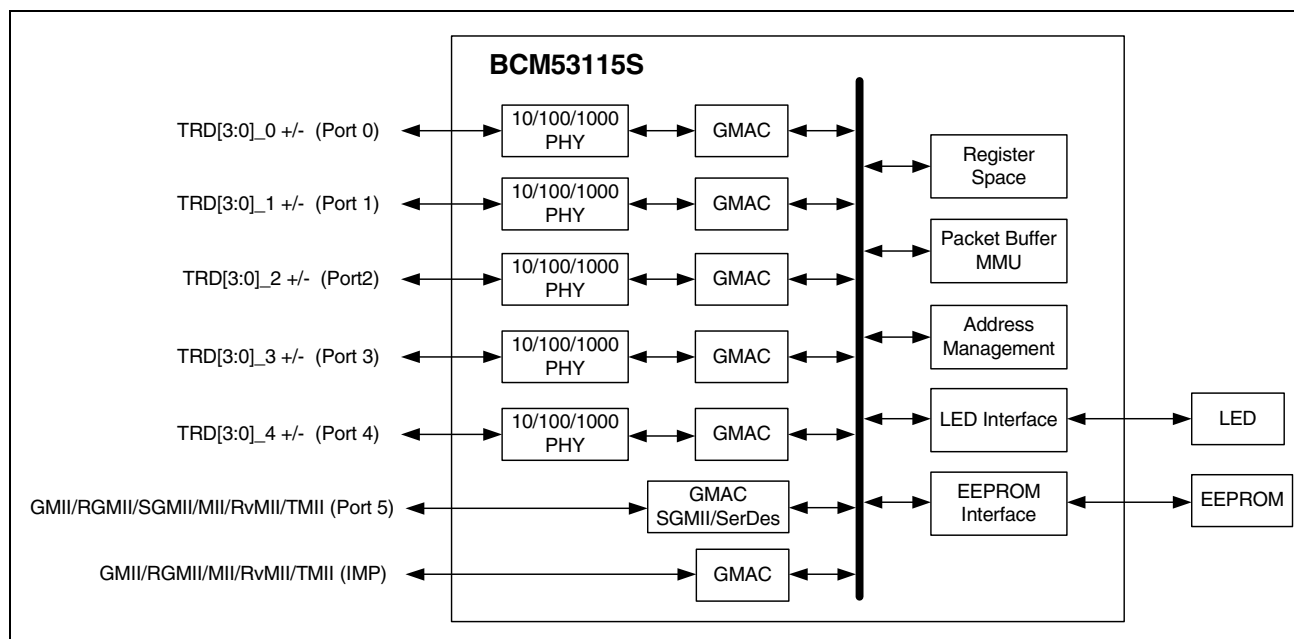
The BCM53115S contains five full-duplex 10/100/1000 BASE-TX Ethernet transceivers. In addition, the BCM53115S has one GMII/RGMII/MII/RvMII/TMII interface for the CPU or a router chip, providing flexible 10/100/1000 Mbps connectivity. A GMII/RGMII/SGMII/MII/RvMII/TMII interface for the WAN port can be configured as an IMP port.

The BCM53115S provides 70+ on-chip MIB counters to collect receive and transmit statistics for each port.

The BCM53115S is available in industrial temperature (I-Temp) and commercial temperature (C-Temp) rated packages. The industrial-grade BCM53115S is provided in a 484-pin PBGA (23 mm x 23 mm) package. The commercial-grade BCM53115S is provided in a 400-pin FBGA (17 mm x 17 mm) package.

### FEATURES

- Seven 10/100/1000 media access controllers
- Five-port 10/100/1000 transceivers for TX
- One GMII/RGMII/MII/RvMII/TMII interface for an inband management port (IMP) for connection to a CPU/management entity without PHY
- One GMII/RGMII/MII/RvMII/TMII interface for WAN port
- Dual IMP ports support, WAN interface (Port 5) to be IMP port-capable
- IEEE 802.1p, MAC Port, TOS, and DiffServ QoS for four queues
- Port-based VLAN
- IEEE 802.1Q-based VLAN with 4K entries
- MAC-based trunking with automatic link failover
- Port-based rate control
- Port mirroring
- DOS attack prevention
  - Support IPv6
  - Ingress mirroring
- IGMP Snooping, MLD snooping support
- Spanning tree support (multiple spanning trees—up to eight)
- Loop detection for unmanaged configurations with Broadcom's patented LoopDTech™ technology
- CableChecker™ with unmanaged mode support
- Double-tagging/QinQ
- IEEE 802.3 as support
- IEEE 802.3x programmable per-port flow control and backpressure, with IEEE 802.1x support for secure user authentication
- EEPROM, MDC/MDIO, and SPI Interface
- 4K entry MAC address table with automatic learning and aging
- 128 KB packet buffer
- 128 multicast group support
- Jumbo frame support up to 9720 byte
- 1.2V for core and 3.3V for I/O
- JTAG support
- 484 PBGA
- 400 FBGA

**Figure 1: Functional Block Diagram**

## Revision History

| <b>Revision</b> | <b>Date</b> | <b>Change Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
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| 53115S-DS06-R   | 02/12/13    | <b>Updated:</b> <ul style="list-style-type: none"> <li>• <a href="#">Table 124: "MII Control Register (Page 10h–14h: Address 00h–01h)," on page 194</a></li> <li>• <a href="#">Table 128: "Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h)," on page 196</a></li> <li>• <a href="#">Table 133: "1000BASE-T Control Register (Page 10h–14h: Address 12h–13h)," on page 201</a></li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 53115S-DS05-R   | 02/22/10    | <b>Updated:</b> <ul style="list-style-type: none"> <li>• Removed TxExcessiveCollision (32 bit) from Table 21: "Transmit-Only Counters (17)," on page 79</li> <li>• "LED Interfaces" on page 116 <ul style="list-style-type: none"> <li>– Added note after Table 30: "LED Output Pins per Port," on page 117</li> <li>– Updated paragraph before Figure 45: "LED Interface Block Diagram," on page 119</li> </ul> </li> <li>• Default for DUPLEX_STATE in Table 77: "Duplex Status Summary Register (Page 01h: Address 08h–09h)," on page 167</li> <li>• Description for bits [21:19] and [10:8] in Table 237: "Port Rate Control Register (Page 41h: Address 10h–33h)," on page 280</li> <li>• Description for bits [10:8] in Table 239: "Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h)," on page 283</li> <li>• Default values in Table 260: "Loop Detection Control Registers (Page 72h: Address 00h–01h)," on page 293</li> <li>• Maximum for VESD in Table 276: "Absolute Maximum Ratings," on page 299</li> <li>• t109 and Maximum for t105 in Table 279: "Reset and Clock Timing," on page 302</li> </ul> |
| 53115S-DS04-R   | 09/09/09    | <b>Updated:</b> <ul style="list-style-type: none"> <li>• "GMII/RGMII/MII/RvMII" to "GMII/RGMII/MII/RvMII/TMII" and "GMII/RGMII/SGMII/MII/RvMII" to "GMII/RGMII/SGMII/MII/RvMII/TMII" interface to interface</li> <li>• "Port" to "Interface" in "Frame Management Port Interface" on page 54</li> </ul> <b>Added:</b> <ul style="list-style-type: none"> <li>• "TMII Interface Timing" on page 257</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 53115S-DS03-R   | 01/13/09    | <b>Updated:</b> <ul style="list-style-type: none"> <li>• Table 29, "Signal Type Definitions," on page 85</li> <li>• Table 37, "Port Control Register (Page 00h: Address 00h–05h)," on page 112</li> <li>• Table 62, "Port State Override Register (Page 00h: Address 58h–5Fh)," on page 125</li> <li>• Table 84, "Mirror Capture Control Register (Page 02h: Address 10h–11h)," on page 133</li> </ul> <b>Added:</b> <ul style="list-style-type: none"> <li>• Figure 65, "Marking Information," on page 272</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

| <b>Revision</b> | <b>Date</b> | <b>Change Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
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| 53115S-DS02-R   | 08/25/08    | <p><b>Updated:</b></p> <ul style="list-style-type: none"> <li>• Default FDX value in Table 164, "MII Control Register (Page 15h: Address 00h-01h)," on page 193</li> <li>• Default PAUSE value in Table 166, "Auto-Negotiation Advertisement Register (Page 15h: Address 08h-09h)," on page 195</li> <li>• Table 170, "SerDes/SGMII Control 1 Register (Page 15h: Address 20h-21h, Block0)," on page 198</li> <li>• Table 172, "SerDes/SGMII Control 3 Register (Page 15h: Address 24h-25h, Block0)," on page 201</li> <li>• Table 173, "SerDes/SGMII Status 1 Register (Page 15h: Address 28h-29h, Block0)," on page 203</li> <li>• Table 174, "SerDes/SGMII Status 2 Register (Page 15h: Address 2Ah-2Bh, Block0)," on page 204</li> <li>• Table 180, "Analog TX1 Register (Page 15h: Address 20h, Block3)," on page 209</li> <li>• Default RESERVED[15:4] value in Table 181, "Analog TX2 Register (Page 15h: Address 22h, Block3)," on page 210</li> <li>• Table 182, "Analog TXAMP Register (Page 15h: Address 24h, Block3)," on page 210</li> <li>• Table 183, "Analog RX1 Register (Page 15h: Address 26h, Block3)," on page 211</li> <li>• Table 275, "Electrical Characteristics," on page 264</li> <li>• RESET low pulse duration values in Table 276, "Reset and Clock Timing," on page 265</li> </ul> |

| <b>Revision</b> | <b>Date</b> | <b>Change Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
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| 53115S-DS01-R   | 05/13/08    | <p><b>Updated:</b></p> <ul style="list-style-type: none"> <li>• Descriptive text in “IGMP Snooping” on page 17</li> <li>• Descriptive text in “CableChecker™” on page 21</li> <li>• Figure 8, “Address Table Organization,” on page 23</li> <li>• IMP_VOL_SEL[1:0], GMII_VOL_SEL[1:0], and SD_PLLAVDD33 text in Table 29, “Signal Type Definitions,” on page 88</li> <li>• Bit 3 and Bit 4 text in Table 42, “LED Refresh Register (Page 00h: Address 0Fh),” on page 117</li> <li>• Default in Table 43, “LED Function 0 Control Register (Page 00h: Address 10h–11h),” on page 118</li> <li>• Default in Table 44, “LED Function 1 Control Register (Page 00h: Address 12h–13h),” on page 119</li> <li>• Bit description in Table 45, “LED Function Map Register (Page 00h: Address 14h–15h),” on page 119</li> <li>• Bit description in Table 46, “LED Enable Map Register (Page 00h: Address 16h–17h),” on page 120</li> <li>• Bit description in Table 47, “LED Mode Map 0 Register (Page 00h: Address 18h–19h),” on page 120</li> <li>• Bit description in Table 51, “WAN Port Select Register (Page 00h: Address 26h–27h),” on page 122</li> <li>• Bit description in Table 81, “Broadcom Tag Control Register (Page 02h: Address 03h),” on page 135</li> <li>• CPU priority map to CPU CoS map in Table 200, “CPU_To_CoS Map Register (Page 30h: Address 64h–67h),” on page 224</li> <li>• Supply voltage parameter in Table 273, “Absolute Maximum Ratings,” on page 263</li> <li>• Supply voltage parameter in Table 274, “Recommended Operating Conditions,” on page 263</li> <li>• Typical values in Table 275, “Electrical Characteristics,” on page 264</li> </ul> <p><b>Deleted:</b></p> <ul style="list-style-type: none"> <li>• “two time sensitive queues” statement from IEEE feature bullet on cover page</li> <li>• Third sentence in first paragraph of “CableChecker™” on page 21</li> </ul> |
| 53115S-DS00-R   | 10/09/07    | Initial release                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

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# About This Document

## Purpose and Audience

This document is for designers interested in integrating the BCM53115S switches into their hardware designs and for others who need specific data about the physical characteristics and operation of the BCM53115S switches.

## Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to:  
<http://www.broadcom.com/press/glossary.php>.

## Document Conventions

The following conventions may be used in this document:

| <b>Convention</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | <b>Description</b>                                                                                                                                                      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Bold</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | User input and actions: for example, type <b>exit</b> , click <b>OK</b> , press <b>Alt+C</b>                                                                            |
| Monospace                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Code: <code>#include &lt;iostream&gt;</code><br>HTML: <code>&lt;td rowspan = 3&gt;</code><br>Command line commands and parameters: <code>w1 [-1] &lt;command&gt;</code> |
| <code>&lt; &gt;</code>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Placeholders for <i>required</i> elements: enter your <code>&lt;username&gt;</code> or <code>w1 &lt;command&gt;</code>                                                  |
| <code>[ ]</code>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Indicates <i>optional</i> command-line parameters: <code>w1 [-1]</code><br>Indicates bit and byte ranges (inclusive): <code>[0:3]</code> or <code>[7:0]</code>          |
| <b>Data Sheet Notational Conventions</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                         |
| <ul style="list-style-type: none"><li>Signal names are shown in uppercase letters (such as DATA).</li><li>A bar over a signal name indicates that it is active low (such as <math>\overline{\text{CE}}</math>).</li><li>In register and signal descriptions, <code>[n:m]</code> indicates a range from bit n to bit m (such as <code>[7:0]</code> indicates bits 7 through 0, inclusive).</li><li>The use of R or Reserved indicates that a bit or a field is reserved by Broadcom for future use. Typically, R is used for individual bits and Reserved is used for fields.</li><li>Numerical modifiers such as K or M follow traditional usage (for example, 1 KB means 1,024 bytes, 100 Mbps [referring to fast Ethernet speed] means 100,000,000 bps, and 133 MHz means 133,000,000 Hz).</li></ul> |                                                                                                                                                                         |

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## Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (<https://support.broadcom.com>). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads and Support site (<http://www.broadcom.com/support/>).

# Section 1: Introduction

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## Overview

The BCM53115S is a single-chip, seven-port Gigabit Ethernet (GbE) switch device. It provides:

- A seven-port nonblocking 10/100/1000 Mbps switch controller
- Five ports with 10/100/1000BASE-TX-compatible transceivers
- Seven integrated Gigabit MACs (GMACs)
- One GMII/RGMII/MII/RvMII/TMII port for PHY-less connection to the management agent
- One GMII/RGMII/SGMII/MII/RvMII/TMII interface for WAN port
- An integrated Motorola® SPI-compatible interface
- High performance, integrated packet buffer memory
- An address resolution engine
- A set of management information base (MIB) statistics registers

The GMACs support full-duplex and half-duplex modes for 10 Mbps and 100 Mbps and full-duplex for 1000 Mbps. Flow control is supported in the half-duplex mode with backpressure. In full-duplex mode, IEEE 802.3x frame-based flow control is supported. The GMACs are IEEE 802.3-compliant and support maximum frame sizes of 9720 bytes.

An integrated address management engine provides address learning and recognition functions at maximum frame rates. The address table provides capacity for learning up to 4K unicast addresses. Addresses are added to the table after receiving an error-free packet.

The MIB statistics registers collect receive and transmit statistics for each port and provide direct hardware support for the Ether-like MIB, MIB II (interfaces), and the first four groups of the RMON MIB. All nine groups of RMON can be supported by using additional capabilities, such as port mirroring/snooping, together with an external microcontroller to process some MIB attributes. The MIB registers can be accessed through the Serial Peripheral Interface Port by an external microcontroller.

## Section 2: Features and Operation

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### Overview

The BCM53115S switches include the following features:

- “Quality of Service” on page 34
- “Port-Based VLAN” on page 38
- “IEEE 802.1Q VLAN” on page 39
- “Double-Tagging” on page 40
- “Jumbo Frame Support” on page 43
- “Port Trunking/Aggregation” on page 43
- “WAN Port” on page 44
- “Rate Control” on page 44
- “Protected Ports” on page 47
- “Port Mirroring” on page 47
- “IGMP Snooping” on page 49
- “MLD Snooping” on page 49
- “IEEE 802.1x Port-Based Security” on page 49
- “DoS Attack Prevention” on page 51
- “MSTP Multiple Spanning Tree” on page 52
- “Software Reset” on page 52
- “Loop Detection” on page 52
- “CableChecker™” on page 53
- “CableChecker™” on page 53
- “Egress PCP Remarking” on page 54
- “Address Management” on page 54

The following sections discuss each feature in more detail.

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## Quality of Service

The Quality of Service (QoS) feature provides up to six internal queues per port to support eight different traffic classes (TC). The traffic classes can be programmed so that higher-priority TC in the switch experiences less delay than lower-priority TC under congested conditions. This can be important in minimizing latency for delay-sensitive traffic. The BCM53115S switches can assign the packet to one of the six egress transmit queues according to information in:

- [“Port-Based QoS” on page 36](#) (ingress port ID)
- [“IEEE 802.1p QoS” on page 36](#)
- [“MACDA-Based QoS” on page 36](#)
- [“TOS/DSCP QoS” on page 36](#)

The [“TC Decision Tree” on page 37](#) decides which priority system is used based on three programmable register bits detailed in [Table 1: “TC Decision Tree Summary,” on page 37](#). The corresponding traffic class is then assigned to one of the six queues on a port-by-port basis.

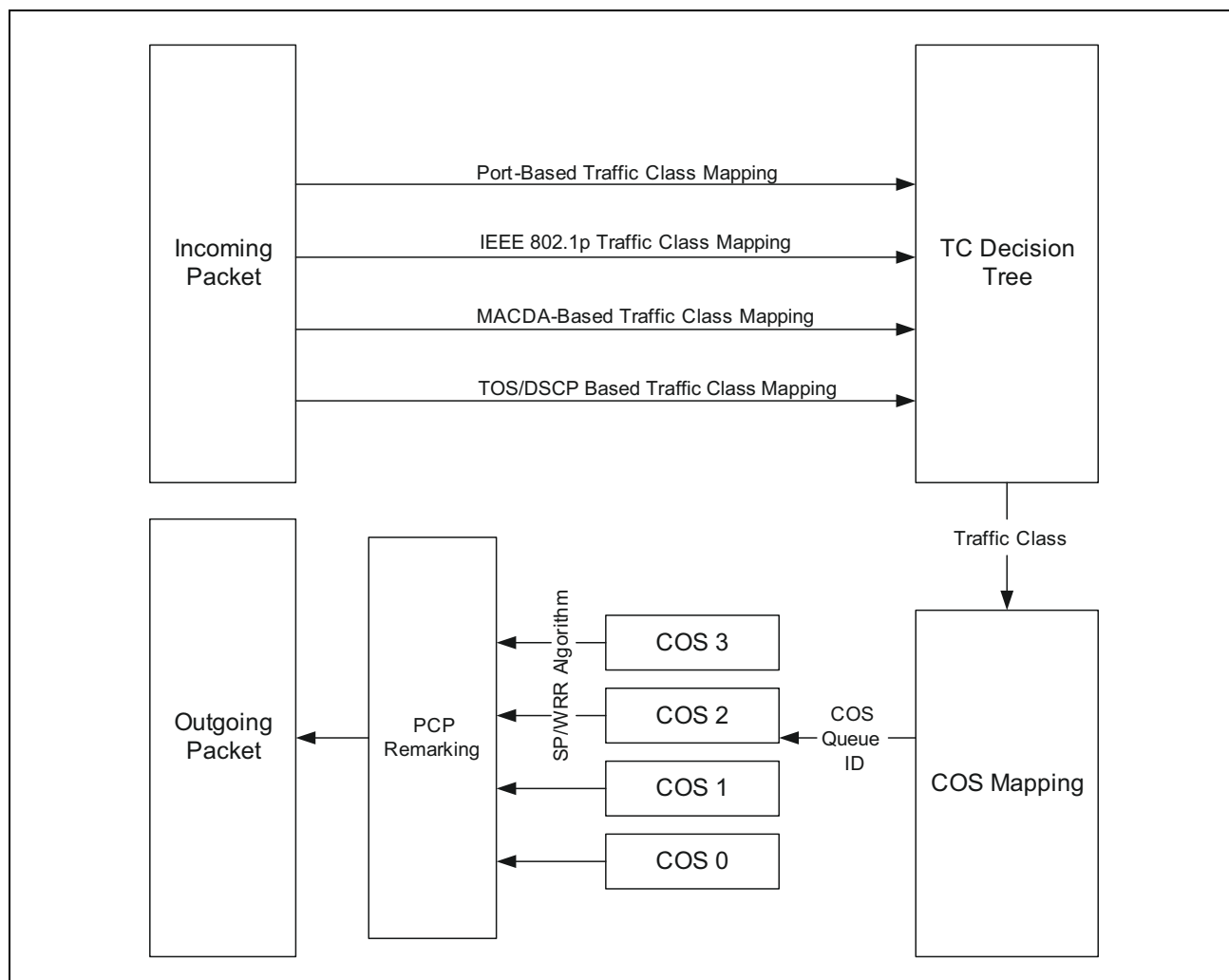


Figure 2: QoS Program Flow

## Egress Transmit Queues

Each Ethernet egress port has six transmit queues (CoS0–CoS3). Each Cos queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purpose. Every Ethernet (ingress) port has its own set of counters to measure the buffer occupancy and the arrival rate related to the traffic received from the port.

The IMP (egress) port serves four queues (CoS0–CoS3) and the traffic generated by the Local Management Packet Generator which generate management report messages back to CPU.

Each CoS queue has its own dedicated counter to measure the buffer occupancy of the queue for congestion management purpose. The IMP (ingress) port also has its own set of counters to measure the buffer occupancy and the arrival rate to the traffic received from the port, but should be used only if it is configured as a regular Ethernet port.

All incoming frames are assigned to an egress transmit queue depending on their assigned TC. Each egress transmit queue is a list specifying an order for packet transmission. The corresponding egress port transmits packets from each of the queues according to a programmable algorithm, with the higher TC queues being given greater access than the lower TC queues. Queue 0 is the lowest-TC queue.

The BCM53115S uses strict priority (SP) and weighted round robin (WRR) algorithm for CoS0–CoS3 queues scheduling. The scheduling is configurable “[TX Queue Control Register \(Page 30h: Address 80h\)](#)” on page 256. as one of following combination of SP and WRR; 4SP, 4WRR, 1SP and 3WRR, 2SP and 2WRR The WRR algorithm weights for each queue can be programmed using the “[TX Queue Weight Register \(Page 30h: Address 81h\)](#)” on page 257.

## Port-Based QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with the TC configured for the corresponding port. The mapping mechanism is globally enabled/disabled by programming the “[QoS Global Control Register \(Page 30h: Address 00h\)](#)” on page 251, the mapping entry is also per-port configured using the “[Default IEEE 802.1Q Tag Register \(Page 34h: Address 10h\)](#)” on page 267. When disabled, the TC that results from this mapping is 000.

## IEEE 802.1p QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC-configured for the corresponding IEEE 802.1p priority code point (PCP). The mapping mechanism is per port enabled/disabled using the “[QoS IEEE 802.1p Enable Register \(Page 30h: Address 04h\)](#)” on page 251, the mapping entries are per-port configured by “[Port N \(N=0-5, 8\) PCP\\_To\\_TC Register \(Page 30h: Address 10h\)](#)” on page 252. When disabled or if the incoming packet is not tagged, the TC that results from this mapping is 000.

## MACDA-Based QoS

MACDA-Based QoS is enabled when the IEEE 802.1p QoS is disabled using the 802\_1P\_EN bit in the “[QoS IEEE 802.1p Enable Register \(Page 30h: Address 04h\)](#)” on page 251. When using MACDA-based QoS, the destination address and VLAN ID is used to index the ARL table as described in “[Address Management](#)” on page 54. The matching ARL entry contains a 3-bit TC field as shown in [Table 7 on page 57](#). These bits set the MACDA-based TC for the frame. The MACDA-based TC is assigned to the TC bits depending upon the result shown in [Table 1 on page 37](#). The TC bits for a learned ARL entry default to 0. To change the default, an ARL entry is written to the ARL table as described in the “[Writing an ARL Entry](#)” on page 61. For more information about the egress transmit queues, see “[Egress Transmit Queues](#)” on page 35.

## TOS/DSCP QoS

The TC of a packet received from an Ethernet (or IMP) port is assigned with TC configured for the corresponding IP TOS/DSCP. The mapping mechanism is per port enabled/disabled using the “[QoS DiffServ Enable Register \(Page 30h: Address 06h\)](#)” on page 252, the mapping entries are globally configured by “[DiffServ Priority Map 0 Register \(Page 30h: Address 30h\)](#)” on page 253 through “[DiffServ Priority Map 3 Register \(Page 30h: Address 42h\)](#)” on page 255. When disabled or the incoming packet is not of IPv4/v6 type, the TC resulted from this mapping is 000.

## TC Decision Tree

The TC decision tree determines which priority system is assigned to TC-mapping bits for the given frame. As summarized above, the TC bits for the frame can be determined according to the ingress port-based TC, IEEE 802.1p TC, MACDA-based TC, or DiffServ TC. The decision on which TC mapping to use is based on the Port\_QoS\_En bit and the QoS\_Layer\_Sel bits of the “QoS Global Control Register (Page 30h: Address 00h)” on page 251. Table 1 summarizes how these programmable bits affect the derived TC. The DiffServ and IEEE 802.1p QoS TC are only available if the respective QoS is enabled, and the received packet has the appropriate tagging.

**Table 1: TC Decision Tree Summary**

| Port_QoS_En | QoS_Layer_Sel | Value of TC Bits                                                                                                                          |
|-------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 0           | 00            | IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping.                                                                   |
| 0           | 01            | DiffServ TC mapping if available; otherwise, TC = 000.                                                                                    |
| 0           | 10            | DiffServ TC mapping for IP frame; otherwise, IEEE 802.1p TC mapping if available; otherwise, MACDA-based TC mapping.                      |
| 0           | 11            | The highest available TC of the following: IEEE 802.1p TC mapping, DiffServ TC mapping, or MACDA-based TC mapping.                        |
| 1           | 00            | Port-based TC mapping.                                                                                                                    |
| 1           | 01            | Port-based TC mapping.                                                                                                                    |
| 1           | 10            | Port-based TC mapping.                                                                                                                    |
| 1           | 11            | The highest available TC of the following: Port-based TC mapping, IEEE 802.1p TC mapping, DiffServ TC mapping, or MACDA-based TC mapping. |

## Queuing Class (CoS) Determination

The BCM53115S supports the CoS mapping through the mapping mechanisms listed below.

- TC to CoS mapping: The queuing class to forward a packet to an Ethernet port is mapped from the TC determined for the packet. The mapping entries are globally configured using the “TC\_To\_CoS Mapping Register (Page 30h: Address 62h–63h)” on page 255.
- CPU to CoS mapping: The queuing class to forward a packet to the external CPU through the IMP port is determined based on the reasons to forward (copy or trap) the packet to CPU. The mapping entries are globally configured using the “CPU\_To\_CoS Map Register (Page 30h: Address 64h–67h)” on page 256.



**Note:** When the BCM53115S is configured in the aggregation mode where the IMP operates as the uplink port to the upstream network processor, the CoS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operates as the interface to the management CPU, and the CoS is decided based on the reasons for forwarding the packet to the CPU.

Table 2 shows the reasons for forwarding a packet to the CPU.

**Table 2: Reasons to Forward a Packet to the CPU**

| <b>ToCPU Reason</b>               | <b>Description</b>                                                                                                                                                                                                            | <b>ToCPU CoS</b> |
|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| Mirroring                         | The packet is forwarded (copied) through the IMP port, because it must be mirrored to the CPU as the capturing device.                                                                                                        | 0                |
| SA Learning                       | The packet is forwarded (copied) through the IMP port, because its SA must be learned by the CPU.                                                                                                                             | 0                |
| Switching                         | The packet is forwarded through the IMP port, because the CPU is one of the intended destination hosts of the packet.                                                                                                         | 0                |
| Protocol Termination              | The packet is forwarded (trapped) through the IMP port because it implies an IEEE 802.1 defined L2 protocol that must be terminated by the CPU.                                                                               | 0                |
| Protocol Snooping                 | The packet is forwarded (copied) through the IMP port because it implies an L3 or application level protocol that must be monitored by the CPU for network security or operation efficiency.                                  | 0                |
| Exception Processing/<br>Flooding | The packet is forwarded (trapped) through the IMP port for some special processing even though the CPU is not the intended destination or because the switch makes the flooding decision to reach all potential destinations. | 0                |

The ToCPU CoS values listed in [Table 2](#) are the default setting and are configurable. In order to prevent out of order delivery of the same packet flow to the CPU, the CoS for the mirroring and SA learning reasons must be programmed with a value that is lower than or equal to the value of the other reasons.

A packet could be forwarded to the CPU for more than one reason, therefore the CoS selection is based on the highest CoS values among all the reasons for the packet.

## Port-Based VLAN

The port-based virtual LAN (VLAN) feature partitions the switching ports into virtual private domains designated on a per port basis. Data switching outside of the port's private domain is not allowed. The BCM53115S provide flexible VLAN configuration for each ingress (receiving) port.

The port-based VLAN feature works as a filter, filtering out traffic destined to nonprivate domain ports. The private domain ports are selected for each ingress port using the [“Port-Based VLAN Control Register \(Page 31h: Address 00h\)” on page 258](#). For each received packet, the ARL resolves the DA and obtains a forwarding vector (list of ports to which the frame will be forwarded). The ARL then applies the VLAN filter to the forwarding vector, effectively masking out the nonprivate domain ports. The frame is only forwarded to those ports that meet the ARL table criteria, as well as the port-based VLAN criteria.

# IEEE 802.1Q VLAN

The BCM53115S support IEEE 802.1Q VLAN and up to approximately 4000 VLAN table entries that reside in the internal embedded memory. Once the VLAN table is programmed and maintained by the microcontroller, the BCM53115S autonomously handle all operations of the protocol. These actions include the stripping or adding of the IEEE 802.1Q tag, depending on the requirements of the individual transmitting port. It also performs all the necessary VLAN lookups in addition to MAC L2 lookups.

## IEEE 802.1Q VLAN Table Organization

Each VLAN table entry, also referred to as a VLAN ID, an Untag map, and a Forward map.

- The Untag map controls whether the egress packet is tagged or untagged.
- The Forward map defines the membership within a VLAN domain.
- The FWD\_MODE indicates whether the packet forwarding should be based on VLAN membership or on ARL flow.

The Untag map and Forward map include bit-wise representation of all the ports.

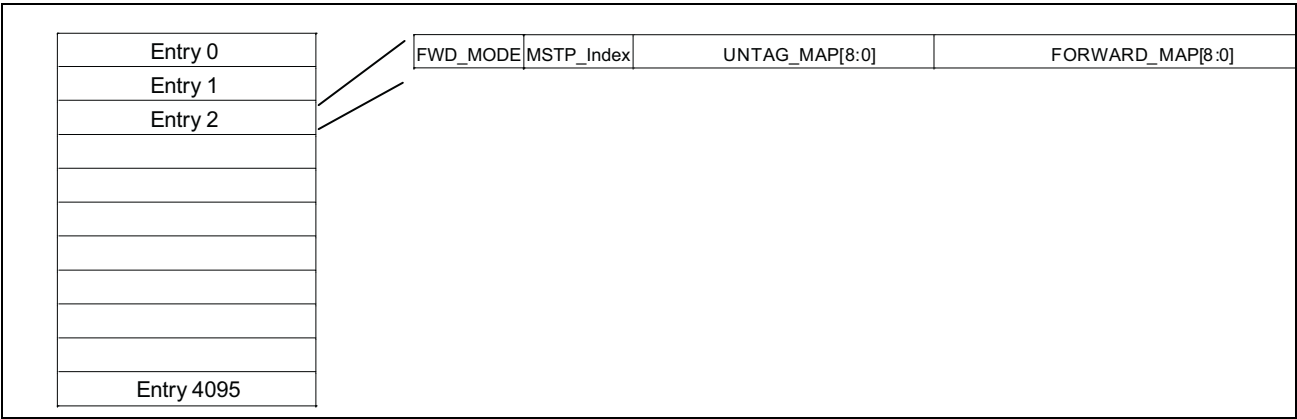


Figure 3: VLAN Table Organization



**Note:** If the MII port is configured as a management port, then the tag is not stripped even if the untag bit is set.

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## Programming the VLAN Table

The IEEE 802.1Q VLAN feature can be enabled by writing to the Enable IEEE 802.1Q bit in the “[Global IEEE 802.1Q Register \(Pages 34h: Address 00h\)](#)” on page 261. The default priority and VID can be assigned to each port in the “[Default IEEE 802.1Q Tag Register \(Page 34h: Address 10h\)](#)” on page 267. These are necessary when tagging a previously untagged frame. The Hashing algorithm uses either [VID, MAC] or [MAC] for the ARL index key, depending on the VLAN Learning Mode bits in the “[Global IEEE 802.1Q Register \(Pages 34h: Address 00h\)](#)” on page 261. If both the VID and MAC address are used, a single MAC address is able to be a member of multiple VLANs simultaneously.

The VLAN table can be written using the following steps:

1. Use the “[VLAN Table Entry Register \(Page 05h: Address 83h–86h\)](#)” on page 190 to define the ports that are part of the VLAN group and the ports that should be untagged.
2. Use the “[VLAN Table Address Index Register \(Page 05h: Address 81h\)](#)” on page 190 to define the VLAN ID of the VLAN group.



**Note:** VLAN ID 0xFFFF is reserved. However VID = 0xFFFF can be forwarded if the VID\_FFF\_Fwding bit is set in the “[Global VLAN Control 5 Register \(Page 34h: Address 06h\)](#)” on page 265.

3. Set bit [1:0] = 00 of the “[VLAN Table Read/Write/Clear Control Register \(Page 05h: Address 80h\)](#)” on page 189 to indicate a write operation.
4. Set bit 7 of the “[VLAN Table Read/Write/Clear Control Register \(Page 05h: Address 80h\)](#)” on page 189 to 1, starting the write operation. This bit returns to 0 when the write is complete.

The VLAN table can be read using the following steps:

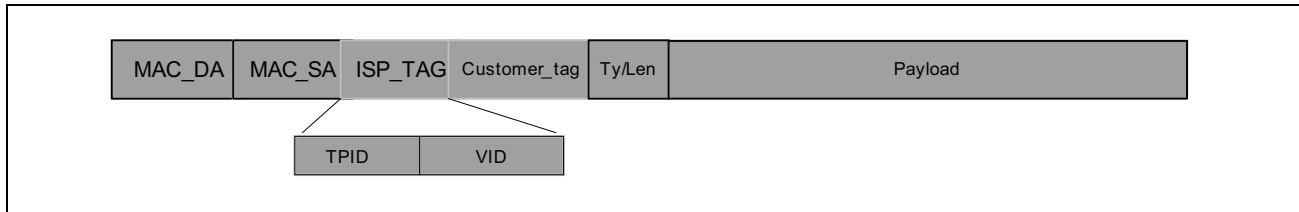
1. Use the “[VLAN Table Address Index Register \(Page 05h: Address 81h\)](#)” on page 190 to define from which VLAN group to read the data.
2. Set bit [1:0] = 01 of the “[VLAN Table Read/Write/Clear Control Register \(Page 05h: Address 80h\)](#)” on page 189 to indicate a read operation.
3. Set bit 7 of the “[VLAN Table Read/Write/Clear Control Register \(Page 05h: Address 80h\)](#)” on page 189 to 1 to start the read operation. This bit returns to 0 when the read is complete.
4. Read the “[VLAN Table Entry Register \(Page 05h: Address 83h–86h\)](#)” on page 190 to obtain the VLAN table entry information.

---

## Double-Tagging

The BCM53115S provide the double-tagging feature, which is useful for ISP applications. When the ISP aggregates incoming traffic from each individual customer, the extra tag (double-tag) can provide an additional layer of tagging to the existing IEEE 802.1Q VLAN. The ISP tag (extra tag) is a way of separating individual customers from other customers. Using the IEEE 802.1Q VLAN tag, the individual customer’s traffic can be separated.

When the double-tagging feature is enabled using the “[Global VLAN Control 4 Register \(Page 34h: Address 05h\)](#)” on page 264 and the Enable IEEE 802.1Q (bit7) of “[Global IEEE 802.1Q Register \(Pages 34h: Address 00h\)](#)” on page 261, users can expect two VLAN tags in a frame: the tag close to MAC\_SA is the ISP tag and the one following is the customer tag as shown in [Figure 4](#).



**Figure 4: ISP Tag Diagram**

The switch uses the ISP tag for ARL and VLAN table accesses and the customer tag as an IEEE 802.1Q tag. There is a per chip programmable register Double Tagging TPID register for ISP tag (default = 9100'h). All ISP tags will be qualified by this Tag Protocol ID (TPID) value.

When the double-tagging feature is enabled, all switch ports are separated into two groups, ISP ports and customer ports. The BCM53115S performs the normalization process for all ingress frames, whether from the ISP port or customer port. The normalization process is to insert an ISP tag, customer tag, or ISP + customer tag (depending whether the ingress frame is without tags or with one tag) to allow all ingress frames with a double-tag. But if the ingress frames are with a double-tag (ISP + customer tag), and the ISP tag TPID matches the TPID specified in the Double Tagging TPID register, it does not perform the normalization process. The ISP ports are defined in the ISP Port Selection Portmap register. When the port (s) corresponding bit(s) are set, that port (s) should be connected ISP, and otherwise connected to customers. Each switch device can have multiple ports assigned as ISP ports, and each ISP is uniquely identified using different VLAN forward maps or the port-based VLAN feature.

## ISP Port

It is possible for ISP port to receive three different types of frames: untagged, ISP-tagged, and ISP+customer-tagged frames.

When the double-tagging feature is enabled and the received frame is untagged (or the TPID does not match with ISP TPID specified in Double Tagging TPID register, the default ISP tag and customer tag are added, and VLAN ID of ISP tag receives it from the port default VID. The frames are forwarded according to the VLAN table. However, if the Port-Based VLAN Control register is enabled, the egress ports specified in the port-VLAN control register override the VLAN table settings. If the received frame is ISP tagged (TPID matches with the ISP tag VLAN ID specified in the double-tagging TPID register), the default customer tag (8100 + default PVID) is added, the ISP VID is used to access the ARL table, and the ISP tag can be stripped on the way out according to the untagged bit setting in the VLAN table. In addition, ISP port frame can forward to the destination port directly based on forward port map of VLAN table by setting FWD\_MODE bit to 1 of VLAN Table Entry register.

The VLAN ID is generated from the ISP tag, and TC is generated from the ingress frame outer tag.

## Customer Port

It is also possible for Customer port to receive two different types of frames: untagged and customer-tagged frames.

When the double-tagging feature is enabled, all the ingress frames perform the normalization process to insert a ISP tag or ISP + Customer tag (depending whether the ingress frame is without tags or with one tag) to allow all ingress frames with a double-tag. The VLAN ID of ISP tag receives it from the port default VID.

The VLAN ID is generated from the ISP tag, and the TC is generated from the ingress frame outer tag.



**Note:** It is illegal to strip out the ISP tag on the ISP egress port by using the untagged bit setting in the VLAN table.



**Note:** Only the VLAN tagged or untagged packets are expected for the ingress of the customer ports. The customer do not add the ISP tags.

There are two possible traffic scenarios; one from a customer port to an ISP port, and one from an ISP port to a customer port.

## Uplink Traffic (from Customer Port to ISP)

Data traffic is traffic received from the customer port without tags or a customer tag, and the frame is destined for an ISP port. The customer ingress port performs a normalization process to allow ingress frames with double-tags (ISP + Customer tag), and the ISP tag VID is based on the port default VID tag.

However, if the ingress frame is with an 802.1p tag, the VID of 802.1p tag is changed by the VID of port default VID tag after the customer port normalization process. The TC do not change.

Control traffic frames can be forwarded to the CPU first and then the CPU forwards to the ISP port if the switch management mode is enabled and if the RESV\_MCAST\_FLOOD bit=0 in the Global VLAN Control 4 register. In this case, the control frame adds an ISP tag by ingress port and forward to the CPU. The CPU can then forward it to the ISP port with or without the ISP tag by using the egress-direct feature.

## Downlink Traffic (from ISP to Customer Port)

Data traffic frame received from ISP port may or may not have ISP tag attached. When the received frame does not have an ISP tag and customer tag, the ISP ingress port does a normalization process to insert double-tags (ISP + Customer tag), and the ISP tag VID is based on the port default VID tag. All ARL and VID table access should be based on the new tag. The traffic is then forwarded to the customer port through proper VLAN configuration. Usually, the software configures so the customer Egress port continuously removes the ISP tag. However, it is based on how the untagged map is configured.

Moreover, if the ingress frame is with an 802.1p tag, the VID of 802.1p tag is changed by the VID of port default VID tag after the ISP port normalization process. The TC will not change.

The Control traffic is forwarded to the CPU when the switch management mode is enable and if the RESV\_MCAST\_FLOOD bit=0 in the Global VLAN Control 4 register. The BCM53115S can also support multiple ISP port configurations by enabled the FWD\_MODE bit of VLAN Table Entry register. There are also two ways to separate traffic that belongs to two different ISP customers:

- Each group (ISP, and customer) is assigned to the same VLAN group, so that traffic does not leak to other ISP.
- Use the Port-based VLAN to separate traffic that belongs to a different ISP.

---

## Jumbo Frame Support

The BCM53115S can receive and transmit frames of extended length on ports linked at gigabit speed. Referred to as jumbo frames, these packets are longer than the standard maximum size which is defined using the [“Standard Maximum Frame Size Register \(Page 40h: Address 05h\)” on page 273](#), but shorter than 9720 bytes. Jumbo packets can only be received or forwarded to 1000BASE-T linked ports that are jumbo-frame enabled. Up to 38 buffer memory pages are required for storing the longest allowed jumbo frame. While there is no physical limitation to the number of ports that can be jumbo enabled, it is recommended that no more than two be enabled simultaneously to ensure system performance. There is no performance penalty for enabling additional jumbo ports beyond the potential strain on memory resources that can occur due to accumulated jumbo packets at multiple ports.

---

## Port Trunking/Aggregation

The BCM53115S supports MAC-based trunking. The trunking feature allows up to four ports to be grouped together as a single-link connection between two switch devices. This increases the effective bandwidth through a link and provides redundancy. The BCM53115S allow up to two trunk groups. Trunks are composed of predetermined ports and can be enabled using the Trunking Group 0 register. Ports within a trunk group must be of the same linked speed. By performing a dynamic hashing algorithm on the MAC address, each packet destined for the trunk is forwarded to one of the valid ports within the trunk group. This method has several key advantages. By dynamically performing this function, the traffic patterns can be more balanced across the ports within a trunk. In addition, the MAC-based algorithm provides dynamic failover. If a port within a trunking group fails, the other port within the trunk automatically assumes all traffic designated for the trunk. It allows for a seamless, automatic redundancy scheme. This hashing function can be performed on either the DA, SA, or DA/SA, depending on the Trunk Hash Selector bit of the [“MAC Trunking Control Register \(Page 32h: Address 00h\)” on page 259](#).

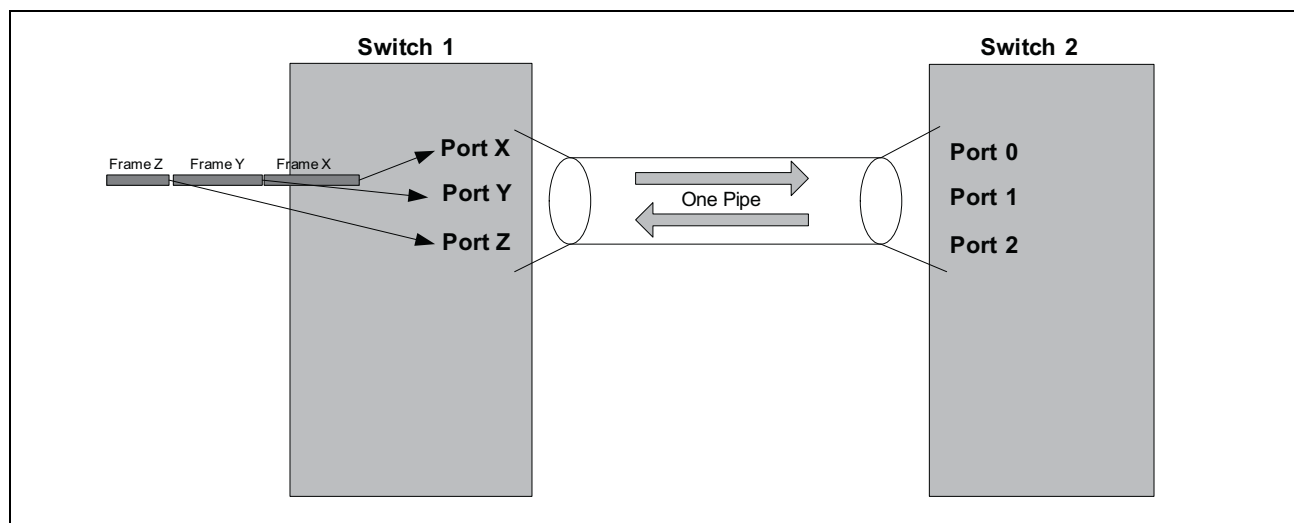


Figure 5: Trunking

## WAN Port

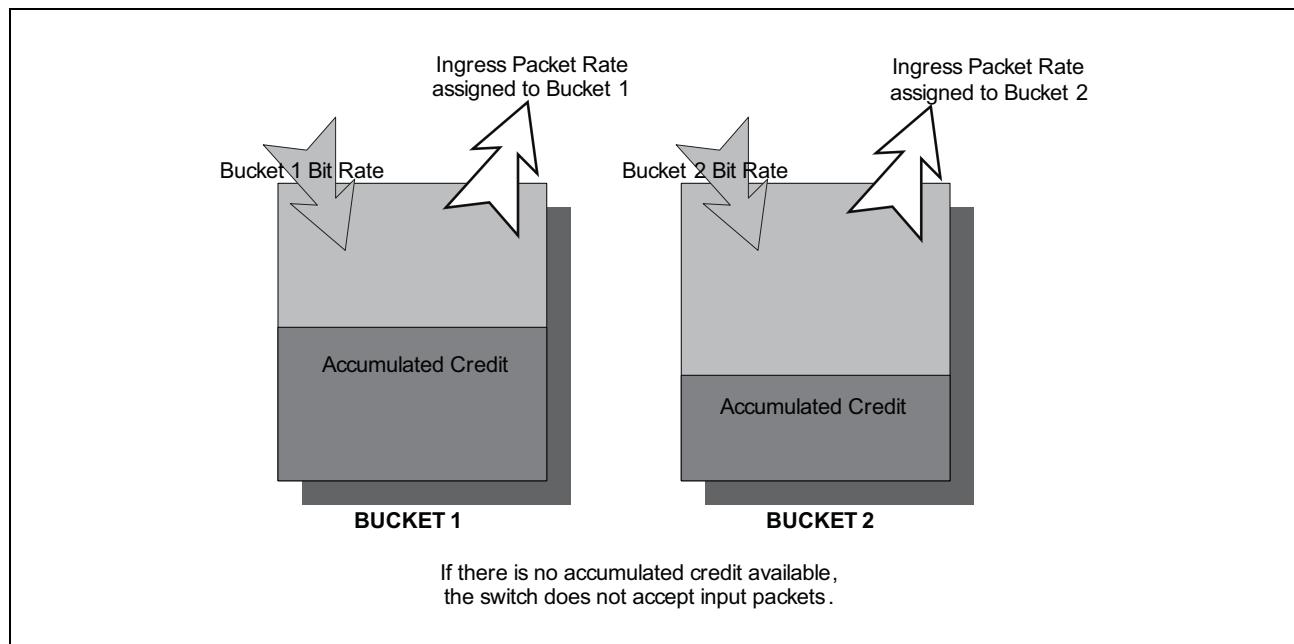
The BCM53115S offers a programmable WAN port feature: It has a WAN Port Select register (page 00h, address 26h). Select a port as a WAN port, then all that port's traffic is forwarded to the CPU port only. The non-WAN port traffic from all other local ports does not flood to the WAN port.

## Rate Control

### Ingress Rate Control

Forwarding broadcast traffic consumes switch resources, which can negatively impact the forwarding of other traffic. The rate-based broadcast storm suppression mechanism is used to protect regular traffic from an overabundance of broadcast or multicast traffic. This feature monitors the rate of ingressed traffic of programmable packet types. If the rates of these packet types exceed the programmable maximum rate, the packets are dropped. To enable the Broadcast Storm Suppression, pull the BC\_SUPP\_EN high during power-on/reset. Alternatively, the feature can be activated in the ["Port Receive Rate Control Register \(Page 41h: Address 10h\)"](#) on page 276.

The broadcast storm suppression mechanism works on a credit-based rate system that figuratively uses a bucket to track the bandwidth of each port (see [Figure 6 on page 45](#)). Credit is continually added to the bucket at a programmable bucket bit rate. Credit is decremented from the bucket whenever one of the programmable packet types is ingressed at the port. If no packets are ingressed for a considerable length of time, the bucket credit continues to increase up to a programmable-maximum bucket size. If a heavy burst of traffic is suddenly ingressed at the port, the bucket credit becomes drained. When the bucket is emptied, incoming traffic is constrained to the bucket bit rate (the rate at which credit is added to the bucket). At this point, excess packets are either dropped or deterred using flow control, depending on the Suppression Drop mode in the “[Ingress Rate Control Configuration Register \(Page 41h: Address 00h\)](#)” on [page 275](#).



**Figure 6: Bucket Flow**

## Two-Bucket System

For added flexibility, the BCM53115S employs two buckets to track the rate of ingressed packets. Each of the two buckets (Bucket 0 and Bucket 1) can be programmed to monitor different packet types. For example, Bucket 0 could monitor broadcast packets, while Bucket 1 monitors multicast packets. Multiple packet types can be monitored by each bucket, and a packet type can be monitored by both buckets.

The rates of each bucket can be individually programmed (see “[Bucket Bit Rate](#)” on [page 46](#)). For example, the broadcast packets of Bucket 0 could have a maximum rate of 3 Mbps, whereas the multicast packets of Bucket 1 could be allowed up to 80 Mbps. The size of each bucket can be programmed using the Suppressed Packet Type Mask of the “[Ingress Rate Control Configuration Register \(Page 41h: Address 00h\)](#)” on [page 275](#). This determines the maximum credit that can accumulate in each bucket. The Rate Count and Bucket Size can be individually programmed for each port, providing another level of flexibility. Suppression control can be enabled or disabled on a per-port basis “[Ingress Rate Control Configuration Register \(Page 41h: Address 00h\)](#)” on [page 275](#). This system allows the user to control dual packet-type rates on a per-port basis.

## Egress Rate Control

The BCM53115S monitor the rate of egress traffic per port. Unlike the Ingress traffic rate control, the Egress Rate Control provides only the per port rate control regardless of traffic types. This feature only uses one bucket to track the rate of egressed packets. The Egress Rate Control feature can be enabled in the [“Port Egress Rate Control Configuration Register \(Page 41h: Address 80h–91h\)”](#) on page 279, and the output rate per port can be controlled by setting the bucket size and Refresh Count in the same register. The Egress Rate Control feature only support absolute bit rate mode (Bit Rate Mode = 0) and the bucket bit rate calculation is shown in [Table 3](#) on page 46.

## Bucket Bit Rate

The relative ingress rates of each bucket can be programmed using the [“Port Receive Rate Control Register \(Page 41h: Address 10h\)”](#) on page 276 on a per port basis. Each port has a programmable Rate Count value for Bucket 0 and Bucket 1. Additionally, the bit rate mode is programmed by the [“Ingress Rate Control Configuration Register \(Page 41h: Address 00h\)”](#) on page 275 on a chip basis. If this bit is 1, the packet rate is automatically scaled according to the port link speed. Ports operating at 1000 Mbps would be allotted a 100 times higher ingress rate than ports linked at 10 Mbps. Together, the Rate Count value and the bit rate mode determine the bucket bit rate, which is a reflection of how quickly data can be ingressed (Kbps) at the given port for a given bucket. The Rate Count values are specified in [Table 3](#). Values outside these ranges are not valid entries.

**Table 3: Bucket Bit Rate**

| Rate Count (RC) | Bit Rate Mode | Link Speed | Bucket Bit Rate Equation          | Approximate Computed Bucket Bit Rate Values (As a Function of RC) |
|-----------------|---------------|------------|-----------------------------------|-------------------------------------------------------------------|
| 1–28            | 0             | Any        | $= (RC \times 8 \times 1M)/125$   | 64 KB, 128 KB, 192 KB,..., 1.792 MB                               |
| 29–127          | 0             | Any        | $= (RC - 27) \times 1M$           | 2 MB, 3 MB, 4 MB,..., 100 MB                                      |
| 128–240         | 0             | Any        | $= (RC - 115) \times 1M \times 8$ | 104 MB, 112 MB, 120 MB,..., 1000 MB                               |
| 1–125           | 1             | 10 Mbps    | $= (RC \times 8 \times 1M)/100$   | 0.08 MB, 0.16 MB, 0.24 MB,... 10 MB                               |
| 1–125           | 1             | 100 Mbps   | $= (RC \times 8 \times 1M)/10$    | 0.8 MB, 1.6 MB, 2.4 MB,..., 100 MB                                |
| 1–125           | 1             | 1000 Mbps  | $= RC \times 8 \times 1M$         | 8 MB, 16 MB, 24 MB,... 1000 MB                                    |

**Note:** 1M represents  $1 \times 10^6$ .

## IMP Port Egress Rate Control

The IMP port egress is configurable of rate limiting at packet-per-second (PPS) granularity, in addition to bits-per-second (BPS) granularity. It can be configured using the [“IMP Port \(IMP/Port 5\) Egress Rate Control Configuration Register \(Page 41h: Address C0h–C1h\)”](#) on page 279.

## Protected Ports

The Protected Ports feature allows certain ports to be designated as protected using the “[Protected Port Selection Register \(Page 00h: Address 24h–25h\)](#)” on page 155. All other ports are unprotected. Traffic between protected port group members is blocked. However, protected ports are able to send traffic to unprotected ports. Unprotected ports can send traffic to any port. Several applications that can benefit from protected ports:

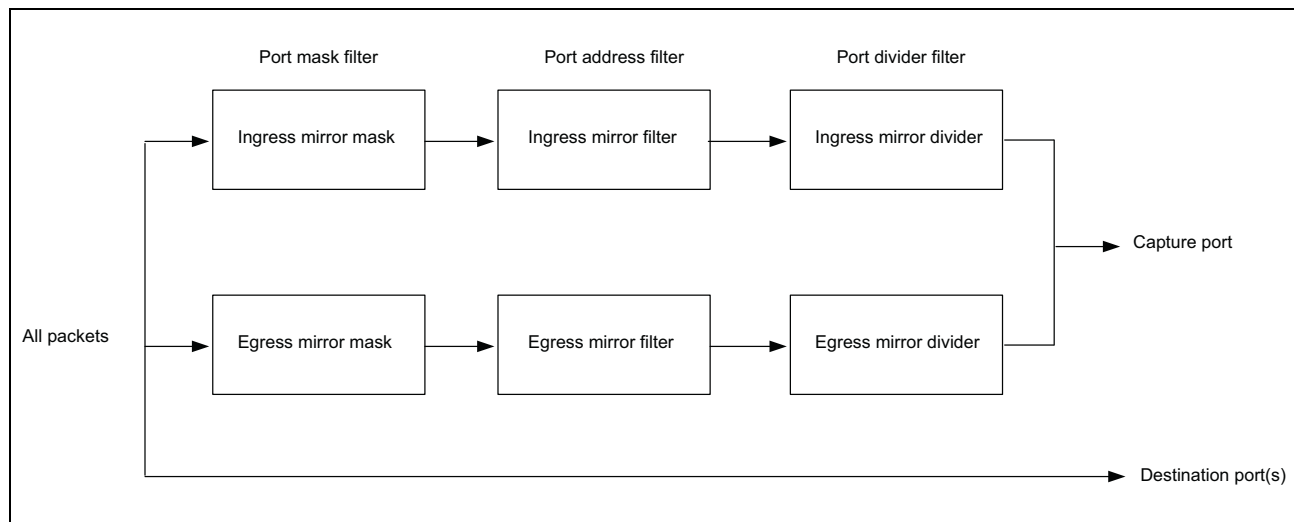
- **Aggregator:** For example, all the available ports are designated as protected ports except a single aggregator port. No traffic incoming to the protected ports is sent within the protected ports group. Any flooded traffic is forwarded only to the aggregator port.
- **To prevent nonsecured ports from monitoring important information on a server port,** the server port and nonsecured ports are designated as protected. The nonsecured ports will not be able to receive traffic from the server port.

## Port Mirroring

The BCM53115S support Port Mirroring, allowing ingress and/or egress traffic to be monitored by a single port designated as the mirror capture port. The BCM53115S can be configured to mirror the ingress traffic and/or egress traffic of any other port (s). Mirroring multiple ports is possible, but can create congestion at the mirror capture port. Several filters are used to decrease congestion.

## Enabling Port Mirroring

Port Mirroring is enabled by setting the Mirror Enable bit in the “[Mirror Capture Control Register \(Page 02h: Address 10h\)](#)” on page 170.



**Figure 7: Mirror Filter Flow**

## Capture Port

The capture port is capable of monitoring other specified ports. Frames transmitted and received at the other ports are forwarded to the Capture port according to the mirror filtering rules discussed below. The Capture port is specified by the Capture Port bits of the [“Mirror Capture Control Register \(Page 02h: Address 10h\)” on page 170](#).

## Mirror Filtering Rules

Mirror filtering rules consist of a set of three filter operations (Port Mask, Packet Address, and Packet Divider) that are applied to traffic ingressed and/or egressed at a switch port.

### Port Mask Filter

The IN\_MIRROR\_MASK bits in the [“Mirror Capture Control Register \(Page 02h: Address 10h\)” on page 170](#) define the receive ports that are monitored. The OUT\_MIRROR\_MASK bits in the [“Egress Mirror Control Register \(Page 02h: Address 1Ch\)” on page 173](#) define the transmit ports that are monitored.

Any number of ingress/egress ports can be programmed to be mirrored, but bandwidth restrictions on the one-mirror capture port should be taken into account to avoid congestion or packet loss.

### Packet Address Filter

The [“Ingress Mirror Control Register \(Page 02h: Address 12h\)” on page 171](#) is used to set the type of filtering that is applied to frames received on the mirrored ports. The IN\_MIRROR\_FILTER bits select among the following:

- Mirror all received frames
- Mirror received frames with DA = x
- Mirror received frames with SA = x

where x is the 48-bit MAC address programmed into the [“Ingress Mirror MAC Address Register \(Page 02h: Address 16h\)” on page 172](#). Likewise, the [“Egress Mirror Control Register \(Page 02h: Address 1Ch\)” on page 173](#) is used to set the type of filtering that is applied to frames transmitted on the egressed mirrored ports. The filtering MAC address is specified in the [“Egress Mirror MAC Address Register \(Page 02h: Address 20h\)” on page 174](#).

### Packet Divider Filter

The IN\_DIV\_EN bit in the [“Ingress Mirror Control Register \(Page 02h: Address 12h\)” on page 171](#) allows further statistical sampling. When IN\_DIV\_EN = 1, the receive frames passing the initial filter are divided by the value IN\_MIRROR\_DIV, which is a 10-bit value stored in the [“Ingress Mirror Divider Register \(Page 02h: Address 14h\)” on page 172](#). Only one out of every n frames is forwarded to the mirror capture port, where n = IN\_MIRROR\_DIV + 1. This allows the following additional capabilities:

- Mirror every n<sup>th</sup> received frame
- Mirror every n<sup>th</sup> received frame with DA = x
- Mirror every n<sup>th</sup> received frame with SA = x

Similarly, the Egress Mirror Divide function is controlled by the “[Egress Mirror Control Register \(Page 02h: Address 1Ch\)](#)” on page 173 and the “[Egress Mirror Divider Register \(Page 02h: Address 1Eh\)](#)” on page 173.



**Note:** When multiple ingress ports have been enabled in the IN\_MIRROR\_MASK, the cumulative total packet count received from all ingress ports is divided by the value of IN\_MIRROR\_DIV to deliver the nth receive frame to the mirror capture port. Egressed frames are governed by the OUT\_MIRROR\_MASK bit and the OUT\_MIRROR\_DIV bit.

---

## IGMP Snooping

The BCM53115S supports IP layer IGMP Snooping which includes IGMP unknown, query, report and leave message using the “[High-Level Protocol Control Register \(Page 02h: Address 50h–53h\)](#)” on page 175. The minimum value of IP header Internet Header Length field is 6.

A frame with a value of 2 in the IP header protocol field and IGMP frames are forwarded to the CPU port. The management CPU can then determine, from the IGMP control packets which port should participate in the multigroup session. The management CPU proactively programs the multicast address in the ARL table or the multiport address entries. If the IGMP\_UKN\_FWD\_EN, IGMP\_QRY\_FWD\_EN, IGMP\_RPTLVE\_FWD\_EN in the “[High-Level Protocol Control Register \(Page 02h: Address 50h–53h\)](#)” on page 175 is enabled, IGMP frames will be trapped to the CPU port only.

---

## MLD Snooping

The BCM53115S supports IP layer MLD Snooping includes MLD query, report and done message using the “[High-Level Protocol Control Register \(Page 02h: Address 50h–53h\)](#)” on page 175.

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## IEEE 802.1x Port-Based Security

IEEE 802.1x is a port-based authentication protocol. By receiving and extracting special frames, the CPU can control whether the ingress and egress ports should forward packets or not. If a user port wants service from another port (authenticator), it must get approved by the authenticator. EAPOL is the protocol used by the authentication process. The BCM53115S detect EAPOL frames by checking the destination address of the frame. The Destination addresses should be either a multicast address as defined in IEEE 802.1x (01-80-C2-00-00-03) or a user-predefined MAC (unicast or multicast) address. Once EAPOL frames are detected, the frames are forwarded to the CPU so it can send the frames to the authenticator server. Eventually, the CPU determines whether the requestor is qualified or not based on its MAC\_Source addresses, and frames are either accepted or dropped. The per-port EAP can be programmed in the register.

BCM53115S provides three modes for implementing the IEEE 802.1x feature. Each mode can be selected by setting the appropriate bits in the register.

The Basic Mode (when EAP Mode = 00'b) is the standard mode, the EAP\_BLK\_MODE bit would be set before authentication to block all of the incoming packets, upon authentication, the EAP\_BLK\_MODE bit would be cleared to allow all the incoming packets. In this mode, the source address of incoming packets is not checked.

The second mode is Extended Mode (when EAP Mode = 10'b), where an extra filtering mechanism is implemented after the port is authenticated. If the Source MAC address is unknown, the incoming packets would be dropped and the unknown SA would not be learned. However if the incoming packet is IEEE 802.1x packet, or special frames, the incoming packets will be forwarded. The definition of the Unknown SA in this case is when the switch cannot match the incoming Source MAC address to any of the addresses in ARL table, or the incoming Source MAC address matches the address in ARL table, but the port number is mismatched. The third mode is Simplified Mode (when EAP Mode = 11'b). In this mode, the unknown Source MAC address packets would be forwarded to CPU rather than dropped. Otherwise, it is same as the Extended Mode operation.



**Note:** The BCM53115S check only the destination addresses to qualify EAPOL frames. Ethernet type fields, packet type fields, or non-IEEE 802.1Q frames are not checked.

## DoS Attack Prevention

The BCM53115S supports the detection of the following DoS (Denial of Service) attack types based on register setting, which can be programmed to drop or not to drop each type of DoS packets respectively.

**Table 4: DoS Attacks Detected by BCM53115S**

| <b>DoS Attack Type</b> | <b>Description</b>                                                                                                                                                                         |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IP_LAND                | IPDA = IPSA in an IPv4/IPv6 datagram                                                                                                                                                       |
| TCP_BLAT               | DPort = SPort in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram                                                                  |
| UDP_BLAT               | DPort = SPort in a UDP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram                                                                  |
| TCP_NULLScan           | Seq_Num = 0 and all TCP_FLAGS = 0 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram                                              |
| TCP_XMASScan           | Seq_Num = 0, FIN = 1, URG = 1, and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram                                     |
| TCP_SYNFINScan         | SYN = 1 and FIN = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram                                                            |
| TCP_SYNErrror          | SYN = 1, ACK = 0, and SRC_Port < 1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram                                          |
| TCP_ShortHDR           | The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size                                       |
| TCP_FragError          | The Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data                                                                                              |
| ICMPv4_Fragment        | The ICMPv4 protocol data unit carried in a fragmented IPv4 datagram                                                                                                                        |
| ICMPv6_Fragment        | The ICMPv6 protocol data unit carried in a fragmented IPv6 datagram                                                                                                                        |
| ICMPv4_LongPing        | The ICMPv4 ping (echo request) protocol data unit carried in an unfragmented IPv4 datagram with its Total Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header |
| ICMPv6_LongPing        | The ICMPv6 ping (echo request) protocol data unit carried in an unfragmented IPv6 datagram with its payload length indicating a value greater than the MAX_ICMPv6_Size                     |

- MIN\_TCP\_Header\_Size is programmable between 0 and 255 bytes, inclusive. The default value is set to 20 bytes (TCP header without options).
- MAX\_ICMPv4\_Size is programmable between 0 and 9.6 KB, inclusive. The default value is set to 512 bytes.
- MIN\_TCP\_Header\_Size is programmable between 0 and 9.6 KB, inclusive. The default value is set to 512 bytes.
- The default control setting for all types of DoS attacks is not to drop the DoS attack packet.

- It is globally configurable whether to perform the SA learning operation with the received packets of the DoS attack type defined in the registers, regardless of the individual DoS attack types.
- Once a packet is detected as a DOS attack type that must be dropped, the packet is dropped regardless of ARL forwarding decisions, but its forwarding based on mirroring function is not affected.

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## MSTP Multiple Spanning Tree

The BCM53115S support up to eight multiple spanning trees. When the EN\_RX\_BPDU bit = 1, the BCM53115S forwards BPDU packets to the management port only.

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## Software Reset

The BCM53115S provide Software Resets. Software Resets can be triggered by programming the [“Software Reset Control Register \(Page 00h: Address 79h\)” on page 162](#).

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## Loop Detection

The BCM53115S provide the Loop Detection feature for unmanaged environments (that is, those without a management CPU). When the Loop Detection feature is enabled and activated, the switch generates Broadcom proprietary tag frames (Loop Discovery Frames) at a programmed interval, and when it detects a loop, it gives a loop detected warning with a blinking LED or with a sound produced by a speaker. This feature does not repair the loop, but only issues a warning.

The Discovery Frame is a broadcast frame, and the switch ensures the forwarding of the frame by providing special priority for the frame by giving it a higher priority over other broadcast frames, assigning highest queue automatically and overwriting the pause condition. The control/options over this feature are provided beginning with the [“Loop Detection Control Register \(Page 72h: Address 00h\)” on page 290](#).

The Loop Discovery frame uses a default multicast address (01-80-C2-00-00-01) in the Loop Detect Source Address register as a source address. Using a multicast address as a source address is illegal in the IEEE standard; however, since this is only intended to be used in the ROBO environment only, it should be allowed. This address scheme is used to avoid a possible disruption in forwarding decision by using a regular random Source Address.

The Loop Discovery frame also uses the Module ID 0 register along with the Module ID 1 register to identify the origin of the Discovery frame. These registers are used to define a Source Chip ID and Source Port ID to distinguish the Discovery Frames from other ROBO chips.

The implementation example for the Loop Detect feature is described in the *BCM53115S Design Guide*.

## CableChecker™

The BCM53115S provide the cable diagnostic capabilities for unmanaged environments. The actual cable diagnostic feature lies in the PHY functional block. The BCM53115S devices let the user monitor the cable diagnostic results through LED display by setting the appropriate bits in the LED refresh registers.

The BCM53115S uses the existing LED display (which is already assigned to various functions) to indicate the cable diagnostic results. [Table 5](#) shows the cable diagnostic result output for each LED function where 1 and 0 represent the LED indication pin status; 1 indicates active and 0 indicates inactive.



### Note:

- The best way for a user to visualize the cable diagnostic test result through LEDs is to bring out the LINK status bit to the LED display along with other functions to be displayed per port. In this way, the user can observe the cable diagnostic result from the flashing (or lit) LED of other functions while LINK LED is off. The switch will turn off the LINK status LED during the cable diagnostic mode.
- The cable diagnostic is expected to be most effective when the user cannot establish the link with the partner.

**Table 5: Cable Diagnostic Output**

| LED Function in LED Function Register | Cable Diagnostic Output                                                                                                                |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| PHYLED4                               | 1 = Cable diagnostic failed<br>0 = Cable diagnostic passed                                                                             |
| LNK                                   | No output during the cable diagnostic mode                                                                                             |
| DPX                                   | 1 = Passed<br>0 = Failed                                                                                                               |
| ACT                                   | 1 = Passed<br>0 = Failed                                                                                                               |
| COL                                   | 1 = Passed<br>0 = Failed                                                                                                               |
| LNK/ACT                               | No output during the cable diagnostic mode                                                                                             |
| DPX/COL                               | 1 = Passed<br>0 = Failed                                                                                                               |
| SPD10M                                | 1 = Failed<br>0 = Passed                                                                                                               |
| SPD100M                               | In LED function0 map<br>1 = Cable diagnostic passed<br>0 = Failed<br>In LED function1 map<br>1 = Cable diagnostic failed<br>0 = Passed |

**Table 5: Cable Diagnostic Output (Cont.)**

| <b>LED Function in LED Function Register</b> | <b>Cable Diagnostic Output</b>                                                                                                         |
|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| SPD1G                                        | 1 = Passed<br>0 = Failed                                                                                                               |
| 10M/ACT                                      | 1 = Failed<br>0 = Passed                                                                                                               |
| 100M/ACT                                     | In LED function0 map<br>1 = Cable diagnostic passed<br>0 = Failed<br>In LED function1 map<br>1 = Cable diagnostic failed<br>0 = Passed |
| 10–100M/ACT                                  | 1 = Failed<br>0 = Passed                                                                                                               |
| 1G/ACT                                       | 1 = Passed<br>0 = Failed                                                                                                               |
| PHYLED3                                      | 1 = Failed<br>0 = Passed                                                                                                               |

## Egress PCP Remarking

The BCM53115S provides an egress PCP remarking feature of the outer tag at each egress port which includes the CFI and PCP field modification based on the internal ARL-generated TC status. The Egress PCP remarking process applies to Ethernet ports only and can be enabled by [“Traffic Remarking Control Register \(Page 91h: Address 00h\)” on page 292](#). Each Ethernet port can provide an 8-entry mapping table indexed by TC to map to the {New CFI, New PCP} field for the outgoing packet using the [“Egress Packet TC to PCP Mapping Register \(Page 91h: Address 10h\)” on page 293](#).

## Address Management

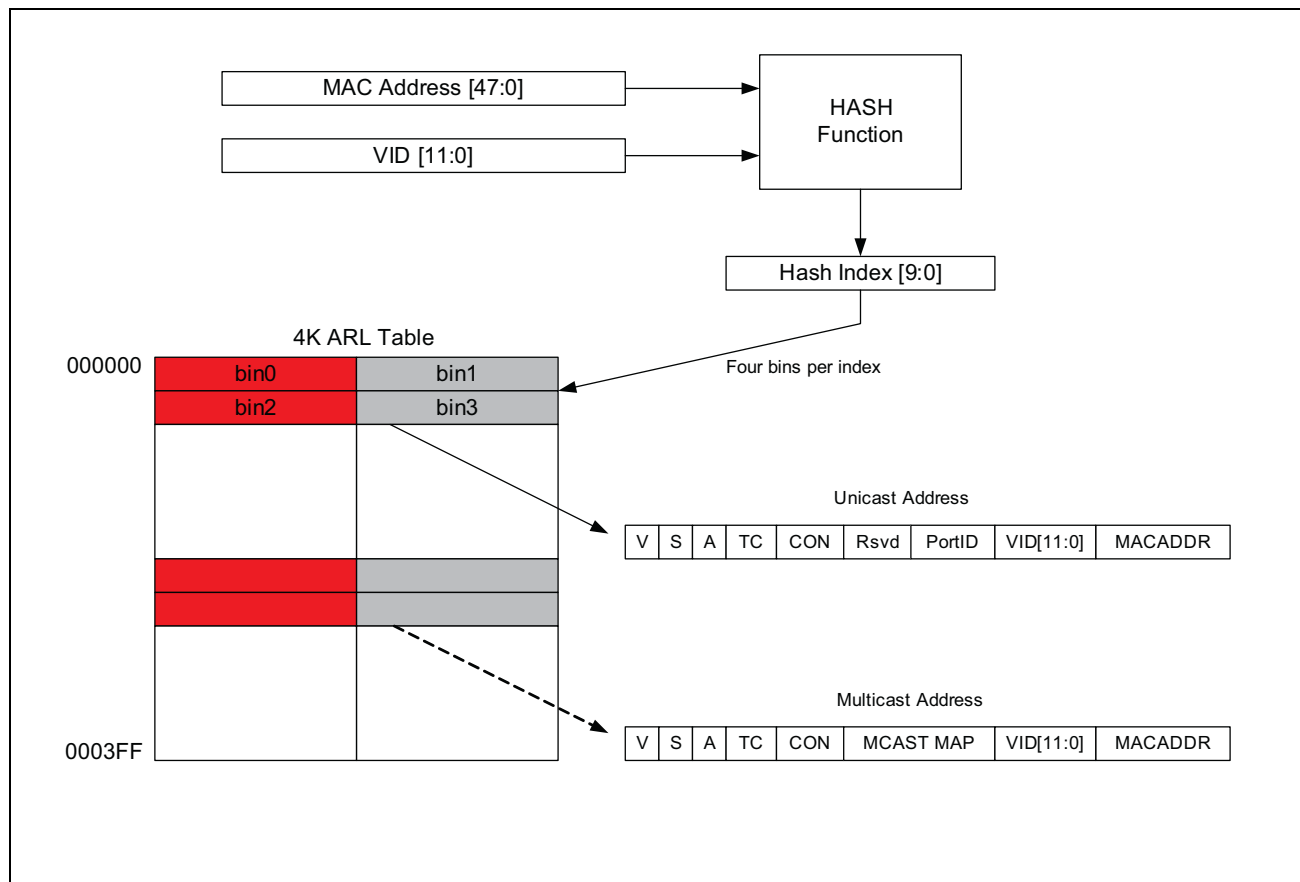
The BCM53115S Address Resolution Logic contains the following features:

- Four bins per bucket address table configuration.
- Hashing of the MAC/VID address to generate the address table point.

The address management unit of the BCM53115S provides wire speed learning and recognition functions. The address table supports 4K unicast/multicast addresses using on-chip memory.

## Address Table Organization

The MAC addresses are stored in embedded SRAM. Each bucket contains four entries or bins. The address table has 1K buckets with four entries in each bucket. This allows up to four different MAC addresses with the same hashed index bits to be simultaneously mapped into the address table. In the ARL DA/SA lookup process, it hashes a 10-bit search index and read out bin0 and bin1 in the first cycle, and read out bin2 and bin3 in the second cycle. These four entries are used for ARL routing and learning.



**Figure 8: Address Table Organization**

The index to the address table is computed using a hash algorithm based on the MAC address and the VLAN ID (VID) if enabled.



**Note:** In the Enable IEEE 802.1Q and VLAN Learning Mode both the MAC address and the VLAN ID (VID) are used to compute the hashed index. See [“IEEE 802.1Q VLAN” on page 39](#) for more information.

The hash algorithm uses the CRC-CCITT polynomial. The input to the hash is reduced to a 16-bit CRC hash value. Bits[9:0] of the hash are used as an index to the approximately 4K locations of the address table.

The CRC-CCITT polynomial is:

$$x^{16} + x^{12} + x^5 + 1$$

## Address Learning

Information is gathered from received unicast packets and learned or stored for the future purpose of forwarding frames addressed to the receiving port. During the receive process, the frame information (such as the Source Address [SA] and VID) is saved until completion of the packet. An entry is created in the ARL table memory if the following conditions are met:

- The packet has been received without error.
- The packet is of legal length.
- The packet has a unicast SA.
- If using IEEE 802.1Q VLAN, the packet is from an SA that belongs to the indicated VLAN domain.
- The packet does not have a reserved multicast destination address. The Multicast Learning bit of the [“Reserved Multicast Control Register \(Page 00h: Address 2Fh\)” on page 156](#) can disable this condition.
- There is free space available in memory to which the hashed index points.

When unicast packets are dynamically learned, the VALID bit is set, the AGE bit is set, and the STATIC bit is cleared in the entry. See [Table 7 on page 57](#) for a description of a unicast ARL entry.

Multicast addresses are not learned into the ARL table, but must be written using one of the [“Programming Interfaces” on page 91](#). See [“Writing an ARL Entry” on page 61](#) and [Table 9 on page 58](#) for more information.

## Address Resolution and Frame Forwarding

Received packets are forwarded based on the information learned or written into the ARL table. Address resolution is the process of locating this information and assigning a forwarding destination to the packet. The destination address (DA) and VID of the received packet are used to calculate a hashed index to the ARL table. The hashed index key is used by the address resolution function to locate a matching ARL entry. The frame is assigned a destination based on the forward field (PORTID or IPMC0) of the ARL entry. If the address resolution function fails to return a matching ARL entry, the packet is flooded to all appropriate ports. The following two sections describe the specifics of address resolution and frame forwarding for [“Unicast Addresses” on page 56](#) and [“Multicast Addresses” on page 57](#).

### Unicast Addresses

Frames containing a unicast destination address are assigned a forwarding field corresponding to a single port. Listed below is the unicast address-resolution algorithm:

- If the multiport addressing feature is enabled and the DA matches one of the programmed multiport addresses, then it is forwarded accordingly. See [“Using the Multiport Addresses” on page 63](#).
- The lower 10 bits of the hashed index key are used as a pointer into the address table memory, and the entry is retrieved.
- If the valid indicator is set and the address stored at one of the locations matches the index key of the packet received, the forwarding field port ID is assigned to the destination port of the packet.
  - If the destination port matches the source port, the packet is not forwarded.
- If the address resolution function fails to return a matching valid ARL entry and the unicast DLF forward bit is set, the frame is forwarded according to the port map in the [“Unicast Lookup Failed Forward Map Register \(Page 00h: Address 32h\)” on page 157](#).

- Otherwise, the packet is flooded to all appropriate ports.

See [Table 6 on page 57](#) for definitions of the unicast index key and the assigned forwarding field. The forwarding field for a unicast packet is the port ID contained in the matching ARL entry. See [Table 7](#) for a description of a unicast ARL entry.

**Table 6: Unicast Forward Field Definitions**

| <i>EN_1QVLAN</i> | <i>Index Key</i> | <i>Forwarding Field</i> |
|------------------|------------------|-------------------------|
| 1                | DA and VID       | Port ID                 |
| 0                | DA               | Port ID                 |

**Table 7: Address Table Entry for Unicast Address**

| <i>Field</i> | <i>Description</i>                                                                                                                 |
|--------------|------------------------------------------------------------------------------------------------------------------------------------|
| VID          | VLAN ID associated with the MAC address.                                                                                           |
| VALID        | 1 = Entry is valid.<br>0 = Entry is empty.                                                                                         |
| STATIC       | 1 = Entry is static — Should not be aged out and is written and updated by software.<br>0 = Entry is dynamically learned and aged. |
| AGE          | 1 = Entry has been accessed or learned since last aging process.<br>0 = Entry has not been accessed since last aging process.      |
| TC           | MACDA-based TC (only valid for static entries). See <a href="#">“Quality of Service” on page 34</a> for more information.          |
| Reserved     | —                                                                                                                                  |
| Reserved     | Only 00 is valid.                                                                                                                  |
| PORTID       | Port identifier. The port associated with the MAC address.                                                                         |
| MAC ADDRESS  | 48-bit MAC address.                                                                                                                |



**Note:** The fields described in [Table 7](#) can be written using the [“ARL Table MAC/VID Entry N \(N = 0–3\) Register \(Page 05h: Address 10h\)” on page 184](#) and [“ARL Table Data Entry N \(N = 0–3\) Register \(Page 05h: Address 18h\)” on page 184](#).

Multicast ARL table entries are described in [Table 9 on page 58](#).

## Multicast Addresses

Frames containing a multicast destination address are assigned a forwarding field corresponding to multiple ports specified in a port map. If the IP\_MULTICAST bit is set, multicast frames are assigned a forwarding field corresponding to a multicast port map from the matching ARL entry (see [“Address Management” on page 54](#)). If no matching ARL entry is found, the packet is flooded to all appropriate ports.

Listed below is the multicast address resolution algorithm:

- If the DA matches one of the globally assigned reserved addresses between 01-80-C2-00-00-00 and 01-80-C2-00-00-2F, the packet is handled as described in [Table 10 on page 60](#).
- If the multiport addressing feature is enabled and the DA matches one of the programmed Multiport Addresses, then it is forwarded accordingly. See [“Using the Multiport Addresses” on page 63](#).
- Otherwise, the lower 10 bits of the hashed index key are used as a pointer into the ARL table memory, and the entry is retrieved.
- If the valid indicator is set, and the address stored at the entry locations matches the index key of the packet received, the forwarding field port map is assigned to the destination port of the packet.
- If the address resolution function fails to return a matching valid ARL entry and the multicast DLF forward bit is set (see [“Address Management” on page 54](#)), the frame is forwarded according to the port map in the [“Multicast Lookup Failed Forward Map Register \(Page 00h: Address 34h–35h\)” on page 158](#).
- Otherwise, all other multicast and broadcast packets are flooded to all appropriate ports.

See [Table 8](#) for definitions of the multicast index key and the assigned forwarding field. The forwarding field for a multicast packet is the port map contained in the matching ARL entry. See [Table 9](#) for a description of a multicast ARL entry. See [“Accessing the ARL Table Entries” on page 61](#) for more information.

**Table 8: Multicast Forward Field Definitions**

| <i>EN_1QVLAN</i> | <i>IP_MULTICAST</i> | <i>Index Key</i> | <i>Forwarding Field</i> |
|------------------|---------------------|------------------|-------------------------|
| 1                | 0                   | DA and VID       | Port ID                 |
| 0                | 0                   | DA               | Port ID                 |
| 1                | 1                   | DA and VID       | IPMCO                   |
| 0                | 1                   | DA               | IPMCO                   |

**Table 9: Address Table Entry for Multicast Address**

| <i>Field</i> | <i>Description</i>                                                                                                        |
|--------------|---------------------------------------------------------------------------------------------------------------------------|
| VID          | VLAN ID associated with the MAC address.                                                                                  |
| VALID        | 1 = Entry is valid.<br>0 = Entry is empty.                                                                                |
| STATIC       | 1 = Entry is static— This entry is not aged out and is written and updated by software.<br>0 = Not defined.               |
| AGE          | The AGE bit is ignored for static ARL table entries.                                                                      |
| TC           | MACDA-based TC (only valid for static entries). See <a href="#">“Quality of Service” on page 34</a> for more information. |
| Reserved     | —                                                                                                                         |
| IPMCO [8:0]  | Multicast forwarding mask.<br>1 = Forwarding enable.<br>0 = Forwarding disable.                                           |
| MAC ADDRESS  | 48-bit MAC address.                                                                                                       |



**Note:** The fields described in [Table 9](#) can be written using the “ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)” on page 184 and “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 184.

Unicast ARL table entries are described in [Table 7 on page 57](#).

## Reserved Multicast Addresses

Table 10 summarizes the actions taken for specific reserved multicast addresses. Packets identified with these destination addresses are handled uniquely since they are designed for special functions. Bits[4:0] of the “Reserved Multicast Control Register (Page 00h: Address 2Fh)” on page 156 program groups of these addresses to be dropped or forwarded. Writing to these bits can change the default action of Unmanaged mode summarized in Table 10 on page 60.

**Table 10: Behavior for Reserved Multicast Addresses**

| <b>MAC Address</b>                  | <b>Function</b>                               | <b>IEEE 802.1 Specified Action</b> | <b>Unmanaged Mode Action</b>                                                  | <b>Managed Mode Action</b>                                                                                                                        |
|-------------------------------------|-----------------------------------------------|------------------------------------|-------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 01-80-C2-00-00-00                   | Bridge group address                          | Drop frame                         | Flood frame                                                                   | Forward frame to IMP only                                                                                                                         |
| 01-80-C2-00-00-01                   | IEEE 802.3x MAC control frame                 | Drop frame                         | Receive MAC determines if it is a valid pause frame and then acts accordingly | Receive MAC determines if valid pause frame and acts accordingly.                                                                                 |
| 01-80-C2-00-00-02                   | Reserved                                      | Drop frame                         | Drop frame                                                                    | Forward to frame management port only                                                                                                             |
| 01-80-C2-00-00-03                   | IEEE 802.1x port-based network access control | Drop frame                         | Drop frame                                                                    | Forward frame to management port only                                                                                                             |
| 01-80-C2-00-00-04–01-80-C2-00-00-0F | Reserved                                      | Drop frame                         | Drop frame                                                                    | Forward frame to management port only                                                                                                             |
| 01-80-C2-00-00-10                   | All LANs bridge management group address      | Forward frame                      | Flood frame                                                                   | Forward frame to all ports including management port                                                                                              |
| 01-80-C2-00-00-11–01-80-C2-00-00-1F | Reserved                                      | Forward frame                      | Flood frame                                                                   | Forward frame to all ports excluding management port                                                                                              |
| 01-80-C2-00-00-20                   | GMRP address                                  | Forward frame                      | Flood frame                                                                   | Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 4 of page 34, offset 04h register) |
| 01-80-C2-00-00-21                   | GVRP address                                  | Forward frame                      | Flood frame                                                                   | Forward frame to all ports excluding management port, or forward frame to management port only (by setting bit 5 of page 34, offset 04h register) |
| 01-80-C2-00-00-22–01-80-C2-00-00-2F | Reserved                                      | Forward frame                      | Flood frame <sup>a</sup>                                                      | Forward frame to all ports excluding management port                                                                                              |

a. Frames flood to all ports. Certain exclusions apply, such as VLAN restrictions.

## Static Address Entries

The BCM53115S supports static ARL table entries that are created and updated using one of the [“Programming Interfaces” on page 91](#). These entries can contain either unicast or multicast destinations. The entries are created by writing the entry location using the [“Page 05h: ARL/VTBL Access Registers” on page 181](#) and setting the STATIC bit. The AGE bit is ignored. Static entries do not automatically learn MAC addresses or port associations and are not aged out by the automatic internal aging process. See [“Writing an ARL Entry” on page 61](#) for details.

## Accessing the ARL Table Entries

ARL table entries are accessed by one of two mechanisms. The first mechanism uses the ARL read/write control, which allows an address-entry location to be read, modified, or written based on the value of a known MAC address. The second mechanism searches the ARL table sequentially, returning all valid entries.

### Reading an ARL Entry

To read an ARL entry:

1. Set the MAC address in the [“MAC Address Index Register \(Page 05h: Address 02h\)” on page 183](#).
2. Set the VLAN ID in the [“VLAN ID Index Register \(Page 05h: Address 08h\)” on page 183](#). This is necessary only if the VID is used in the index key.
3. Set the ARL\_R/W bit to 1 in the [“ARL Table Read/Write Control Register \(Page 05h: Address 00h\)” on page 182](#).
4. Set the START/DONE bit to 1 in the [“ARL Table Read/Write Control Register \(Page 05h: Address 00h\)” on page 182](#). This initiates the read operation.

The MAC address and VID are used to calculate the hashed index to the ARL table. The matching ARL entry is read. The contents of entry are stored in the [“ARL Table MAC/VID Entry N \(N = 0–3\) Register \(Page 05h: Address 10h\)” on page 184](#) and the [“ARL Table Data Entry N \(N = 0–3\) Register \(Page 05h: Address 18h\)” on page 184](#).

Entries that do not have the VALID bit set should be ignored. The contents of the MAC/VID registers must be compared against the known MAC address and VID. Entries that do not match may be a valid entry, but are not a valid match for the index key. All other read entries are considered valid ARL entries.

### Writing an ARL Entry

To write an ARL entry:

1. Follow the steps in [“Reading an ARL Entry”](#) to read the ARL entry matching the MAC address and VID that are written to the table.
2. Keep the values that remain from the previous read operation.
  - [“MAC Address Index Register \(Page 05h: Address 02h\)” on page 183](#)
  - [“VLAN ID Index Register \(Page 05h: Address 08h\)” on page 183](#)
  - [“ARL Table MAC/VID Entry N \(N = 0–3\) Register \(Page 05h: Address 10h\)” on page 184](#)
  - [“ARL Table Data Entry N \(N = 0–3\) Register \(Page 05h: Address 18h\)” on page 184](#)

3. Modify the correct entry as necessary. Set the STATIC bit so that the entry is not aged out.
4. Set the ARL\_R/W bit to 0 in the [“ARL Table Read/Write Control Register \(Page 05h: Address 00h\)” on page 182](#).
5. Set the START/DONE bit to 1 in the [“ARL Table Read/Write Control Register \(Page 05h: Address 00h\)” on page 182](#). This initiates the write operation.

The MAC address and VID are used to calculate the hashed index to the ARL table.

## Searching the ARL Table

The second method to access the ARL table is through the ARL search control. The entire ARL table is searched sequentially, revealing each valid ARL entry. Setting the Start/Done bit in the [“ARL Table Search Control Register \(Page 05h: Address 50h\)” on page 186](#) begins the search from the top of the ARL table. This bit is cleared when the search is complete. During the ARL search, the Search Valid bit indicates when a found valid entry is available in the [“ARL Table Search MAC/VID Result N \(N=0-1\) Register \(Page 05h: Address 60h\)” on page 187](#) and the [“ARL Table Search Data Result N \(N=0-1\) Register \(Page 05h: Address 68h\)” on page 188](#). When the host reads the contents of the ARL Table Search Data Result 1 register which located in Page 05h: Address 78h, the search process automatically continues to seek the next valid entry in the address table. Invalid address entries are skipped, providing the host with an efficient way of searching the entire address table.

The ARL search and ARL read/write operations execute in parallel with other register accesses. This allows the host processor to start a read, write, or search process and then read/write other registers, returning periodically to see if the operation has completed.

## Address Aging

The aging process periodically removes dynamically learned addresses from the ARL table. When an ARL entry is learned or referenced, the AGE bit is set to 1. The aging process scans the ARL table at regular intervals, aging out entries not accessed during the previous one to two aging intervals. The aging interval is programmable using the Aging Enable and AGE TIME bit in the [“Aging Time Control Register \(Page 02h: Address 06h\)” on page 170](#).

Entries that are written and updated using one of the [“Programming Interfaces” on page 91](#), should have the STATIC bit set. Thus, they are not affected by the aging process.

For each entry in the ARL table, the aging process performs the following:

- If the VALID bit is not set, no further action is required.
- If the VALID bit is set and the STATIC is set, no further action is required.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is set, then clear the AGE bit. This keeps the entry in the table, but marks it so that it is removed if it is not accessed before the subsequent aging scan.
- If the VALID bit is set, the STATIC bit is not set, and the AGE bit is reset, then reset the VALID bit. This effectively deletes the entry from the ARL table. The entry has been aged out.

## Fast Aging

The fast aging function can be enabled per port or VLAN ID:

The port fast aging can be enabled by setting the Start/Done of the “Fast-Aging Control Register (Page 00h: Address 88h)” on page 162, the Fast Age All Ports bit of the “Fast-Aging Port Control Register (Page 00h: Address 89h)” on page 163, and the appropriate port bits in the “Fast-Aging Port Control Register (Page 00h: Address 89h)” on page 163.

The VLAN ID fast aging can be enabled by setting the Start/Done of the “Fast-Aging Control Register (Page 00h: Address 88h)” on page 162, the Fast Age All VID bit of the “Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)” on page 163, and the appropriate VLAN ID bits of the “Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)” on page 163.

## Using the Multiport Addresses

The “Multiport Address N (N=0–5) Register (Page 04h: Address 10h)” on page 180 can be used to forward a given MAC address and Ether Type to multiple ports. Packets with a corresponding DA are forwarded to the port map contained in the “Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)” on page 181. These registers must be controlled using the “Multiport Control Register (Page 04h: Address 0Eh–0Fh)” on page 179.

## Section 3: System Functional Blocks

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### Overview

The BCM53115S include the following blocks:

- “Media Access Controller” on page 64
- “Integrated 10/100/1000 PHY” on page 66
- “Frame Management” on page 75
- “MIB Engine” on page 78
- “Integrated High-Performance Memory” on page 86
- “Switch Controller” on page 86

Each of these is discussed in more detail in the following sections.

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### Media Access Controller

The BCM53115S contains six 10/100/1000 GMACs, and one MAC.

The MAC automatically selects the appropriate speed (CSMA/CD or full-duplex) based on the PHY auto-negotiation result. In full-duplex mode, IEEE 802.3x PAUSE frame-based flow control is also determined through auto-negotiation. The MAC is IEEE 802.3-, IEEE 802.3u-, and IEEE 802.3x-compliant.

### Receive Function

The MAC initiates frame reception following the assertion of receive data valid indication from the physical layer. The MAC monitors the frame for the following error conditions:

- Receive error indication from the PHY
- Runt frame error if frame is fewer than 64 bytes
- CRC error
- Long frame error if frame is greater than standard max frame size or 9,720 bytes for jumbo-enabled ports.



**Note:** Frames longer than standard max frame size which configured using the “[Standard Maximum Frame Size Register \(Page 40h: Address 05h\)](#)” on page 273 are considered oversized frames. When jumbo-frame mode is enabled, only the frames longer than 9,720 bytes are bad frames and dropped.

If no errors are detected, the frame is processed by the switch controller. Frames with errors are discarded. Receive functions can be disabled by writing to “[Port Traffic Control Register \(Page 00h: Address 00h\)](#)” on page 148.

## Transmit Function

Frame transmission begins with the switch controller queuing a frame to the MAC transmitter. The frame data is transmitted as received from the switch controller. The transmit controller is responsible for preamble insertion, carrier deferral, collision backoff, and inter-packet gap enforcement.

In 10/100 Mbps half-duplex mode, when a frame is queued for transmission, the transmit controller behaves as specified by the IEEE 802.3 requirements for frame deferral. Following deferral, the transmitter adds 8 bytes of preamble and SFD to the frame data received from the switch controller. If, during frame transmission, a collision is observed and the collision window timer has not expired, the transmit controller asserts jam and then executes the backoff algorithm. The frame is retransmitted when appropriate. On the 16th consecutive collision, the backoff algorithm starts over at the initial state, the collision counter is reset and attempts to transmit the current frame continue. Following a late collision, the frame is aborted, and the switch controller is allowed to queue the next frame for transmission.

While in full-duplex mode, the transmit controller ignores carrier activity and collision indication. Transmission begins after the switch controller queues the frame, and the 96-bit times of IPG have been observed. Transmit functions can be disabled by writing to “[Port Traffic Control Register \(Page 00h: Address 00h\)](#)” on [page 148](#).

## Flow Control

The BCM53115S implement an intelligent flow-control algorithm to minimize the system impact resulting from traffic congestion. Buffer memory allocation is adaptive to the status of each port’s speed and duplex mode, providing an optimal balance between flow management and per-port memory depth. The BCM53115S initiate flow control in response to buffer memory conditions on a per-port basis.

The MACs are capable of flow control in both full-and half-duplex modes.

### 10/100 Mbps Half-Duplex

In 10/100 half-duplex mode, the MAC back-pressures a receiving port by transmitting a 96-bit time jam packet to the port. A single jam packet is asserted for each received packet for the duration of the time the port is in the flow-control state.

### 10/100/1000 Mbps Full-Duplex

Flow control in full-duplex mode functions as specified by the IEEE 802.3x requirements. In the receiver, MAC flow-control frames are recognized and, when properly received, set the flow-control pause time for the transmit controller. The pause time is assigned from the 2-byte pause time field following the pause opcode. MAC control PAUSE frames are not forwarded from the receiver to the switch controller.

When the switch controller requests flow control, the transmit controller transmits a MAC control PAUSE frame with the pause time set to maximum. When the condition that caused the flow control state is no longer present, a second MAC control PAUSE frame is sent with the pause time field set to 0.

The flow control capabilities of the BCM53115S are enabled based on the results of auto-negotiation and the state of the ENFDXFLOW and ENHDXFLOW control signals loaded during reset. Flow control in half-duplex mode is independent of the state of the link partner flow control (IEEE 802.3x) capability. See [Table 11 on page 66](#) for detailed information.

**Table 11: Flow Control Modes**

| <b>Link Partner Flow Control (IEEE 802.3x)</b> | <b>Control Input ENFDXFLOW</b> | <b>Control Input ENHDXFLOW</b> | <b>Auto-Negotiated Link Speed</b> | <b>Flow Control Mode</b> |
|------------------------------------------------|--------------------------------|--------------------------------|-----------------------------------|--------------------------|
| X                                              | X                              | 0                              | Half duplex                       | Disabled                 |
| X                                              | X                              | 1                              | Half duplex                       | Jam pattern              |
| 0                                              | 0                              | X                              | Full duplex                       | Disabled                 |
| 0                                              | 1                              | X                              | Full duplex                       | Disabled                 |
| 1                                              | 0                              | X                              | Full duplex                       | Disabled                 |
| 1                                              | 1                              | X                              | Full duplex                       | IEEE 802.3x flow control |

## Integrated 10/100/1000 PHY

There are five integrated PHY blocks in the BCM53115S. For more information see [“Copper Interface” on page 88](#). The following sections describe the operations of the internal PHY block.

### Encoder

There are five integrated PHY blocks in the BCM53115S. The PHY is the Ethernet transceiver that appropriately processes data presented by the MAC into an analog data stream to be transmitted at the MDI interface, which performs the reverse process on data received at the MDI interface. The registers of the PHY are read using the [“Programming Interfaces” on page 91](#). The following sections describe the operations of the internal PHY block. For more information, see [“Copper Interface” on page 88](#).

In 10BASE-T mode, Manchester encoding is performed on the data stream that is transmitted on the twisted-pair cable. The multimode transmit digital-to-analog converter (DAC) performs preequalization for 100m of Category 3 cabling.

In 100BASE-TX mode, the BCM53115S transmits a continuous data stream over the twisted-pair cable. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start-of-stream delimiter (/J/K codes) and appending an end-of-stream delimiter (/T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets. The encoded data stream is serialized and then scrambled by the stream cipher block, as described in [“Stream Cipher” on page 69](#). The scrambled data is then encoded into MLT3 signal levels.

In 1000BASE-T mode, the BCM53115S simultaneously transmits and receives a continuous data stream on all 4 pairs of the Category 5 cable. Byte-wide data from the transmit data pins is scrambled when the transmit enable is asserted, and the trellis (a PAM5 symbol on each of the four twisted-pairs) is encoded into a four-dimensional code group and then inserted into the transmit data stream. The transmit packet is encapsulated by replacing the first 2 bytes of the preamble with a start-of-stream delimiter, and appending an end-of-stream delimiter to the end of the packet. When the transmit error input is asserted during a packet transmission, a transmit error code group is sent in place of the corresponding data code group. The transmitter sends idle code groups or carrier extend code groups between packets. Carrier extension is used by the MAC to separate packets within a multiple-packet burst and is indicated by asserting the transmit error signal and placing 0Fh on the transmit data pins while the transmit enable is low. A carrier extend error is indicated by replacing the transmit data input with 1Fh during carrier extension.

The encoding complies with IEEE standard IEEE 802.3ab and is fully compatible with previous versions of the Broadcom 1000BASE-T PHYs.

## Decoder

In 10BASE-T mode, Manchester decoding is performed on the data stream.

In 100BASE-TX mode, following equalization and clock recovery, the receive data stream is converted from MLT3 to serial nonreturn-to-zero (NRZ) data. The NRZ data is descrambled by the stream cipher block, as described later in this document. The descrambled data is then deserialized and aligned into 5-bit code groups. The 5-bit code groups are decoded into 4-bit data nibbles. The start-of-stream delimiter is replaced with preamble nibbles, and the end-of-stream delimiter and idle codes are replaced with 0h. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM53115S asserts the MII receive error (RX\_ER) signal. RX\_ER is also asserted when the link fails, or when the descrambler loses lock during packet reception.

In 1000BASE-T mode, the receive data stream is:

- Passed through the Viterbi decoder
- Descrambled
- Translated back into byte-wide data

The start-of-stream delimiter is replaced with preamble bytes, and the end-of-stream delimiter and idle codes are replaced with 00h. Carrier extend codes are replaced with 0Fh or 1Fh. Decoding complies with IEEE standard IEEE 802.3ab and is fully compatible with previous versions of Broadcom 1000BASE-T PHYs.

## Link Monitor

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the TRD pins for the presence of valid link pulses.

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal is detected on the receive pair, the link monitor enters the Link Fail state and the transmission and reception of data packets is disabled. When a valid signal is detected on the receive pair for a minimum of 1 ms, the link monitor enters the Link Pass state, and the transmit and receive functions are enabled.

Following auto-negotiation in 1000BASE-T mode, the master transceiver begins sending data on the media. The slave transceiver also begins transmitting when it has recovered the master transceiver's timing. Each end of the link continuously monitors its local receiver status. When the local receiver status has been good for at least 1 microsecond, the link monitor enters the Link Pass state, and the transmission and reception of data packets are enabled. When the local receiver status is bad for more than 750 ms, the link monitor enters the Link Fail state and the transmission and reception of data packets are disabled.

## Digital Adaptive Equalizer

The digital adaptive equalizer removes intersymbol interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The BCM53115S achieves an optimum signal-to-noise ratio by using a combination of feed forward equalization (FFE) and decision feedback equalization (DFE) techniques. Under harsh noise environments, these powerful techniques achieve a bit error rate (BER) of less than  $1 \times 10^{-12}$  for transmissions up to 100m on Category 5 twisted-pair cabling (100m on Category 3 UTP cable for 10BASE-T mode). The all-digital nature of the design makes the performance very tolerant to noise. The filter coefficients are self-adapting to accommodate varying conditions of cable quality and cable length.

## Echo Canceled

Because of the bidirectional nature of the channel in 1000BASE-T mode, an echo impairment is caused by each transmitter. The output of the echo filter is added to the FFE output to remove the transmitted signal impairment from the incoming receive signal. The echo canceler coefficients are self-adapting to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

## Cross Talk Canceled

The BCM53115S transmits and receives a continuous data stream on four channels. For a given channel, the signals sent by the other three local transmitters cause impairments on the received signal because of near-end crosstalk (NEXT) between the pairs. It is possible to cancel the effect because each receiver has access to the data for the other three pairs that cause this interference. The output of the adaptive NEXT canceling filters is added to the FFE output to cancel the NEXT impairment.

## Analog-to-Digital Converter

Each receive channel has its own 125 MHz analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital adaptive equalizer. Advanced analog circuit techniques achieve the following results:

- Low offset
- High power-supply noise rejection
- Fast settling time
- Low bit error rate

## Clock Recovery/Generator

The clock recovery and generator block creates the transmit and receive clocks for 1000BASE-T, 100BASE-TX, and 10BASE-T operation.

In 10BASE-T or 100BASE-TX mode, the transmit clock is locked to the 25 MHz crystal input, and the receive clock is locked to the incoming data stream.

In 1000BASE-T mode, the two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo and NEXT impairments by ensuring that the transmitter and receiver at each end of the link are operating at the same frequency.

## Baseline Wander Correction

1000BASE-T and 100BASE-TX data streams are not always DC-balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can vary with data content. This effect, which is known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM53115S automatically compensates for baseline wander by removing the DC offset from the input signal, thereby significantly reducing the probability of a receive symbol error.

In 10BASE-T mode, baseline wander correction is not performed because the Manchester coding provides a perfect DC balance.

## Multimode TX Digital-to-Analog Converter

The multimode transmit digital-to-analog converter (DAC) transmits PAM5, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that decreases the unwanted high frequency signal components, reducing electromagnetic interference (EMI). The transmit DAC uses a current drive output that is well-balanced, and therefore, produces very low noise transmit signals.

## Stream Cipher

In 1000BASE-T and 100BASE-TX modes, the transmit data stream is scrambled to reduce radiated emissions and to ensure that there are adequate transitions within the data stream. The 1000BASE-T scrambler also ensures that there is no correlation among symbols on the four different wire pairs and in the transmit and receive data streams. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range and eliminating peaks at certain frequencies. The randomization of the data stream also assists the digital adaptive equalizers and echo/crosstalk cancelers. The algorithms in these circuits require there to be no sequential or cross-channel correlation among symbols in the various data streams.

In 100BASE-TX mode, the transmit data stream is scrambled by exclusive ORing the encoded serial data stream. This is done with the output of an 11-bit wide linear feedback shift register (LFSR), producing a 2047-bit nonrepeating sequence.

In 1000BASE-T mode, the transmit data stream is scrambled by exclusive ORing the input data byte with an 8-bit wide cipher text word. The cipher text word generates each symbol period from eight uncorrelated maximal length data sequences that are produced by linear remapping of the output of a 33-bit wide LFSR. After the scrambled data bytes are encoded, the sign of each transmitted symbol is again randomized by a 4-bit wide cipher text word that is generated in the same manner as the 8-bit word. The master and slave transmitters use different scrambler sequences to generate the cipher text words. For repeater or switch applications, where all ports can transmit the same data simultaneously, signal energy is randomized further by using a unique seed to initialize the scrambler sequence for each PHY.

The receiver descrambles the incoming data stream by exclusive ORing it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle code groups. The descrambler locks to the scrambler state after detecting a sufficient number of consecutive idle codes. The BCM53115S enables transmission and reception of packet data only when the descrambler is locked. The receiver continually monitors the input data stream to ensure that it has not lost synchronization by checking that inter-packet gaps containing idles or frame extensions are received at expected intervals. When the BCM53115S detects loss of synchronization, it notifies the remote PHY of the inability to receive packets (1000BASE-T mode only) and attempts to resynchronize to the received data stream. If the descrambler is unable to resynchronize for a period of 750 ms, the BCM53115S is forced into the Link Fail state.

In 10BASE-T mode, scrambling is not required to reduce radiated emissions.

## Wire Map and Pair Skew Correction

During 1000BASE-T operation, the BCM53115S has the ability to automatically detect and correct some UTP cable wiring errors. The symbol decoder detects and compensates for (internal to the BCM53115S) the following errors:

- Wiring errors caused by the swapping of pairs within the UTP cable.
- Polarity errors caused by the swapping of wires within a pair.

The BCM53115S also automatically compensates for differences in the arrival times of symbols on the four pairs of the UTP cable. The varying arrival times are caused by differing propagation delays (commonly referred to as delay skew) between the wire pairs. The BCM53115S can tolerate delay skews of up to 64 ns long. Auto-negotiation must be enabled to take advantage of the wire map correction.

During 10/100 Mbps operation, pair swaps are corrected. Delay skew is not an issue though, because only one pair of wires is used in each direction.

## Automatic MDI Crossover

During copper auto-negotiation, one end of the link needs to perform an MDI crossover so that each transceiver's transmitter is connected to the other receiver. The BCM53115S can perform an automatic media-dependent interface (MDI) crossover, eliminating the need for crossover cables or cross-wired (MDIX) ports. During auto-negotiation, the BCM53115S normally transmits and receives on the TRD pins.

When connecting to another device that does not perform MDI crossover, the BCM53115S automatically switches its TRD in pairs when necessary to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

During 1000BASE-T operation, the BCM53115S swaps the transmit symbols on pairs 0 and 1 and pairs 2 and 3 if auto-negotiation completes in the MDI crossover state. The 1000BASE-T receiver automatically detects pair swaps on the receive inputs and aligns the symbols properly within the decoder. The automatic MDI crossover function cannot be disabled when in 1000BASE-T mode. During 10BASE-TX and 100BASE-T operation, pair swaps automatically occur within the device and do not require user intervention. The automatic MDI crossover function by default only works when auto-negotiation is enabled. This function can be disabled during auto-negotiation by writing to “PHY Extended Control Register (Page 10h–14h: Address 20h)” on [page 204](#) bit 14=1.



**Note:** This function only operates when the copper auto-negotiation is enabled.

## 10/100BASE-TX Forced Mode Auto-MDIX

The automatic MDI crossover function can also be enabled when in forced 10BASE-T or forced 100BASE-TX mode. This feature allows the user to disable the copper auto-negotiation in either 10BASE-T or 100BASE-TX and still take advantage of the automatic MDI crossover function. Whenever the forced link is down for at least 4 seconds, then auto-negotiation is internally enabled with its automatic MDI crossover function until link pulses or 100Tx idles are detected. Once detected, the PHY returns to forced mode operation.

The user should set the same speed in register 0 and the auto-negotiation advertisement register 4.



**Note:** This function only operates when the copper auto-negotiation is disabled.

## Resetting the PHY

The BCM53115S provides a hardware reset pin, RESET, which resets all internal nodes to a known state. Hardware reset is accomplished by holding the RESET pin low for at least 1 ms. Once RESET is brought high, the PHY will complete its reset sequence within 5 ms. All outputs will be inactive until the PHY has completed its reset sequence. The PHY will keep the inputs inactive for 5 ms after the deassertion of hardware reset. The hardware configuration pins and the PHY address pins will be read on the deassertion of hardware reset.

The BCM53115S also has a software reset capability. To enable the software reset, a 1 must be written to the bit. This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if 0 is written to this bit. Mode pins that are labelled sample on reset (SOR) are latched during hardware reset. Similarly, software resets also latch new values for the SOR mode pins.

## PHY Address

The BCM53115S has five unique PHY addresses for MII management of the internal PHYs. The PHY addresses for each port are as follows,

- PHY address for Port 0 is 0
- PHY address for Port 1 is 1
- PHY address for Port 2 is 2
- PHY address for Port 3 is 3
- PHY address for Port 4 is 4

## Super Isolate Mode

When in Super Isolate mode, the transmit and receive functions on the Copper Media Dependent Interface are disabled (No link will be established with the PHY's copper link partner). Any data received from the switch will be ignored by the BCM53115S and no data will be sent from the BCM53115S.

## Standby Power-Down Mode

The BCM53115S can be placed into standby power-down mode using software commands. In this mode, all PHY functions except for the serial management interface are disabled. To enter standby power-down mode, set MII Control register (page 10h–14h: address 00h), bit 11 = 1. There are three ways to exit standby power-down mode:

- Clear MII Control register (address 00h), bit 11 = 0.
- Set the software RESET bit 15, MII Control register (page 10h–14h: address 00h).
- Assert the hardware RESET pin.

Read or write operations to any MII register, other than MII Control register, while the device is in the standby power-down mode returns unpredictable results. Upon exiting standby power-down mode, the BCM53115S remains in an internal reset state for 40  $\mu$ s and then resumes normal operation.

## Auto Power-Down Mode

The BCM53115S can be placed into auto power-down mode. Auto power-down mode reduces device power when the signal from the copper link partner is not present. The auto power-down mode works whether the device is in Auto-negotiation Enabled or Forced mode. This mode is enabled by setting bit 5 = 1 of Auto Power-Down register. When auto power-down mode is enabled, the BCM53115S automatically enters the low-power mode when energy on the line is lost, and it resumes normal operation when energy is detected. When the BCM53115S is in auto power-down mode, it wakes up after 2.7s or 5.4s, which determined by bit 4 of Auto Power-Down register, and sends link pulses while monitoring for energy from the link partner. The BCM53115S enters normal operation and establishes a link if energy is detected, otherwise the wake-up mode continues for a duration of 84 ms to 1260 ms. This is determined by the timer bits [3:0] of Auto Power-Down register. before going back to low-power mode.

## External Loopback Mode

The External Loopback mode allows in-circuit testing of the BCM53115S as well as the transmit path through the magnetics and the RJ-45 connector. External loopback can be performed with and without a jumper block. External loopback with a jumper block tests the path through the magnetics and RJ-45 connector. External loopback without the jumper block only tests the BCM53115S's transmit and receive circuitry. In 1000BASE-T, 100BASE-TX, and 10BASE-T modes, a jumper block must be inserted into the RJ-45 connector to support external loopback. The jumper block should have the following RJ-45 pins connected together:

1-----3  
2-----6  
4-----7  
5-----8

The following six tables describe how the external loopback is enabled for 1000BASE-T, 100BASE-TX, and 10BASE-T modes with and without a jumper block.

**Table 12: 1000BASE-T External Loopback With External Loopback Plug**

| Register Writes                            | Comments                                                  |
|--------------------------------------------|-----------------------------------------------------------|
| Write 1800h to 1000BASE-T Control register | Enable 1000BASE-T Master Mode                             |
| Write 0040h to MII Control register        | Enable Force 1000BASE-T                                   |
| Write 8400h to Auxiliary Control register  | Enable External Loopback Mode with external loopback plug |

**Table 13: 1000BASE-T External Loopback Without External Loopback Plug**

| Register Writes                            | Comments                                                     |
|--------------------------------------------|--------------------------------------------------------------|
| Write 1800h to 1000BASE-T Control register | Enable 1000BASE-T Master Mode                                |
| Write 0040h to MII Control register        | Enable Force 1000BASE-T                                      |
| Write 8400h to Auxiliary Control register  | Enable External Loopback Mode                                |
| Write 0014h to Auxiliary Control register  | Enable External Loopback Mode without external loopback plug |

**Table 14: 100BASE-TX External Loopback With External Loopback Plug**

| Register Writes                     | Comments                                 |
|-------------------------------------|------------------------------------------|
| Write 2100h to MII Control register | Enable Force 100BASE-TX full-duplex mode |

**Table 15: 100BASE-TX External Loopback Without External Loopback Plug**

| Register Writes                           | Comment                                                      |
|-------------------------------------------|--------------------------------------------------------------|
| Write 2100h to MII Control register       | Enable Force 100BASE-TX full-duplex mode                     |
| Write 0014h to Auxiliary Control register | Enable external loopback mode without external loopback plug |

**Table 16: 10BASE-T External Loopback With External Loopback Plug**

| <b>Register Writes</b>              | <b>Comments</b>                        |
|-------------------------------------|----------------------------------------|
| Write 0100h to MII Control register | Enable Force 10BASE-T full-duplex mode |

**Table 17: 10BASE-T External Loopback Without External Loopback Plug**

| <b>Register Writes</b>                    | <b>Comments</b>                                              |
|-------------------------------------------|--------------------------------------------------------------|
| Write 0100h to MII Control register       | Enable Force 10BASE-T full-duplex mode                       |
| Write 0014h to Auxiliary Control register | Enable external loopback mode without external loopback plug |



**Note:** To exit the External Loopback mode, a software or hardware reset is recommended.

## Full-Duplex Mode

The BCM53115S supports full-duplex operation. While in full-duplex mode, a transceiver can simultaneously transmit and receive packets on the cable.

## Copper Mode

When auto-negotiation is disabled, full-duplex operation can be enabled by setting bit 8 of “[MII Control Register \(Page 10h–14h: Address 00h–01h\)](#)” on page 194.

When auto-negotiation is enabled, the full-duplex capability is advertised for:

- 10BASE-T when bit 6 of “[Auto-Negotiation Advertisement Register \(Page 10h–14h: Address 08h\)](#)” on page 196.
- 100BASE-T when bit 8 “[Auto-Negotiation Advertisement Register \(Page 10h–14h: Address 08h\)](#)” on page 196 is set.
- 1000BASE-T when bit 9 of “[1000BASE-T Control Register \(Page 10h–14h: Address 12h\)](#)” on page 201 is set.

## Master/Slave Configuration

In 1000BASE-T mode, the BCM53115S and its link partner perform loop timing. One end of the link must be configured as the timing master, and the other end as the slave. Master/slave configuration is performed by the auto-negotiation function. The auto-negotiation function first looks at the manual master/slave configuration bits advertised by the local PHY and the link partner. If neither PHY requests manual configuration, then the auto-negotiation function looks at the advertised repeater/DTE settings. If one PHY is advertised as a repeater port and the other is advertised as a DTE port, then the repeater port is configured as the master and the DTE port as the slave. Each end generates an 11-bit random seed if the two settings are equal, and the end with the higher seed is configured as the master. If the local PHY and the link partner generate the same random seed, then auto-negotiation is restarted.

If both ends of the link attempt to force the same manual configuration (both master or both slave), or the random seeds match seven consecutive times, then the BCM53115S sets the Master/Slave Configuration Fault bit in the 1000BASE-T Status register, and auto-negotiation is restarted. This is used to set the BCM53115S to manual master/slave configuration or to set the advertised repeater/DTE configuration.

## Next Page Exchange

The 1000BASE-T configuration requires the exchange of three auto-negotiation next pages between the BCM53115S and its link partner. Exchange of 1000BASE-T Next Page information takes place automatically when the BCM53115S is configured to advertise 1000BASE-T capability.

The BCM53115S also supports software controlled Next Page exchanges. This includes the three 1000BASE-T Next Pages, which are always sent first. The BCM53115S automatically generates the appropriate message code field for the 1000BASE-T pages. When the BCM53115S is not configured to advertise 1000BASE-T capability, the 1000BASE-T Next Pages are not sent.

When the BCM53115S is not configured to advertise 1000BASE-T capability and bit 15 of “[Auto-Negotiation Advertisement Register \(Page 10h–14h: Address 08h\)](#)” on page 196, BCM53115S does not advertise Next Page ability.

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## Frame Management

The BCM53115S provides a Frame Management block that works in conjunction with one of the GMII ports operate in IMP mode as the full duplex packet streaming interface to the external CPU, with in-band messaging mechanism for management purpose.

## In-Band Management Port

The BCM53115S provides two GMII ports and supports a dual IMP ports (IMP port and port 5) feature. One (IMP port) or both GMII ports (IMP port and Port 5) can be configured as the management port using the “[Global Management Configuration Register \(Page 02h: Address 00h\)](#)” on page 169. In the dual IMP feature, all traffic to the CPU from LAN ports will be forwarded to IMP port, and all traffic to the CPU from WAN ports will be forwarded to port 5. When the GMII port is defined as the Frame Management Port, it is referred to as the in-band management port (IMP).

The IMP can be used as a full-duplex 10/100/1000 Mbps port, which can be used to forward management information to the external management agent, such as BPDUs, mirrored frames, or frames addressed to other static address entries that have been identified as a special interest to the management system.

As IMP is defined as the frame management port, normal frame data is forwarded to the port based on the state of the RX\_UCST\_EN, RX\_MCST\_EN and RX\_BCST\_EN bits in the “[IMP Port Control Register \(Page 00h: Address 08h\)](#)” on page 149. If these bits are cleared, no frame data will be forwarded to the Frame Management Port, with the exception that frames meeting the mirror ingress/egress rules criteria, will always be forwarded to the designated frame management port.

Packets transferred over the IMP port are tagged with the Broadcom proprietary header to carry the necessary information which is of interest to the management entity running on the CPU, as shown below, except for the PAUSE frame. The IMP port must support normal Ethernet pause based flow control mechanism.

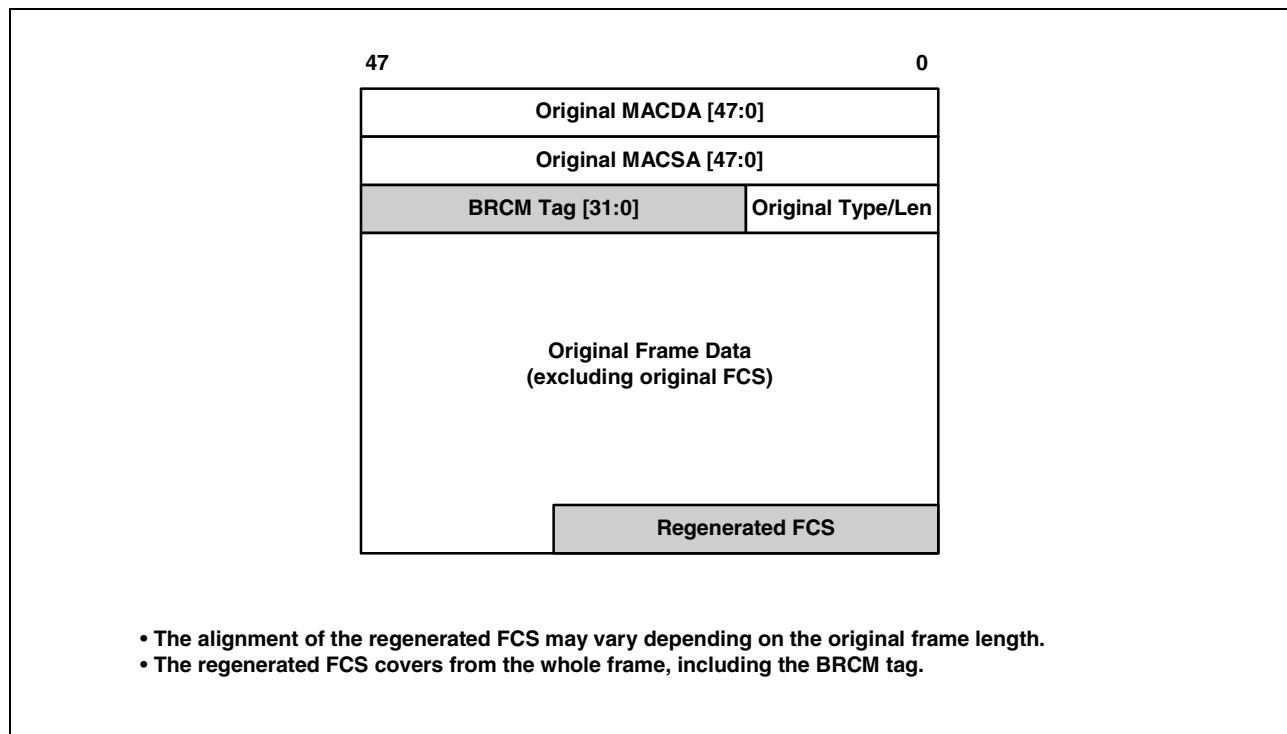


Figure 9: IMP Packet Encapsulation Format

The BRCM tag is designed for asymmetric operation across the IMP port. The information carried from the switching device to the CPU is different from the information carried from the CPU to the switching device.

Similarly, the host system must insert the BRCM tag fields into frames it wished to send into the management port, to be routed to specific egress ports. The OPCODE within the tag field determines how the frame is handled, and allows frames to be forwarded using the normal address lookup using a port ID designation within the Tag.

The BRCM tag are transmitted with the convention of highest significant octet first, followed by the next lowest significant octet, and so on, with the least significant bit of each octet transmitted out from the MAC first. So, for the BRCM tag field in [Table 18](#), the most significant octet would be transmitted first (bits [24:31]), with bit 24 being the first bit transmitted.

## Broadcom Tag Format for Egress Packet Transfer

When a packet is forwarded by the switching device to the external CPU for processing, the BRCM tag is formatted as shown in the table below.

**Table 18: Egress Broadcom Tag Format (IMP to CPU)**

| 31–29        | 28–24    | 23–16    | 15–8             | 7–5     | 4–0          |
|--------------|----------|----------|------------------|---------|--------------|
| OPCODE = 000 | Reserved | Reserved | REASON_CODE[7:0] | TC[2:0] | SRC_PID[4:0] |

- **OPCODE 000**  
This indicates the packet transfer with explicit reasons to help the external CPU to direct the packet for the appropriate packet processing entities.
- **REASON\_CODE [7:0]**  
This indicates the reasons why the packet is forwarded to the external CPU so that the CPU can identify the appropriate software routines for packet processing.
  - Bit [0] indicates mirroring
  - Bit [1] indicates SA learning
  - Bit [2] indicates switching
  - Bit [3] indicates protocol termination
  - Bit [4] indicates protocol snooping
  - Bit [5] indicates flooding/exception processing
  - Bit [6] and Bit[7] are reserved
- **TC [2:0]**  
This indicates the traffic class classified by the switching device when forwarding the packet to the CPU.
- **SRC\_PID [4:0]**  
This indicates the ingress port of the switching device where the packet is received.

## Broadcom Tag Format for Ingress Packet Transfer

For packet transfer from the external CPU to the switching device, the BRCM tag is formatted as shown in [Table 19](#).

**Table 19: Ingress BRCM Tag (CPU to IMP)**

| 31–29      | 28–26   | 25–24   | 23–0     |               |
|------------|---------|---------|----------|---------------|
| OPCODE=000 | TC[2:0] | TE[1:0] | Reserved |               |
| 31–29      | 28–26   | 25–24   | 23       | 22–0          |
| OPCODE=001 | TC[2:0] | TE[1:0] | Reserved | DST_MAP[22:0] |

- **OPCODE 000**

It indicates that the external CPU is not dictating how the packet is forwarded, and the packet is forwarded by the switching device based on the original Ethernet packet information.

- **OPCODE 001**

This indicates the packet is forwarded to multiple (or single) egress ports by the switching device based on the explicit direction of the external CPU.

- **DST\_MAP [22:0]**

This indicates the egress port bit map to which the external CPU intends to forward the packet. Bits[5:0] = Port[5:0], Bit 8 = IMP port.

- **TC [2:0]**

This indicates the traffic class with which the external CPU intends to forward the packet.

- **TE (tag enforcement)**

This indicates the 802.1Q/P tagging/untagging encapsulation enforcement for the packet transmission.

00 = No enforcement (follow VLAN untag mask rules)

01 = Untag enforcement

10 = Tag enforcement

11 = Reserved

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## MIB Engine

The MIB Engine is responsible for processing status words received from each port. Based on whether it is a receive status or transmit status, appropriate MIB counters are updated. The BCM53115S implement 70-plus MIB counters on a per-port basis. MIB counters can be categorized into three groups: receive-only counters, transmit-only counters, and receive or transmit counters. This latter group can, as a group, be selectively steered to the receive or transmit process on a per-port basis. The section below describes each individual counter.

The BCM53115S offers the MIB snapshot feature per port using the enabled [“Page 70h: MIB Snapshot Control Register” on page 288](#). A snapshot of a selected port MIB registers can be captured and available to the users while MIB counters are continuing to count.

If bit[7:6] = 10 of [“Page 70h: MIB Snapshot Control Register” on page 288](#), the captured snapshot MIB counters can be read from [“Page 71h: Port Snapshot MIB Control Register” on page 289](#) after bit 7 of [“Page 70h: MIB Snapshot Control Register” on page 288](#) is cleared to 0. Registers in [“MII Control Register \(Page 15h: Address 00h\)” on page 227](#) can be read for live counter.

If bit[7:6] = 11 of [“Page 70h: MIB Snapshot Control Register” on page 288](#), the captured snapshot MIB counters can be read from [“Page 71h: Port Snapshot MIB Control Register” on page 289](#) or [“MII Control Register \(Page 15h: Address 00h\)” on page 227](#) (depending on which port is captured) after bit 7 of [“Page 70h: MIB Snapshot Control Register” on page 288](#) is cleared to 0. The live counters cannot be read.

## MIB Counters per Port

The total number of counters per port is 43.

**Table 20: Recieve-Only Counters (19)**

| <b>Receive-Only Counter</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RxDropPkts (32 bit)         | Number of good packets received by a port that were dropped due to a lack of resources (such as lack of input buffers) or were dropped due to a lack of resources before a determination of the validity of the packet was able to be made (such as receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxExcessSizeDisc, the RxAlignmentErrors, or the RxFCSErrors counters. |
| RxOctets (64 bit)           | Number of data bytes received by a port (excluding preamble but including FCS) including bad packets.                                                                                                                                                                                                                                                                                                                         |
| RxBroadcastPkts (32 bit)    | Number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets. The maximum packet size can be programmed.                                                                                                                                                                                                          |
| RxMulticastPkts (32 bit)    | Number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets. The maximum packet size can be programmed.                                                                                                                                                                                                            |
| RxSACHanges (32 bit)        | Number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network. The maximum packet size can be programmed.                                                                                                                                                                                                  |
| RxUndersizePkts (32 bit)    | Number of good packets received by a port that are less than 64 bytes long (excluding framing bits, but including the FCS)                                                                                                                                                                                                                                                                                                    |
| RxOversizePkts (32 bit)     | Number of good packets received by a port that are greater than standard maximum frame size. The maximum packet size can be programmed.                                                                                                                                                                                                                                                                                       |
| RxFragments (32 bit)        | Number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error                                                                                                                                                                                                                                                                                  |
| RxJabbers (32 bit)          | Number of packets received by a port that are longer than standard maximum frame size and have either an FCS error or an alignment error                                                                                                                                                                                                                                                                                      |
| RxUnicastPkts (32 bit)      | Number of good packets received by a port that are addressed to a unicast address. The maximum packet size can be programmed.                                                                                                                                                                                                                                                                                                 |
| RxAlignmentErrors (32 bit)  | Number of packets received by a port that have a length (excluding framing bits but including FCS) between 64 and standard maximum frame size, inclusive, and have a bad FCS with a nonintegral number of bytes                                                                                                                                                                                                               |
| RxFCSErrors (32 bit)        | Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard maximum frame size, inclusive, and have a bad FCS with an integral number of bytes                                                                                                                                                                                                                |
| RxGoodOctets (64 bit)       | Total number of bytes in all good packets received by a port (excluding framing bits, but including FCS). The maximum packet size can be programmed.                                                                                                                                                                                                                                                                          |
| JumboPktCount (32 bit)      | Number of good packets received by a port that are greater than the standard maximum size and less than or equal to the jumbo packet size, regardless of CRC or alignment errors                                                                                                                                                                                                                                              |

**Table 20: Receive-Only Counters (19) (Cont.)**

| <b>Receive-Only Counter</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RxPausePkts (32 bit)        | Number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC Control Frame EtherType field (88–08h), a destination MAC address of either the MAC Control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE opcode (00–01), must be a minimum of 64 bytes in length (excluding preamble but including FCS) and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half-/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network. |
| RxSymbolErrors (32 bit)     | Total number of times a valid-length packet was received at a port and at least one invalid data symbol was detected. The counter only increments once per carrier event and does not increment on detection of a collision during the carrier event.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| RxDiscard (32 bit)          | Number of good packets received by a port that were discarded by the forwarding process                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| InRangeErrors (32 bit)      | Number of packets received with good CRC and one of the following: <ul style="list-style-type: none"> <li>Value of length/type field is between 46 and 1500, inclusive, and does not match the number of (MAC client data + PAD) data octets received</li> <li>Value of length/type field is less than 46 and the number of data octets received is greater than 46 (which does not require padding)</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| OutOfRangeErrors (32 bit)   | Number of packets received with good CRC and the value of length/type field is greater than 1500 and less than 1536                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

**Table 21: Transmit-Only Counters (17)**

| <b>Transmit-Only Counters</b> | <b>Description</b>                                                                                                                                                                                                                                               |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TxDropPkts (32 bit)           | This counter is incremented every time a transmit packet is dropped due to a lack of resources (such as a transmit FIFO underflow) or an internal MAC sublayer transmit error is not counted by either the TxLateCollision or the TxExcessiveCollision counters. |
| TxOctets (64 bit)             | Total number of good bytes of data transmitted by a port (excluding preamble but including FCS)                                                                                                                                                                  |
| TxBroadcastPkts (32 bit)      | Number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.                                                                                       |
| TxMulticastPkts (32 bit)      | Number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.                                                                                       |
| TxCollisions (32 bit)         | Number of collisions experienced by a port during packet transmissions                                                                                                                                                                                           |
| TxUnicastPkts (32 bit)        | Number of good packets transmitted by a port that are addressed to a unicast address                                                                                                                                                                             |

**Table 21: Transmit-Only Counters (17) (Cont.)**

| <b>Transmit-Only Counters</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TxSingleCollision (32 bit)    | Number of packets successfully transmitted by a port that have experienced exactly one collision                                                                                                                                                                                                                                                                                                                                         |
| TxMultipleCollision (32 bit)  | Number of packets successfully transmitted by a port that have experienced more than one collision                                                                                                                                                                                                                                                                                                                                       |
| TxDeferredTransmit (32 bit)   | Number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy. This only applies to the half-duplex mode while the Carrier Sensor is busy.                                                                                                                                                                                                                                      |
| TxLateCollision (32 bit)      | Number of times that a collision is detected later than 512 bit-times into the transmission of a packet                                                                                                                                                                                                                                                                                                                                  |
| TxPausePkts (32 bit)          | Number of PAUSE events at each port                                                                                                                                                                                                                                                                                                                                                                                                      |
| TxFramelnDisc (32 bit)        | Number of valid packets received which are discarded by the forwarding process due to lack of space on an output queue (not maintained or reported in the MIB counters). Located in the Congestion Management registers (page 0Ah). This attribute only increments if a network device is not acting in compliance with a flow control request, or the BCM53115S internal flow-control/buffering scheme has been configured incorrectly. |
| TxQ0PKT(32 bit)               | Total number of good packets transmitted on CoS0, specified in MIB queue select register when QoS is enabled.                                                                                                                                                                                                                                                                                                                            |
| TxQ1PKT(32 bit)               | Total number of good packets transmitted on CoS1, specified in MIB queue select register when QoS is enabled.                                                                                                                                                                                                                                                                                                                            |
| TxQ2PKT(32 bit)               | Total number of good packets transmitted on CoS2, specified in MIB queue select register when QoS is enabled.                                                                                                                                                                                                                                                                                                                            |
| TxQ3PKT(32 bit)               | Total number of good packets transmitted on CoS3, specified in MIB queue select register when QoS is enabled.                                                                                                                                                                                                                                                                                                                            |

**Table 22: Transmit or Receive Counters (10)**

| <b>Transmit or Receive Counter</b> | <b>Description</b>                                                                                              |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------|
| Pkts64Octets (32 bit)              | Number of packets (including error packets) that are 64 bytes long                                              |
| Pkts65to127Octets (32 bit)         | Number of packets (including error packets) that are between 65 and 127 bytes long                              |
| Pkts128to255Octets (32 bit)        | Number of packets (including error packets) that are between 128 and 255 bytes long                             |
| Pkts256to511Octets (32 bit)        | Number of packets (including error packets) that are between 256 and 511 bytes long                             |
| Pkts512to1023Octets (32 bit)       | Number of packets (including error packets) that are between 512 and 1023 bytes long                            |
| Pkts1024toMaxPktOctets (32 bit)    | Number of packets that (include error packets) are between 1024 and the standard maximum packet size, inclusive |

Table 23 on page 82 identifies the mapping of the BCM53115S MIB counters and their generic mnemonics to the specific counters and mnemonics for each of the key IETF MIBs that are supported. Direct mappings are defined. However, there are several additional statistics counters which are indirectly supported that make up the full complement of counters required to fully support each MIB. These are shown in Table 24 on page 84.

Finally, Table 25 on page 85 identifies the additional counters supported by the BCM53115S and references the specific standard or reason for the inclusion of the counter.

**Table 23: Directly Supported MIB Counters**

| <b>BCM53115S MIB</b> | <b>Ethernet-Like MIB RFC 1643</b> | <b>Bridge MIB RFC 1493</b> | <b>MIB II Interface RFC 1213/1573</b> | <b>RMON MIB RFC 1757</b> |
|----------------------|-----------------------------------|----------------------------|---------------------------------------|--------------------------|
| RxDropPkts           | dot3StatsInternalMACReceiveErrors | dot1dTpPortInDiscards      | ifInDiscards                          | –                        |
| RxOctets             | –                                 | –                          | ifInOctets                            | etherStatsOctets         |
| RxBroadcastPkts      | –                                 | –                          | ifInBroadcastPkts                     | etherStatsBroadcastPkts  |
| RxMulticastPkts      | –                                 | –                          | ifInMulticastPkts                     | etherStatsMulticastPkts  |
| RxSACChanges         | Note 2                            | Note 2                     | Note 2                                | Note 2                   |
| RxUndersizePkts      | –                                 | –                          | –                                     | etherStatsUndersizePkts  |
| RxOversizePkts       | dot3StatsFrameToo Longs           | –                          | –                                     | etherStatsOversizePkts   |
| RxFragments          | –                                 | –                          | –                                     | etherStatsFragments      |
| RxJabbers            | –                                 | –                          | –                                     | etherStatsJabbers        |
| RxUnicastPkts        | –                                 | –                          | ifInUcastPkts                         | –                        |
| RxAlignmentErrors    | dot3StatsAlignmentErrors          | –                          | –                                     | –                        |
| RxFCSErrors          | dot3StatsFCSErrors                | –                          | –                                     | –                        |
| RxGoodOctets         | –                                 | –                          | –                                     | –                        |
| RxExcessSizeDisc     | Note 2                            | Note 2                     | Note 2                                | Note 2                   |
| RxPausePkts          | Note 2                            | Note 2                     | Note 2                                | Note 2                   |
| RxSymbolErrors       | Note 2                            | Note 2                     | Note 2                                | Note 2                   |
| Note 1               | –                                 | –                          | ifInErrors                            | –                        |
| Note 1               | –                                 | –                          | ifInUnknownProtos                     | –                        |
| Note 1               | –                                 | dot1dTpPortInFrames        | –                                     | –                        |

**Table 23: Directly Supported MIB Counters (Cont.)**

| <b>BCM53115S MIB</b>   | <b>Ethernet-Like MIB RFC 1643</b>  | <b>Bridge MIB RFC 1493</b> | <b>MIB II Interface RFC 1213/1573</b> | <b>RMON MIB RFC 1757</b>        |
|------------------------|------------------------------------|----------------------------|---------------------------------------|---------------------------------|
| TxDropPkts             | dot3StatsInternalMACTransmitErrors | —                          | ifOutDiscards                         | —                               |
| TxOctets               | —                                  | —                          | ifOutOctetsNote 3                     | —                               |
| Note 1                 | —                                  | dot1dTpPortOutFrames       | —                                     | —                               |
| TxBroadcastPkts        | —                                  | —                          | ifOutBroadcastPkts                    | —                               |
| TxMulticastPkts        | —                                  | —                          | ifOutMulticastPkts                    | —                               |
| TxCollisions           | —                                  | —                          | —                                     | etherStatsCollisions            |
| TxUnicastPkts          | —                                  | —                          | ifOutUcastPkts                        | —                               |
| TxSingleCollision      | dot3StatsSingleCollisionFrames     | —                          | —                                     | —                               |
| TxMultipleCollision    | dot3StatsMultipleCollisionFrames   | —                          | —                                     | —                               |
| TxDeferredTransmit     | dot3StatsDeferredTransmissions     | —                          | —                                     | —                               |
| TxLateCollision        | dot3StatsLateCollision             | —                          | —                                     | —                               |
| TxExcessiveCollision   | dot3StatsExcessiveCollision        | —                          | —                                     | —                               |
| TxFramelnDisc          | Note 2                             | Note 2                     | Note 2                                | Note 2                          |
| TxPausePkts            | Note 2                             | Note 2                     | Note 2                                | Note 2                          |
| Note 4                 | dot3StatsCarrierSenseErrors        | —                          | —                                     | —                               |
| Note 1                 | —                                  | —                          | ifOutErrors                           | —                               |
| Pkts64Octets           | —                                  | —                          | —                                     | etherStatsPkt64Octets           |
| Pkts65to127Octets      | —                                  | —                          | —                                     | etherStatsPkt65to127Octets      |
| Pkts128to255Octets     | —                                  | —                          | —                                     | etherStatsPkt128to255Octets     |
| Pkts256to511Octets     | —                                  | —                          | —                                     | etherStatsPkt256to511Octets     |
| Pkts512to1023Octets    | —                                  | —                          | —                                     | etherStatsPkt512to1023Octets    |
| Pkts1024toMaxPktOctets | —                                  | —                          | —                                     | etherStatsPkt1024toMaxPktOctets |
| Note 1                 | —                                  | —                          | —                                     | etherStatsDropEvents            |
| Note 1                 | —                                  | —                          | —                                     | etherStatsPkts                  |
| Note 1                 | —                                  | —                          | —                                     | etherStatsCRCAlignErrors        |

**Table 23: Directly Supported MIB Counters (Cont.)**

| <b>BCM53115S MIB</b> | <b>Ethernet-Like MIB RFC 1643</b> | <b>Bridge MIB RFC 1493</b> | <b>MIB II Interface RFC 1213/1573</b> | <b>RMON MIB RFC 1757</b> |
|----------------------|-----------------------------------|----------------------------|---------------------------------------|--------------------------|
| Note 4               | dot3StatsSQETestErrors            | —                          | —                                     | —                        |

**Note 1:** Derived by summing two or more of the supported counters. See [Table 24 on page 84](#) for specific details.

**Note 2:** Extensions required by recent standards developments or BCM53115S operation specifics.

**Note 3:** The MIB II interfaces specification for if OutOctets includes preamble/SFD and errored bytes. Because IEEE 802.3-compliant MACs have no requirement to keep track of the number of transmit bytes in an errored frame, this count is impossible to maintain. The TxOctets counter maintained by the BCM53115S is consistent with good bytes transmitted, excluding preamble, but including FCS. The count can be adjusted to more closely match the if OutOctets definition by adding the preamble for TxGoodPkts and possibly an estimate of the octets involved in TxCollisions and TxLateCollision.

**Note 4:** The attributes TxCarrierSenseErrors and TxSQETestErrors are not supported in the BCM53115S. These attributes were originally defined to support coax-based AUI transceivers. The BCM53115S integrated transceiver design means these error conditions are eliminated. MIBs intending to support such counters should return a value of 0 (not supported).

**Table 24: Indirectly Supported MIB Counters**

| <b>BCM53115S MIB</b>                                                                              | <b>Ethernet-Like MIB RFC 1643</b> | <b>Bridge MIB RFC 1493</b> | <b>MIB II Interface RFC 1213/1573</b> | <b>RMON MIB RFC 1757</b> |
|---------------------------------------------------------------------------------------------------|-----------------------------------|----------------------------|---------------------------------------|--------------------------|
| RxErrorPkts =<br>RxAlignmentErrors + RxFCSErrors +<br>RxFragments + RxOversizePkts +<br>RxJabbers | —                                 | —                          | ifInErrors                            | —                        |
| —                                                                                                 | —                                 | —                          | ifInUnknownProtos                     | —                        |
| RxGoodPkts =<br>RxUnicastPkts + RxMulticastPkts +<br>RxBroadcastPkts                              | —                                 | dot1dTpPortIn<br>Frames    | —                                     | —                        |
| DropEvents =<br>RxDropPkts + TxDropPkts                                                           | —                                 | —                          | —                                     | etherStatsDropEvents     |
| RxTotalPkts =<br>RxGoodPkts + RxErrorPkts                                                         | —                                 | —                          | —                                     | etherStatsPkts           |
| RxCRCAlignErrors = RxCRCErrors<br>+ RxAlignmentErrors                                             | —                                 | —                          | —                                     | etherStatsCRCAlignErrors |
| —                                                                                                 | dot3StatsSQETestErrors            | —                          | —                                     | —                        |

**Table 24: Indirectly Supported MIB Counters (Cont.)**

| <b>BCM53115S MIB</b>                                           | <b>Ethernet-Like MIB RFC 1643</b> | <b>Bridge MIB RFC 1493</b> | <b>MIB II Interface RFC 1213/1573</b> | <b>RMON MIB RFC 1757</b> |
|----------------------------------------------------------------|-----------------------------------|----------------------------|---------------------------------------|--------------------------|
| RxFramesTooLong = RxOversizePkts + RxJabber                    | dot3StatsFrameTooLongs            | –                          | –                                     | –                        |
| TxGoodPkts = TxUnicastPkts + TxMulticastPkts + TxBroadcastPkts | –                                 | dot1dTpPortOut Frames      | –                                     | –                        |
| TxErrorPkts = TxExcessiveCollision + TxLateCollisionNote 1     | –                                 | –                          | ifOutErrors                           | –                        |

**Note 1:** The number of packets transmitted from a port that experienced a late collision or excessive collisions. While some media types operate in half-duplex mode, frames that experience carrier sense errors are also summed in this counter. The BCM53115S integrated design means this error condition is eliminated.

**Table 25: BCM53115S Supported MIB Extensions**

| <b>BCM53115S MIB</b> | <b>Appropriate Standards Reference</b>                                                                                                                                                                  |
|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RxSACHanges          | IEEE 802.3u Clause 30 — Repeater Port Managed Object Class<br>aSourceAddressChanges                                                                                                                     |
| RxExcessSizeDisc     | The BCM53115S cannot store packets in excess of 1536 bytes (excluding preamble/SFD, but inclusive of FCS). This counter indicates packets that were discarded by the BCM53115S due to excessive length. |
| RxPausePkts          | IEEE 802.3x Clause 30 — PAUSE Entity Managed Object Class<br>aPAUSEMACCtrlFramesReceived                                                                                                                |
| RxSymbolErrors       | IEEE 802.3u Clause 30 — Repeater Port Managed Object Class<br>aSymbolErrorDuringPacket                                                                                                                  |
| TxFramelnDisc        | Internal diagnostic use for optimization of flow control and buffer allocation algorithm                                                                                                                |
| TxPausePkts          | Number of PAUSE events at a given port                                                                                                                                                                  |

---

## Integrated High-Performance Memory

The BCM53115S embeds a 128 KB high-performance SRAM for storing the following, thus eliminating the need for external memory and allowing for the implementation of extremely low-cost systems:

- Packet data
- The ARL table
- The VLAN table
- The TX queues
- Descriptors

The internal RAM controller efficiently executes memory transfers and achieves nonblocking performance for stand-alone 5-port applications.

---

## Switch Controller

The core of the BCM53115S devices is a cost-effective and high-performance switch controller. The controller manages packet forwarding between the MAC receive and transmit ports through the frame buffer memory with a store and forward architecture. The switch controller encompasses the functions of buffer management, memory arbitration, and transmit descriptor queueing.

## Buffer Management

The frame buffer memory is divided into pages (units of data consisting of 256 bytes each). Each received packet may be allocated more than one page. For example, six pages are required to store a 1522-byte frame. Frame data is stored in the buffer memory as the packet is received. After reception, the frame is queued to the egress port(s) transmit queue. This list tracks the transmission of the packet. After successful packet transmission, the buffer memory is released to the free buffer pool.

## Memory Arbitration

Processes requesting access to the internal memory include the receive and transmit frame data handlers, address resolution, the VLAN lookup, learning and aging functions, egress descriptor update, and output-port queue managers. These processes are arbitrated to provide fair access to the memory and minimize the latency of critical processes to provide a fully nonblocking solution.

## Transmit Output Port Queues

Frames are maintained in the egress port using a linked list. Two levels of linked lists are used to maintain one output queue (see [Figure 10](#)). The first level is the TXQ linked list, and the second level is the buffer tag linked list. The TXQ linked list is used to maintain frame TC order for each port. For each frame, the buffer tag linked list is used to maintain the order of the buffer pages corresponding to each frame.

Each egress port supports up to six transmit queues for servicing Quality of Service (QoS). All six transmit queues share the 512 entries of the TXQ table. The TXQ table is maintained as a linked list, and each node in the TXQ uses one entry in the TXQ table. The TXQ size for each priority can be programmed to up to 512 entries.

When the QoS function has been turned off, the switch controller maintains one output queue for each egress port. The TXQ table is maintained in a per-port individual internal memory. Each node in the queue represents a pointer that points to a frame buffer tag. Each buffer tag includes frame information and a pointer to the next buffer tag. Each buffer tag has an associated page allocated in the frame buffer. For a packet with a frame size larger than 256 bytes, multiple buffer tags are required. For instance, a 9720-byte jumbo frame requires 38 buffer tags for handling the frame.

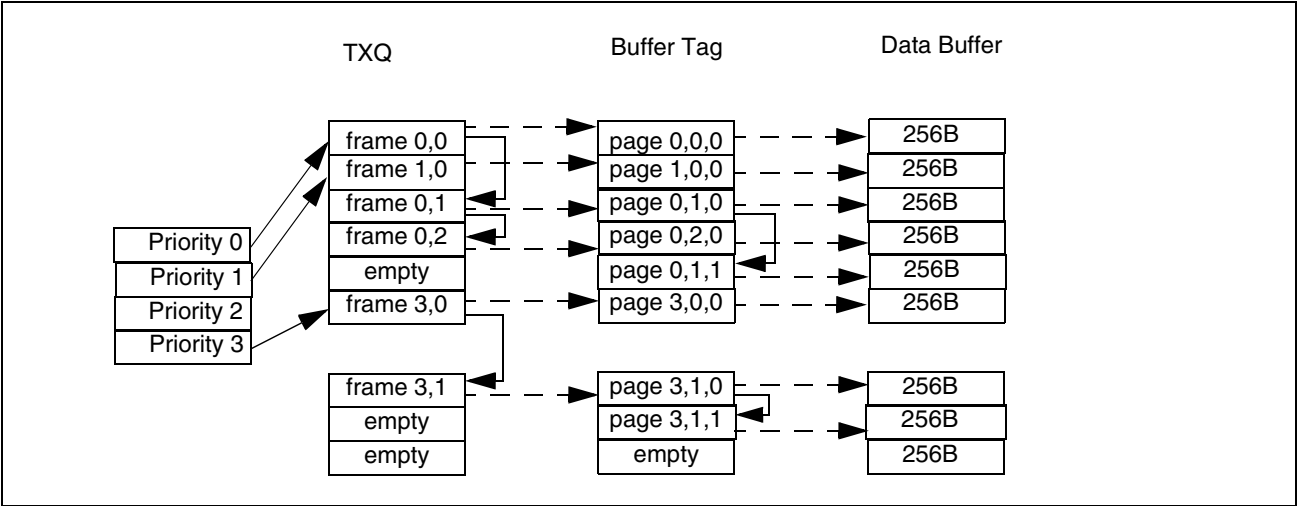


Figure 10: TXQ and Buffer Tag Structure

## Section 4: System Interfaces

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### Overview

The BCM53115S include the following interfaces:

- “Copper Interface” on page 88
- “SGMII/SerDes Interface” on page 89
- “Frame Management Port Interface” on page 89
- “WAN Interface” on page 91
- “Configuration Pins” on page 91
- “Programming Interfaces” on page 91
- “MDC/MDIO Interface” on page 109
- “LED Interfaces” on page 116

Each interface is discussed in detail in these sections.

---

### Copper Interface

The internal PHYs transmit and receive data using the analog copper interface. This section discusses the following topics:

- “Auto-Negotiation” on page 88
- “Lineside (Remote) Loopback Mode” on page 89
- “Reverse MII Interface (RvMII)” on page 90
- “GMII Interface” on page 90
- “RGMII Interface” on page 90
- “SPI-Compatible Programming Interface” on page 92
- “EEPROM Interface” on page 106
- “MDC/MDIO Interface Register Programming” on page 109
- “Pseudo-PHY” on page 110

### Auto-Negotiation

The BCM53115S negotiate a mode of operation over the copper media using the auto-negotiation mechanism defined in the IEEE 802.3u and IEEE 802.3ab specifications. When the auto-negotiation function is enabled, the BCM53115S automatically choose the mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM53115S can be configured to advertise the following modes:

- 100BASE-T full-duplex and/or half-duplex
- 100BASE-TX full-duplex and/or half-duplex

- 10BASE-T full-duplex and/or half-duplex

The transceiver negotiates with its link partner and chooses the highest common operating speed and duplex mode, commonly referred to as highest common denominator (HCD). Auto-negotiation can be disabled by software control, but is required for 1000BASE-T operation.

## Lineside (Remote) Loopback Mode

The lineside loopback mode allows the testing of the copper interface from the link partner. This mode is enabled by setting bit 15 of the Miscellaneous Test register. The MDI receive packet is passed through the PCS and sent back out as the MDI transmit packet. The PCS receive data appears on the internal MAC interface.

## SGMII/SerDes Interface

The BCM53115S provides one GMII/RGMII/SGMII/MII/RvMII interface for the WAN port, and it can be configured in SGMII or SerDes mode.

In SGMII mode, the transmit and receive differential pairs are running at 1.25 Gbps. The receive and transmit clocks are embedded within the data stream. Because the data is 8b/10b encoded, the actual throughput is 1 Gbps. SGMII is an LVDS interface and commonly connected to an external PHY for a 10/100/1000BASE-T application. The BCM53115S supports auto-negotiation on its SGMII interface. When the device operates at 10 Mbps or 100 Mbps, the SGMII differential pair replicates the data 100 and 10 times, respectively.

In SerDes mode, the differential pair also runs at 1.25 Gbps. With 8b/10b encoding, the actual data throughput is 1 Gbps. Therefore, fiber is a typical application using this interface, which can be connected directly to an optical module with an option of being DC- or AC-coupled for 1000BASE-X application.

## Frame Management Port Interface

The dedicated frame management port provides high-speed connection to transfer management packets to an external management agent. For more information about frame management, see [“Frame Management” on page 75](#). The port is configurable to Reverse MII (RvMII), GMII, or RGMII using the strap pins or software configuration.

## MII/TMII Interface

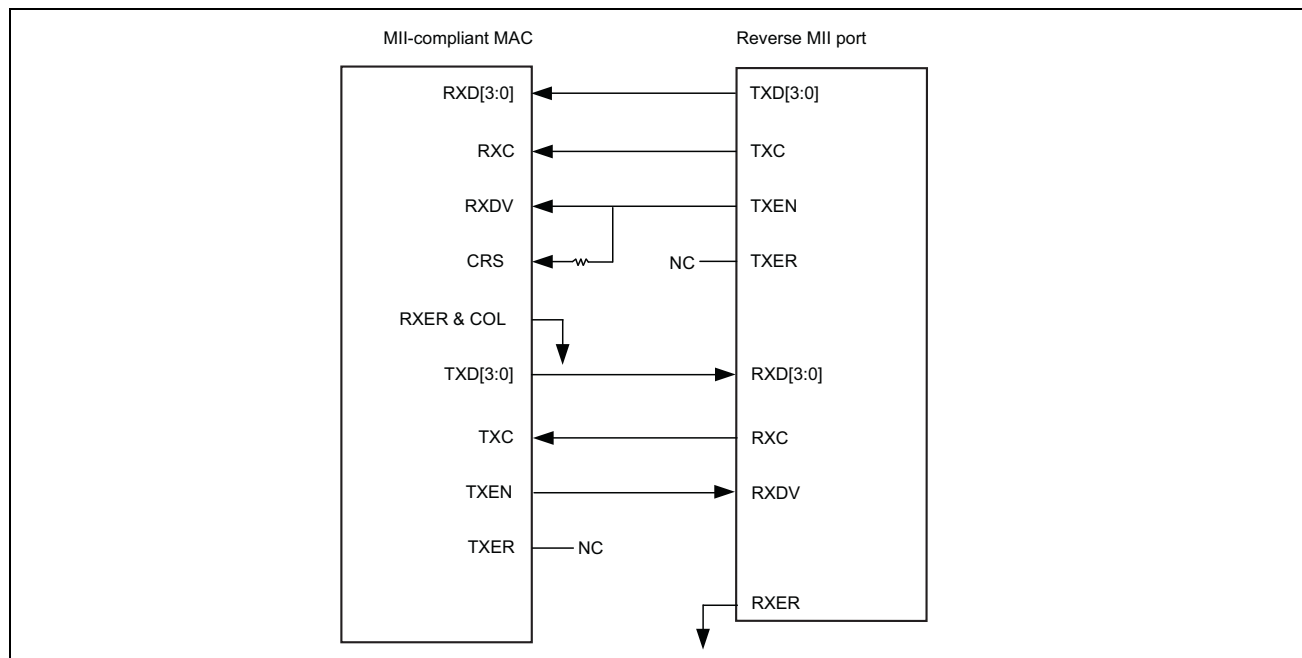
The BCM53115S provides a fully IEEE 802.3u-compatible MII interface. This interface can run at the standard 100 Mbps speed with 25 MHz clocks from the link partner, or it can run at the 200 Mbps with 50 MHz clocks from an external source.



**Note:** RvTMII (Reverse TMII) is not supported by the BCM53115S device.

## Reverse MII Interface (RvMII)

The media independent interface (MII) serves as a digital data interface between the BCM53115S and an external 10/100 Mbps management entity. Reverse MII notation reflects the MII port interfacing to a MAC-based external agent. The RvMII contains all the signals required to transmit and receive data at 100 Mbps and 10 Mbps for both full-duplex and half-duplex operation. See [Figure 11](#) for connection information.



**Figure 11: RvMII Interface Connection**

## GMII Interface

The Gigabit Media Independent Interface (GMII) serves as a digital data interface between the BCM53115S and an external gigabit management entity. Transmit and receive data is clocked on the rising edge of the clocks. The GMII transmits data synchronously using the TXD[7:0] and RXD[7:0] data signals.

## RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) serves as a digital data interface between the BCM53115S and an external gigabit management entity. Transmit and receive data is clocked on the rising and falling edge of the clocks. This reduces the number of data signals crossing the MAC interface without affecting the data transmission rate. The RGMII transmits data synchronously using the TXD[3:0] and RXD[3:0] data signals.

---

## WAN Interface

The BCM53115S provides one GMII/RGMII/SGMII/MII/RvMII interface (port 5) for WAN port or integrated gateways application. Port 5 is IMP port-capable; the BCM53115S provides dual-IMP (both IMP port and port 5) feature using the enabled bit [7:6] of [“Global Management Configuration Register \(Page 02h: Address 00h\)” on page 169](#).

Port 5 can be configured as IMP port in BCM53115S dual-IMP enabled only.

---

## Configuration Pins

Initial configuration of the BCM53115S takes place during power-on/reset by loading internal control values from hardware strap pins. The value of the pin is loaded when the reset sequence completes, and the pin transitions to normal operation. Pull-up or pull-down resistors can be added to these pins to control the device configuration. If the pins are left floating, the default value is determined based on the internal pull-up or pull-down configuration. See [“Signal Descriptions” on page 121](#) for more information.

---

## Programming Interfaces

The BCM53115S can be programmed using the SPI interface or the EEPROM interface. The interfaces share a common pin set that is configured using the CPU\_EEPROM\_SEL strap pin. The [“SPI-Compatible Programming Interface” on page 92](#) provides access for a general-purpose microcontroller, allowing read and write access to the internal BCM53115S register space. It is configured to be compatible with the Motorola Serial Peripheral Interface (SPI) protocol. Alternatively, the [“EEPROM Interface” on page 106](#) can be connected to an external EEPROM for writing register values upon power-up initialization.

The internal address space of the BCM53115S devices is broken into a number of pages. Each page groups a logical set of registers associated with a specific function. Each page provides a logical address space of 256 bytes, although, in general, only a small portion of the address space in each page is utilized.

An explanation follows for using the serial interface with an SPI-compatible CPU ([“SPI-Compatible Programming Interface” on page 92](#)) or an EEPROM ([“EEPROM Interface” on page 106](#)). Either mode can be selected with the strap pin, CPU\_EEPROM\_SEL. Either mode has access to the same register space.

## SPI-Compatible Programming Interface

One way to access the BCM53115S internal registers is to use the serial peripheral interconnect (SPI) compatible interface. This four-pin interface is designed to support a fully functional, bi-directional Motorola® serial peripheral interface (SPI) for register read/write accesses. The maximum speed of operation is 2 MHz. The SPI interface shares pins with the EEPROM interface. To select the SPI interface, pull up or float the CPU\_EEPROM\_SEL pin. (The internal pull-up resistor defaults SPI interface over EEPROM interface.)

The SPI is a four-pin interface consisting of the following:

- Device select ( $\overline{SS}$ : slave select, input to BCM53115S)
- Device clock (SCK: operates at speeds up to 2 MHz, input to BCM53115S)
- Data write line (MOSI: Master Out/Slave In, input to BCM53115S)
- Data read line (MISO: Master In/Slave Out, output from BCM53115S)



**Note:** All the RoboSwitch™ SPI interfaces are designed to operate in slave mode. Therefore, the SCK and SS signals are driven by the external master host device when accessing the BCM53115S registers. For more detailed descriptions reader may refer to the *Motorola SPI spec MC68HC08AS20-Rev. 4.0*.

### $\overline{SS}$ : Slave Select

The  $\overline{SS}$  signal is used to select a slave device and to indicate the beginning of transmission. The BCM53115S SPI interface operates in the clock phase one (CPHA = 1) transmission format. In this format, the SS signal is driven active low while the SCK signal is high, and remains low throughout the transmission including multiple-byte transfers. The minimum time requirement between SS operation is 200 ns.

### SCK: Serial Clock

The serial clock SCK maximum operating frequency is 2 MHz for the BCM53115S family of devices. The SCK is used to clock data into and out of the Slave ROBO device. The SCK signal is expected to remain high when the interface is idle. This is because the BCM53115S SPI design is based on CPOL = 1 (Clock Polarity = 1). This is not programmable on BCM53115S. The BCM53115S is designed so that data is driving by the falling edge and sampling by the rising edge of the SCK clock. This clock is not a free-running clock, it is generated only during a data transaction, and remains high when the clock is idle.

### MOSI: Master Output Slave Input

The MOSI signal is used by the master device to transmit the data to the slave device. The data is put on the bus and is expected to be clocked in by a rising edge of the SCK clock signal. This line is used to issue a command and to set the register page and address value of read/write operations.

### MISO: Master Input Slave Output

The MISO signal is used by the Slave device to output the data to the master device. The data is put on the bus and is expected to be clocked out by a rising edge of the SCK clock signal. This line is used to transmit the status and the content of the register of read operation.

A layer of protocol is added to the basic SPI definition to facilitate transfers from the BCM53115S. This protocol establishes the definition of the first 2 bytes issued by the master to the BCM53115S slave during an SPI transfer. The first byte issued from the SPI master in any transaction is defined as a command byte, which is always followed by a register address byte, and any additional bytes are data bytes.

The SPI mode supports two different access mechanisms, normal SPI and fast SPI, determined by the content of the command byte. [Figure 12](#) shows the normal SPI command byte, and [Figure 13](#) shows the Fast SPI command byte. These two mechanisms should not be mixed in an implementation; the CPU should always initiate transfers consistently with only one of the two mechanisms.

|   |   |   |          |                    |           |                    |                     |
|---|---|---|----------|--------------------|-----------|--------------------|---------------------|
| 0 | 1 | 1 | MODE = 0 | CHIP ID 2<br>(MSB) | CHIP ID 1 | CHIP ID 0<br>(LSB) | Read/Write<br>(0/1) |
|---|---|---|----------|--------------------|-----------|--------------------|---------------------|

**Figure 12: Normal SPI Command Byte**

|                      |             |                      |          |                    |           |                    |                     |
|----------------------|-------------|----------------------|----------|--------------------|-----------|--------------------|---------------------|
| Byte Offset<br>(MSB) | Byte Offset | Byte Offset<br>(LSB) | MODE = 1 | CHIP ID 2<br>(MSB) | CHIP ID 1 | CHIP ID 0<br>(LSB) | Read/Write<br>(0/1) |
|----------------------|-------------|----------------------|----------|--------------------|-----------|--------------------|---------------------|

**Figure 13: Fast SPI Command Byte**

The MODE bit (bit 4) of the command byte determines the meaning of bits 7:5. If bit 4 is a 0, it is a normal SPI command byte, and bits 7:5 should be defined as 011b. If bit 4 is a 1, bits 7:5 indicate a fast SPI command byte, and bits 7:5 indicate the byte offset into the register that the BCM53115S starts to read from (byte offsets are not supported for write operations).

In command bytes, bits[3:1] indicate the CHIP ID to be accessed. Because the BCM53115S operates as a single-chip system, the CHIP ID is 000.



**Note:** The SS# signal must also be active for any BCM53115S device to recognize that it is being accessed.

Bit 0 of the command byte is the R/W signal (0 = Read, 1 = Write) and determines the transmission direction of the data.

The byte following the command byte is an 8-bit register address. Initially, this sets the page address, followed by another command byte that contains the register base address in that page, which is used as the location to store the next byte of data received in the case of a write operation, or the next address from which to retrieve data in the case of a read operation. This base address increments as each byte of data is transmitted/received, allowing a contiguous block data from a register to be stored/read in a single transmission. When the fast SPI command byte mode is used, the actual start location of a read operation can be modified by the offset contained in bits 7:5 of the command byte. Reading/writing data from/to separate registers, even if those registers are contiguous in the current page, must be performed by supplying a new command byte and register address for each register, with the address as defined in the appropriate page register map.

Non-contiguous blocks are also stored/read through the use of multiple transmissions, which allow a new command byte and register base address to be specified. The SS signal must remain low for the entire read or write transaction, as shown in [Figure 14 on page 94](#) and [Figure 15 on page 94](#), with the transaction terminated by the deassertion of the SS line by the master.

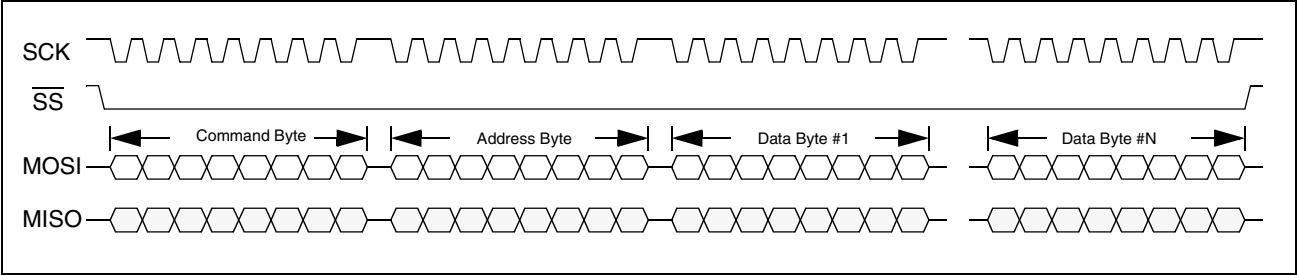


Figure 14: SPI Serial Interface Write Operation

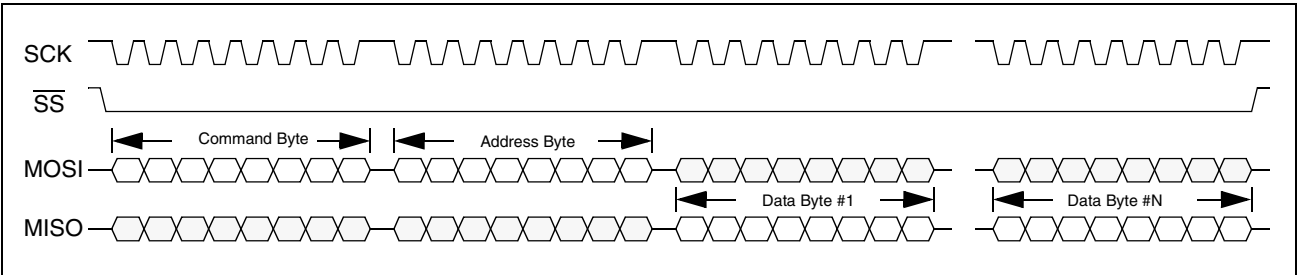


Figure 15: SPI Serial Interface Read Operation

The following diagram shows the typical connection block diagram for SPI interface with/without external PHY devices.

Without External PHY

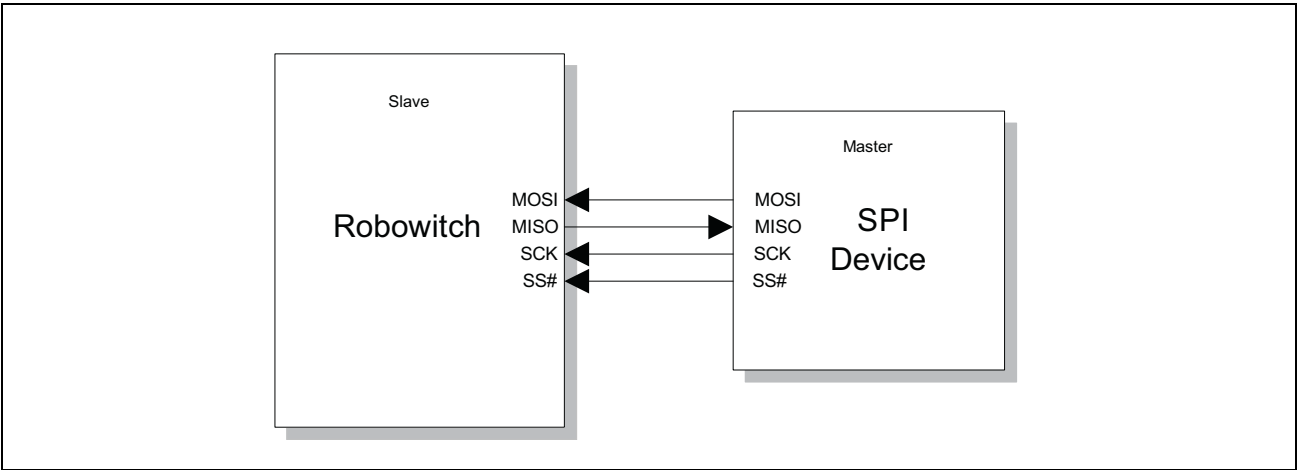


Figure 16: SPI Interface Without External PHY Device

## External PHY Registers

The BCM53115S also uses the MDIO/MDC interface for polling registers of an external PHY. In this case, the MDIO/MDC interface polls the external PHY registers pulling the data internal to the BCM53115S. Then, the external PHYs and retrieved from the register data using the SPI interface. The MDIO/MDC interface is not used as a method to access internal PHY registers. This must be done using the SPI interface.

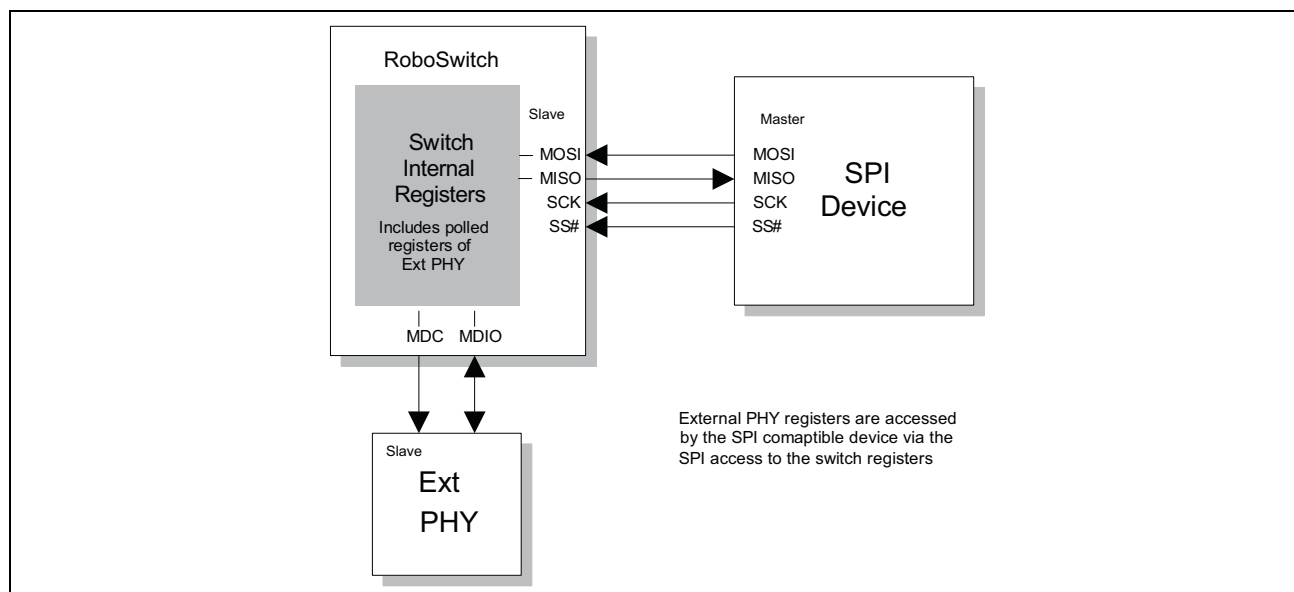


Figure 17: Accessing External PHY Registers

## Reading and Writing BCM53115S Registers Using SPI

BCM53115S internal register read and write operations are executed by issuing a command followed by multiple accesses of the SPI registers in the BCM53115S. There are three SPI interface registers in the BCM53115S that are used by the master device to access the internal switch registers. The SPI interface registers are:

- SPI Page register (page: global, address: FFh): used to specify the value of the specific register pages.
- SPI Data I/O register (page: global, address: F0h): used to write and read the specific register's content.
- SPI Status Register (page: global, address: FEh): used to check for an operation completion.
  - Bit 7 = SPIF, SPI read/write complete flag
  - Bit 6 = Reserved
  - Bit 5 = RACK, SPI read data ready acknowledgement
  - Bit 4:3 = Reserved
  - Bit 2 = MDIO\_Start, Start/Done MDC/MDIO operation
  - Bit 1 = Reserved
  - Bit 0 = Reserved

The BCM53115S SPI interface supports the following operating modes.

- Normal read mode

- Fast read mode
- Normal write mode



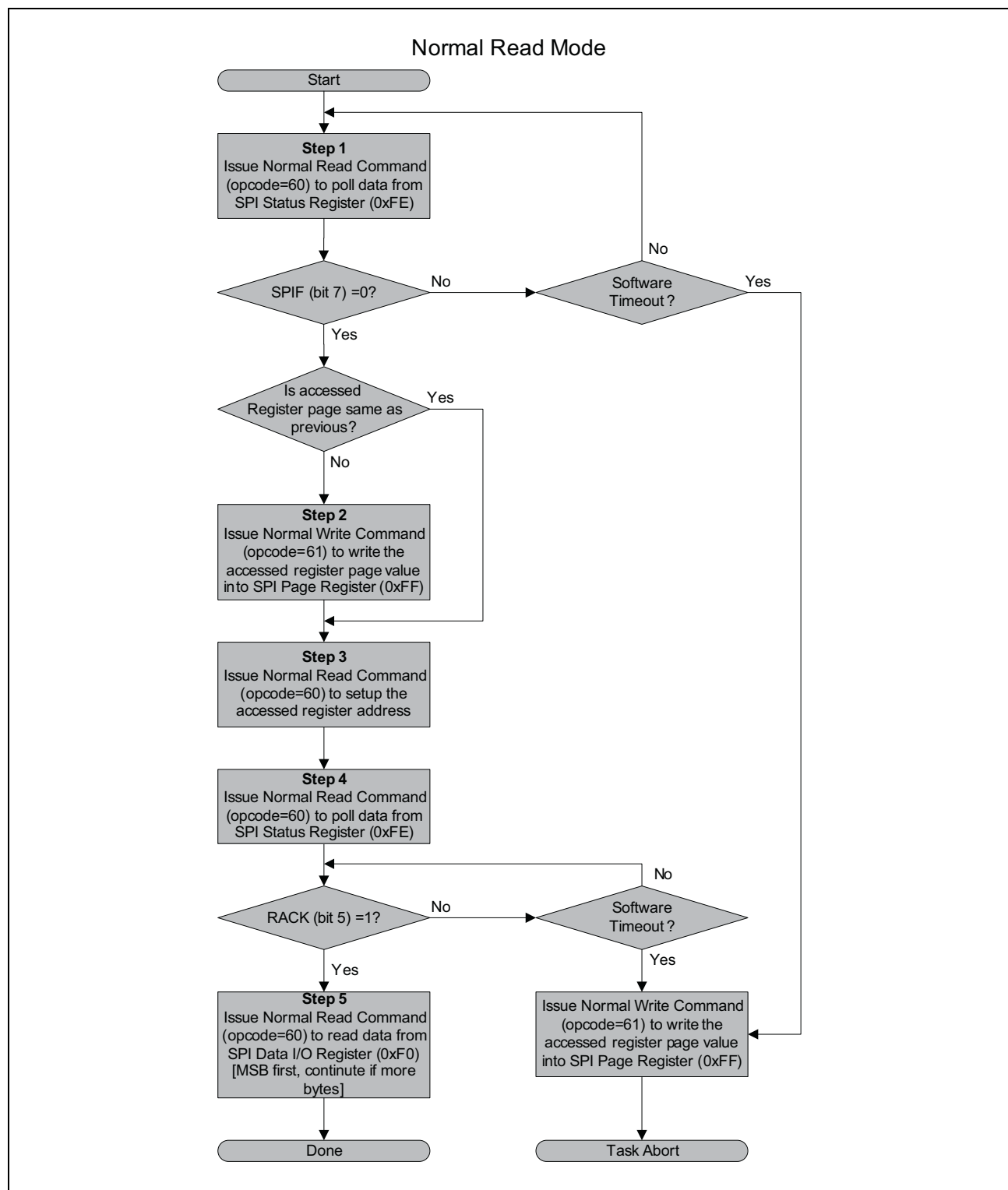
**Note:** The RoboSwitch family does not support fast-write mode.

The details of each modes are described in the following paragraphs.

## Normal Read Operation

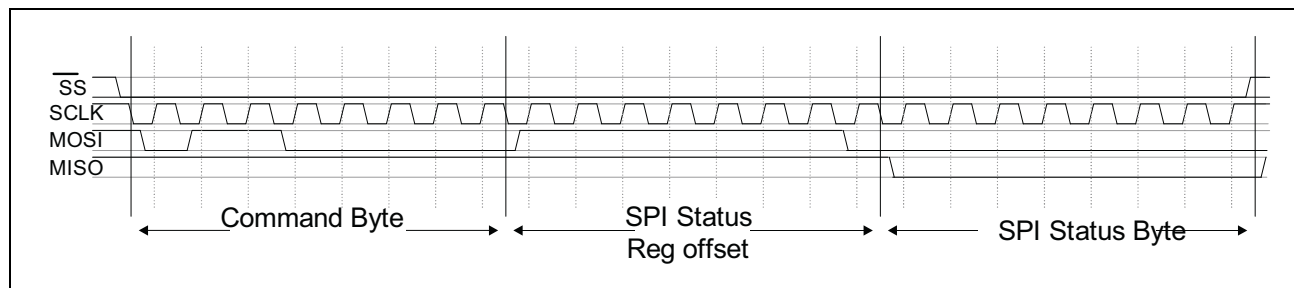
Normal Read operation consists of five transactions (five  $\overline{SS}$  operations):

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine the operation can start.
2. Issue a normal write command (opcode = 0x61) to write the register page value into the SPI Page register 0xFF.
3. Issue a normal read command (opcode = 0x60) to setup the required RoboSwitch register address.
4. Issue a normal read command (opcode = 0x60) to poll the RACK bit in the SPI status register(0xFE) to determine the completion of read (register content gets loaded in SPI Data I/O register).
5. Issue a normal read command (opcode = 0x60) to read the specific registers' content placed in the SPI Data I/O register (0xF0).

**Figure 18: Normal Read Operation**

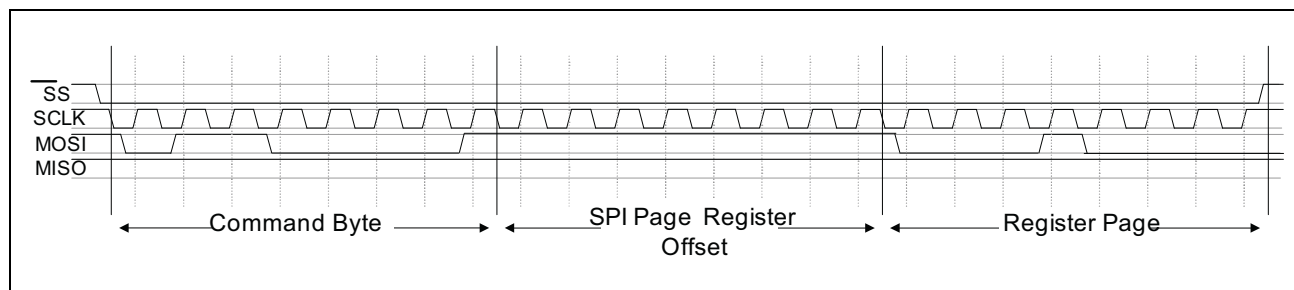
**Example:** Read from 1000BASE-T Control register (Page 10h, Offset 12h).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a normal read command byte: 0 1 1 0 0 0 0 (opcode = 0x60)
  - Clock in the SPI Status register address (0xFE)
  - Clock out the SPI Status register value: 0 0 0 0 0 0 0 (SPIF bit 7=0)
  - Deassert  $\overline{SS}$  while SCK is high idle state



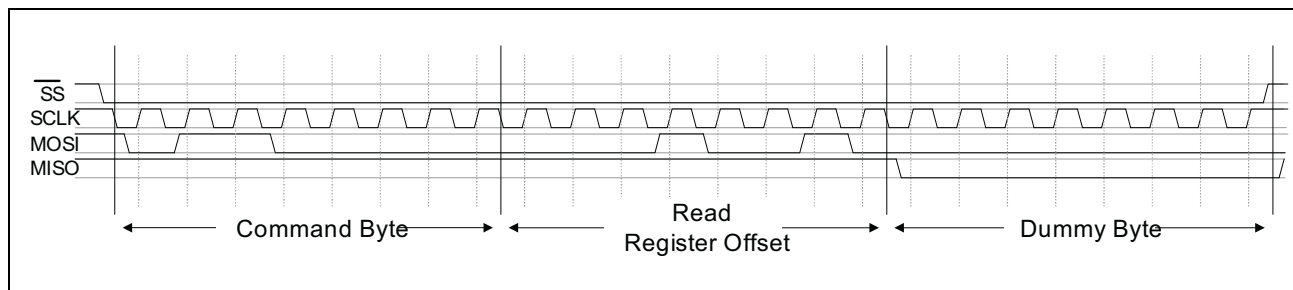
**Figure 19: Normal Read Mode to Check the SPIF Bit of SPI Status Register**

2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 into the SPI Page register (0xFF). This step is required only if previous the read/write was not to/from page 10h.
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a normal write command byte: 0 1 1 0 0 0 0 1 (opcode = 0x61)
  - Clock in offset of page register (0xFF)
  - Clock in the accessed register page value: 0 0 0 1 0 0 0 0 (page register: 0x10)
  - Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 20: Normal Read Mode to Setup the Accessed Register Page Value**

3. Issue a normal read command (opcode = 0x60) and write the accessed register address value 0x12, and clock out 8 bits to complete the read cycle, but discard result (this is where the state machine triggers a internal data transfer from Address 0x12 to the SPI Data I/O register)
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
  - Clock in the address of accessed register address value (0x12)
  - Clock out eight clocks for the dummy read, and discard results on MISO
  - Deassert  $\overline{SS}$  while SCK is high idle state

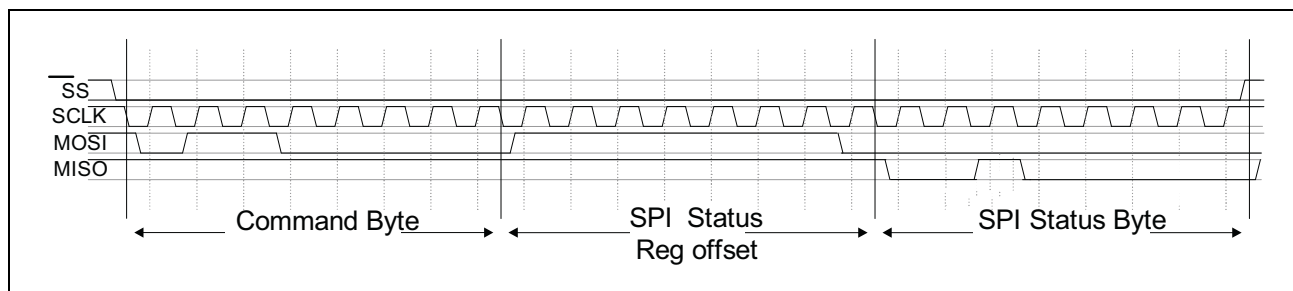


**Figure 21: Normal Read Mode to Setup the Accessed Register Address Value (Dummy Read)**



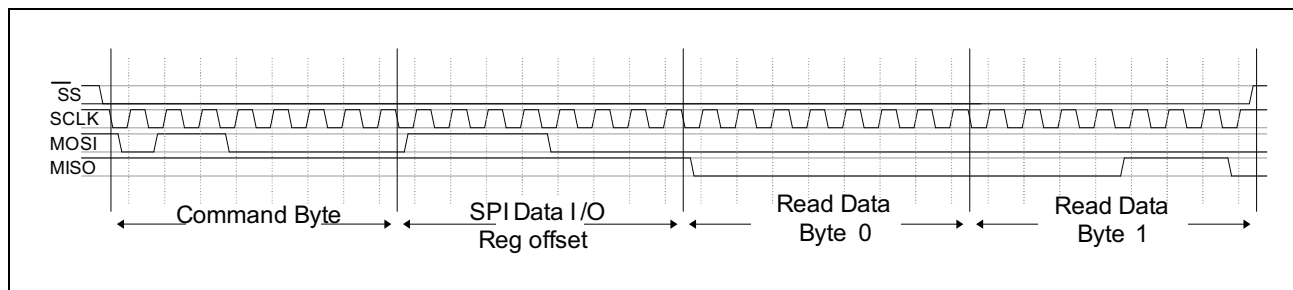
**Note:** This dummy read is always eight clock cycles, whether or not it is an 8-bit register.

4. Issue a normal read command (opcode = 0x60) to read the SPI Status to check the RACK bit for completion of the register content transfer to the SPI Data I/O register.(this step may be repeated until the proper bit set is read.)
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
  - Clock in offset for SPI Status register (0xFE): 1 1 1 1 1 1 1 0
  - Clock out the content of SPI Status bits
  - Repeat the polling until the content of SPI Status register value: 0 0 1 0 0 0 0 0 (RACK bit 5= 1)
  - Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 22: Normal Read Mode to Check the SPI Status for Completion of Read**

5. Issue a normal read command (opcode = 0x60) to read the data from the SPI Data I/O register:
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
  - Clock in offset of SPI Data I/O register (0xF0)
  - Clock out first data byte on MISO line: 0 0 0 0 0 0 0 0 (byte 0: bit 7 to bit 0: MSB to LSB)
  - Clock out next byte (in this case, last) on MISO line: 0 0 0 0 1 1 1 0 (byte 1: bit 15 to bit 8)
  - [Continue if more bytes]
  - Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 23: Normal Read Mode to Obtain the Register Content**

## Fast Read Operation

Fast Read operation consists of 3 transactions (three  $\overline{SS}$  operations)

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status Register (0xFE) to determine the operation can start.
2. Issue a fast read command (opcode = 0x10) to setup the accessed Register Page value into the Page register (0xFF).
3. Issue a fast read command (opcode = 0x10) to setup the accessed register address value, to trigger an actual read, and retrieve the accessed register content till the completion

Fast Read mode process is different from Normal Read mode, once the switch receives a fast read command followed by the register page and address information, the status and the data (register content) will be put on the MISO line without going through the SPI Status register or SPI Data I/O register. Once RACK bit of the bytes following the fast read command with Address information is recognized the register content will be put on MISO line immediately following the byte with RACK bit set. The Fast Read process is described in the following paragraphs with a flowchart followed by a step by step description.

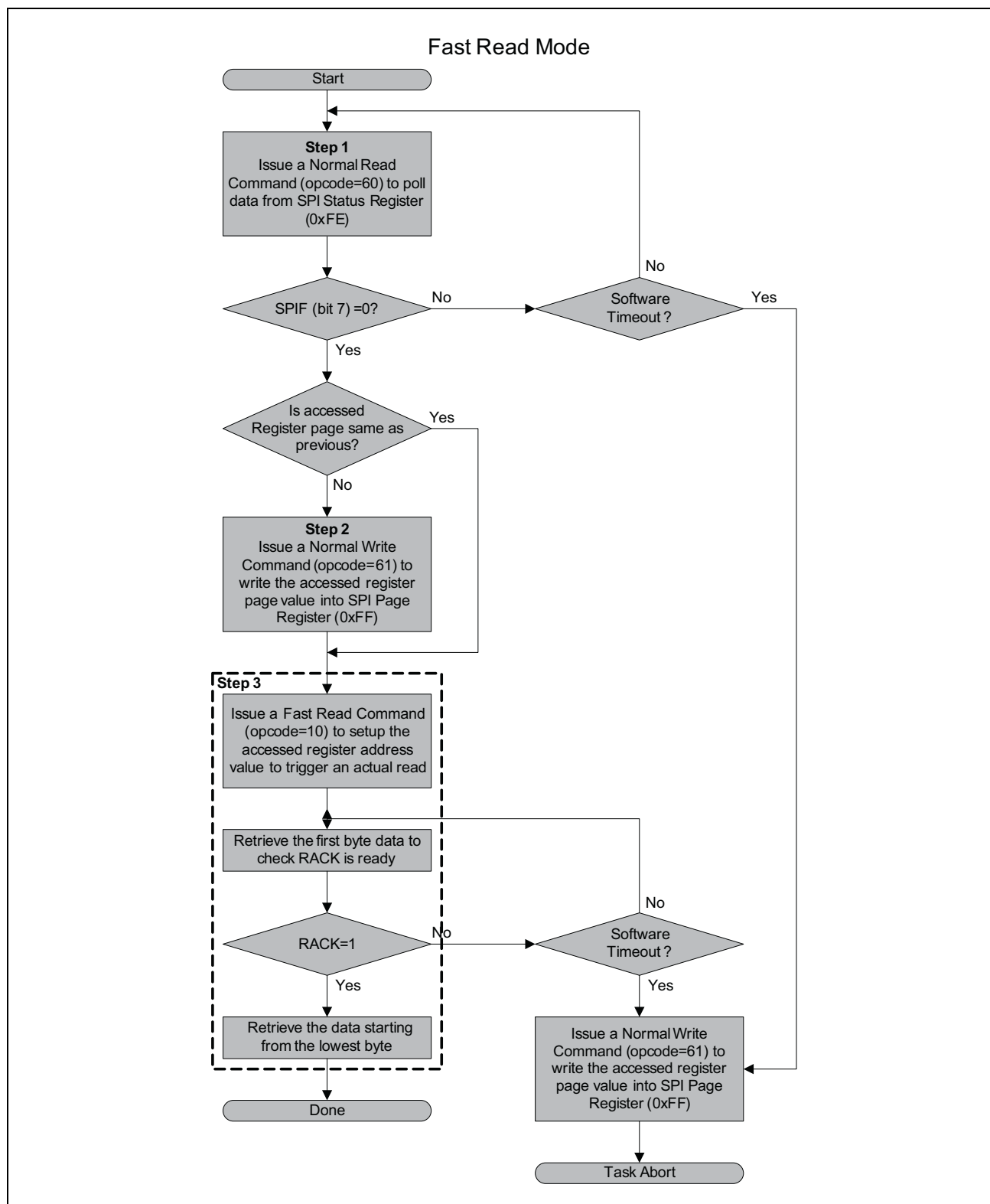
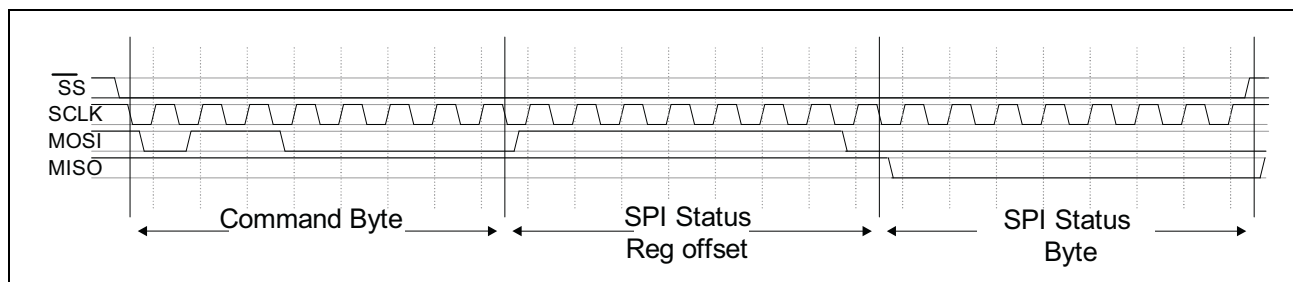


Figure 24: Fast Read Operation

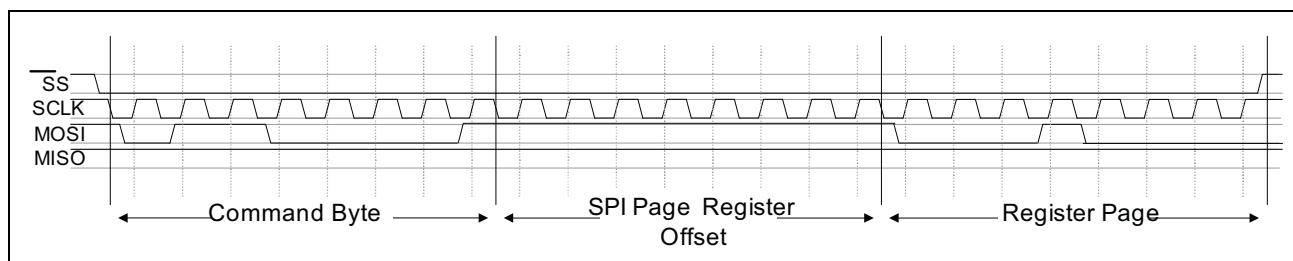
**Example:** Read from 1000BASE-T Control register (Page 10h, Offset 12h).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
  - Clock in the SPI Status register address (0xFE)
  - Clock in the accessed register page value: 0 0 0 0 0 0 0 0 (SPIF bit 7=0)
  - Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 25: Normal Read Mode to Check the SPIF Bit of SPI Status Register**

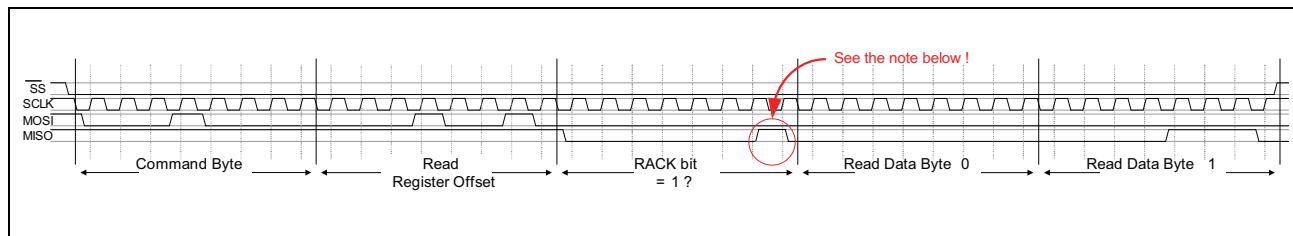
2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 in to the SPI Page register (0xFF). This step is required only if previous read/write was not to/from page 10h.
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a fast read command byte: 0 11 0 0 0 0 0 1 (opcode = 0x61)
  - Clock in offset of page register (0xFF)
  - Clock in the accessed register page value: 0 0 0 1 0 0 0 0 (page register: 0x10)
  - Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 26: Fast Read Mode to Setup New Page Value**

3. Issue a fast read command (opcode = 0x10), followed by the address of the accessed register (0x12), check for a read completion by checking the RACK bit in the SPI Status register, and finally clock out the read data.
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a fast read command byte: 0 0 0 1 0 0 0 0 (opcode = 0x10)
  - Clock in the address of accessed register (0x12)
  - Clock out bytes until bit 0 or bit 1 = 1: 0 0 0 0 0 0 0 1 (RACK bit 0 = 1)
  - Clock out first data byte: 0 0 0 0 0 0 0 0 (byte 0: bit 7 to bit 0)

- Clock out next data (in this case, last) byte: 0 0 0 0 1 1 1 0 (Byte 1: Bit 15 to Bit 8)
- [Continue if more bytes]
- Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 27: Fast Read to Read the Register**



**Note:** There is an errata on the RACK output timing in Fast Read mode. The RACK (bit 0) must be sampled prior to toggling the clock to shift out the bit 0.

## Normal Write Operation

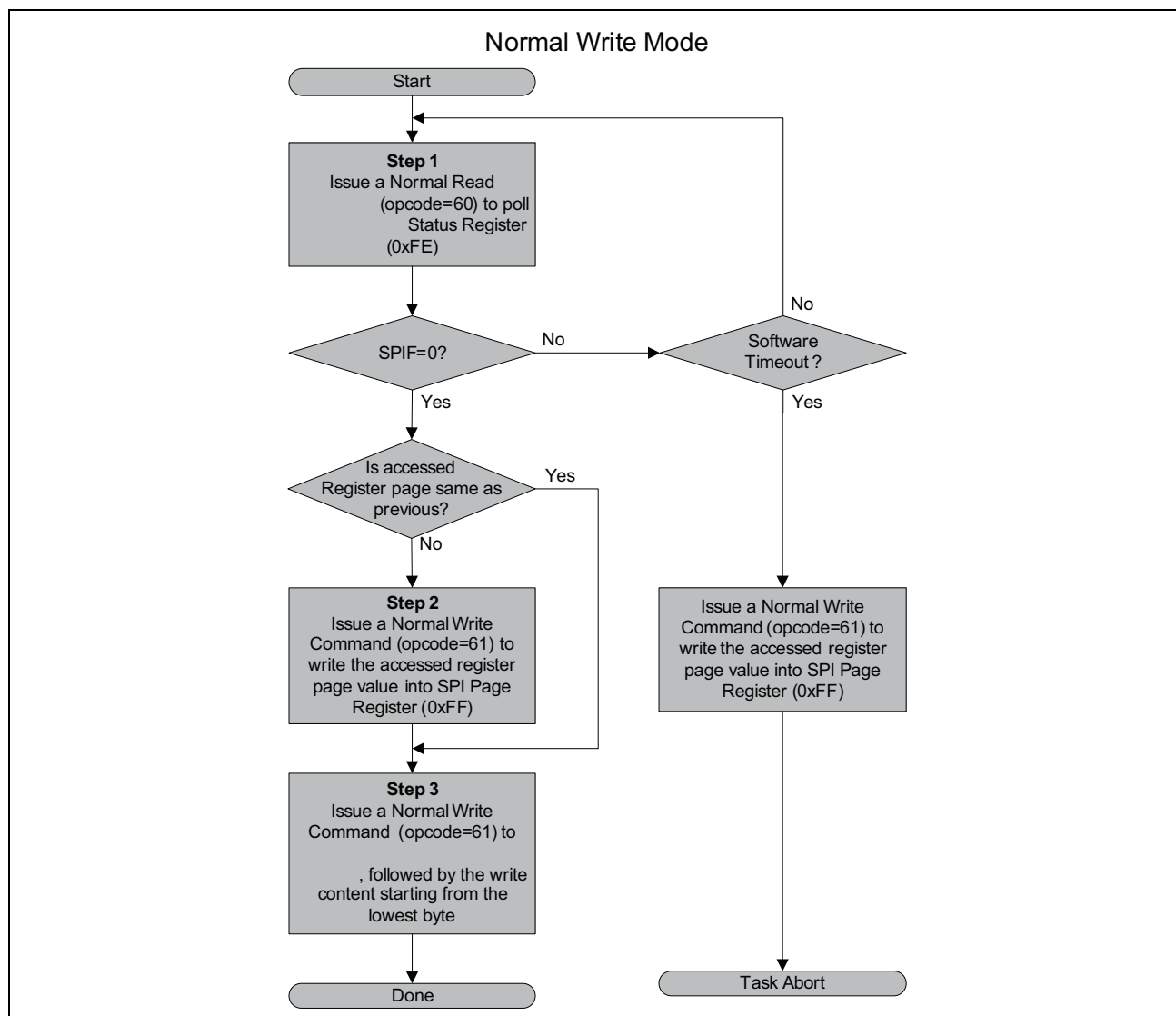
Normal write operation consists of 3 transactions (three  $\overline{SS}$  operations)

1. Issue a normal read command (opcode = 0x60) to poll the SPIF bit in the SPI Status register (0xFE) to determine the operation can start.
2. Issue a normal write command (opcode = 0x61) to setup the accessed register page value into the page register (0xFF).
3. Issue a normal write command (opcode = 0x61) to set up the accessed register address value, followed by the write content starting from a lower byte.

The normal write mode process is described in the following paragraphs with a flowchart followed by a step by step description.



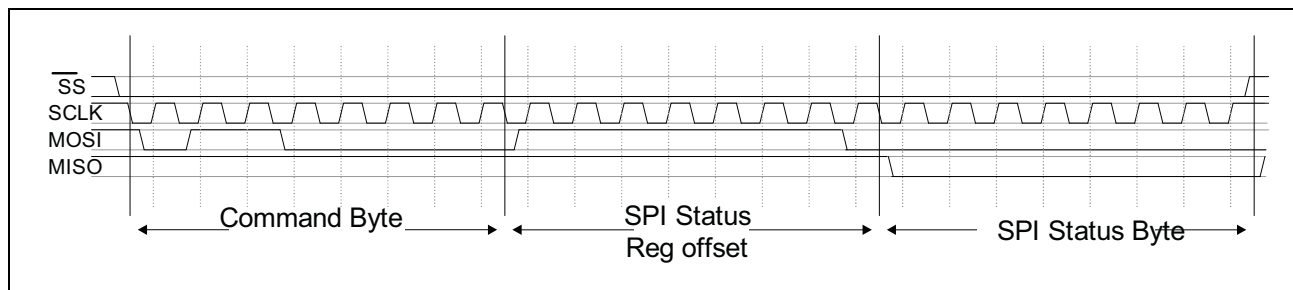
**Note:** The RoboSwitch does not support Fast Write Mode.



**Figure 28: Normal Write Operation**

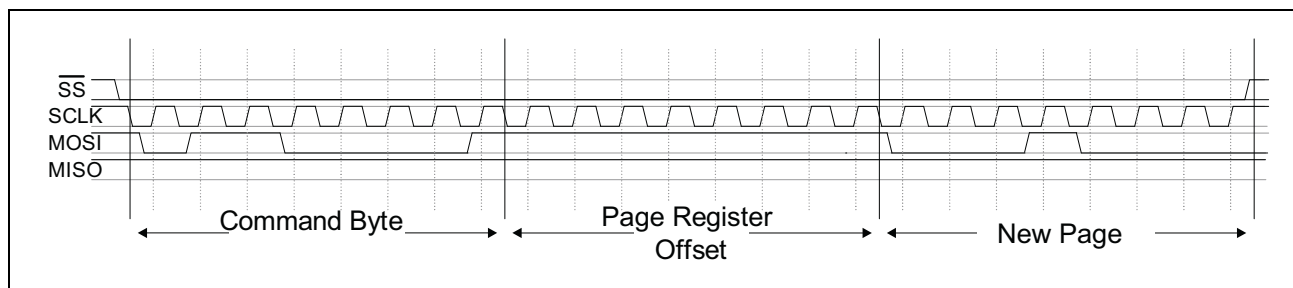
**Example:** 0x1600h is written to 1000BASE-T Control register (Page 0x10, Offset 0x12).

1. Issue a normal read command (opcode = 0x60) to check the SPIF bit in the SPI Status register (0xFE).
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a normal read command byte: 0 1 1 0 0 0 0 0 (opcode = 0x60)
  - Clock in the SPI Status register address (0xFE)
  - Clock in the accessed register page value: 0 0 0 0 0 0 0 0 (SPIF bit 7 = 0)
  - Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 29: Normal Read Mode to Check the SPIF Bit of SPI Status Register**

2. Issue a normal write command (opcode = 0x61) and write the accessed register page value of 0x10 into the SPI Page register (0xFF). This step is required only if previous the read/write was not from/to page 0x10.
  - Assert  $\overline{SS}$  while SCK is high idle state
  - Clock in a normal write command byte: 0 1 1 0 0 0 1 (opcode = 0x61)
  - Clock in offset of page register (0xFF)
  - Clock in 1 byte of the accessed register page value (page register 0x10)
  - Deassert  $\overline{SS}$  while SCK is high idle state



**Figure 30: Normal Write to Setup the Register Page Value**

3. Issue a normal write command (opcode = 0x61) and write the address of the accessed register followed by the write content starting from a lower byte.
  - Assert  $\overline{SS}$  while SCK is high idle state
    - Clock in a normal write command byte: 0 1 1 0 0 0 1 (opcode = 0x61)
    - Clock in offset of address of accessed register (0x12)
    - Clock in lower data byte first: 0 0 0 0 0 0 0 0 (byte 0: bit 7 to bit 0)
    - Clock in upper data byte next: 0 0 0 1 0 1 1 0 (byte 1: bit 15 to bit 8)
    - [Continue if more bytes]
  - Deassert  $\overline{SS}$  while SCK is high idle state

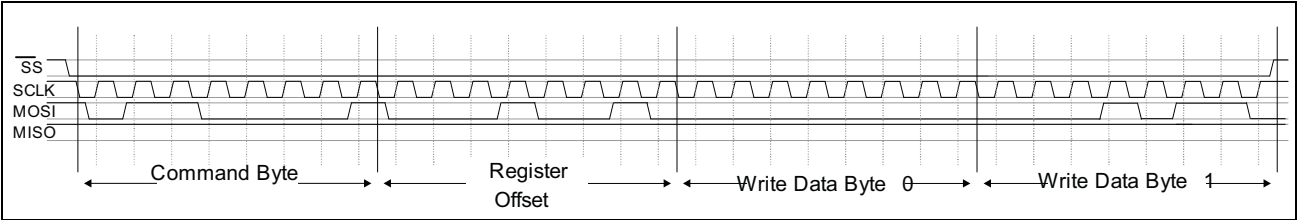


Figure 31: Normal Write to Write the Register Address Followed by Written Data

EEPROM Interface

The BCM53115S can be connected using the serial interface to a low-cost external serial EEPROM, enabling it to download register-programming instructions during power-on initialization. For each programming instruction fetched from the EEPROM, the instruction executes immediately and affects the register file.

During the chip-initialization phase, the data is sequentially read-in from the EEPROM after the internal memory has been cleared. The first data read-in is the HEADER and it matches a predefined magic code. In the case where the HEADER data does not match the instruction fetch, the process stops, and the EEPROM controller treats it as if no EEPROM exists. If the magic code matches, the fetch instruction process continues until it reaches the instruction length defined in the HEADER.

Due to the different access cycles of different capacity EEPROMs, the strap pins EEPROM\_TYPE[1:0] are used to support the various EEPROM devices according to Table 26.

Table 26: EEPROM\_TYPE[1:0] Settings

| EEPROM_TYPE[1:0] | EEPROM |
|------------------|--------|
| 00               | 93C46  |
| 01               | 93C56  |
| 10               | 93C66  |
| 11               | 93C86  |

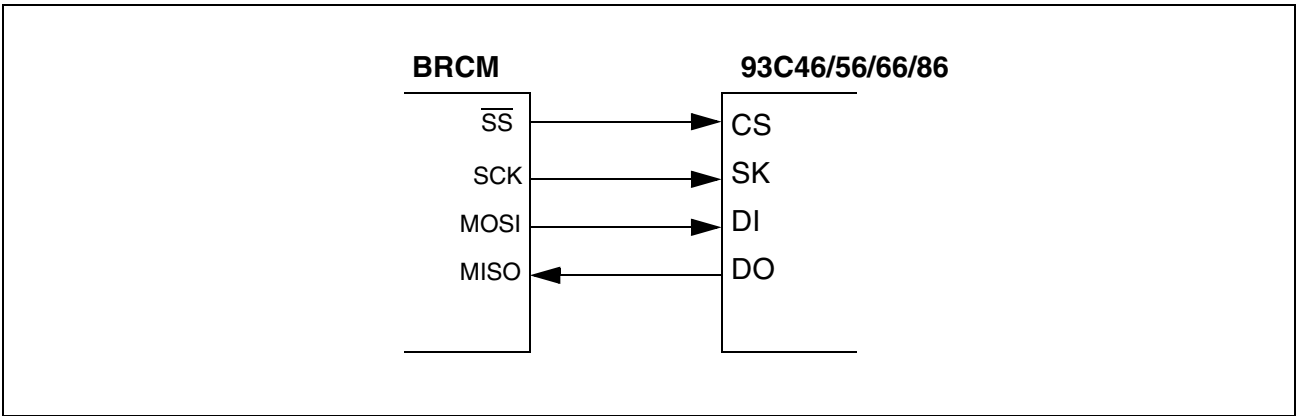


Figure 32: Serial EEPROM Connection

EEPROM Format

The EEPROM should be configured to x16 word format. The header contains key and length information as shown in [Table 27 on page 107](#). The actual data stored in the EEPROM is byte-swapped as shown in [Table 28 on page 107](#).

- Upper 5 bits are magic code 15h, which indicates that valid data follows.
- Bit 10 is for speed indication. A 0 means normal speed. A 1 indicates speedup. The default is 0.
- Lower 10 bits indicate the total length of all entries. For example:
  - 93C46 up to 64 words
  - 93C56 up to 128 words
  - 93C66 up to 256 words
  - 93C86 up to 1024 words

Table 27: EEPROM Header Format

| Bits [15:11]    | Bit 10 | Bits [9:0]                                                                             |
|-----------------|--------|----------------------------------------------------------------------------------------|
| Magic code, 15h | Speed  | Total entry number<br>93C46 = 0–63<br>93C56 = 0–127<br>93C66 = 0–255<br>93C86 = 0–1023 |

Table 28: EEPROM Contents

| Bits [7:0]         | Bits [15:11]    | Bit 10 | Bits [9:8]         |
|--------------------|-----------------|--------|--------------------|
| Total entry number | Magic code, 15h | Speed  | Total entry number |

[Figure 33](#) shows an EEPROM programming example.

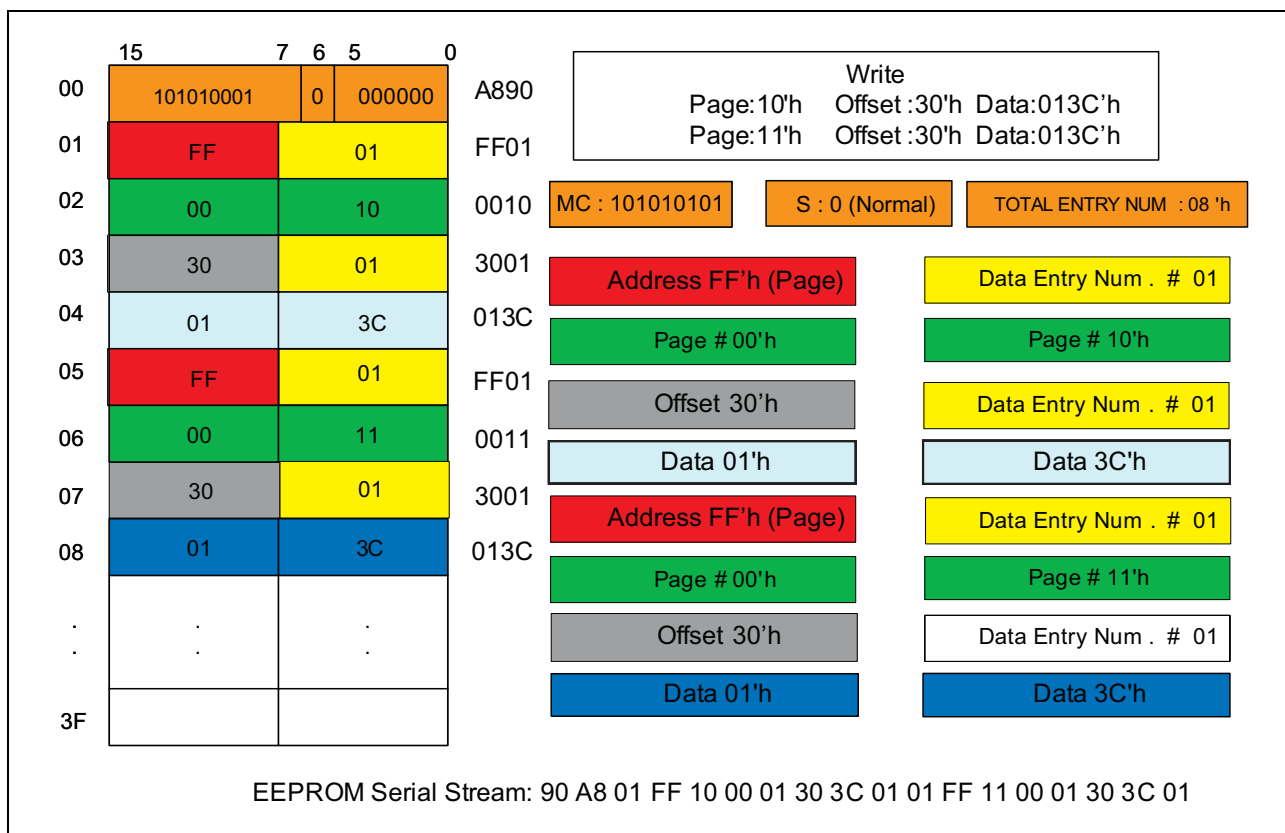


Figure 33: EEPROM Programming Example

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## MDC/MDIO Interface

The BCM53115S offers an MDC/MDIO interface for accessing the switch registers as well as the PHY registers. An external management entity can access the switch registers through this interface when the SPI interface is not used. (that is, when the SPI clock is in idle mode.) The switch registers are accessed through the Pseudo PHY interface, and the PHY registers are accessed directly by using PHY addresses.

An external PHY can be connected to the GMII interface of the IMP port and port 5. Through the SPI interface, by accessing the Page 88h and Page 85h, the external PHY MII registers can be accessed. The actual PHY address can be assigned through the [“MDIO IMP PORT Address Register \(Page 00h: Address 78h\)” on page 161](#) and [“MDIO WAN Port Address Register \(Page 00h: Address 75h\)” on page 161](#).



**Note:** The PHY registers are not accessible through the Pseudo PHY operation.

## MDC/MDIO Interface Register Programming

The BCM53115S are designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification. The MDC pin of the BCM53115S sources a 2.5 MHz clock. Serial bidirectional data transmitted using the MDIO pin is synchronized with the MDC clock. Each MII read or write instruction is initiated by the BCM53115S and contains the following:

- **Preamble (PRE).** To signal the beginning of an MII instruction after reset, at least 32 consecutive 1-bits must be written to the MDIO pin. A preamble of 32 1-bits is required only for the first read or write following reset. A preamble of fewer than 32 1-bits causes the remainder of the instruction to be ignored.
- **Start of Frame (ST).** A 01 pattern indicates that the start of the instruction follows.
- **Operation Code (OP).** A read instruction is indicated by 10, while a write instruction is indicated by 01.
- **PHY Address (PHYAD).** A 5-bit PHY address follows, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips.
- **Register Address (REGAD).** A 5-bit register address follows, with the MSB transmitted first.
- **Turnaround (TA).** The next bit times are used to avoid contention on the MDIO pin when a read operation is performed. When a write operation is being performed, 10 must be sent by the BCM53115S chip during these two bit times. When a read operation is being performed, the MDIO pin of the BCM53115S must be put in a high-impedance state during these bit times. The external PHY drives the MDIO pin to 0 during the second bit time.
- **Data.** The last 16 bits of the Instruction are the actual data bits. During a write operation, these bits are written to the MDIO pin with the most significant bit (MSB) transmitted first by the BCM53115S. During a read operation, the data bits are driven by the external PHY with the MSB transmitted first.

Pseudo-PHY

The MDC/MDIO can be used by an external management entity to read/write register values internal to the BCM53115S. This mode offers an alternative programming interface to the chip. The BCM53115S operate in slave mode with a PHY address of 30d. The following figures show the register setup flow chart for accessing the registers using the MDC/MDIO interface.

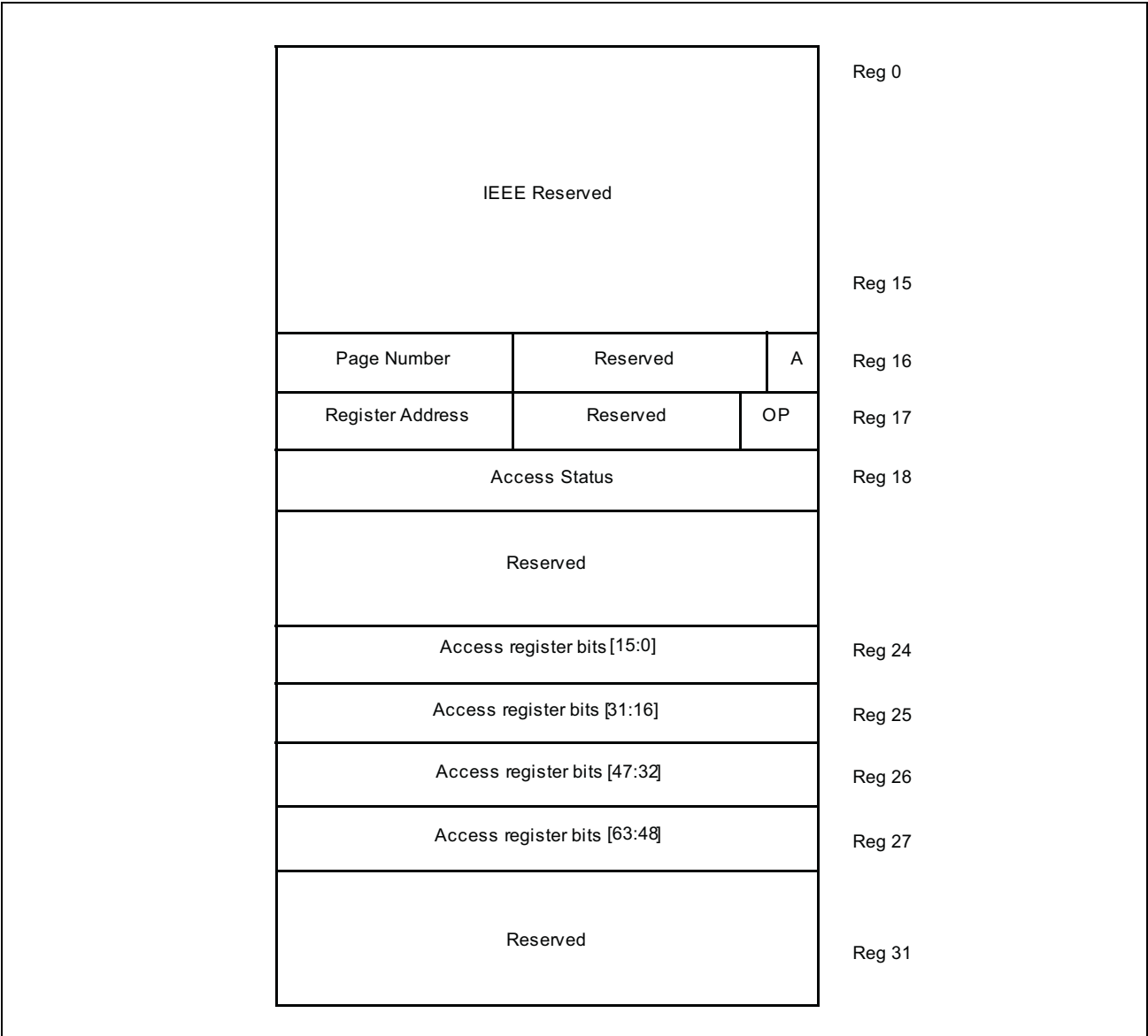
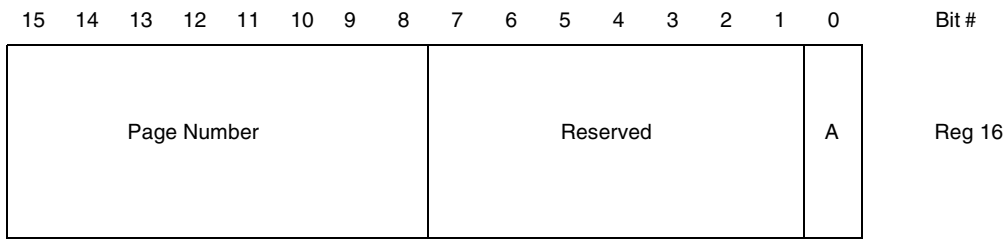


Figure 34: Pseudo-PHY MII Register Definitions



|                  |    |    |    |    |    |   |   |          |   |   |   |   |   |    |   |        |
|------------------|----|----|----|----|----|---|---|----------|---|---|---|---|---|----|---|--------|
| 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1  | 0 | Bit #  |
| Register Address |    |    |    |    |    |   |   | Reserved |   |   |   |   |   | OP |   | Reg 17 |

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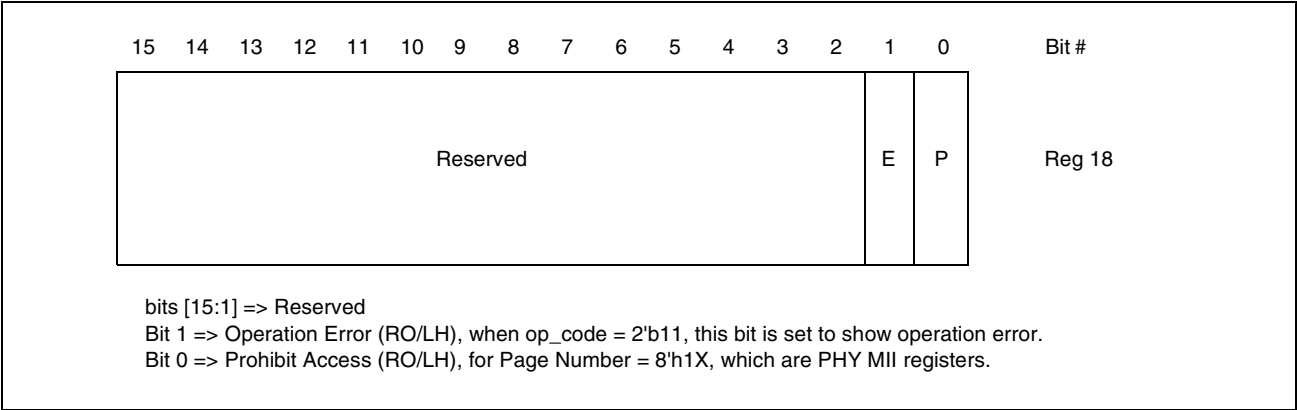


Figure 37: Pseudo-PHY MII Register 18: Register Access Status Bit Definition

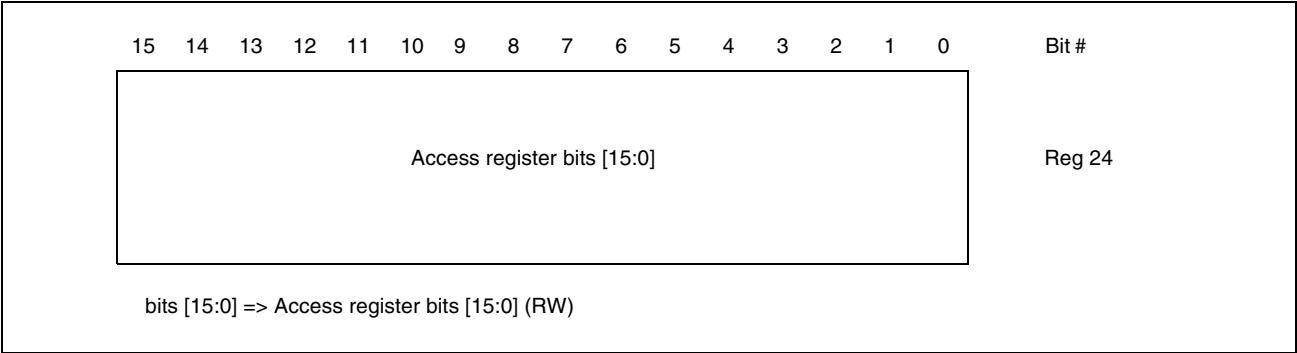


Figure 38: Pseudo-PHY MII Register 24: Access Register Bit Definition

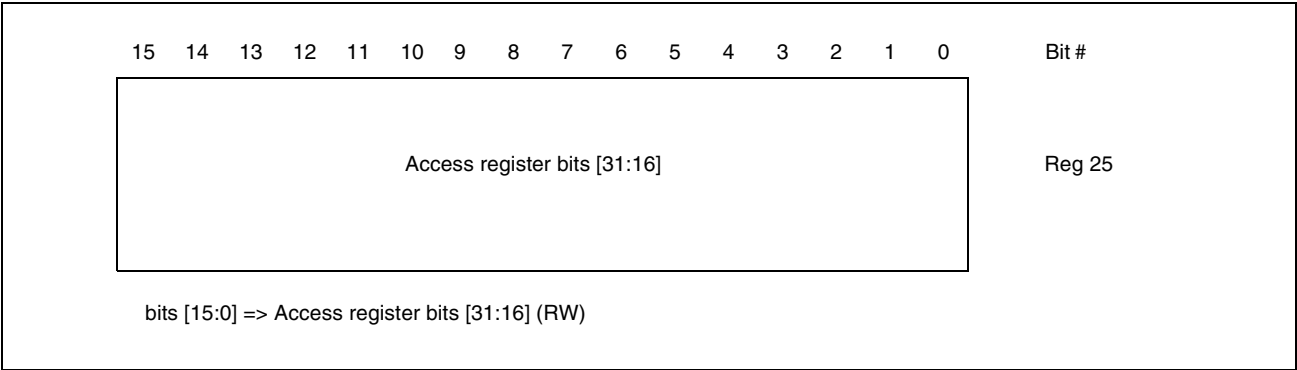


Figure 39: Pseudo-PHY MII Register 25: Access Register Bit Definition

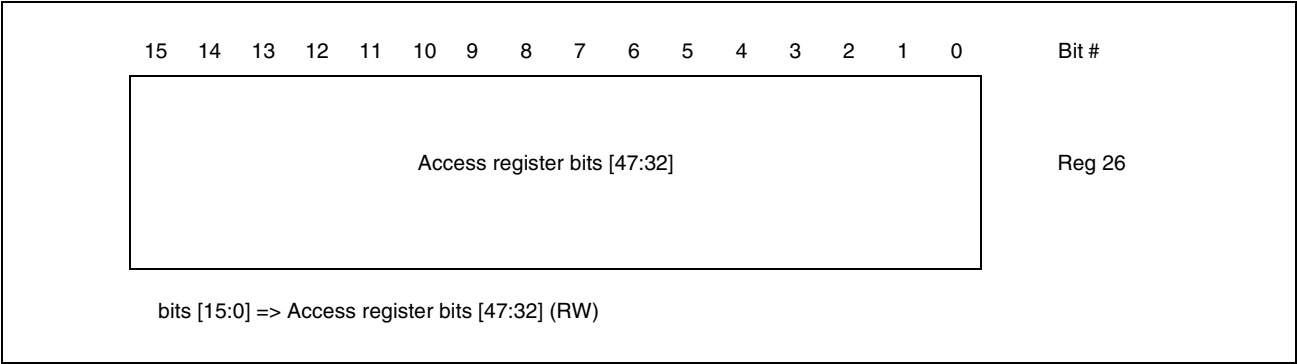


Figure 40: Pseudo-PHY MII Register 26: Access Register Bit Definition

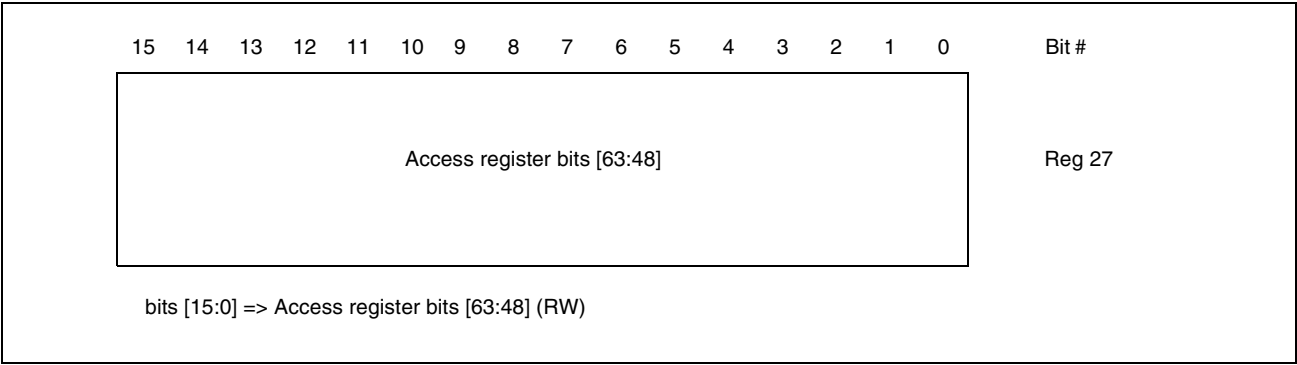


Figure 41: Pseudo-PHY MII Register 27: Access Register Bit Definition

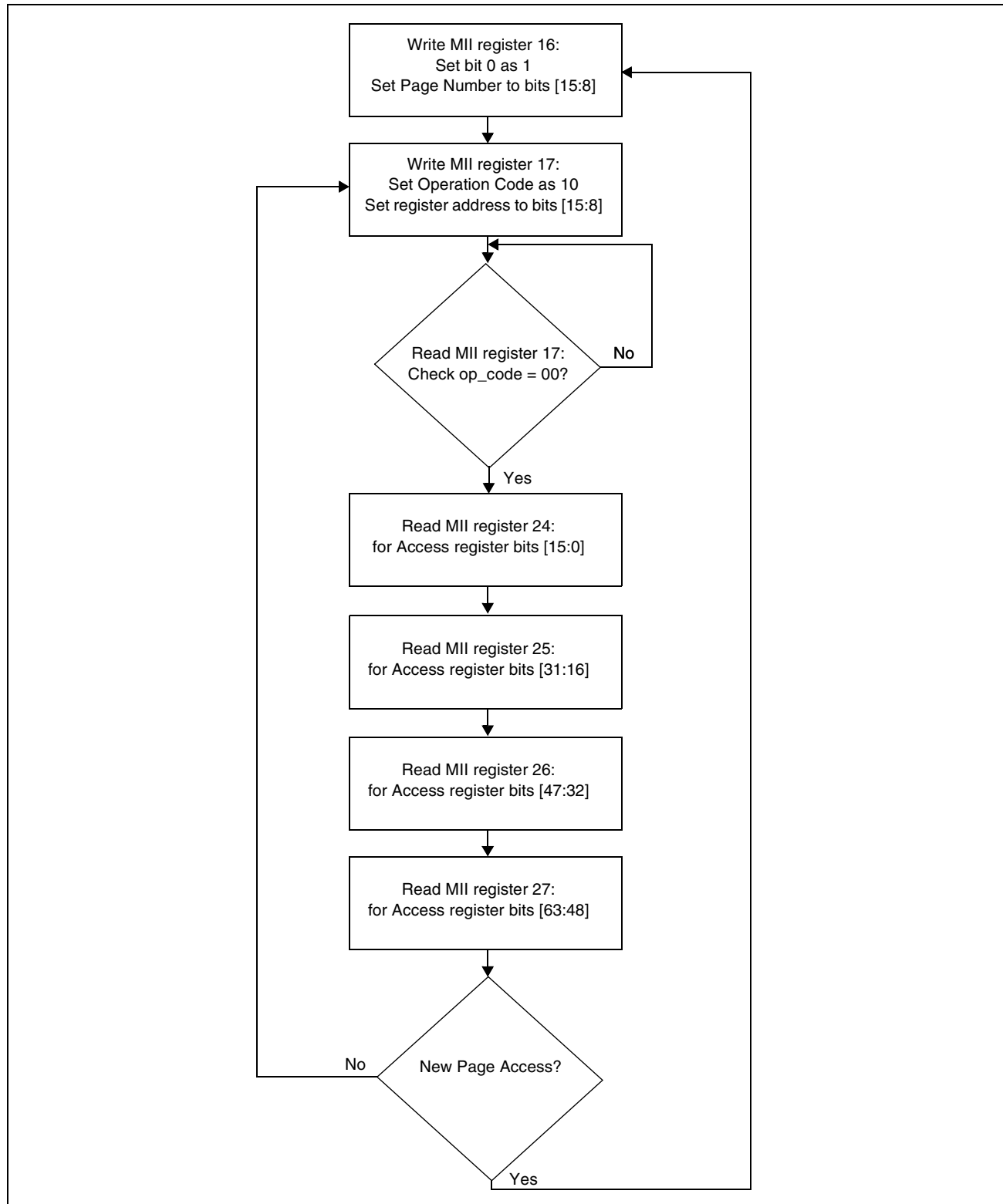


Figure 42: Read Access to the Register Set Using the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

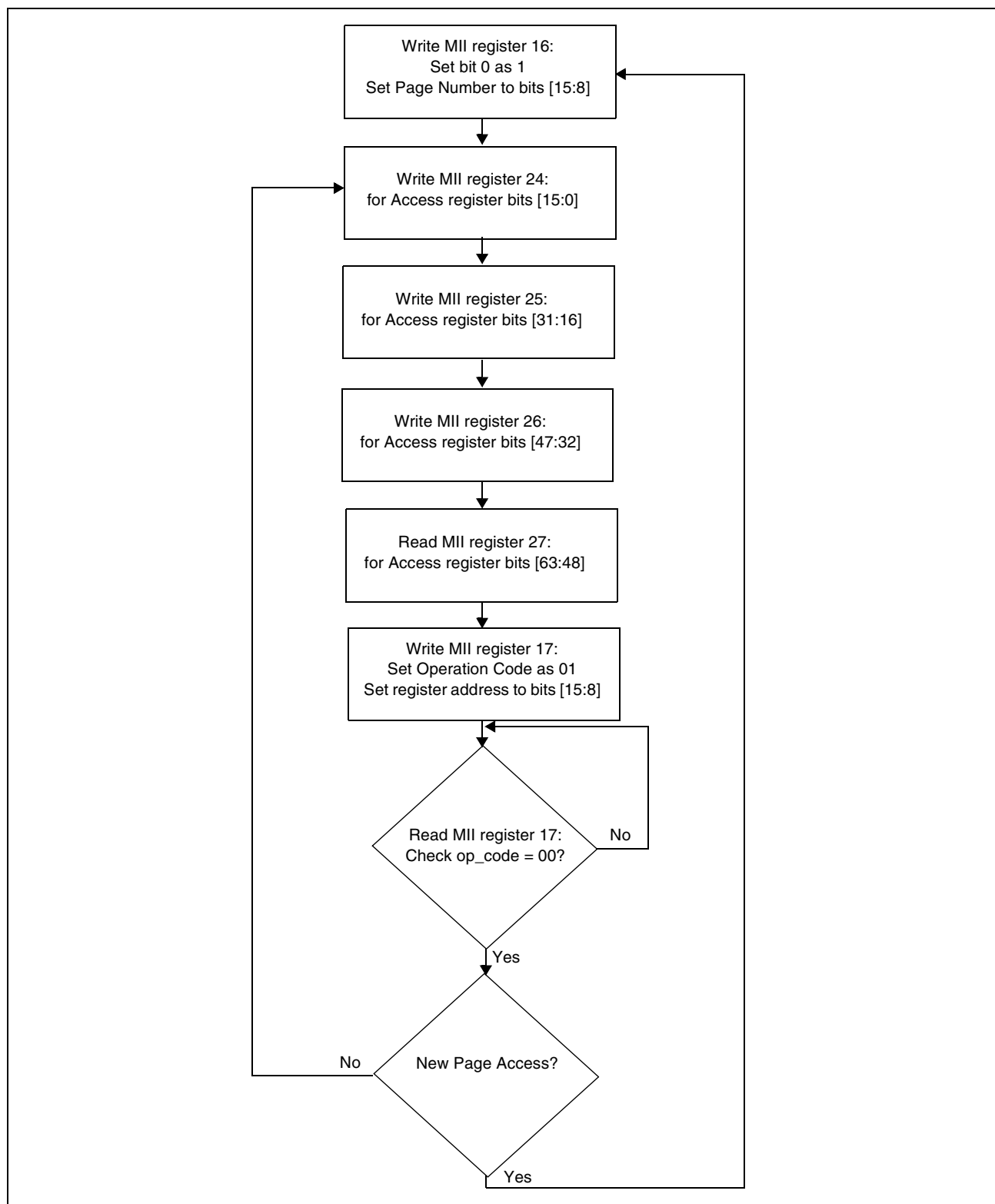


Figure 43: Write Access to the Register Set Using the Pseudo-PHY (PHYAD = 11110) MDC/MDIO Path

Table 29 summarizes the complete management frame format.

**Table 29: MII Management Frame Format**

| <i>Operation</i> | <i>PRE</i> | <i>ST</i> | <i>OP</i> | <i>PHYAD</i> | <i>REGAD</i> | <i>TA</i> | <i>Data</i> | <i>Direction</i> |
|------------------|------------|-----------|-----------|--------------|--------------|-----------|-------------|------------------|
| Read             | 1 ... 1    | 01        | 10        | AAAAA        | RRRRR        | ZZ        | Z ... Z     | Driven by master |
|                  |            |           |           |              |              | Z0        | D ... D     | Driven by slave  |
| Write            | 1 ... 1    | 01        | 01        | AAAAA        | RRRRR        | 10        | D ... D     | Driven to master |

See “MDC/MDIO Interface” on page 109 for more information regarding the timing requirements.

## LED Interfaces

The BCM53115S provides flexible visibility per-port status of various functions. The LED Interface offers an option to display different functions for each port given the number of LED bits available. The BCM53115S provides a total of 20 LED pins. In a 5-port switch application, these are dedicated as four LED pins per port as shown in Table 30. If one or more ports are not used in an application and are disabled using the LED Enable Map register (page 00h: address 16h), and no more than four LED pins are to be used per port, the locations of the pins for the enabled ports are the same as if all five ports were used, with four pins reserved per port, regardless of whether the port is enabled.

For example, if Port4, Port3, and Port2 LED displays are disabled (value of register page 00h, address 16h = 0003), Port0 and Port1 LED display are still from LED pins LED16–19 (Port0), LED12–15 (Port1), just as if all five ports were used. If Port1 and Port0 LED displays are disabled (value of register page 00h, address 16h = 001C), Port2, Port3, and Port4 are still from LED pins LED8–11 (Port2), LED4–7 (Port3), and LED0–3 (Port4), also just as if all five ports were used.

To set up the LED interface, configure strap pins LED\_MODE[1:0] or select the desired display the functions in the LED Function 0 Control register/LED Function 1 Control register. The per-port LED display is fixed with four functions.

- To configure the strap pins, set the predefined functions to be displayed by setting the strap pins LED\_MODE[1:0]. The predefined functions are described in Table 32: “Signal Type Definitions,” on page 121. Per-port LED display is four fixed functions and occupies four LED pins.
- To configure LED display function in the two LED Function Control registers, assign each port to one of the “LED Function 0 Control Register (Page 00h: Address 10h)” on page 152 and “LED Function 1 Control Register (Page 00h: Address 12h)” on page 153 by enabling the bits in the “LED Function Map Register (Page 00h: Address 14h–15h)” on page 153. The LED interface shifts out the status of the selected functions for ports enabled in the “LED Enable Map Register (Page 00h: Address 16h–17h)” on page 154.

Only four or less than four functions can be selected, and the per-port LED display occupies four LED pins (four fixed functions). For example, if LED display function using the “LED Function 1 Control Register (Page 00h: Address 12h)” on page 153 is configured and the value is set to 0324h (four LED functions) or 0320h (three LED functions), the per-port LED display has four fixed functions and occupies four LED pins per port, Port4 (LED0–3), Port3 (LED4–7), ....Port0 (LED16–19).

The status of enabled ports is sent out from a higher port number to the lowest port number. The output order that is in the shift out is from LED[0], LED[1], LED[2],.....LED[19]. The output port order for LED is from high port number to low port number, and the output bit order within the port LED is from MSB to LSB.

The LED MODE MAP 0 and 1 (page 00h: address 18h and 1Ah) can be set to select:

- LED to blinking,
- LED on, or
- LED auto mode.

Bit 7, LED\_EN, of the “[LED Refresh Register \(Page 00h: Address 0Fh\)](#)” on [page 151](#) is default enabled. When this bit 7 is enabled, the LED display of each port status is normal and truly reflects each port link up/link down status. If bit 7 is disabled, the LED status is latched in its current state.

LED signals are active low, and for the dual function LEDs, LNK, DPX, and Speed state are active low. The ACT (activity) indicator is indicated by blinking.

**Table 30: LED Output Pins per Port**

| <b>Port</b> | <b>LED Output Pins</b> |
|-------------|------------------------|
| Port 4      | LED [0:3]              |
| Port 3      | LED [4:7]              |
| Port 2      | LED [8:11]             |
| Port 1      | LED [12:15]            |
| Port 0      | LED [16:19]            |



**Note:** The BCM53115S device may display a short LED blink during power up (~1 ms). This behavior can be eliminated either by connecting an NC pin to ground (pin U14 for the BCM53115KFB; pin AA18 for the BCM53115IPB) or by connecting ACT\_LOOP\_DETECT pin to 3.3V if the loop detection function is not used (pin F09 for the BCM53115KFB; pin D08 for the BCM53115IPB). Refer to the BCM53115 errata document, 53115-ES40x-R, for more information.

Figure 44 shows the LED Interface register structure.

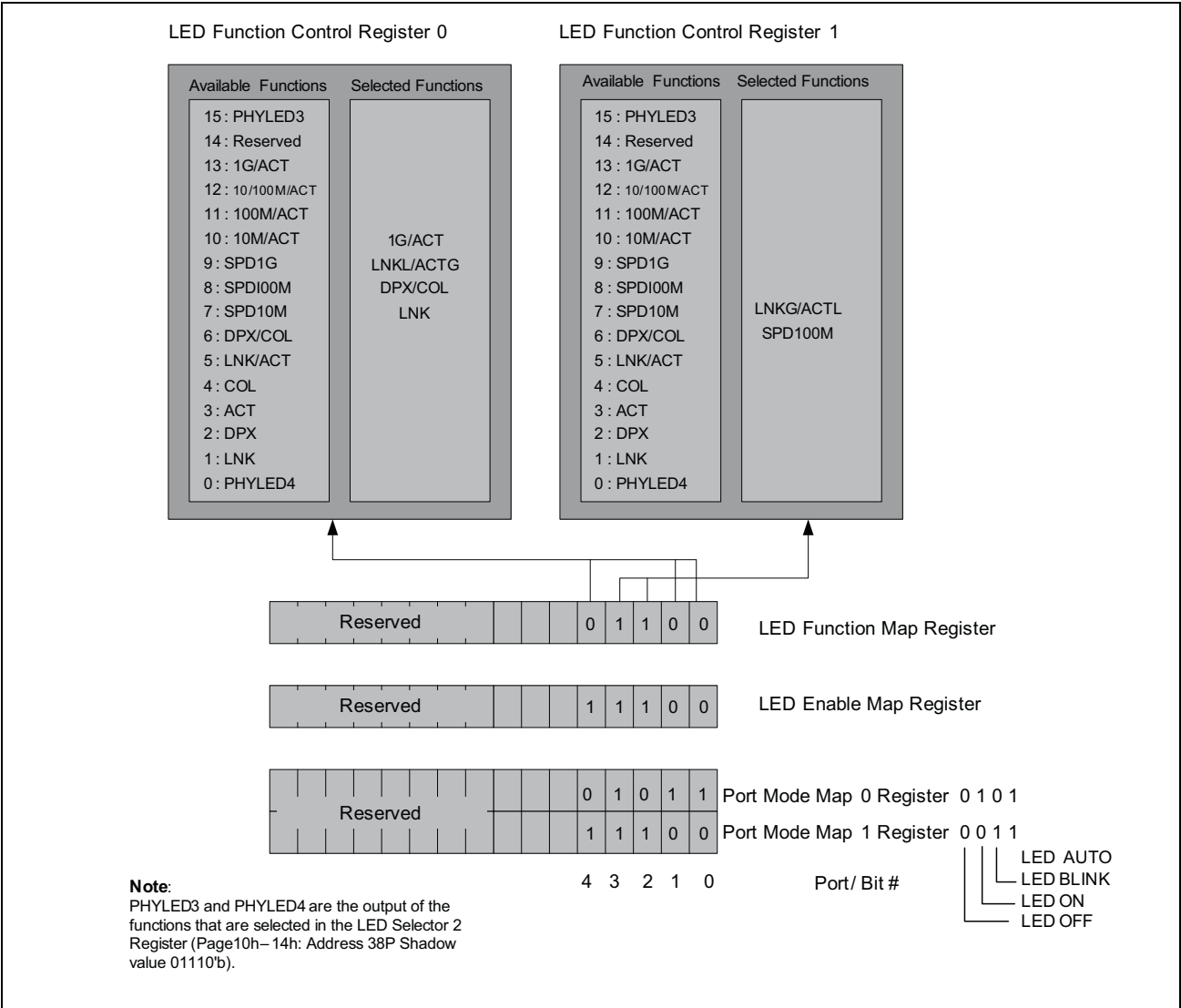


Figure 44: LED Interface Register Structure Diagram

The BCM53115S offer two LED Interfaces, Parallel LED Interface and Serial Interface. As shown in Figure 45, the source of LED status stream is the same for both interfaces; the status bit stream is based on the programmed register settings. The Parallel LED Interface provides all the shifting and storing of the status internally, so that it does not require any external shift registers, but it requires more I/O pins to be connected on the part.

The Serial LED Interface is being output through two pins (LEDDATA, LEDCLK). It saves the number of I/O pins but requires the user to design in the external shift registers. The serial LED interface provides the LED display for ports 0–5.

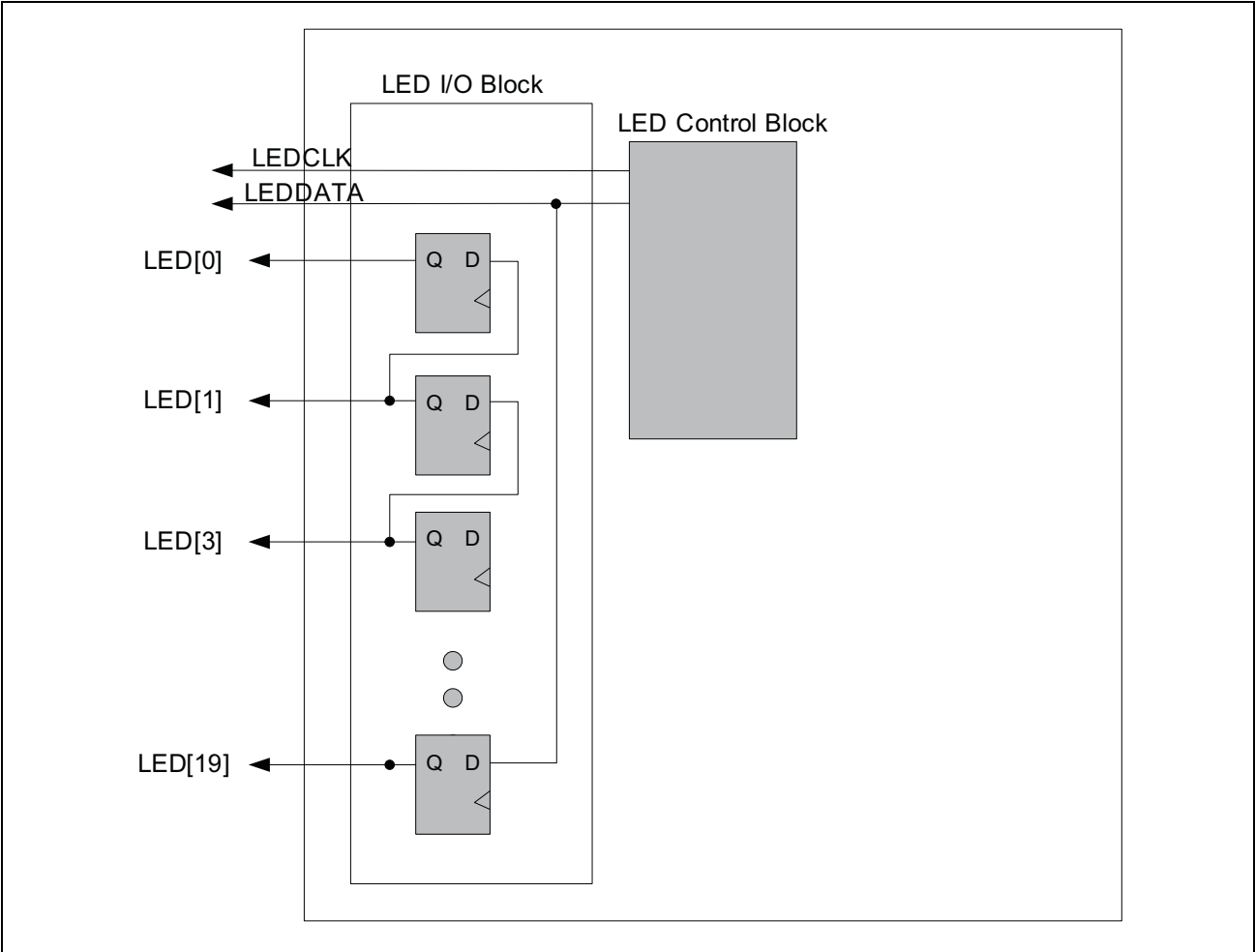


Figure 45: LED Interface Block Diagram

Dual LED is used for displaying more than one status using one LED cell. By packing two different colors LED into one holder, dual LED can display more than two states in one cell. Figure 46 shows a typical dual LED usage. Green LED is to display LNKG/ACT status, while Yellow LED is to display LNKF/ACT status.

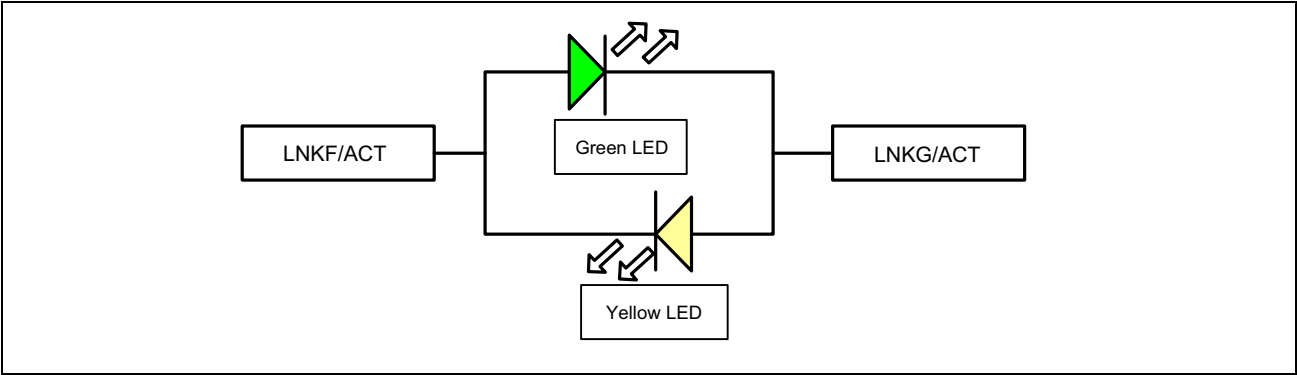


Figure 46: Dual LED Usage Example

## Section 5: Hardware Signal Definition Table

### I/O Signal Types

The following conventions are used to identify the I/O types shown in [Table 31](#). The I/O pin type is useful in referencing the DC-pin characteristics.

**Table 31: I/O Signal Type Definitions**

| <b>Abbreviation</b> | <b>Description</b>          |
|---------------------|-----------------------------|
| XYZ                 | Active low signal           |
| 3T                  | 3.3V tolerant               |
| A                   | Analog pin type             |
| B                   | Bias pin type               |
| CS                  | Continuously sampled        |
| D                   | Digital pin type            |
| DNC                 | Do not connect              |
| GND                 | Ground                      |
| I                   | Input                       |
| I/O                 | Bidirectional               |
| IPU                 | Input with internal pull-up |
| O <sub>3S</sub>     | Tristated Signal            |
| O <sub>DO</sub>     | Open-drain output           |
| O                   | Output                      |
| PD                  | Internal pull-down          |
| SOR                 | Sample on reset             |
| PWR                 | Power pin supply            |
| PU                  | Internal pull-up            |
| XT                  | Crystal pin type            |

## Signal Descriptions

**Table 32: Signal Type Definitions**

| Signal Name      | Type  | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Serial Interface |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD0_0±          | IA/OA | Transmit/Receive Pairs. In TRD [pair number]_[port number]± 1000BASE-T mode, differential data from the media is transmitted and received on all four signal pairs. In auto-negotiation and 10BASE-T and 100BASE-TX modes, the BCM53115S normally transmits on TRD[0]_[port number]± and receives on TRD[1]_{port number}±. Auto-MDIX operation can reverse the pairs TRD[0]_{4:0}± and TRD[1]_{4:0}± |
| TRD1_0±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD2_0±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD3_0±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD0_1±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD1_1±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD2_1±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD3_1±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD0_2±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD1_2±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD2_2±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD3_2±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD0_3±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD1_3±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD2_3±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD3_3±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD0_4±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD1_4±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD2_4±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| TRD3_4±          |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| Clock/Reset      |       |                                                                                                                                                                                                                                                                                                                                                                                                       |
| RESET            | IPU   | Hardware reset input: Active low Schmitt-triggered input. Resets the BCM53115S.                                                                                                                                                                                                                                                                                                                       |
| XTALI            | IXT   | 25 MHz Crystal Oscillator Input/Output. A continuous 25 MHz reference clock must be supplied to the BCM53115S by connecting a 25 MHz crystal between these two pins or by driving XTALI with an external 25 MHz oscillator clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTALO unconnected. The maximum XTALI input voltage is 3.3V. |
| XTALO            | OXT   |                                                                                                                                                                                                                                                                                                                                                                                                       |
| OSC_XTAL_SEL     | IPD   | Oscillator/crystal selection<br>1 = External clock source using oscillator<br>0 = External clock source using crystal                                                                                                                                                                                                                                                                                 |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b>   | <b>Type</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>IMP Interface</b> |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| IMP_TXCLK            | I/O         | <p>MII Transmit Clock. This is an input pin in MII mode, or GMII mode but speed is 100Mbps/10Mbps. It synchronizes the TXD[3:0] and connects to the PHY Entity TXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz.</p> <p>RvMII Receive Clock. This is an output pin in RvMII mode. It synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/Management Entity RXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. This output pin has an internal 25Ω series termination resistor.</p> <p>This clock is not use in the other conditions.</p>                                                                                                              |
| IMP_TXD[3:0]         | O           | <p>GMII Transmit Data Output (first nibble). Data bits TXD[3:0] are clocked on the rising edge of TXCLK.</p> <p>RGMII Transmit Data Output. For 1000 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mbps and 100 Mbps, data bits TXD[3:0] are clocked on the rising edge of TXCLK.</p> <p>RvMII Receive Data Output. Clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/Management entity.</p> <p>MII Transmit Data Output. Clocked on the rising edge of TXCLK supplied by MAC/Management entity.</p> <p>These output pins have internal 25Ω series termination resistor.</p> |
| IMP_TXD[7:4]         | O           | <p>GMII Transmit Data Output (second nibble). Data bits [7:4] are clocked on the rising edge of TXCLK. These output pins have internal 25Ω series termination resistor.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| IMP_TXEN             | O           | <p>GMII/MII Transmit Enable. Active high. TXEN indicates the data on the TXD pins are encoded and transmitted.</p> <p>RGMII Transmit Control. On the rising edge of TXCLK, TXEN indicates that a transmit frame is in progress, and the data present on the TXD[3:0] output pins is valid. On the falling edge of TXCLK, TXEN is a derivative of GMII mode TXEN and TXER signals.</p> <p>RvMII Receive Data Valid. Active high. Connected to RXDV pin of MAC/Management entity. Indicates that a receive frame is in progress, and the data present on the TXD[3:0] output pins is valid.</p> <p>This output pin has an internal 25Ω series termination resistor.</p>                                                  |
| IMP_TXER             | O           | <p>GMII/MII Transmit Error. Active high. Asserting TXER when TXEN is high indicates a transmission error. TXER is also used to indicate Carrier Extension when operating in half-duplex mode. This output pin has an internal 25Ω series termination resistor.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b> | <b>Type</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IMP_RXCLK          | I           | GMII Receive Clock. 125 MHz for 1000 Mbps operation.<br>RGMII Receive Clock. 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. Data bits RXD[3:0] are clocked in on the rising edge of the RXCLK, and data bits RXD[7:4] are clocked in on the falling edge of the RXCLK.<br>MII Receive Clock. 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation.                                                                                                                                                                                                     |
|                    | O           | RvMII Transmit Clock. Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/Management entity TXC. 25 MHz for 100 Mbps mode, and 2.5 MHz for 10 Mbps mode. This output pin has an internal 25Ω series termination resistor.                                                                                                                                                                                                                                                                                                                                                                                  |
| IMP_RXD[3:0]       | I           | GMII Receive Data Inputs (first nibble). Data bits RXD[3:0] are clocked on the rising edge of RXCLK.<br>RGMII Receive Data Inputs. For 1000 Mbps operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mbps and 100 Mbps modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK.<br>RvMII Transmit Data Inputs. Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/Management entity.<br>MII Receive Data Input. Data bits RXD[3:0] are clocked on the rising edge of RXCLK. |
| IMP_RXD[7:4]       | I           | GMII Receive Data Inputs (second nibble). Data bits RXD[7:4] are clocked out on the rising edge of RXCLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| IMP_RXDV           | I           | GMII/MII Receive Data Valid. Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid.<br>RGMII Receive Data Valid. Functional equivalent of GMII RXDV on the rising edge of RXCLK and functional equivalent of a logical derivative of GMII RXDV and RXER on the falling edge of RXCLK.<br>RvMII Transmit Enable. Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/Management entity.                                                                                          |
| IMP_RXER           | I           | GMII/MII Receive Error. Indicates an error during the receive frame.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| IMP_CRS            | I           | Carrier Sense. Active-high, indicates traffic on link                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| IMP_COL            | I           | Collision Detect. In half-duplex mode, active-high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal.                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b>                                                            | <b>Type</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------------------------------------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IMP_GTX_CLK                                                                   | O           | <p>GMII Transmit clock. This clock is driven to synchronize the transmit data in 1000 Mbps speed in GMII mode.</p> <p>RGMII Transmit Clock. This clock is driven to synchronize the transmit data in RGMII mode(125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation). In RGMII mode, both edges of the clock are used to align with TXD[3:0].</p> <p>IMP_GTX_CLK is used in RGMII and 1000 Mbps speed in GMII mode.</p> <p>IMP_TXCLK is used for MII mode, and 10/100 Mbps speed in GMII mode. This output pin has an internal 25Ω series termination resistor.</p> |
| <b>WAN Interface of Port 5, GMII_CTRL= 1 (GMII/RGMII/RvMII/MII interface)</b> |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| GMII_GTXCLK                                                                   | O           | <p>GMII Transmit clock. This clock is driven to synchronize the transmit data in 1000 Mbps speed in GMII mode.</p> <p>RGMII Transmit Clock. This clock is driven to synchronize the transmit data in RGMII mode(125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation). In RGMII mode, both edges of the clock are used to align with TXD[3:0].</p> <p>GMII_GTXCLK is used in RGMII and 1000 Mbps speed in GMII mode.</p> <p>GMII_TXCLK is used for MII mode, and 10/100 Mbps speed in GMII mode. This output pin has an internal 25Ω series termination resistor</p> |
| GMII_TXCLK                                                                    | I/O         | <p>MII Transmit Clock. This is an input pin in MII mode, or GMII mode but speed is 100 Mbps/10 Mbps. It synchronizes the TXD[3:0] and connects to the PHY Entity TXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz.</p> <p>RvMII Receive Clock. This is an output pin in RvMII mode. It synchronizes the TXD[3:0] in RvMII mode and connects to the MAC/Management Entity RXC. In 100 Mbps mode, this is 25 MHz, and in 10 Mbps mode, this is 2.5 MHz. This output pin has an internal 25Ω series termination resistor.</p> <p>This clock is not uses in the other conditions.</p>      |
| GMII_TXEN                                                                     | O           | <p>GMII/MII Transmit Enable. Active high. TXEN indicates the data on the TXD pins are encoded and transmitted.</p> <p>RvMII Receive Data Valid. Active high. Connected to RXDV pin of MAC/Management entity. Indicates that a receive frame is in progress, and the data present on the TXD[3:0] output pins is valid. This output pin has an internal 25Ω series termination resistor.</p>                                                                                                                                                                                                                       |
| GMII_TXER                                                                     | O           | <p>GMII/MII Transmit Error. Active high. Asserting TXER when TXEN is high indicates a transmission error. TXER is also used to indicate Carrier Extension when operating in half-duplex mode. This output pin has an internal 25Ω series termination resistor.</p>                                                                                                                                                                                                                                                                                                                                                |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b> | <b>Type</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GMII_TXD[3:0]      | O           | <p>GMII Transmit Data Output (first nibble). Data bits TXD[3:0] are clocked on the rising edge of TXCLK.</p> <p>RGMII Transmit Data Output. For 1000 Mbps operation, data bits TXD[3:0] are clocked on the rising edge of TXCLK, and data bits TXD[7:4] are clocked on the falling edge of TXCLK. For 10 Mbps and 100 Mbps, data bits TXD[3:0] are clocked on the rising edge of TXCLK.</p> <p>RvMII Receive Data Output. Clocked on the rising edge of TXCLK and connected to the RXD pins of the external MAC/Management entity.</p> <p>MII Transmit Data Output. Clocked on the rising edge of TXCLK supplied by MAC/Management entity.</p> <p>These output pins have internal 25Ω series termination resistor.</p> |
| GMII_TXD[7:4]      | O           | <p>GMII transmit data output (second nibble): Data bits [7:4] are clocked on the rising edge of TXCLK. These output pins have internal 25Ω series termination resistor.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| GMII_CRS           | I           | Carrier sense: Active-high, indicates traffic on link                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| GMII_COL           | I           | Collision detect: In half-duplex mode, active-high input indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous input signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| GMII_RXCLK         | I           | <p>GMII receive clock: 125 MHz for 1000 Mbps operation</p> <p>RGMII receive clock: 125 MHz for 1000 Mbps operation, 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation. Data bits RXD[3:0] are clocked in on the rising edge of the RXCLK, and data bits RXD[7:4] are clocked in on the falling edge of the RXCLK.</p> <p>MII Receive Clock. 25 MHz for 100 Mbps operation, and 2.5 MHz for 10 Mbps operation.</p>                                                                                                                                                                                                                                                                                       |
|                    | O           | <p>RvMII transmit clock: Synchronizes the RXD[3:0] in RvMII mode and connects to the MAC/Management entity TXC. 25 MHz for 100 Mbps mode, and 2.5 MHz for 10 Mbps mode. This output pin has an internal 25Ω series termination resistor.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| GMII_RXDV          | I           | <p>GMII/MII receive data valid: Active high. RXDV indicates that a receive frame is in progress, and the data present on the RXD output pins is valid.</p> <p>RGMII Receive Data Valid. Functional equivalent of GMII RXDV on the rising edge of RXCLK and functional equivalent of a logical derivative of GMII RXDV and RXER on the falling edge of RXCLK.</p> <p>RvMII Transmit Enable. Active high. Indicates the data on the RXD[3:0] pins are encoded and transmitted. Connects to the TXEN of the external MAC/Management entity.</p>                                                                                                                                                                           |
| GMII_RXER          | I           | GMII/MII receive error: Indicates an error during the receive frame.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b>                                                    | <b>Type</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------------------------------------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GMII_RXD[3:0]                                                         | I           | GMII receive data inputs (first nibble): Data bits RXD[3:0] are clocked on the rising edge of RXCLK.<br>RGMII Receive Data Inputs. For 1000 Mbps operation, data bits RXD[3:0] are clocked-out on the rising edge of RXCLK, and data bits RXD[7:4] are clocked on the falling edge of RXCLK. In 10 Mbps and 100 Mbps modes, data bits RXD[3:0] are clocked on the rising edge of RXCLK.<br>RvMII Transmit Data Inputs. Clocked on the rising edge of RXCLK and connected to the TXD pins of the external MAC/Management entity.<br>MII Receive Data Input. Data bits RXD[3:0] are clocked on the rising edge of RXCLK. |
| GMII_RXD[7:4]                                                         | I           | GMII receive data inputs (second nibble): Data bits RXD[7:4] are clocked out on the rising edge of RXCLK.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <b>WAN Interface of Port 5, GMII_CTRL= 0 (SGMII/SerDes Interface)</b> |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SGRX-<br>SGRX+<br>SGTX-<br>SGTX+                                      | IA/OA       | Serial transmit/receive pairs: Differential serial input and output data pairs                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| SD                                                                    | IPU         | Serial signal detection                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| <b>MDC/MDIO Interface</b>                                             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| MDIO                                                                  | I/OPD       | Management data I/O: In master mode, this serial input/output data signal is used to read from and write to the MII registers of the external transceivers. In slave mode, it is used by an external entity to read/write to the switch registers using the Pseudo-PHY. See the MDC/MDIO interface for more information.                                                                                                                                                                                                                                                                                               |
| MDC                                                                   | I/OPD       | Management data clock: In master mode, this 2.5 MHz clock sourced by BCM53115S to the external PHY device. In slave mode, it is sourced by an external entity.                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| <b>Test Interface</b>                                                 |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| TCK                                                                   | IPU         | JTAG test clock input: Clock Input used to synchronize JTAG control and data transfers. If unused, may be left unconnected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| TDI                                                                   | IPU         | JTAG Test Data Input. Serial data input to the JTAG TAP Controller. Sampled on the rising edge of TCK. If unused, may be left unconnected. Shared with MOSI.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| TDO                                                                   | O           | JTAG test data output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| TMS                                                                   | IPU         | JTAG mode select input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| TRST                                                                  | IPU         | JTAG test reset: active low<br>Resets the JTAG controller. This signal must be pulled low during normal operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b>        | <b>Type</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                             |
|---------------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Configuration Pins</b> |             |                                                                                                                                                                                                                                                                                                                                |
| BC_SUPP_EN                | IPD, SOR    | Broadcast suppression enable<br>0 = Disable rate-based broadcast suppression.<br>1 = Enable rate-based broadcast suppression.<br>See <a href="#">“Rate Control” on page 44</a> for more information.                                                                                                                           |
| CLK_FREQ1                 | IPD, SOR    | System clock selection: Determines rate of system clock.                                                                                                                                                                                                                                                                       |
| CLK_FREQ0                 | IPU, SOR    | 00 = 83 MHz<br>01 = 91 MHz (normal operation)<br>10 = 100 MHz<br>11 = 111 MHz                                                                                                                                                                                                                                                  |
| CPU_EEPROM_SEL            | IPU, SOR    | CPU or EEPROM interface selection<br>CPU_EEPROM_SEL = 0: Enable EEPROM interface.<br>CPU_EEPROM_SEL = 1: Enable SPI Interface, The SPI interface has to be enabled (CPU_EEPROM_SEL=1) for Pseudo-PHY accesses through the MDC/MDIO Interface.<br>See <a href="#">“Programming Interfaces” on page 91</a> for more information. |
| ENFDXFLOW                 | IPU, SOR    | Enable automatic full-duplex flow control.<br>In combination with the results of auto-negotiation, sets the flow control mode. See <a href="#">“Flow Control” on page 65</a> for more information.                                                                                                                             |
| ENHDXFLOW                 | IPU, SOR    | Enable automatic backpressure. When this pin is pulled high, it enables half-duplex backpressure flow control when a port is configured to half-duplex.<br>See <a href="#">“Flow Control” on page 65</a> for more information.                                                                                                 |
| EEPROM_TYPE[1:0]          | IPD, SOR    | Extended EEPROM interface selection<br>EEPROM_EXT[1:0] = 00: Supports 93C46 EEPROM<br>EEPROM_EXT[1:0] = 01: Supports 93C56 EEPROM<br>EEPROM_EXT[1:0] = 10: Supports 93C66 EEPROM<br>EEPROM_EXT[1:0] = 11: Supports 93C86 EEPROM<br>See <a href="#">“EEPROM Interface” on page 106</a> for more information.                    |
| HW_FWDG_EN                | IPD,SOR     | Forwarding enable: Active high. If this pin is pulled low at power-up, frame forwarding is disabled.                                                                                                                                                                                                                           |
| DIS_IMP                   | IPD,SOR     | Disables IMP port<br>0 = Enable IMP port, and external pull-down resistor is required.<br>1 = Disable IMP port, and external pull-up resistor is required.                                                                                                                                                                     |

**Table 32: Signal Type Definitions (Cont.)**

| Signal Name                                                     | Type                                                            | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
|-----------------------------------------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|---------|-------------|---------|---------|---------|---------|--|---------------|-----------------------------------------------------------------|-----------------------------------------------------------------|----------|--------|---------|-------------|---------|---------|---------|---------|-----------------------------------------------------------------|-----------------------------------------------------------------|---------|-------|---------|---------|-----|---------|--|-----|-----------------------------------------------------------------|-----------------------------------------------------------------|----------|--------|---------|----------|-----|---------|--|-----|
| LED MODE[1:0]                                                   | Bit 0 = IPD,<br>Bit 1 = IPU,<br>SOR                             | <p>LED mode: Users can select predefined functions to be displayed for each port by setting the bits accordingly. By default, the “<a href="#">LED Function Map Register (Page 00h: Address 14h–15h)</a>” points to the “<a href="#">LED Function 1 Control Register (Page 00h: Address 12h)</a>” settings.</p> <p>When LED MODE[1:0] = 00</p> <table><tr><td>Default LED Function 0 Control Register (page 00h, address 10h)</td><td>Default LED Function 1 Control Register (page 00h, address 12h)</td></tr><tr><td>SPD100M</td><td>SPD1G (LSB)</td></tr><tr><td>LNK/ACT</td><td>SPD100M</td></tr><tr><td>PHYLED4</td><td>LNK/ACT</td></tr><tr><td></td><td>PHYLED4 (MSB)</td></tr></table> <p>When LED MODE[1:0] = 01</p> <table><tr><td>Default LED Function 0 Control Register (page 00h, address 10h)</td><td>Default LED Function 1 Control Register (page 00h, address 12h)</td></tr><tr><td>100M/ACT</td><td>1G/ACT</td></tr><tr><td>10M/ACT</td><td>10/100M/ACT</td></tr><tr><td>DPX/COL</td><td>DPX/COL</td></tr><tr><td>PHYLED4</td><td>PHYLED4</td></tr></table> <p>When LED MODE[1:0] = 10</p> <table><tr><td>Default LED Function 0 Control Register (page 00h, address 10h)</td><td>Default LED Function 1 Control Register (page 00h, address 12h)</td></tr><tr><td>SPD100M</td><td>SPD1G</td></tr><tr><td>LNK/ACT</td><td>SPD100M</td></tr><tr><td>DPX</td><td>LNK/ACT</td></tr><tr><td></td><td>DPX</td></tr></table> <p>When LED MODE[1:0] = 11</p> <table><tr><td>Default LED Function 0 Control Register (page 00h, address 10h)</td><td>Default LED Function 1 Control Register (page 00h, address 12h)</td></tr><tr><td>100M/ACT</td><td>1G/ACT</td></tr><tr><td>10M/ACT</td><td>100M/ACT</td></tr><tr><td>DPX</td><td>10M/ACT</td></tr><tr><td></td><td>DPX</td></tr></table> | Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) | SPD100M | SPD1G (LSB) | LNK/ACT | SPD100M | PHYLED4 | LNK/ACT |  | PHYLED4 (MSB) | Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) | 100M/ACT | 1G/ACT | 10M/ACT | 10/100M/ACT | DPX/COL | DPX/COL | PHYLED4 | PHYLED4 | Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) | SPD100M | SPD1G | LNK/ACT | SPD100M | DPX | LNK/ACT |  | DPX | Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) | 100M/ACT | 1G/ACT | 10M/ACT | 100M/ACT | DPX | 10M/ACT |  | DPX |
| Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| SPD100M                                                         | SPD1G (LSB)                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| LNK/ACT                                                         | SPD100M                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| PHYLED4                                                         | LNK/ACT                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
|                                                                 | PHYLED4 (MSB)                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| 100M/ACT                                                        | 1G/ACT                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| 10M/ACT                                                         | 10/100M/ACT                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| DPX/COL                                                         | DPX/COL                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| PHYLED4                                                         | PHYLED4                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| SPD100M                                                         | SPD1G                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| LNK/ACT                                                         | SPD100M                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| DPX                                                             | LNK/ACT                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
|                                                                 | DPX                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| Default LED Function 0 Control Register (page 00h, address 10h) | Default LED Function 1 Control Register (page 00h, address 12h) |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| 100M/ACT                                                        | 1G/ACT                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| 10M/ACT                                                         | 100M/ACT                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| DPX                                                             | 10M/ACT                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
|                                                                 | DPX                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |
| IMP_SPD_SEL[1:0]                                                | Bit 0: IPD,<br>Bit 1: IPU                                       | <p>IMP port speed select</p> <p>00 = 10 Mbps</p> <p>01 = 100 Mbps</p> <p>10 = 1000 Mbps (default)</p> <p>11 = Illegal</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                 |                                                                 |         |             |         |         |         |         |  |               |                                                                 |                                                                 |          |        |         |             |         |         |         |         |                                                                 |                                                                 |         |       |         |         |     |         |  |     |                                                                 |                                                                 |          |        |         |          |     |         |  |     |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b>     | <b>Type</b>                      | <b>Description</b>                                                                                                                                                                                                    |
|------------------------|----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IMP_MODE[1:0]          | Bit 0: IPU,<br>Bit 1: IPU<br>SOR | IMP port mode: Sets the mode of the IMP port based on the value of the pins at power-on reset.<br>00 = RGMII mode<br>01 = MII mode<br>10 = RvMII mode<br>11 = GMII mode                                               |
| IMP_DUPLEX             | IPU                              | 0 = IMP in half-duplex mode<br>1 = IMP in full-duplex mode                                                                                                                                                            |
| IMP_LINK               | IPD                              | 0 = IMP link-down<br>1 = IMP link-up                                                                                                                                                                                  |
| IMP_PAUSE_CAP_RX       | IPU                              | Enable IMP port pause capable in RX<br>0 = Disable Pause capable<br>1 = Enable Pause capable                                                                                                                          |
| IMP_PAUSE_CAP_TX       | IPU                              | Enable IMP port pause capable in TX<br>0 = Disable Pause capable<br>1 = Enable Pause capable                                                                                                                          |
| IMP_RXC_DELAY          | IPD, SOR                         | RXCLK clock timing delay: active high. This pin enables the RXCLK to data-sampling timing delay. See <a href="#">“RGMII Interface Timing” on page 306</a> for more information.                                       |
| IMP_TXC_DELAY          | IPD, SOR                         | TXCLK clock timing delay: active high. This pin enables the TXCLK to data timing delay in RGMII mode. See <a href="#">“RGMII Interface Timing” on page 306</a> for more information.                                  |
| IMP_VOL_SEL[1:0]       | IPD                              | IMP interface voltage control. RGMII must be set to 01 for 2.5V; GMII/MII/RvMII must be set to 00 for 3.3V.<br>00: 3.3V<br>01: 2.5V<br>10: Reserved<br>11: Reserved                                                   |
| IMP_DUMB_FWDG_EN       | IPD,SOR                          | IMP port in blocking state for unmanaged mode<br>0 = Blocking for dumb mode<br>1 = Forwarding for dumb mode<br>When this pin is pulled up, the IMP port is not in management mode, the IMP port is in a regular port. |
| EN_CLK25_OUT/CLK25_OUT | OPD,SOR                          | Enable CLK25 out and CLK_25 output: EN_CLK25_OUT is a strap pin function.<br>0 = Disable clock out<br>1 = Enable clock out                                                                                            |
| EN_CLK50_OUT/CLK50_OUT | OPD,SOR                          | Enable CLK50 out and CLK_50 output. EN_CLK50_OUT is a strap pin function.<br>0 = Disable clock out<br>1 = Enable clock out                                                                                            |
| ACT_LOOP_DET           | IPD                              | Loop detection feature activation                                                                                                                                                                                     |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b>   | <b>Type</b>               | <b>Description</b>                                                                                                                                                                                            |
|----------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LOOP_DET_EN          | IPD,SOR                   | Enable loop detection mode                                                                                                                                                                                    |
| LOOP_IMP_SEL         | IPD,SOR                   | Exclude IMP port in loop detection function.<br>0 = Exclude IMP port from loop detection function<br>1 = Include IMP port in loop detection function                                                          |
| LOOP_DETECTED        | OPD                       | Loop found: This signal is to indicate there is a loop detected in the local network connection.                                                                                                              |
| GMII_CTRL            | IPD,SOR                   | Strap pin for WAN interface control of port 5<br>0 = SGMII/SerDes interface<br>1 = GMII/RGMII/RvMII/MII interface                                                                                             |
| GMII_MODE[1:0]       | Bit 0: IPU,<br>Bit 1: IPU | Strap pin for WAN interface mode of port 5<br>00 = RGMII<br>01 = MII<br>10 = RvMII<br>11 = GMII                                                                                                               |
| GMII_RXC_DELAY       | IPD, SOR                  | RXCLK clock timing delay: active high. This pin enables the RXCLK output delay.<br>Only use in RGMII interface of port 5, GMII_CTRL = 1, GMII_MODE[1:0] = 00                                                  |
| GMII_TXC_DELAY       | IPD, SOR                  | GTCLK clock timing delay: active high. This pin enables the GTCLK input delay.<br>Only use in RGMII Interface of Port 5, GMII_CTRL = 1, GMII_MODE[1:0] = 00                                                   |
| GMII_VOL_SEL[1:0]    | IPD                       | WAN interface port 5 voltage control when GMII_CTRL = 1: RGMII must be set to 01 for 2.5V; GMII/MII/RvMII must be set to 00 for 3.3V.<br>00 = 3.3V<br>01 = 2.5V<br>10 = Reserved<br>11 = Reserved             |
| <b>LED Interface</b> |                           |                                                                                                                                                                                                               |
| LED{19:0}            | O                         | Parallel LED indicators:<br>LED{19:0} = 5 ports × 4 LEDs = 20 (exclude IMP)                                                                                                                                   |
| LEDCLK               | OPD                       | LED shift clock: This clock is periodically active to enable LEDDATA to shift into external registers.                                                                                                        |
| LEDDATA              | OPD                       | Serial LED data output: Serial LED data for all ports is shifted out when LEDCLK is active. LEDMODE[1:0] pins set the serial data content. See the LED interface for a functional description of this signal. |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b>            | <b>Type</b>    | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Programming Interfaces</b> |                |                                                                                                                                                                                                                                                                                                                                                                                                         |
| SCK                           | IPD<br>OPD     | SPI serial clock: The clock input to the BCM53115S SPI interface is supplied by the SPI master, which supports up to 2 MHz, and is enabled if CPU_EEPROM_SEL is high during power-on reset.<br>EEPROM Serial Clock. The clock output to an external EEPROM device, and is enabled if CPU_EEPROM_SEL is low during power-on reset.<br>See the programming interfaces for more information.               |
| SS/CS                         | IPU<br>OPU     | SPI slave select: Active low signal which enables an SPI interface read or write operation. Enable if CPU_EEPROM_SEL is high during power-on reset.<br>EEPROM Chip Select. Active high control signal that enables a read operation from an external EEPROM device. Enable if CPU_EEPROM_SEL is low during power-on reset.<br>See the programming interfaces for more information.                      |
| MOSI/DI                       | IPD, 3T<br>OPD | SPI master-out/slave-in: Input signal which receives control and address information for the SPI interface, as well as serial data during write operations. Enabled if CPU_EEPROM_SEL is high during power-on reset.<br>EEPROM Data In. Serial data input to an external EEPROM device. Enabled if CPU_EEPROM_SEL is low during power-on reset.<br>See the programming interfaces for more information. |
| MISO/DO                       | OPD<br>IPD     | SPI master-in/slave-out: Output signal which transmits serial data during an SPI interface read operations. Enabled if CPU_EEPROM_SEL is high during power-on reset.<br>EEPROM Data Out. Serial data output to an external EEPROM device. Enable if CPU_EEPROM_SEL is low during power-on reset.<br>See the programming interfaces for more information.                                                |
| <b>Interrupt Pin</b>          |                |                                                                                                                                                                                                                                                                                                                                                                                                         |
| INT                           | O3S            | Link status change interrupt: If the interrupt is enabled, this pin asserted low when link status change occurs.<br>This pin is tristate after reading Link Status register (page 01h: address 2h).                                                                                                                                                                                                     |
| <b>Bias</b>                   |                |                                                                                                                                                                                                                                                                                                                                                                                                         |
| GPHY1_RDAC                    | Bias           | A 1.24-K $\Omega$ resistor to GND is required.                                                                                                                                                                                                                                                                                                                                                          |
| GPHY2_RDAC                    | Bias           | A 1.24-k $\Omega$ resistor to GND is required.                                                                                                                                                                                                                                                                                                                                                          |
| <b>Power Interfaces</b>       |                |                                                                                                                                                                                                                                                                                                                                                                                                         |
| AVDDH                         | —              | 3.3V analog I/O power                                                                                                                                                                                                                                                                                                                                                                                   |
| AVDDL                         | —              | 1.2V analog core power                                                                                                                                                                                                                                                                                                                                                                                  |
| DVDD                          | —              | 1.2V digital core power                                                                                                                                                                                                                                                                                                                                                                                 |

**Table 32: Signal Type Definitions (Cont.)**

| <b>Signal Name</b> | <b>Type</b> | <b>Description</b>                                                                                                                               |
|--------------------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| OVDD               | —           | Power for GMII/RGMII/MII/RvMII of IMP depends on IMP_VOL_SEL[1:0] configuration.<br>3.3V if IMP_VOL_SEL[1:0] =00<br>2.5V if IMP_VOL_SEL[1:0] =01 |
| OVDD2              | —           | 3.3V digital I/O power                                                                                                                           |
| OVDD3              | —           | Power for WAN interface port 5 depends on GMII_VOL_SEL[1:0] configuration.<br>3.3V if GMII_VOL_SEL[1:0] =00<br>2.5V if GMII_VOL_SEL[1:0] =01     |
| GPHY1_BAVDD        | —           | 3.3V analog power                                                                                                                                |
| GPHY2_BAVDD        | —           | 3.3V analog power                                                                                                                                |
| PLL_AVDD           | —           | 1.2V analog power                                                                                                                                |
| GPHY1_PLLVDD       | —           | 1.2V analog power                                                                                                                                |
| GPHY2_PLLVDD       | —           | 1.2V analog power                                                                                                                                |
| GMII_VOL_REF       | —           | Port 5 WAN interface reference power<br>Connect this pin to ground                                                                               |
| IMP_VOL_REF        | —           | IMP interface reference power<br>Connect this pin to ground                                                                                      |
| SDVDD              | —           | 1.2V analog power                                                                                                                                |
| SD_PLLAVDD         | —           | 1.2V analog power                                                                                                                                |
| SD_PLLAVDD33       | —           | 3.3V analog power for XTAL_AVDD (XTALI, XTALO)                                                                                                   |
| AVSS               | —           | Shared digital ground                                                                                                                            |
| DVSS               | —           | Shared digital ground                                                                                                                            |
| PLL_AVSS           | —           | Shared analog ground                                                                                                                             |
| SDVSS              | —           | Shared digital ground                                                                                                                            |
| SD_PLLAVSS         | —           | Shared digital ground                                                                                                                            |
| <b>No Connect</b>  |             |                                                                                                                                                  |
| NC                 | —           | —                                                                                                                                                |

## Section 6: Pin Assignment

### BCM53115SKFB Pin List by Signal Name

*Table 33: BCM53115SKFB Pin List by Signal Name*

| <i>Signal</i>   | <i>Ball</i> | <i>Signal</i>  | <i>Ball</i> | <i>Signal</i> | <i>Ball</i> | <i>Signal</i> | <i>Ball</i> |
|-----------------|-------------|----------------|-------------|---------------|-------------|---------------|-------------|
| ACT_LOOP_DETECT | F9          | AVSS           | V18         | DVSS          | F15         | DVSS          | K5          |
| AVDDH           | D1          | AVSS           | W3          | DVSS          | G5          | DVSS          | K6          |
| AVDDH           | F4          | AVSS           | W18         | DVSS          | G6          | DVSS          | K7          |
| AVDDH           | H4          | AVSS           | Y3          | DVSS          | G7          | DVSS          | K8          |
| AVDDH           | K4          | BC_SUPP_EN     | V10         | DVSS          | G8          | DVSS          | K9          |
| AVDDH           | R4          | CLK_FREQ0      | U5          | DVSS          | G11         | DVSS          | K10         |
| AVDDH           | R17         | CLK_FREQ1      | T6          | DVSS          | G12         | DVSS          | K11         |
| AVDDH           | T16         | CPU_EEPROM_SEL | W10         | DVSS          | G13         | DVSS          | K12         |
| AVDDH           | T18         | DIS_IMP        | V5          | DVSS          | G14         | DVSS          | K13         |
| AVDDH           | U4          | DVDD           | D20         | DVSS          | G15         | DVSS          | K14         |
| AVDDH           | W4          | DVDD           | E6          | DVSS          | G16         | DVSS          | K15         |
| AVDDH           | Y18         | DVDD           | E14         | DVSS          | G18         | DVSS          | K18         |
| AVDDL           | E4          | DVDD           | E15         | DVSS          | H5          | DVSS          | L5          |
| AVDDL           | G4          | DVDD           | E16         | DVSS          | H6          | DVSS          | L6          |
| AVDDL           | J4          | DVDD           | F5          | DVSS          | H7          | DVSS          | L7          |
| AVDDL           | T4          | DVDD           | F7          | DVSS          | H8          | DVSS          | L8          |
| AVDDL           | T17         | DVDD           | F11         | DVSS          | H9          | DVSS          | L9          |
| AVDDL           | U18         | DVDD           | F12         | DVSS          | H10         | DVSS          | L10         |
| AVDDL           | V4          | DVDD           | F13         | DVSS          | H11         | DVSS          | L11         |
| AVDDL           | Y4          | DVDD           | G9          | DVSS          | H12         | DVSS          | L12         |
| AVSS            | D2          | DVDD           | H16         | DVSS          | H13         | DVSS          | L13         |
| AVSS            | E3          | DVDD           | L18         | DVSS          | H14         | DVSS          | L14         |
| AVSS            | F3          | DVDD           | R10         | DVSS          | H15         | DVSS          | L15         |
| AVSS            | G3          | DVDD           | R12         | DVSS          | J5          | DVSS          | L16         |
| AVSS            | H3          | DVDD           | T8          | DVSS          | J6          | DVSS          | M5          |
| AVSS            | J3          | DVDD           | Y6          | DVSS          | J7          | DVSS          | M6          |
| AVSS            | K3          | DVSS           | B3          | DVSS          | J8          | DVSS          | M7          |
| AVSS            | L3          | DVSS           | B5          | DVSS          | J9          | DVSS          | M8          |
| AVSS            | M3          | DVSS           | B7          | DVSS          | J10         | DVSS          | M9          |
| AVSS            | N3          | DVSS           | B12         | DVSS          | J11         | DVSS          | M10         |
| AVSS            | P3          | DVSS           | C15         | DVSS          | J12         | DVSS          | M11         |
| AVSS            | R3          | DVSS           | E19         | DVSS          | J13         | DVSS          | M12         |
| AVSS            | T3          | DVSS           | F6          | DVSS          | J14         | DVSS          | M13         |
| AVSS            | U3          | DVSS           | F8          | DVSS          | J15         | DVSS          | M14         |
| AVSS            | V3          | DVSS           | F14         | DVSS          | J16         | DVSS          | M15         |

| <i>Signal</i>              | <i>Ball</i> | <i>Signal</i>    | <i>Ball</i> | <i>Signal</i>   | <i>Ball</i> | <i>Signal</i> | <i>Ball</i> |
|----------------------------|-------------|------------------|-------------|-----------------|-------------|---------------|-------------|
| DVSS                       | N5          | GMII_COL         | G17         | IMP_DUPLEX      | B10         | LED14         | C13         |
| DVSS                       | N6          | GMII_CRS         | J17         | IMP_GTXCLK      | C5          | LED15         | B13         |
| DVSS                       | N7          | GMII_CTRL        | Y8          | IMP_LINK        | E9          | LED16         | D15         |
| DVSS                       | N8          | GMII_GTXCLK      | F19         | IMP_MODE0       | Y14         | LED17         | B15         |
| DVSS                       | N9          | GMII_MODE0       | V14         | IMP_MODE1       | T13         | LED18         | D14         |
| DVSS                       | N10         | GMII_MODE1       | V15         | IMP_PAUSECAP_RX | D13         | LED19         | C14         |
| DVSS                       | N11         | GMII_RXC_DELAY   | V16         | IMP_PAUSECAP_TX | C10         | LED2          | D9          |
| DVSS                       | N12         | GMII_RXCLK       | G20         | IMP_RXC_DELAY   | U11         | LED3          | A13         |
| DVSS                       | N13         | GMII_RXD0        | J20         | IMP_RXCLK       | B4          | LED4          | A14         |
| DVSS                       | N14         | GMII_RXD1        | J19         | IMP_RXD0        | C3          | LED5          | D10         |
| DVSS                       | N15         | GMII_RXD2        | J18         | IMP_RXD1        | A3          | LED6          | E11         |
| DVSS                       | P5          | GMII_RXD3        | H20         | IMP_RXD2        | C2          | LED7          | D11         |
| DVSS                       | P6          | GMII_RXD4        | H19         | IMP_RXD3        | A2          | LED8          | B11         |
| DVSS                       | P7          | GMII_RXD5        | H18         | IMP_RXD4        | B2          | LED9          | B14         |
| DVSS                       | P8          | GMII_RXD6        | H17         | IMP_RXD5        | A1          | LEDCLK        | A19         |
| DVSS                       | P9          | GMII_RXD7        | G19         | IMP_RXD6        | C1          | LEDDATA       | A20         |
| DVSS                       | P10         | GMII_RXDV        | L17         | IMP_RXD7        | B1          | LEDMODE0      | W5          |
| DVSS                       | P11         | GMII_RXER        | K17         | IMP_RXDV        | A4          | LEDMODE1      | Y5          |
| DVSS                       | P12         | GMII_TXC_DELAY   | T15         | IMP_RXER        | E5          | LOOP_DET_EN   | Y15         |
| DVSS                       | P13         | GMII_TXCLK       | F18         | IMP_SPD_SEL0    | A11         | LOOP_DETECTED | E10         |
| DVSS                       | P14         | GMII_TXD0        | C17         | IMP_SPD_SEL1    | A12         | LOOP_IMP_SEL  | W15         |
| DVSS                       | P15         | GMII_TXD1        | D17         | IMP_TXC_DELAY   | T12         | MDC           | A16         |
| DVSS                       | R5          | GMII_TXD2        | E17         | IMP_TXCLK       | B6          | MDIO          | B16         |
| DVSS                       | R7          | GMII_TXD3        | C18         | IMP_TXD0        | A6          | MISO          | B17         |
| DVSS                       | R8          | GMII_TXD4        | D18         | IMP_TXD1        | A7          | MOSI          | A18         |
| DVSS                       | R9          | GMII_TXD5        | B19         | IMP_TXD2        | B8          | NC            | T11         |
| DVSS                       | R11         | GMII_TXD6        | C19         | IMP_TXD3        | C7          | NC            | G10         |
| DVSS                       | R13         | GMII_TXD7        | D19         | IMP_TXD4        | A8          | NC            | K16         |
| DVSS                       | R14         | GMII_TXEN        | C20         | IMP_TXD5        | A9          | NC            | L4          |
| DVSS                       | T5          | GMII_TXER        | B20         | IMP_TXD6        | B9          | NC            | N16         |
| DVSS                       | U10         | GMII_VOL_REF     | F16         | IMP_TXD7        | A10         | NC            | R6          |
| DVSS                       | U12         | GMII_VOL_SEL0    | W14         | IMP_TXEN        | A5          | NC            | T7          |
| DVSS                       | U15         | GMII_VOL_SEL1    | V13         | IMP_TXER        | D6          | NC            | T9          |
| DVSS                       | V6          | GPHY1_BVDD       | N4          | IMP_VOL_REF     | E7          | NC            | T10         |
| DVSS                       | Y10         | GPHY1_PLLVDD     | M4          | IMP_VOL_SEL0    | T14         | NC            | U9          |
| DVSS                       | Y12         | GPHY1_RDAC       | P4          | IMP_VOL_SEL1    | R15         | NC            | U14         |
| EEPROM_TYPE0               | U6          | GPHY2_BVDD       | W17         | INT             | C9          | NC            | U16         |
| EEPROM_TYPE1               | W6          | GPHY2_PLLVDD     | V17         | LED0            | D7          | NC            | U17         |
| EN_CLK25_OUT/<br>CLK25_OUT | U13         | GPHY2_RDAC       | Y17         | LED1            | D8          | NC            | V7          |
| EN_CLK50_OUT/<br>CLK50_OUT | Y13         | HW_FWDG_EN       | U8          | LED10           | C16         | NC            | W9          |
| ENFDXFLOW                  | W8          | IMP_COL          | D3          | LED11           | A15         | NC            | W16         |
| ENHDXFLOW                  | Y9          | IMP_CRS          | D4          | LED12           | D12         | OSC_XTAL_SEL  | Y16         |
|                            |             | IMP_DUMB_FWDG_EN | U7          | LED13           | C12         | OVDD2         | F10         |

| <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> |
|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|
| OVDD                 | C4                 | TDI                  | W11                | TRST                 | V9                 |
| OVDD                 | C6                 | TDO                  | Y11                | XTALI                | L19                |
| OVDD                 | C8                 | TMS                  | W12                | XTALO                | L20                |
| OVDD                 | D5                 | TRD[0]-{0}           | E2                 |                      |                    |
| OVDD2                | C11                | TRD[0]-{1}           | J2                 |                      |                    |
| OVDD2                | E8                 | TRD[0]-{2}           | N2                 |                      |                    |
| OVDD2                | E12                | TRD[0]-{3}           | U2                 |                      |                    |
| OVDD2                | E13                | TRD[0]-{4}           | Y19                |                      |                    |
| OVDD2                | R16                | TRD[0]+{0}           | E1                 |                      |                    |
| OVDD2                | V8                 | TRD[0]+{1}           | J1                 |                      |                    |
| OVDD2                | V11                | TRD[0]+{2}           | N1                 |                      |                    |
| OVDD2                | W7                 | TRD[0]+{3}           | U1                 |                      |                    |
| OVDD2                | W13                | TRD[0]+{4}           | Y20                |                      |                    |
| OVDD3                | E18                | TRD[1]-{0}           | F2                 |                      |                    |
| OVDD3                | E20                | TRD[1]-{1}           | K2                 |                      |                    |
| OVDD3                | F17                | TRD[1]-{2}           | P2                 |                      |                    |
| OVDD3                | F20                | TRD[1]-{3}           | V2                 |                      |                    |
| PLL_AVDD             | M17                | TRD[1]-{4}           | W19                |                      |                    |
| PLL_AVDD             | P17                | TRD[1]+{0}           | F1                 |                      |                    |
| PLL_AVSS             | N17                | TRD[1]+{1}           | K1                 |                      |                    |
| RESET                | Y7                 | TRD[1]+{2}           | P1                 |                      |                    |
| SCK                  | A17                | TRD[1]+{3}           | V1                 |                      |                    |
| SD                   | D16                | TRD[1]+{4}           | W20                |                      |                    |
| SD_PLLAVDD           | K19                | TRD[2]-{0}           | G2                 |                      |                    |
| SD_PLLAVDD           | M16                | TRD[2]-{1}           | L2                 |                      |                    |
| SD_PLLAVDD33         | M18                | TRD[2]-{2}           | R2                 |                      |                    |
| SD_PLLAVSS           | K20                | TRD[2]-{3}           | W2                 |                      |                    |
| SD_PLLAVSS           | P16                | TRD[2]-{4}           | V19                |                      |                    |
| SDVDD                | M19                | TRD[2]+{0}           | G1                 |                      |                    |
| SDVDD                | P19                | TRD[2]+{1}           | L1                 |                      |                    |
| SDVDD                | T19                | TRD[2]+{2}           | R1                 |                      |                    |
| SDVSS                | M20                | TRD[2]+{3}           | W1                 |                      |                    |
| SDVSS                | N18                | TRD[2]+{4}           | V20                |                      |                    |
| SDVSS                | P18                | TRD[3]-{0}           | H2                 |                      |                    |
| SDVSS                | P20                | TRD[3]-{1}           | M2                 |                      |                    |
| SDVSS                | R18                | TRD[3]-{2}           | T2                 |                      |                    |
| SDVSS                | T20                | TRD[3]-{3}           | Y2                 |                      |                    |
| SGRX-                | R19                | TRD[3]-{4}           | U19                |                      |                    |
| SGRX+                | R20                | TRD[3]+{0}           | H1                 |                      |                    |
| SGTX-                | N19                | TRD[3]+{1}           | M1                 |                      |                    |
| SGTX+                | N20                | TRD[3]+{2}           | T1                 |                      |                    |
| SS                   | B18                | TRD[3]+{3}           | Y1                 |                      |                    |
| TCK                  | V12                | TRD[3]+{4}           | U20                |                      |                    |

## BCM53115SKFB Pin List by Ball Number

**Table 34: BCM53115SKFB Pin List by Ball Number**

| <b>Ball</b> | <b>Signal</b> | <b>Ball</b> | <b>Signal</b>   | <b>Ball</b> | <b>Signal</b> | <b>Ball</b> | <b>Signal</b>   |
|-------------|---------------|-------------|-----------------|-------------|---------------|-------------|-----------------|
| A1          | IMP_RXD5      | B9          | IMP_TXD6        | D8          | LED1          | F7          | DVDD            |
| A10         | IMP_TXD7      | C1          | IMP_RXD6        | D9          | LED2          | F8          | DVSS            |
| A11         | IMP_SPD_SELO  | C10         | IMP_PAUSECAP_TX | E1          | TRD[0]+{0}    | F9          | ACT_LOOP_DETECT |
| A12         | IMP_SPD_SEL1  | C11         | OVDD2           | E10         | LOOP_DETECTED | G1          | TRD[2]+{0}      |
| A13         | LED3          | C12         | LED13           | E11         | LED6          | G10         | NC              |
| A14         | LED4          | C13         | LED14           | E12         | OVDD2         | G11         | DVSS            |
| A15         | LED11         | C14         | LED19           | E13         | OVDD2         | G12         | DVSS            |
| A16         | MDC           | C15         | DVSS            | E14         | DVDD          | G13         | DVSS            |
| A17         | SCK           | C16         | LED10           | E15         | DVDD          | G14         | DVSS            |
| A18         | MOSI          | C17         | GMII_TXD0       | E16         | DVDD          | G15         | DVSS            |
| A19         | LEDCLK        | C18         | GMII_TXD3       | E17         | GMII_TXD2     | G16         | DVSS            |
| A2          | IMP_RXD3      | C19         | GMII_TXD6       | E18         | OVDD3         | G17         | GMII_COL        |
| A20         | LEDDATA       | C2          | IMP_RXD2        | E19         | DVSS          | G18         | DVSS            |
| A3          | IMP_RXD1      | C20         | GMII_TXEN       | E2          | TRD[0]-{0}    | G19         | GMII_RXD7       |
| A4          | IMP_RXDV      | C3          | IMP_RXD0        | E20         | OVDD3         | G2          | TRD[2]-{0}      |
| A5          | IMP_TXEN      | C4          | OVDD            | E3          | AVSS          | G20         | GMII_RXCLK      |
| A6          | IMP_TXD0      | C5          | IMP_GTXCLK      | E4          | AVDDL         | G3          | AVSS            |
| A7          | IMP_TXD1      | C6          | OVDD            | E5          | IMP_RXER      | G4          | AVDDL           |
| A8          | IMP_TXD4      | C7          | IMP_TXD3        | E6          | DVDD          | G5          | DVSS            |
| A9          | IMP_TXD5      | C8          | OVDD            | E7          | IMP_VOL_REF   | G6          | DVSS            |
| B1          | IMP_RXD7      | C9          | INT             | E8          | OVDD2         | G7          | DVSS            |
| B10         | IMP_DUPLEX    | D1          | AVDDH           | E9          | IMP_LINK      | G8          | DVSS            |
| B11         | LED8          | D10         | LED5            | F1          | TRD[1]+{0}    | G9          | DVDD            |
| B12         | DVSS          | D11         | LED7            | F10         | OVDD2         | H1          | TRD[3]+{0}      |
| B13         | LED15         | D12         | LED12           | F11         | DVDD          | H10         | DVSS            |
| B14         | LED9          | D13         | IMP_PAUSECAP_RX | F12         | DVDD          | H11         | DVSS            |
| B15         | LED17         | D14         | LED18           | F13         | DVDD          | H12         | DVSS            |
| B16         | MDIO          | D15         | LED16           | F14         | DVSS          | H13         | DVSS            |
| B17         | MISO          | D16         | SD              | F15         | DVSS          | H14         | DVSS            |
| B18         | SS            | D17         | GMII_TXD1       | F16         | GMII_VOL_REF  | H15         | DVSS            |
| B19         | GMII_TXD5     | D18         | GMII_TXD4       | F17         | OVDD3         | H16         | DVDD            |
| B2          | IMP_RXD4      | D19         | GMII_TXD7       | F18         | GMII_TXCLK    | H17         | GMII_RXD6       |
| B20         | GMII_TXER     | D2          | AVSS            | F19         | GMII_GTXCLK   | H18         | GMII_RXD5       |
| B3          | DVSS          | D20         | DVDD            | F2          | TRD[1]-{0}    | H19         | GMII_RXD4       |
| B4          | IMP_RXCLK     | D3          | IMP_COL         | F20         | OVDD3         | H2          | TRD[3]-{0}      |
| B5          | DVSS          | D4          | IMP_CRS         | F3          | AVSS          | H20         | GMII_RXD3       |
| B6          | IMP_TXCLK     | D5          | OVDD            | F4          | AVDDH         | H3          | AVSS            |
| B7          | DVSS          | D6          | IMP_TXER        | F5          | DVDD          | H4          | AVDDH           |
| B8          | IMP_TXD2      | D7          | LED0            | F6          | DVSS          | H5          | DVSS            |

| <i><b>Ball Signal</b></i> | <i><b>Ball Signal</b></i> | <i><b>Ball Signal</b></i> | <i><b>Ball Signal</b></i>      |
|---------------------------|---------------------------|---------------------------|--------------------------------|
| H6 DVSS                   | K9 DVSS                   | N11 DVSS                  | R14 DVSS                       |
| H7 DVSS                   | L1 TRD[2]+{1}             | N12 DVSS                  | R15 IMP_VOL_SEL1               |
| H8 DVSS                   | L10 DVSS                  | N13 DVSS                  | R16 OVDD2                      |
| H9 DVSS                   | L11 DVSS                  | N14 DVSS                  | R17 AVDDH                      |
| J1 TRD[0]+{1}             | L12 DVSS                  | N15 DVSS                  | R18 SDVSS                      |
| J10 DVSS                  | L13 DVSS                  | N16 NC                    | R19 SGRX-                      |
| J11 DVSS                  | L14 DVSS                  | N17 PLL_AVSS              | R2 TRD[2]-{2}                  |
| J12 DVSS                  | L15 DVSS                  | N18 SDVSS                 | R20 SGRX+                      |
| J13 DVSS                  | L16 DVSS                  | N19 SGTX-                 | R3 AVSS                        |
| J14 DVSS                  | L17 GMII_RXDV             | N2 TRD[0]-{2}             | R4 AVDDH                       |
| J15 DVSS                  | L18 DVDD                  | N20 SGTX+                 | R5 DVSS                        |
| J16 DVSS                  | L19 XTALI                 | N3 AVSS                   | R6 NC                          |
| J17 GMII_CRS              | L2 TRD[2]-{1}             | N4 GPHY1_BVDD             | R7 DVSS                        |
| J18 GMII_RXD2             | L20 XTALO                 | N5 DVSS                   | R8 DVSS                        |
| J19 GMII_RXD1             | L3 AVSS                   | N6 DVSS                   | R9 DVSS                        |
| J2 TRD[0]-{1}             | L4 NC                     | N7 DVSS                   | T1 TRD[3]+{2}                  |
| J20 GMII_RXD0             | L5 DVSS                   | N8 DVSS                   | T10 NC                         |
| J3 AVSS                   | L6 DVSS                   | N9 DVSS                   | T11 NC                         |
| J4 AVDDL                  | L7 DVSS                   | P1 TRD[1]+{2}             | T12 IMP_TXC_DELAY              |
| J5 DVSS                   | L8 DVSS                   | P10 DVSS                  | T13 IMP_MODE1                  |
| J6 DVSS                   | L9 DVSS                   | P11 DVSS                  | T14 IMP_VOL_SELO               |
| J7 DVSS                   | M1 TRD[3]+{1}             | P12 DVSS                  | T15 GMII_TXC_DELAY             |
| J8 DVSS                   | M10 DVSS                  | P13 DVSS                  | T16 AVDDH                      |
| J9 DVSS                   | M11 DVSS                  | P14 DVSS                  | T17 AVDDL                      |
| K1 TRD[1]+{1}             | M12 DVSS                  | P15 DVSS                  | T18 AVDDH                      |
| K10 DVSS                  | M13 DVSS                  | P16 SD_PLLAVSS            | T19 SDVDD                      |
| K11 DVSS                  | M14 DVSS                  | P17 PLL_AVDD              | T2 TRD[3]-{2}                  |
| K12 DVSS                  | M15 DVSS                  | P18 SDVSS                 | T20 SDVSS                      |
| K13 DVSS                  | M16 SD_PLLAVDD            | P19 SDVDD                 | T3 AVSS                        |
| K14 DVSS                  | M17 PLL_AVDD              | P2 TRD[1]-{2}             | T4 AVDDL                       |
| K15 DVSS                  | M18 SD_PLLAVDD33          | P20 SDVSS                 | T5 DVSS                        |
| K16 NC                    | M19 SDVDD                 | P3 AVSS                   | T6 CLK_FREQ1                   |
| K17 GMII_RXER             | M2 TRD[3]-{1}             | P4 GPHY1_RDAC             | T7 NC                          |
| K18 DVSS                  | M20 SDVSS                 | P5 DVSS                   | T8 DVDD                        |
| K19 SD_PLLAVDD            | M3 AVSS                   | P6 DVSS                   | T9 NC                          |
| K2 TRD[1]-{1}             | M4 GPHY1_PLLVDD           | P7 DVSS                   | U1 TRD[0]+{3}                  |
| K20 SD_PLLAVSS            | M5 DVSS                   | P8 DVSS                   | U10 DVSS                       |
| K3 AVSS                   | M6 DVSS                   | P9 DVSS                   | U11 IMP_RXC_DELAY              |
| K4 AVDDH                  | M7 DVSS                   | R1 TRD[2]+{2}             | U12 DVSS                       |
| K5 DVSS                   | M8 DVSS                   | R10 DVDD                  | U13 EN_CLK25_OUT/<br>CLK25_OUT |
| K6 DVSS                   | M9 DVSS                   | R11 DVSS                  | U14 NC                         |
| K7 DVSS                   | N1 TRD[0]+{2}             | R12 DVDD                  | U15 DVSS                       |
| K8 DVSS                   | N10 DVSS                  | R13 DVSS                  |                                |

| <b>Ball</b> | <b>Signal</b>    | <b>Ball</b> | <b>Signal</b>              |
|-------------|------------------|-------------|----------------------------|
| U16         | NC               | W19         | TRD[1]-{4}                 |
| U17         | NC               | W2          | TRD[2]-{3}                 |
| U18         | AVDDL            | W20         | TRD[1]+{4}                 |
| U19         | TRD[3]-{4}       | W3          | AVSS                       |
| U2          | TRD[0]-{3}       | W4          | AVDDH                      |
| U20         | TRD[3]+{4}       | W5          | LEDMODE0                   |
| U3          | AVSS             | W6          | EEPROM_TYPE1               |
| U4          | AVDDH            | W7          | OVDD2                      |
| U5          | CLK_FREQ0        | W8          | ENFDXFLOW                  |
| U6          | EEPROM_TYPE0     | W9          | NC                         |
| U7          | IMP_DUMB_FWDG_EN | Y1          | TRD[3]+{3}                 |
| U8          | HW_FWDG_EN       | Y10         | DVSS                       |
| U9          | NC               | Y11         | TDO                        |
| V1          | TRD[1]+{3}       | Y12         | DVSS                       |
| V10         | BC_SUPP_EN       | Y13         | EN_CLK50_OUT/<br>CLK50_OUT |
| V11         | OVDD2            | Y14         | IMP_MODE0                  |
| V12         | TCK              | Y15         | LOOP_DET_EN                |
| V13         | GMII_VOL_SEL1    | Y16         | OSC_XTAL_SEL               |
| V14         | GMII_MODE0       | Y17         | GPHY2_RDAC                 |
| V15         | GMII_MODE1       | Y18         | AVDDH                      |
| V16         | GMII_RXC_DELAY   | Y19         | TRD[0]-{4}                 |
| V17         | GPHY2_PLLVDD     | Y2          | TRD[3]-{3}                 |
| V18         | AVSS             | Y20         | TRD[0]+{4}                 |
| V19         | TRD[2]-{4}       | Y3          | AVSS                       |
| V2          | TRD[1]-{3}       | Y4          | AVDDL                      |
| V20         | TRD[2]+{4}       | Y5          | LEDMODE1                   |
| V3          | AVSS             | Y6          | DVDD                       |
| V4          | AVDDL            | Y7          | RESET                      |
| V5          | DIS_IMP          | Y8          | GMII_CTRL                  |
| V6          | DVSS             | Y9          | ENHDXFLOW                  |
| V7          | NC               |             |                            |
| V8          | OVDD2            |             |                            |
| V9          | TRST             |             |                            |
| W1          | TRD[2]+{3}       |             |                            |
| W10         | CPU_EEPROM_SEL   |             |                            |
| W11         | TDI              |             |                            |
| W12         | TMS              |             |                            |
| W13         | OVDD2            |             |                            |
| W14         | GMII_VOL_SEL0    |             |                            |
| W15         | LOOP_IMP_SEL     |             |                            |
| W16         | NC               |             |                            |
| W17         | GPHY2_BVDD       |             |                            |
| W18         | AVSS             |             |                            |

## BCM53115SIPB Pin List by Signal Name

*Table 35: BCM53115SIPB Pin List by Signal Name*

| <i>Signal</i>   | <i>Ball</i> | <i>Signal</i>  | <i>Ball</i> | <i>Signal</i> | <i>Ball</i> | <i>Signal</i> | <i>Ball</i> |
|-----------------|-------------|----------------|-------------|---------------|-------------|---------------|-------------|
| ACT_LOOP_DETECT | D8          | AVSS           | AB20        | DVSS          | F5          | DVSS          | H15         |
| AVDDH           | H4          | BC_SUPP_EN     | AA11        | DVSS          | F6          | DVSS          | H16         |
| AVDDH           | K4          | CLK_FREQ0      | W6          | DVSS          | F7          | DVSS          | H17         |
| AVDDH           | M4          | CLK_FREQ1      | Y7          | DVSS          | F8          | DVSS          | J5          |
| SDVSS           | T20         | CPU_EEPROM_SEL | AB10        | DVSS          | F9          | DVSS          | J6          |
| AVDDH           | U4          | DIS_IMP        | Y5          | DVSS          | F10         | DVSS          | J7          |
| AVDDH           | V20         | DVDD           | E4          | DVSS          | F11         | DVSS          | J8          |
| AVDDH           | V21         | DVDD           | E6          | DVSS          | F12         | DVSS          | J9          |
| AVDDH           | W4          | DVDD           | E11         | DVSS          | F13         | DVSS          | J10         |
| AVDDH           | AA4         | DVDD           | E12         | DVSS          | F14         | DVSS          | J11         |
| AVDDL           | G4          | DVDD           | E13         | DVSS          | F15         | DVSS          | J12         |
| AVDDL           | J4          | DVDD           | E14         | DVSS          | F16         | DVSS          | J13         |
| AVDDL           | L4          | DVDD           | E15         | DVSS          | F17         | DVSS          | J14         |
| AVDDL           | V4          | DVDD           | E16         | DVSS          | F21         | DVSS          | J15         |
| AVDDL           | W20         | DVDD           | E17         | DVSS          | G5          | DVSS          | J16         |
| AVDDL           | Y4          | DVDD           | E18         | DVSS          | G6          | DVSS          | J17         |
| AVDDL           | Y20         | DVDD           | E22         | DVSS          | G7          | DVSS          | K5          |
| AVDDL           | AB4         | DVDD           | H18         | DVSS          | G8          | DVSS          | K6          |
| AVSS            | F1          | DVDD           | J18         | DVSS          | G9          | DVSS          | K7          |
| AVSS            | F2          | DVDD           | L20         | DVSS          | G10         | DVSS          | K8          |
| AVSS            | G3          | DVDD           | V9          | DVSS          | G11         | DVSS          | K9          |
| AVSS            | H3          | DVDD           | V10         | DVSS          | G12         | DVSS          | K10         |
| AVSS            | J3          | DVDD           | V13         | DVSS          | G13         | DVSS          | K11         |
| AVSS            | K3          | DVDD           | V14         | DVSS          | G14         | DVSS          | K12         |
| AVSS            | L3          | DVDD           | V17         | DVSS          | G15         | DVSS          | K13         |
| AVSS            | M3          | DVDD           | AB6         | DVSS          | G16         | DVSS          | K14         |
| AVSS            | N3          | DVSS           | A20         | DVSS          | G17         | DVSS          | K15         |
| AVSS            | P3          | DVSS           | B3          | DVSS          | G18         | DVSS          | K16         |
| AVSS            | R3          | DVSS           | B5          | DVSS          | G20         | DVSS          | K17         |
| AVSS            | T3          | DVSS           | B7          | DVSS          | H5          | DVSS          | K18         |
| AVSS            | U3          | DVSS           | B12         | DVSS          | H6          | DVSS          | L5          |
| AVSS            | U20         | DVSS           | C17         | DVSS          | H7          | DVSS          | L6          |
| AVSS            | V3          | DVSS           | D2          | DVSS          | H8          | DVSS          | L7          |
| AVSS            | V22         | DVSS           | D14         | DVSS          | H9          | DVSS          | L8          |
| AVSS            | W3          | DVSS           | D15         | DVSS          | H10         | DVSS          | L9          |
| AVSS            | Y3          | DVSS           | E2          | DVSS          | H11         | DVSS          | L10         |
| AVSS            | AA3         | DVSS           | E3          | DVSS          | H12         | DVSS          | L11         |
| AVSS            | AA20        | DVSS           | F3          | DVSS          | H13         | DVSS          | L12         |
| AVSS            | AB3         | DVSS           | F4          | DVSS          | H14         | DVSS          | L13         |

| <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i>       | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> |
|----------------------|--------------------|----------------------|--------------------|----------------------------|--------------------|----------------------|--------------------|
| DVSS                 | L14                | DVSS                 | P17                | DVSS                       | U17                | GMII_TXD1            | D19                |
| DVSS                 | L15                | DVSS                 | R5                 | DVSS                       | U18                | GMII_TXD2            | D20                |
| DVSS                 | L16                | DVSS                 | R6                 | DVSS                       | V5                 | GMII_TXD3            | C20                |
| DVSS                 | L17                | DVSS                 | R7                 | DVSS                       | V7                 | GMII_TXD4            | C21                |
| DVSS                 | M5                 | DVSS                 | R8                 | DVSS                       | V11                | GMII_TXD5            | D21                |
| DVSS                 | M6                 | DVSS                 | R9                 | DVSS                       | V12                | GMII_TXD6            | H20                |
| DVSS                 | M7                 | DVSS                 | R10                | DVSS                       | V15                | GMII_TXD7            | E21                |
| DVSS                 | M8                 | DVSS                 | R11                | DVSS                       | V16                | GMII_TXEN            | D22                |
| DVSS                 | M9                 | DVSS                 | R12                | DVSS                       | W13                | GMII_TXER            | C22                |
| DVSS                 | M10                | DVSS                 | R13                | DVSS                       | Y6                 | GMII_VOL_REF         | F18                |
| DVSS                 | M11                | DVSS                 | R14                | DVSS                       | Y11                | GMII_VOL_SELO        | AB16               |
| DVSS                 | M12                | DVSS                 | R15                | DVSS                       | Y15                | GMII_VOL_SEL1        | AA15               |
| DVSS                 | M13                | DVSS                 | R16                | DVSS                       | AA8                | GPHY1_BAVDD          | R4                 |
| DVSS                 | M14                | DVSS                 | R17                | DVSS                       | AA17               | GPHY1_PLLVDD         | P4                 |
| DVSS                 | M15                | DVSS                 | R18                | DVSS                       | AB13               | GPHY1_RDAC           | T4                 |
| DVSS                 | M16                | DVSS                 | R19                | EEPROM_TYPE0               | W7                 | NC                   | AA19               |
| DVSS                 | M17                | DVSS                 | T5                 | EEPROM_TYPE1               | AB8                | AVDDH                | Y19                |
| PLL_AVSS             | M18                | DVSS                 | T6                 | EN_CLK25_OUT/<br>CLK25_OUT | Y14                | NC                   | AB19               |
| DVSS                 | N5                 | DVSS                 | T7                 | EN_CLK50_OUT/<br>CLK50_OUT | AB14               | HW_FWDG_EN           | W10                |
| DVSS                 | N6                 | DVSS                 | T8                 | ENFDXFLOW                  | Y8                 | IMP_COL              | D3                 |
| DVSS                 | N7                 | DVSS                 | T9                 | ENHDXFLOW                  | AB9                | IMP_CRS              | D4                 |
| DVSS                 | N8                 | DVSS                 | T10                | GMII_COL                   | E19                | IMP_DUMB_FWDG_EN     | V8                 |
| DVSS                 | N9                 | DVSS                 | T11                | GMII_CRS                   | H19                | IMP_DUPLEX           | C9                 |
| DVSS                 | N10                | DVSS                 | T12                | GMII_CTRL                  | AA6                | IMP_GTXCLK           | C5                 |
| DVSS                 | N11                | DVSS                 | T13                | GMII_GTXCLK                | G21                | IMP_LINK             | D10                |
| DVSS                 | N12                | DVSS                 | T14                | GMII_MODE0                 | AA16               | IMP_MODE0            | AB15               |
| DVSS                 | N13                | DVSS                 | T15                | GMII_MODE1                 | Y16                | IMP_MODE1            | W15                |
| DVSS                 | N14                | DVSS                 | T16                | GMII_RXC_DELAY             | Y18                | IMP_PAUSECAP_RX      | C14                |
| DVSS                 | N15                | DVSS                 | T17                | GMII_RXCLK                 | F22                | IMP_PAUSECAP_TX      | B10                |
| DVSS                 | N16                | DVSS                 | T18                | GMII_RXD0                  | K22                | IMP_RXC_DELAY        | Y13                |
| DVSS                 | N17                | GPHY2_PLLVDD         | T19                | GMII_RXD1                  | K21                | IMP_RXCLK            | B4                 |
| DVSS                 | P5                 | DVSS                 | U5                 | GMII_RXD2                  | K20                | IMP_RXD0             | C3                 |
| DVSS                 | P6                 | DVSS                 | U6                 | GMII_RXD3                  | J22                | IMP_RXD1             | A3                 |
| DVSS                 | P7                 | DVSS                 | U7                 | GMII_RXD4                  | J21                | IMP_RXD2             | C2                 |
| DVSS                 | P8                 | DVSS                 | U8                 | GMII_RXD5                  | J20                | IMP_RXD3             | A2                 |
| DVSS                 | P9                 | DVSS                 | U9                 | GMII_RXD6                  | H22                | IMP_RXD4             | B2                 |
| DVSS                 | P10                | DVSS                 | U10                | GMII_RXD7                  | G19                | IMP_RXD5             | A1                 |
| DVSS                 | P11                | DVSS                 | U11                | GMII_RXDV                  | K19                | IMP_RXD6             | C1                 |
| DVSS                 | P12                | DVSS                 | U12                | GMII_RXER                  | J19                | IMP_RXD7             | B1                 |
| DVSS                 | P13                | DVSS                 | U13                | GMII_TXC_DELAY             | Y17                | IMP_RXDV             | A4                 |
| DVSS                 | P14                | DVSS                 | U14                | GMII_TXCLK                 | F20                | IMP_RXER             | E5                 |
| DVSS                 | P15                | DVSS                 | U15                | GMII_TXD0                  | C19                | IMP_SPD_SELO         | A11                |
| DVSS                 | P16                | DVSS                 | U16                |                            |                    | IMP_SPD_SEL1         | A12                |

| <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> |
|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|
| IMP_TXC_DELAY        | W14                | MDC                  | A18                | PLL_AVDD             | N19                | TRD[1]-{4}           | AA21               |
| IMP_TXCLK            | B6                 | MDIO                 | B18                | PLL_AVSS             | L19                | TRD[1]+{0}           | H1                 |
| IMP_TXD0             | A6                 | MISO                 | B20                | RESET                | AB7                | TRD[1]+{1}           | M1                 |
| IMP_TXD1             | A7                 | MOSI                 | A21                | RESET                | AB7                | TRD[1]+{2}           | T1                 |
| IMP_TXD2             | B8                 | NC                   | V6                 | SCK                  | A19                | TRD[1]+{3}           | Y1                 |
| IMP_TXD3             | C7                 | NC                   | W11                | SD                   | D18                | TRD[1]+{4}           | AA22               |
| IMP_TXD4             | A8                 | NC                   | W9                 | SD_PLLAVDD           | L21                | TRD[2]-{0}           | J2                 |
| IMP_TXD5             | A9                 | NC                   | W8                 | SD_PLLAVDD           | P19                | TRD[2]-{1}           | N2                 |
| IMP_TXD6             | B9                 | NC                   | W12                | SD_PLLAVDD33         | M20                | TRD[2]-{2}           | U2                 |
| IMP_TXD7             | A10                | GPHY2_BVDD           | U19                | SD_PLLAVSS           | L22                | TRD[2]-{3}           | AA2                |
| IMP_TXEN             | A5                 | NC                   | AA10               | SD_PLLAVSS           | N18                | TRD[2]-{4}           | Y21                |
| IMP_TXER             | D6                 | NC                   | V19                | SDVDD                | N21                | TRD[2]+{0}           | J1                 |
| IMP_VOL_REF          | E7                 | NC                   | L18                | SDVDD                | R21                | TRD[2]+{1}           | N1                 |
| IMP_VOL_SELO         | W16                | NC                   | E10                | SDVDD                | U21                | TRD[2]+{2}           | U1                 |
| IMP_VOL_SEL1         | W17                | NC                   | N4                 | SDVSS                | N20                | TRD[2]+{3}           | AA1                |
| INT                  | D7                 | GPHY2_RDAC           | W19                | SDVSS                | N22                | TRD[2]+{4}           | Y22                |
| LED0                 | D11                | NC                   | P18                | SDVSS                | P20                | TRD[3]-{0}           | K2                 |
| LED1                 | D12                | NC                   | W5                 | SDVSS                | R20                | TRD[3]-{1}           | P2                 |
| LED10                | C18                | NC                   | AA18               | SDVSS                | R22                | TRD[3]-{2}           | V2                 |
| LED11                | A17                | NC                   | AA9                | SDVSS                | U22                | TRD[3]-{3}           | AB2                |
| LED12                | A14                | OSC_XTAL_SEL         | AB18               | SGRX-                | T22                | TRD[3]-{4}           | W21                |
| LED13                | A13                | OVDD2                | C10                | SGRX+                | T21                | TRD[3]+{0}           | K1                 |
| LED14                | B14                | OVDD                 | C4                 | SGTX-                | P21                | TRD[3]+{1}           | P1                 |
| LED15                | B15                | OVDD                 | C6                 | SGTX+                | P22                | TRD[3]+{2}           | V1                 |
| LED16                | D17                | OVDD                 | C8                 | SS                   | B21                | TRD[3]+{3}           | AB1                |
| LED17                | B17                | OVDD                 | D1                 | TCK                  | Y12                | TRD[3]+{4}           | W22                |
| LED18                | C15                | OVDD                 | D5                 | TDI                  | AB12               | TRST                 | Y10                |
| LED19                | C16                | OVDD                 | E1                 | TDO                  | AB11               | XTALI                | M21                |
| LED2                 | D13                | OVDD2                | B19                | TMS                  | AA13               | XTALO                | M22                |
| LED3                 | A15                | OVDD2                | C11                | TRD[0]-{0}           | G2                 |                      |                    |
| LED4                 | A16                | OVDD2                | D16                | TRD[0]-{1}           | L2                 |                      |                    |
| LED5                 | C12                | OVDD2                | E8                 | TRD[0]-{2}           | R2                 |                      |                    |
| LED6                 | C13                | OVDD2                | E9                 | TRD[0]-{3}           | W2                 |                      |                    |
| LED7                 | B13                | OVDD2                | V18                | TRD[0]-{4}           | AB21               |                      |                    |
| LED8                 | B11                | OVDD2                | Y9                 | TRD[0]+{0}           | G1                 |                      |                    |
| LED9                 | B16                | OVDD2                | AA7                | TRD[0]+{1}           | L1                 |                      |                    |
| LEDCLK               | A22                | OVDD2                | AA12               | TRD[0]+{2}           | R1                 |                      |                    |
| LEDDATA              | B22                | OVDD2                | AA14               | TRD[0]+{3}           | W1                 |                      |                    |
| LEDMODE0             | AA5                | OVDD3                | E20                | TRD[0]+{4}           | AB22               |                      |                    |
| LEDMODE1             | AB5                | OVDD3                | F19                | TRD[1]-{0}           | H2                 |                      |                    |
| LOOP_DET_EN          | AB17               | OVDD3                | G22                | TRD[1]-{1}           | M2                 |                      |                    |
| LOOP_DETECTED        | D9                 | OVDD3                | H21                | TRD[1]-{2}           | T2                 |                      |                    |
| LOOP_IMP_SEL         | W18                | PLL_AVDD             | M19                | TRD[1]-{3}           | Y2                 |                      |                    |

## BCM53115SIPB Pin List by Ball Number

**Table 36: BCM53115SIPB Pin List by Ball Number**

| <b>Signal</b> | <b>Ball</b> | <b>Signal</b>              | <b>Ball</b> | <b>Signal</b>   | <b>Ball</b> | <b>Signal</b>   | <b>Ball</b> |
|---------------|-------------|----------------------------|-------------|-----------------|-------------|-----------------|-------------|
| IMP_RXD5      | A1          | LEDMODE0                   | AA5         | IMP_RXD4        | B2          | DVSS            | D15         |
| IMP_TXD7      | A10         | GMII_CTRL                  | AA6         | MISO            | B20         | OVDD2           | D16         |
| IMP_SPD_SELO  | A11         | OVDD2                      | AA7         | SS              | B21         | LED16           | D17         |
| IMP_SPD_SEL1  | A12         | DVSS                       | AA8         | LEDDATA         | B22         | SD              | D18         |
| LED13         | A13         | NC                         | AA9         | DVSS            | B3          | GMII_TXD1       | D19         |
| LED12         | A14         | TRD[3]+{3}                 | AB1         | IMP_RXCLK       | B4          | DVSS            | D2          |
| LED3          | A15         | CPU_EEPROM_SEL             | AB10        | DVSS            | B5          | GMII_TXD2       | D20         |
| LED4          | A16         | TDO                        | AB11        | IMP_TXCLK       | B6          | GMII_TXD5       | D21         |
| LED11         | A17         | TDI                        | AB12        | DVSS            | B7          | GMII_TXEN       | D22         |
| MDC           | A18         | DVSS                       | AB13        | IMP_TXD2        | B8          | IMP_COL         | D3          |
| SCK           | A19         | EN_CLK50_OUT/<br>CLK50_OUT | AB14        | IMP_TXD6        | B9          | IMP_CRS         | D4          |
| IMP_RXD3      | A2          | IMP_MODE0                  | AB15        | IMP_RXD6        | C1          | OVDD            | D5          |
| DVSS          | A20         | GMII_VOL_SELO              | AB16        | OVDD2           | C10         | IMP_TXER        | D6          |
| MOSI          | A21         | LOOP_DET_EN                | AB17        | OVDD2           | C11         | INT             | D7          |
| LEDCLK        | A22         | OSC_XTAL_SEL               | AB18        | LED5            | C12         | ACT_LOOP_DETECT | D8          |
| IMP_RXD1      | A3          | NC                         | AB19        | LED6            | C13         | LOOP_DETECTED   | D9          |
| IMP_RXDV      | A4          | TRD[3]–{3}                 | AB2         | IMP_PAUSECAP_RX | C14         | OVDD            | E1          |
| IMP_TXEN      | A5          | AVSS                       | AB20        | LED18           | C15         | NC              | E10         |
| IMP_TXD0      | A6          | TRD[0]–{4}                 | AB21        | LED19           | C16         | DVDD            | E11         |
| IMP_TXD1      | A7          | TRD[0]+{4}                 | AB22        | DVSS            | C17         | DVDD            | E12         |
| IMP_TXD4      | A8          | AVSS                       | AB3         | LED10           | C18         | DVDD            | E13         |
| IMP_TXD5      | A9          | AVDDL                      | AB4         | GMII_TXD0       | C19         | DVDD            | E14         |
| TRD[2]+{3}    | AA1         | LEDMODE1                   | AB5         | IMP_RXD2        | C2          | DVDD            | E15         |
| NC            | AA10        | DVDD                       | AB6         | GMII_TXD3       | C20         | DVDD            | E16         |
| BC_SUPP_EN    | AA11        | RESET                      | AB7         | GMII_TXD4       | C21         | DVDD            | E17         |
| OVDD2         | AA12        | EEPROM_TYPE1               | AB8         | GMII_TXER       | C22         | DVDD            | E18         |
| TMS           | AA13        | ENHDXFLOW                  | AB9         | IMP_RXD0        | C3          | GMII_COL        | E19         |
| OVDD2         | AA14        | IMP_RXD7                   | B1          | OVDD            | C4          | DVSS            | E2          |
| GMII_VOL_SEL1 | AA15        | IMP_PAUSECAP_TX            | B10         | IMP_GTXCLK      | C5          | OVDD3           | E20         |
| GMII_MODE0    | AA16        | LED8                       | B11         | OVDD            | C6          | GMII_TXD7       | E21         |
| DVSS          | AA17        | DVSS                       | B12         | IMP_TXD3        | C7          | DVDD            | E22         |
| NC            | AA18        | LED7                       | B13         | OVDD            | C8          | DVSS            | E3          |
| NC            | AA19        | LED14                      | B14         | IMP_DUPLEX      | C9          | DVDD            | E4          |
| TRD[2]–{3}    | AA2         | LED15                      | B15         | OVDD            | D1          | IMP_RXER        | E5          |
| AVSS          | AA20        | LED9                       | B16         | IMP_LINK        | D10         | DVDD            | E6          |
| TRD[1]–{4}    | AA21        | LED17                      | B17         | LED0            | D11         | IMP_VOL_REF     | E7          |
| TRD[1]+{4}    | AA22        | MDIO                       | B18         | LED1            | D12         | OVDD2           | E8          |
| AVSS          | AA3         | OVDD2                      | B19         | LED2            | D13         | OVDD2           | E9          |
| AVDDH         | AA4         |                            |             | DVSS            | D14         | AVSS            | F1          |

| <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> |
|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|
| DVSS                 | F10                | TRD[1]+{0}           | H1                 | DVSS                 | J9                 | DVSS                 | L8                 |
| DVSS                 | F11                | DVSS                 | H10                | TRD[3]+{0}           | K1                 | DVSS                 | L9                 |
| DVSS                 | F12                | DVSS                 | H11                | DVSS                 | K10                | TRD[1]+{1}           | M1                 |
| DVSS                 | F13                | DVSS                 | H12                | DVSS                 | K11                | DVSS                 | M10                |
| DVSS                 | F14                | DVSS                 | H13                | DVSS                 | K12                | DVSS                 | M11                |
| DVSS                 | F15                | DVSS                 | H14                | DVSS                 | K13                | DVSS                 | M12                |
| DVSS                 | F16                | DVSS                 | H15                | DVSS                 | K14                | DVSS                 | M13                |
| DVSS                 | F17                | DVSS                 | H16                | DVSS                 | K15                | DVSS                 | M14                |
| GMII_VOL_REF         | F18                | DVSS                 | H17                | DVSS                 | K16                | DVSS                 | M15                |
| OVDD3                | F19                | DVDD                 | H18                | DVSS                 | K17                | DVSS                 | M16                |
| AVSS                 | F2                 | GMII_CRS             | H19                | DVSS                 | K18                | DVSS                 | M17                |
| GMII_TXCLK           | F20                | TRD[1]–{0}           | H2                 | GMII_RXDV            | K19                | PLL_AVSS             | M18                |
| DVSS                 | F21                | GMII_TXD6            | H20                | TRD[3]–{0}           | K2                 | PLL_AVDD             | M19                |
| GMII_RXCLK           | F22                | OVDD3                | H21                | GMII_RXD2            | K20                | TRD[1]–{1}           | M2                 |
| DVSS                 | F3                 | GMII_RXD6            | H22                | GMII_RXD1            | K21                | SD_PLLAVDD33         | M20                |
| DVSS                 | F4                 | AVSS                 | H3                 | GMII_RXD0            | K22                | XTALI                | M21                |
| DVSS                 | F5                 | AVDDH                | H4                 | AVSS                 | K3                 | XTALO                | M22                |
| DVSS                 | F6                 | DVSS                 | H5                 | AVDDH                | K4                 | AVSS                 | M3                 |
| DVSS                 | F7                 | DVSS                 | H6                 | DVSS                 | K5                 | AVDDH                | M4                 |
| DVSS                 | F8                 | DVSS                 | H7                 | DVSS                 | K6                 | DVSS                 | M5                 |
| DVSS                 | F9                 | DVSS                 | H8                 | DVSS                 | K7                 | DVSS                 | M6                 |
| TRD[0]+{0}           | G1                 | DVSS                 | H9                 | DVSS                 | K8                 | DVSS                 | M7                 |
| DVSS                 | G10                | TRD[2]+{0}           | J1                 | DVSS                 | K9                 | DVSS                 | M8                 |
| DVSS                 | G11                | DVSS                 | J10                | TRD[0]+{1}           | L1                 | DVSS                 | M9                 |
| DVSS                 | G12                | DVSS                 | J11                | DVSS                 | L10                | TRD[2]+{1}           | N1                 |
| DVSS                 | G13                | DVSS                 | J12                | DVSS                 | L11                | DVSS                 | N10                |
| DVSS                 | G14                | DVSS                 | J13                | DVSS                 | L12                | DVSS                 | N11                |
| DVSS                 | G15                | DVSS                 | J14                | DVSS                 | L13                | DVSS                 | N12                |
| DVSS                 | G16                | DVSS                 | J15                | DVSS                 | L14                | DVSS                 | N13                |
| DVSS                 | G17                | DVSS                 | J16                | DVSS                 | L15                | DVSS                 | N14                |
| DVSS                 | G18                | DVSS                 | J17                | DVSS                 | L16                | DVSS                 | N15                |
| GMII_RXD7            | G19                | DVDD                 | J18                | DVSS                 | L17                | DVSS                 | N16                |
| TRD[0]–{0}           | G2                 | GMII_RXER            | J19                | NC                   | L18                | DVSS                 | N17                |
| DVSS                 | G20                | TRD[2]–{0}           | J2                 | PLL_AVSS             | L19                | SD_PLLAVSS           | N18                |
| GMII_GTXCLK          | G21                | GMII_RXD5            | J20                | TRD[0]–{1}           | L2                 | PLL_AVDD             | N19                |
| OVDD3                | G22                | GMII_RXD4            | J21                | DVDD                 | L20                | TRD[2]–{1}           | N2                 |
| AVSS                 | G3                 | GMII_RXD3            | J22                | SD_PLLAVDD           | L21                | SDVSS                | N20                |
| AVDDL                | G4                 | AVSS                 | J3                 | SD_PLLAVSS           | L22                | SDVDD                | N21                |
| DVSS                 | G5                 | AVDDL                | J4                 | AVSS                 | L3                 | SDVSS                | N22                |
| DVSS                 | G6                 | DVSS                 | J5                 | AVDDL                | L4                 | AVSS                 | N3                 |
| DVSS                 | G7                 | DVSS                 | J6                 | DVSS                 | L5                 | NC                   | N4                 |
| DVSS                 | G8                 | DVSS                 | J7                 | DVSS                 | L6                 | DVSS                 | N5                 |
| DVSS                 | G9                 | DVSS                 | J8                 | DVSS                 | L7                 | DVSS                 | N6                 |

| <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i> | <i><b>Ball</b></i> | <i><b>Signal</b></i>       | <i><b>Ball</b></i> |
|----------------------|--------------------|----------------------|--------------------|----------------------|--------------------|----------------------------|--------------------|
| DVSS                 | N7                 | DVSS                 | R6                 | DVSS                 | U5                 | AVDDH                      | W4                 |
| DVSS                 | N8                 | DVSS                 | R7                 | DVSS                 | U6                 | NC                         | W5                 |
| DVSS                 | N9                 | DVSS                 | R8                 | DVSS                 | U7                 | CLK_FREQ0                  | W6                 |
| TRD[3]+{1}           | P1                 | DVSS                 | R9                 | DVSS                 | U8                 | EEPROM_TYPE0               | W7                 |
| DVSS                 | P10                | TRD[1]+{2}           | T1                 | DVSS                 | U9                 | NC                         | W8                 |
| DVSS                 | P11                | DVSS                 | T10                | TRD[3]+{2}           | V1                 | NC                         | W9                 |
| DVSS                 | P12                | DVSS                 | T11                | DVDD                 | V10                | TRD[1]+{3}                 | Y1                 |
| DVSS                 | P13                | DVSS                 | T12                | DVSS                 | V11                | TRST                       | Y10                |
| DVSS                 | P14                | DVSS                 | T13                | DVSS                 | V12                | DVSS                       | Y11                |
| DVSS                 | P15                | DVSS                 | T14                | DVDD                 | V13                | TCK                        | Y12                |
| DVSS                 | P16                | DVSS                 | T15                | DVDD                 | V14                | IMP_RXC_DELAY              | Y13                |
| DVSS                 | P17                | DVSS                 | T16                | DVSS                 | V15                | EN_CLK25_OUT/<br>CLK25_OUT | Y14                |
| NC                   | P18                | DVSS                 | T17                | DVSS                 | V16                | DVSS                       | Y15                |
| SD_PLLAVDD           | P19                | DVSS                 | T18                | DVDD                 | V17                | GMII_MODE1                 | Y16                |
| TRD[3]–{1}           | P2                 | GPHY2_PLLVDD         | T19                | OVDD2                | V18                | GMII_TXC_DELAY             | Y17                |
| SDVSS                | P20                | TRD[1]–{2}           | T2                 | NC                   | V19                | GMII_RXC_DELAY             | Y18                |
| SGTX–                | P21                | SDVSS                | T20                | TRD[3]–{2}           | V2                 | AVDDH                      | Y19                |
| SGTX+                | P22                | SGRX+                | T21                | AVDDH                | V20                | TRD[1]–{3}                 | Y2                 |
| AVSS                 | P3                 | SGRX–                | T22                | AVDDH                | V21                | AVDDL                      | Y20                |
| GPHY1_PLLVDD         | P4                 | AVSS                 | T3                 | AVSS                 | V22                | TRD[2]–{4}                 | Y21                |
| DVSS                 | P5                 | GPHY1_RDAC           | T4                 | AVSS                 | V3                 | TRD[2]+{4}                 | Y22                |
| DVSS                 | P6                 | DVSS                 | T5                 | AVDDL                | V4                 | AVSS                       | Y3                 |
| DVSS                 | P7                 | DVSS                 | T6                 | DVSS                 | V5                 | AVDDL                      | Y4                 |
| DVSS                 | P8                 | DVSS                 | T7                 | NC                   | V6                 | DIS_IMP                    | Y5                 |
| DVSS                 | P9                 | DVSS                 | T8                 | DVSS                 | V7                 | DVSS                       | Y6                 |
| TRD[0]+{2}           | R1                 | DVSS                 | T9                 | IMP_DUMB_FWDG_EN     | V8                 | CLK_FREQ1                  | Y7                 |
| DVSS                 | R10                | TRD[2]+{2}           | U1                 | DVDD                 | V9                 | ENFDXFLOW                  | Y8                 |
| DVSS                 | R11                | DVSS                 | U10                | TRD[0]+{3}           | W1                 | OVDD2                      | Y9                 |
| DVSS                 | R12                | DVSS                 | U11                | HW_FWDG_EN           | W10                |                            |                    |
| DVSS                 | R13                | DVSS                 | U12                | NC                   | W11                |                            |                    |
| DVSS                 | R14                | DVSS                 | U13                | NC                   | W12                |                            |                    |
| DVSS                 | R15                | DVSS                 | U14                | DVSS                 | W13                |                            |                    |
| DVSS                 | R16                | DVSS                 | U15                | IMP_TXC_DELAY        | W14                |                            |                    |
| DVSS                 | R17                | DVSS                 | U16                | IMP_MODE1            | W15                |                            |                    |
| DVSS                 | R18                | DVSS                 | U17                | IMP_VOL_SEL0         | W16                |                            |                    |
| DVSS                 | R19                | DVSS                 | U18                | IMP_VOL_SEL1         | W17                |                            |                    |
| TRD[0]–{2}           | R2                 | GPHY2_BVDD           | U19                | LOOP_IMP_SEL         | W18                |                            |                    |
| SDVSS                | R20                | TRD[2]–{2}           | U2                 | GPHY2_RDAC           | W19                |                            |                    |
| SDVDD                | R21                | AVSS                 | U20                | TRD[0]–{3}           | W2                 |                            |                    |
| SDVSS                | R22                | SDVDD                | U21                | AVDDL                | W20                |                            |                    |
| AVSS                 | R3                 | SDVSS                | U22                | TRD[3]–{4}           | W21                |                            |                    |
| GPHY1_BAVDD          | R4                 | AVSS                 | U3                 | TRD[3]+{4}           | W22                |                            |                    |
| DVSS                 | R5                 | AVDDH                | U4                 | AVSS                 | W3                 |                            |                    |

## Section 7: Register Definitions

### Register Definition

BCM53115S register sets can be accessed through the programming interfaces described on [page 91](#). The register space is organized into pages, each containing a certain set of registers. [Table 37](#) lists the pages defined in BCM53115S. To access a page, the page register (0xFF) is written with the page value. The registers contained in the page can then be accessed by their addresses. See [“Programming Interfaces” on page 91](#) for more information.

### Register Notations

In the register description tables, the following notation in the R/W column is used to describe the ability to read or to write:

- R/W = Read or write
- RO = Read only
- LH = Latched high
- LL = Latched low
- H = Fixed high
- L = Fixed low
- SC = Clear on read

Reserved bits must be written as the default value and ignored when read.

### Global Page Register

**Table 37: Global Page Register Map**

| <b>Page</b> | <b>Description</b>                                                     |
|-------------|------------------------------------------------------------------------|
| 00h         | <a href="#">“Page 00h: Control Registers” on page 147</a>              |
| 01h         | <a href="#">“Page 01h: Status Registers” on page 164</a>               |
| 02h         | <a href="#">“Page 02h: Management/Mirroring Registers” on page 168</a> |
| 03h         | Reserved                                                               |
| 04h         | <a href="#">“Page 04h: ARL Control Register” on page 177</a>           |
| 05h         | <a href="#">“Page 05h: ARL/VTBL Access Registers” on page 181</a>      |
| 06h, 07h    | Reserved                                                               |
| 08h         | Reserved                                                               |

**Table 37: Global Page Register Map (Cont.)**

| <b>Page</b>       | <b>Description</b>                                                                        |
|-------------------|-------------------------------------------------------------------------------------------|
| 09h               | Reserved                                                                                  |
| 0Ah               | Reserved                                                                                  |
| 0Bh–0Fh           | Reserved                                                                                  |
| 10h–14h           | <a href="#">“Page 10h–14h: Internal GPHY MII Registers” on page 192</a>                   |
| 15h               | <a href="#">“Page 15h: Internal SerDes Port (Port 5) Register” on page 226</a>            |
| 16h–1Fh           | Reserved                                                                                  |
| 20h–28h           | <a href="#">“Page 20h–28h: Port MIB Registers” on page 246</a>                            |
| 29h–2Fh           | Reserved                                                                                  |
| 30h               | <a href="#">“Page 30h: QoS Registers” on page 250</a>                                     |
| 31h               | <a href="#">“Page 31h: Port-Based VLAN Registers” on page 258</a>                         |
| 32h               | <a href="#">“Page 32h: Trunking Registers” on page 259</a>                                |
| 33h               | Reserved                                                                                  |
| 34h               | <a href="#">“Page 34h: IEEE 802.1Q VLAN Registers” on page 260</a>                        |
| 35h               | Reserved                                                                                  |
| 36h               | <a href="#">“Page 36h: DOS Prevent Register” on page 269</a>                              |
| 37h–3Fh           | Reserved                                                                                  |
| 40h               | <a href="#">“Page 40h: Jumbo Frame Control Register” on page 272</a>                      |
| 41h               | <a href="#">“Page 41h: Broadcast Storm Suppression Register” on page 274</a>              |
| 42h               | <a href="#">“Page 42h: EAP Register” on page 282</a>                                      |
| 43h               | <a href="#">“Page 43h: MSPT Register” on page 286</a>                                     |
| 44h–6Fh           | Reserved                                                                                  |
| 70h               | <a href="#">“Page 70h: MIB Snapshot Control Register” on page 288</a>                     |
| 71h               | <a href="#">“Page 71h: Port Snapshot MIB Control Register” on page 289</a>                |
| 72h               | <a href="#">“Page 72h: Loop Detection Register” on page 289</a>                           |
| 73h–7Fh           | Reserved                                                                                  |
| 80h–83h           | Reserved                                                                                  |
| 84h               | Reserved                                                                                  |
| 85h               | <a href="#">“Page 85h: WAN Interface (Port 5) External PHY MII Registers” on page 292</a> |
| 86h–87h           | Reserved                                                                                  |
| 88h               | <a href="#">“Page 88h: IMP Port External PHY MII Registers Page Summary” on page 292</a>  |
| 90h               | Reserved                                                                                  |
| 91h               | <a href="#">“Page 91h: Traffic Remarking Register” on page 292</a>                        |
| 92h–9Fh           | Reserved                                                                                  |
| A0h               | Reserved                                                                                  |
| A1h               | Reserved                                                                                  |
| A2h–EFh           | Reserved                                                                                  |
| Maps to all pages | <a href="#">“Global Registers” on page 294</a>                                            |

## Page 00h: Control Registers

**Table 38: Control Registers (Page 00h)**

| Address | Bits   | Register Name                                                                                          |
|---------|--------|--------------------------------------------------------------------------------------------------------|
| 00h–05h | 8/port | <a href="#">“Port Traffic Control Register (Page 00h: Address 00h)” on page 148</a>                    |
| 06h–07h | 8      | Reserved                                                                                               |
| 08h     | 8      | <a href="#">“IMP Port Control Register (Page 00h: Address 08h)” on page 149</a>                        |
| 09h–0Ah | 8      | Reserved                                                                                               |
| 0Bh     | 8      | <a href="#">“Switch Mode Register (Page 00h: Address 0Bh)” on page 150</a>                             |
| 0Ch–0Dh | 16     | Reserved                                                                                               |
| 0Eh     | 8      | <a href="#">“IMP Port State Override Register (Page 00h: Address 0Eh)” on page 150</a>                 |
| 0Fh     | 8      | <a href="#">“LED Refresh Register (Page 00h: Address 0Fh)” on page 151</a>                             |
| 10h–11h | 16     | <a href="#">“LED Function 0 Control Register (Page 00h: Address 10h)” on page 152</a>                  |
| 12h–13h | 16     | <a href="#">“LED Function 1 Control Register (Page 00h: Address 12h)” on page 153</a>                  |
| 14h–15h | 16     | <a href="#">“LED Function Map Register (Page 00h: Address 14h–15h)” on page 153</a>                    |
| 16h–17h | 16     | <a href="#">“LED Enable Map Register (Page 00h: Address 16h–17h)” on page 154</a>                      |
| 18h–19h | 16     | <a href="#">“LED Mode Map 0 Register (Page 00h: Address 18h–19h)” on page 154</a>                      |
| 1Ah–1Bh | 16     | <a href="#">“LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)” on page 154</a>                      |
| 1Ch–1Eh | –      | Reserved                                                                                               |
| 1Fh     | 8      | Reserved                                                                                               |
| 20h     | –      | Reserved                                                                                               |
| 21h     | 8      | <a href="#">“Port Forward Control Register (Page 00h: Address 21h)” on page 155</a>                    |
| 22h–23h | –      | Reserved                                                                                               |
| 24h–25h | 16     | <a href="#">“Protected Port Selection Register (Page 00h: Address 24h–25h)” on page 155</a>            |
| 26h–27h | 16     | <a href="#">“WAN Port Select Register (Page 00h: Address 26h–27h)” on page 155</a>                     |
| 28h–2Bh | 32     | <a href="#">“Pause Capability Register (Page 00h: Address 28h–2Bh)” on page 156</a>                    |
| 2Ch–2Eh | –      | Reserved                                                                                               |
| 2Fh     | 8      | <a href="#">“Reserved Multicast Control Register (Page 00h: Address 2Fh)” on page 156</a>              |
| 30h     | –      | Reserved                                                                                               |
| 31h     | 8      | Reserved                                                                                               |
| 32h–33h | 16     | <a href="#">“Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h)” on page 157</a>       |
| 34h–35h | 16     | <a href="#">“Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)” on page 158</a> |
| 36h–37h | 16     | <a href="#">“MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)” on page 158</a>                |
| 38h–39h | 16     | <a href="#">“Pause Pass Through for RX Register (Page 00h: Address 38h–39h)” on page 159</a>           |
| 3Ah–3Bh | 16     | <a href="#">“Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)” on page 159</a>           |
| 3Ch–3Dh | 16     | <a href="#">“Disable Learning Register (Page 00h: Address 3Ch–3Dh)” on page 159</a>                    |

**Table 38: Control Registers (Page 00h) (Cont.)**

| <b>Address</b> | <b>Bits</b> | <b>Register Name</b>                                                                         |
|----------------|-------------|----------------------------------------------------------------------------------------------|
| 3Eh–3Fh        | 16          | <a href="#">“Software Learning Register (Page 00h: Address 3Eh–3Fh)” on page 160</a>         |
| 40h–49h        | –           | Reserved                                                                                     |
| 4Ah–4Bh        | –           | Reserved                                                                                     |
| 4Ch–57h        | –           | Reserved                                                                                     |
| 58h–5Dh        | 8/port      | <a href="#">“Port State Override Register (Page 00h: Address 58h)” on page 160</a>           |
| 60h–65h        | –           | Reserved                                                                                     |
| 66h–74h        | –           | Reserved                                                                                     |
| 75h            | –           | <a href="#">“MDIO WAN Port Address Register (Page 00h: Address 75h)” on page 161</a>         |
| 78h            | –           | <a href="#">“MDIO IMP PORT Address Register (Page 00h: Address 78h)” on page 161</a>         |
| 79h            | –           | <a href="#">“Software Reset Control Register (Page 00h: Address 79h)” on page 162</a>        |
| 7Ah–7Fh        | –           | Reserved                                                                                     |
| 80h            | 8           | <a href="#">“Pause Frame Detection Control Register (Page 00h: Address 80h)” on page 162</a> |
| 81h–87h        | –           | Reserved                                                                                     |
| 88h            | 8           | <a href="#">“Fast-Aging Control Register (Page 00h: Address 88h)” on page 162</a>            |
| 89h            | 8           | <a href="#">“Fast-Aging Port Control Register (Page 00h: Address 89h)” on page 163</a>       |
| 8Ah–8Bh        | 16          | <a href="#">“Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)” on page 163</a>    |
| F0h–F7h        | 8           | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294, bytes 0-7</a>         |
| F8h–FDh        | –           | Reserved                                                                                     |
| 8Ch–EFh        | –           | Reserved                                                                                     |
| FEh            | 8           | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>                      |
| FFh            | 8           | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                            |

## Port Traffic Control Register (Page 00h: Address 00h)

**Table 39: Port Traffic Control Register Address Summary**

| <b>Address</b> | <b>Description</b> |
|----------------|--------------------|
| 00h            | Port 0             |
| 01h            | Port 1             |
| 02h            | Port 2             |
| 03h            | Port 3             |
| 04h            | Port 4             |
| 05h            | Port 5             |

**Table 40: Port Control Register (Page 00h: Address 00h–05h)**

| <b>Bit</b> | <b>Name</b>    | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                         | <b>Default</b>                              |
|------------|----------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|
| 7:5        | STP_STATE[2:0] | R/W        | CPU writes the current computed states of its spanning tree algorithm for a given port.<br>000 = No spanning tree (default for unmanaged mode)<br>001 = Disabled state (default for managed mode)<br>010 = Blocking state<br>011 = Listening state<br>100 = Learning state<br>101 = Forwarding state<br>110–111 = Reserved | ~HW_FWDG_EN<br>(controlled by Strap option) |
| 4:2        | Reserved       | –          | –                                                                                                                                                                                                                                                                                                                          | 000                                         |
| 1          | TX_DISABLE     | R/W        | 0 = Enable the transmit function of the port at the MAC level.<br>1 = Disable the transmit function of the port at the MAC level.                                                                                                                                                                                          | 0                                           |
| 0          | RX_DISABLE     | R/W        | 0 = Enable the receive function of the port at the MAC level.<br>1 = Disable the receive function of the port at the MAC level.                                                                                                                                                                                            | 0                                           |

## IMP Port Control Register (Page 00h: Address 08h)

**Table 41: IMP Port Control Register (Page 00h: Address 08h)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                         | <b>Default</b> |
|------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 7:5        | Reserved    | R/W        | –                                                                                                                                                                                                                                                                                                                                                                          | –              |
| 4          | RX_UCST_EN  | R/W        | Receive unicast enable<br>Allow unicast frames to be forwarded to the IMP, when the IMP is configured as the frame management port, and the frame was matching address table entry.<br>When cleared, unicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. Ignored if the IMP is not selected as the Frame Management Port. | 0              |
| 3          | RX_MCST_EN  | R/W        | Receive multicast enable<br>Allow multicast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port, and the frame was flooded due to no matching address table entry.<br>When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port.                                          | 0              |

**Table 41: IMP Port Control Register (Page 00h: Address 08h) (Cont.)**

| Bit | Name       | R/W | Description                                                                                                                                                                                                                                                     | Default |
|-----|------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 2   | RX_BCST_EN | R/W | Receive broadcast enable<br>Allow broadcast frames to be forwarded to the IMP, when the IMP is configured as the Frame Management Port.<br>When cleared, multicast frames that meet the mirror ingress/egress rules are forwarded to the frame management port. | 0       |
| 1:0 | Reserved   | R/W | –                                                                                                                                                                                                                                                               | 0       |

## Switch Mode Register (Page 00h: Address 0Bh)

**Table 42: Switch Mode Register (Page 00h: Address 0Bh)**

| Bit | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                  | Default     |
|-----|--------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 7:2 | Reserved     | RO  | –                                                                                                                                                                                                                                                                                                                                            | 000001      |
| 1   | SW_FWDG_EN   | R/W | Software forwarding enable<br>SW_FWDG_EN = 1: Frame forwarding is enabled.<br>SW_FWDG_EN = 0: Frame forwarding is disabled.<br>Managed switch implementations should be configured to disable forwarding on power-on to allow the processor to configure the internal address table and other parameters before frame forwarding is enabled. | HW_FWDG_EN  |
| 0   | SW_FWDG_MODE | R/W | Software forwarding mode<br>0 = Unmanaged mode.<br>1 = Managed mode.<br>The ARL treats reserved multicast addresses differently depending on this selection.                                                                                                                                                                                 | ~HW_FWDG_EN |

## IMP Port State Override Register (Page 00h: Address 0Eh)

**Table 43: IMP Port State Override Register (Page 00h: Address 0Eh)**

| Bit | Name                       | R/W | Description                                                                                     | Default |
|-----|----------------------------|-----|-------------------------------------------------------------------------------------------------|---------|
| 7   | MII_SW_OR                  | R/W | MII software override<br>0 = Use MII hardware pin status.<br>1 = Use contents of this register. | 0       |
| 6   | Reserved                   | R/W | Reserved                                                                                        | 0       |
| 5   | TX Flow Control Capability | RO  | Link partner flow control capability<br>0 = Not PAUSE capable<br>1 = PAUSE capable              | 0       |

**Table 43: IMP Port State Override Register (Page 00h: Address 0Eh)**

| <b>Bit</b> | <b>Name</b>                | <b>R/W</b> | <b>Description</b>                                                                 | <b>Default</b> |
|------------|----------------------------|------------|------------------------------------------------------------------------------------|----------------|
| 4          | RX Flow Control Capability | R/W        | Link partner flow control capability<br>0 = Not PAUSE-capable<br>1 = PAUSE-capable | 0              |
| 3:2        | SPEED                      | R/W        | Speed<br>00 = 10 Mbps<br>01 = 100 Mbps<br>10 = 1000 Mbps                           | 10             |
| 1          | FDX                        | R/W        | Full duplex<br>0 = Half duplex<br>1 = Full duplex                                  | 1              |
| 0          | LINK                       | R/W        | Link status<br>0 = Link fail<br>1 = Link pass                                      | 0              |

## LED Control Register (Page 00h: Address 0Fh–1Bh)

**Table 44: LED Control Register Address Summary**

| <b>Address</b> | <b>Description</b>                |
|----------------|-----------------------------------|
| 0Fh            | LED refresh control register      |
| 10h–11h        | LED function 0 control register   |
| 12h–13h        | LED function 1 control register   |
| 14h–15h        | LED function map control register |
| 16h–17h        | LED enable map register           |
| 18h–19h        | LED mode map 0 register           |
| 1Ah–1Bh        | LED mode map 1 register           |

## LED Refresh Register (Page 00h: Address 0Fh)

**Table 45: LED Refresh Register (Page 00h: Address 0Fh)**

| <b>Bit</b> | <b>Name</b>          | <b>R/W</b> | <b>Description</b>                                          | <b>Default</b> |
|------------|----------------------|------------|-------------------------------------------------------------|----------------|
| 7          | LED_EN               | R/W        | Enable LED                                                  | 1              |
| 6          | POST_EXEC            | R/W        | Write 1 to restart POST.                                    | 0              |
| 5          | POST_PSCAN_EN        | R/W        | When enabled, switch scans the port during the POST period. | 0              |
| 4          | POST_Cable_diag_en   | R/W        | Enable cable diagnostics display during POST                | 0              |
| 3          | Normal_Cable_diag_en | R/W        | Enable cable diagnostics display in normal mode             | 0              |

**Table 45: LED Refresh Register (Page 00h: Address 0Fh)**

| Bit | Name             | R/W | Description                                                                                                                                                                                                                                                                                                                                                          | Default |
|-----|------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 2:0 | LED_Refresh_rate | R/W | LED refresh count register (that is, LED blinking rate)<br>Refresh time = (N + 1) × 10 ms <ul style="list-style-type: none"> <li>• 000 = Reserved</li> <li>• 001 = 20 ms/25 Hz</li> <li>• 010 = 30 ms/16 Hz</li> <li>• 011 = 40 ms/12 Hz</li> <li>• 100 = 50 ms/10 Hz</li> <li>• 101 = 60 ms/8 Hz</li> <li>• 110 = 70 ms/7 Hz</li> <li>• 111 = 80 ms/6 Hz</li> </ul> | 3h      |

## LED Function 0 Control Register (Page 00h: Address 10h)

**Table 46: LED Function 0 Control Register (Page 00h: Address 10h–11h)**

| Bit  | Name         | R/W | Description                                                                                                                                                                                                                                                                                          | Default                                                                                                                                                  |
|------|--------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | LED_FUNCTION | R/W | The following is the list of functions assigned to each bit:<br>15 = PHYLED3<br>14 = Reserved<br>13 = 1G/ACT<br>12 = 10/100M/ACT<br>11 = 100M/ACT<br>10 = 10M/ACT<br>9 = SPD1G<br>8 = SPD100M<br>7 = SPD10M<br>6 = DPX/COL<br>5 = LNK/ACT<br>4 = COL<br>3 = ACT<br>2 = DPX<br>1 = LNK<br>0 = PHYLED4 | LED<br>MODE[1:0]=00:<br>16'h0121<br><br>LED<br>MODE[1:0]=01:<br>16'h0C41<br><br>LED<br>MODE[1:0]=10:<br>16'h0124<br><br>LED<br>MODE[1:0]=11:<br>16'h0C04 |

## LED Function 1 Control Register (Page 00h: Address 12h)

**Table 47: LED Function 1 Control Register (Page 00h: Address 12h–13h)**

| Bit  | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                                                 | Default                                                                                                                                         |
|------|--------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | LED_FUNCTION | R/W | <p>The following is the list of functions assigned to each bit:</p> <p>15 = PHYLED3</p> <p>14 = Reserved</p> <p>13 = 1G/ACT</p> <p>12 = 10/100M/ACT</p> <p>11 = 100M/ACT</p> <p>10 = 10M/ACT</p> <p>9 = SPD1G</p> <p>8 = SPD100M</p> <p>7 = SPD10M</p> <p>6 = DPX/COL</p> <p>5 = LNK/ACT</p> <p>4 = COL</p> <p>3 = ACT</p> <p>2 = DPX</p> <p>1 = LNK</p> <p>0 = PHYLED4</p> | <p>LED MODE[1:0] = 00: 16'h0321</p> <p>LED MODE[1:0] = 01: 16'h3041</p> <p>LED MODE[1:0] = 10: 16'h0324</p> <p>LED MODE[1:0] = 11: 16'h2C04</p> |

## LED Function Map Register (Page 00h: Address 14h–15h)

**Table 48: LED Function Map Register (Page 00h: Address 14h–15h)**

| Bit  | Name         | R/W | Description                                                                                                                                                                                                                                                                 | Default |
|------|--------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved     | R/W | —                                                                                                                                                                                                                                                                           | 0       |
| 8:0  | LED_FUNC_MAP | R/W | <p>Per-port select function bit. Each port LED follows the function table specified for each port.</p> <p>1 = Select function 1.</p> <p>0 = Select function 0.</p> <p>Bits [4:0] correspond to ports [4:0].</p> <p>Bit 5 corresponds to port 5 in serial LED interface.</p> | 1FFh    |

## LED Enable Map Register (Page 00h: Address 16h–17h)

*Table 49: LED Enable Map Register (Page 00h: Address 16h–17h)*

| <i>Bit</i> | <i>Name</i> | <i>R/W</i> | <i>Description</i>                                                                                                                                | <i>Default</i> |
|------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15:9       | Reserved    | R/W        | –                                                                                                                                                 | 0              |
| 8:0        | LED_EN_MAP  | R/W        | Per-port enable bit<br>1 = Enable<br>0 = Disable<br>Bits [4:0] correspond to ports [4:0].<br>Bit 5 corresponds to port 5 in serial LED interface. | 9'h1F          |

## LED Mode Map 0 Register (Page 00h: Address 18h–19h)

*Table 50: LED Mode Map 0 Register (Page 00h: Address 18h–19h)*

| <i>Bit</i> | <i>Name</i>   | <i>R/W</i> | <i>Description</i>                                                                                                                                              | <i>Default</i> |
|------------|---------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15:9       | Reserved      | R/W        | –                                                                                                                                                               | 0              |
| 8:0        | LED_MODE_MAP0 | R/W        | Combine with LED_MODE_MAP1 to decide per port LED output mode.<br>Bits [4:0] correspond to ports [4:0].<br>Bit 5 corresponds to port 5 in serial LED interface. | 1FFh           |

## LED Mode Map 1 Register (Page 00h: Address 1Ah–1Bh)

*Table 51: LED Function Map 1 Control Register (Page 00h: Address 1Ah–1Bh)*

| <i>Bit</i> | <i>Name</i>   | <i>R/W</i> | <i>Description</i>                                                                                                     | <i>Default</i> |
|------------|---------------|------------|------------------------------------------------------------------------------------------------------------------------|----------------|
| 15:9       | Reserved      | R/W        | –                                                                                                                      | 0              |
| 8:0        | LED_MODE_MAP1 | R/W        | Per-port select function bit<br>LED_FUNC_MAP[1:0]<br>00 = LED off<br>01 = LED on<br>10 = LED blinking<br>11 = LED auto | 1FFh           |

See “LED Interfaces” on page 116 for more information.

## Port Forward Control Register (Page 00h: Address 21h)

**Table 52: Port Forward Control Register (Page 00h: Address 21h)**

| Bit | Name            | R/W | Description                                                                                                                                                                         | Default |
|-----|-----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | MCST_DLF_FWD_EN | R/W | 1 = Forward multicast lookup failed frames according to multicast lookup failed forward map register (Page 00h: Address 34h)<br>0 = Flood multicast packet if fail ARL table lookup | 0       |
| 6   | UCST_DLF_FWD_EN | R/W | 1 = Forward unicast lookup failed frames according to Unicast Lookup failed forward map register (Page 00h: Address 32h)<br>0 = Flood unicast packet if fail ARL table lookup       | 0h      |
| 5:1 | Reserved        | R/W | —                                                                                                                                                                                   | 0       |
| 0   | Reserved        | R/W | —                                                                                                                                                                                   | 1       |

See “Egress PCP Remarking” on page 54 for more information.

## Protected Port Selection Register (Page 00h: Address 24h–25h)

**Table 53: Protected Port Selection Register (Page 00h: Address 24h–25h)**

| Bit  | Name        | R/W | Description                                                                                                                                                                                            | Default |
|------|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved    | RO  | —                                                                                                                                                                                                      | 0       |
| 8:0  | PORT_SELECT | R/W | Protected port selection<br>Bit 8 = IMP port<br>Bits [4:0] correspond to ports [4:0], respectively.<br>1 = Port protected. Cannot send/receive to other protected ports.<br>0 = Port is not protected. | 0       |

See “Protected Ports” on page 47 for more information.

## WAN Port Select Register (Page 00h: Address 26h–27h)

**Table 54: WAN Port Select Register (Page 00h: Address 26h–27h)**

| Bit   | Name     | R/W | Description | Default |
|-------|----------|-----|-------------|---------|
| 15:10 | Reserved | RO  | —           | 0       |
| 9     | Reserved | R/W | —           | —       |
| 8:6   | Reserved | R/W | —           | —       |

**Table 54: WAN Port Select Register (Page 00h: Address 26h–27h) (Cont.)**

| Bit | Name         | R/W | Description                                                                                                                                                                                                                   | Default |
|-----|--------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 5:0 | WAN_PORT_MAP | R/W | Set assigned WAN port to 1.<br>Bits [5:0] correspond to ports [5:0], respectively.<br>Port 5 can be selected as a WAN port only in<br>EN_IMP_PORT = 10 of Global Management Configuration<br>register (page02h: address 00h). | 0       |

## Pause Capability Register (Page 00h: Address 28h–2Bh)

**Table 55: Pause Capability Register (Page 00h: Address 28h–2Bh)**

| Bit   | Name            | R/W | Description                                                                                                         | Default |
|-------|-----------------|-----|---------------------------------------------------------------------------------------------------------------------|---------|
| 31:24 | Reserved        | RO  | –                                                                                                                   | 0       |
| 23    | EN_OVERRIDE     | R/W | Forces the content of this register setting to be used<br>over the auto negotiation result.                         | 0       |
| 22:18 | Reserved        | –   | –                                                                                                                   | –       |
| 17:9  | EN_RX_PAUSE_CAP | –   | Enabling the receive pause capability.<br>Bit 17 = IMP port<br>Bits [14:9] correspond to ports [5:0], respectively. | 0h      |
| 8:0   | EN_TX_PAUSE_CAP | –   | Enables the transmit pause capability.<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.   | 0h      |

## Reserved Multicast Control Register (Page 00h: Address 2Fh)

**Table 56: Reserved Multicast Control Register (Page 00h: Address 2Fh)**

| Bit | Name               | R/W | Description                                                                                                                                                                                                                                                                                                                             | Default |
|-----|--------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Multicast Learning | R/W | Multicast learning enable<br>0 = Do not learn unicast source addresses of frames<br>that have a reserved multicast destination address.<br>1 = Learn unicast source addresses even from frames<br>that have a reserved multicast destination address.<br>See “ <a href="#">Address Management</a> ” on page 54 for more<br>information. | 0       |
| 6:5 | Reserved           | R/W | –                                                                                                                                                                                                                                                                                                                                       | 0       |
| 4   | En_Mul_4           | R/W | Specifies if packets with the destination addresses in<br>the below range are to be forwarded to the<br>appropriate port or dropped when operating in<br>unmanaged mode.<br>01-80-C2-00-00-20–01-80-C2-00-00-2F<br>0 = Forward<br>1 = Drop                                                                                              | 0       |

**Table 56: Reserved Multicast Control Register (Page 00h: Address 2Fh) (Cont.)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                | <b>Default</b> |
|------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 3          | En_Mul_3    | R/W        | Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-11–01-80-C2-00-00-1F<br>0 = Forward<br>1 = Drop | 0              |
| 2          | En_Mul_2    | R/W        | Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-10<br>0 = Forward<br>1 = Drop                                  | 0              |
| 1          | En_mul_1    | R/W        | Specifies if packets with the destination addresses in the below range are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-02–01-80-C2-00-00-0F<br>0 = Forward<br>1 = Drop | 1              |
| 0          | En_Mul_0    | R/W        | Specifies if packets with the destination address below are to be forwarded to the appropriate port or dropped when operating in unmanaged mode.<br>01-80-C2-00-00-00<br>0 = Forward<br>1 = Drop                                  | 0              |

See [“Multicast Addresses” on page 57](#) for more information.

## Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h)

**Table 57: Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b> | <b>Default</b> |
|------------|-------------|------------|--------------------|----------------|
| 15:9       | Reserved    | RO         | —                  | 0              |

**Table 57: Unicast Lookup Failed Forward Map Register (Page 00h: Address 32h–33h)**

| Bit | Name        | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Default |
|-----|-------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 8:0 | UNI_DLF_MAP | R/W | <p>Unicast lookup failed forward map</p> <p>Bit 8 = IMP port</p> <p>Bits [5:0] correspond to ports [5:0], respectively.</p> <p>When the UCST_DLF_FWD_EN bit in “Port Forward Control Register (Page 00h: Address 21h)” on page 155 is enabled and a unicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped.</p> <p>0 = Do not forward a unicast lookup failure to this port.</p> <p>1 = Forward a unicast lookup failure to this port.</p> | 0       |

See “Unicast Addresses” on page 56 for more information.

## Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)

**Table 58: Multicast Lookup Failed Forward Map Register (Page 00h: Address 34h–35h)**

| Bit  | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Default |
|------|--------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved     | RO  | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 0       |
| 8:0  | MCST_DLF_MAP | R/W | <p>Multicast lookup failed forward map</p> <p>Bit 8 = IMP port</p> <p>Bits [5:0] correspond to ports [5:0], respectively.</p> <p>When the MCST_DLF_FWD_EN bit in port forward control register (Page 00h:Address 21h) is enabled and a multicast lookup failure occurs, the ARL table forwards the frame according to the contents of this register. If this register remains in default value, the frame is dropped.</p> <p>0 = Do not forward a multicast lookup failure to this port.</p> <p>1 = Forward a multicast lookup failure to this port.</p> | 0       |

See “Multicast Addresses” on page 57 for more information.

## MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)

**Table 59: MLF IPMC Forward Map Register (Page 00h: Address 36h–37h)**

| Bit  | Name     | R/W | Description | Default |
|------|----------|-----|-------------|---------|
| 15:9 | Reserved | RO  | –           | 0       |

**Table 59: MLF IMPC Forward Map Register (Page 00h: Address 36h–37h)**

| Bit | Name             | R/W | Description                                                                                 | Default |
|-----|------------------|-----|---------------------------------------------------------------------------------------------|---------|
| 8:0 | MLF_IPMC_FWD_MAP | R/W | IPMC forward map<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively. | 0       |

## Pause Pass Through for RX Register (Page 00h: Address 38h–39h)

**Table 60: Pause Pass Through for RX Register (Page 00h: Address 38h–39h)**

| Bit  | Name                  | R/W | Description                                                                                                                                                      | Default |
|------|-----------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:8 | Reserved              | RO  | –                                                                                                                                                                | 0       |
| 7:0  | IGNORE_PAUSE_FRAME_RX | R/W | RX pause pass through map<br>1 = Ignore IEEE 802.3x<br>0 = Comply with IEEE 802.3x pause frame receiving.<br>Bits [5:0] correspond to ports [5:0], respectively. | 0       |

## Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)

**Table 61: Pause Pass Through for TX Register (Page 00h: Address 3Ah–3Bh)**

| Bit  | Name                  | R/W | Description                                                                                                                                                                          | Default |
|------|-----------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved              | RO  | –                                                                                                                                                                                    | 0       |
| 8:0  | IGNORE_PAUSE_FRAME_TX | R/W | TX pause pass through map<br>1 = Ignore IEEE 802.3x.<br>0 = Comply with IEEE 802.3x pause frame receiving<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively. | 0       |

## Disable Learning Register (Page 00h: Address 3Ch–3Dh)

**Table 62: Disable Learning Register (Page 00h: Address 3Ch–3Dh)**

| Bit  | Name         | R/W | Description                                                                                                            | Default |
|------|--------------|-----|------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved     | RO  | –                                                                                                                      | 0       |
| 8:0  | DIS_LEARNING | R/W | 1 = Disable learning<br>0 = Enable learning<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively. | 0       |

## Software Learning Register (Page 00h: Address 3Eh–3Fh)

**Table 63: Software Learning Control Register (Page 00h: Address 3Eh–3Fh)**

| Bit  | Name          | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Default |
|------|---------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved      | RO  | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | –       |
| 8:0  | SW_LEARN_CNTL | R/W | <p>1 = Software learning control enabled</p> <p>The behaviors are as follows.</p> <ul style="list-style-type: none"> <li>Forwarding behavior: Incoming packet with unknown SA will be copied to CPU port.</li> <li>Learning behavior: Allow S/W to decide whether incoming packet learn or not. In S/W learning mode, the H/W learning mechanism will be disabled automatically.</li> <li>Refreshed behavior: Allow refreshed mechanism to operate properly even through the H/W learning had been disabled.</li> </ul> <p>0 = Software learning control disabled<br/>Forwarding/Learning/Refreshed behavior to keep hardware operation.</p> <p>Bit 8 = IMP port</p> <p>Bits [5:0] correspond to ports [5:0].</p> | 0       |

## Port State Override Register (Page 00h: Address 58h)

**Table 64: Port State Override Register Address Summary**

| Address | Description |
|---------|-------------|
| 58h     | Port 0      |
| 59h     | Port 1      |
| 5Ah     | Port 2      |
| 5Bh     | Port 3      |
| 5Ch     | Port 4      |
| 5Dh     | Port 5      |

**Table 65: Port State Override Register (Page 00h: Address 58h–5Fh)**

| Bit | Name              | R/W | Description                                                                                                                                                                                   | Default |
|-----|-------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Reserved          | R/W | –                                                                                                                                                                                             | –       |
| 6   | Software Override | R/W | Writing 1 to this bit allows the values of the bits [5:0] to be written to the external PHY. Writing 0 to this bit prevents these values from overriding the present external PHY conditions. | 0       |

**Table 65: Port State Override Register (Page 00h: Address 58h–5Fh) (Cont.)**

| <b>Bit</b> | <b>Name</b>            | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                              | <b>Default</b> |
|------------|------------------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 5          | TX Flow Control Enable | R/W        | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>0 = Flow control disabled for transmit traffic.<br>1 = Flow control enabled for transmit traffic. | 0              |
| 4          | RX Flow Control Enable | R/W        | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>0 = Flow control disabled for receive traffic.<br>1 = Flow control enabled for receive traffic.   | 0              |
| 3:2        | Speed                  | R/W        | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>00 = 10 Mbps<br>01 = 100 Mbps<br>10 = 1000 Mbps<br>11 = Illegal state                             | 10             |
| 1          | Duplex Mode            | R/W        | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written to 1.<br>0 = Half duplex<br>1 = Full duplex                                                                | 1              |
| 0          | Link State             | R/W        | The value of this bit overrides the existing conditions of the external PHY port if bit 6 is written 1.<br>1 = Link-up<br>0 = Link-down                                                                         | 1              |

## MDIO WAN Port Address Register (Page 00h: Address 75h)

**Table 66: MDIO WAN Port Address Register (Page 00h: Address 75h)**

| <b>Bit</b> | <b>Name</b>      | <b>R/W</b> | <b>Description</b>         | <b>Default</b> |
|------------|------------------|------------|----------------------------|----------------|
| 7:5        | Reserved         | RO         | —                          | 0              |
| 4:0        | WAN_MDIO_ADDRESS | R/W        | WAN port MDIO SCAN address | 15h            |

## MDIO IMP PORT Address Register (Page 00h: Address 78h)

**Table 67: MDIO IMP PORT Address Register (Page 00h: Address 78h)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b> | <b>Default</b> |
|------------|-------------|------------|--------------------|----------------|
| 7:5        | Reserved    | RO         | —                  | 0              |

**Table 67: MDIO IMP PORT Address Register (Page 00h: Address 78h)**

| Bit | Name             | R/W | Description           | Default |
|-----|------------------|-----|-----------------------|---------|
| 4:0 | IMP_MDIO_ADDRESS | R/W | IMP PORT MDIO address | 18h     |

## Software Reset Control Register (Page 00h: Address 79h)

**Table 68: Software Reset Control Register (Page 00h: Address 79h)**

| Bit | Name      | R/W | Description                                                                                                                                                                          | Default |
|-----|-----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | SW_RST    | R/W | Software reset (Bit4 “EN_SW_RST” MUST be enabled – as well). Software reset, write “1” to activate a RESET, “0” to clear the reset state.<br>1 = Activate reset.<br>0 = Clear reset. | –       |
| 6:5 | Reserved  | –   | –                                                                                                                                                                                    | –       |
| 4   | EN_SW_RST | R/W | Enable software reset.                                                                                                                                                               | 0       |
| 3:0 | Reserved  | R/W | –                                                                                                                                                                                    | –       |

## Pause Frame Detection Control Register (Page 00h: Address 80h)

**Table 69: Pause Frame Detection Control Register (Page 00h: Address 80h)**

| Bit | Name            | R/W | Description                                                                                   | Default |
|-----|-----------------|-----|-----------------------------------------------------------------------------------------------|---------|
| 7:1 | Reserved        | RO  | –                                                                                             | 0       |
| 0   | PAUSE_IGNORE_DA | R/W | 0 = Check DA field on pause frame detection.<br>1 = Ignore DA field on pause frame detection. | 0       |

## Fast-Aging Control Register (Page 00h: Address 88h)

**Table 70: Fast-Aging Control Register (Page 00h: Address 88h)**

| Bit | Name                | R/W | Description                                                                                                                                                                                                                   | Default |
|-----|---------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Fast_Age_Start/Done | R/W | Set bit to 1 triggers the fast aging process.<br>When the fast aging process is done, this bit is cleared to 0.                                                                                                               | 0       |
| 6   | Reserved            | –   | –                                                                                                                                                                                                                             | –       |
| 5   | EN_AGE_MCAST        | R/W | Enable Aging Multicast Entry<br>1 = Aging multicast Entries in ARL Table<br>0 = Disable Aging Multicast Entries in ARL Table<br><b>Note:</b> The EN_AGE_MCAST and the EN_AGE_Port can not enable (set to 1) at the same time. | 0       |
| 4   | EN_AGE_SPT          | R/W | When set, check spanning tree ID.                                                                                                                                                                                             | –       |

**Table 70: Fast-Aging Control Register (Page 00h: Address 88h)**

| <b>Bit</b> | <b>Name</b>    | <b>R/W</b> | <b>Description</b>               | <b>Default</b> |
|------------|----------------|------------|----------------------------------|----------------|
| 3          | EN_AGE_VLAN    | R/W        | When set, check VLAN ID.         | —              |
| 2          | EN_AGE_Port    | R/W        | When set, check port ID.         | —              |
| 1          | EN_AGE_Dynamic | R/W        | When set, age out dynamic entry. | —              |
| 0          | EN_AGE_Static  | R/W        | When set, age out static entry.  | —              |

## Fast-Aging Port Control Register (Page 00h: Address 89h)

**Table 71: Fast-Aging Port Control Register (Page 00h: Address 89h)**

| <b>Bit</b> | <b>Name</b>          | <b>R/W</b> | <b>Description</b>                                                                  | <b>Default</b> |
|------------|----------------------|------------|-------------------------------------------------------------------------------------|----------------|
| 7:4        | Reserved             | R/W        | —                                                                                   | 0              |
| 3:0        | Fast Age Single Port | R/W        | Fast age single port select<br>Writing bits [3:0] selects the port to be fast-aged. | 0              |

## Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)

**Table 72: Fast-Aging VID Control Register (Page 00h: Address 8Ah–8Bh)**

| <b>Bit</b> | <b>Name</b>         | <b>R/W</b> | <b>Description</b>                                                                 | <b>Default</b> |
|------------|---------------------|------------|------------------------------------------------------------------------------------|----------------|
| 15:12      | Reserved            | R/W        | —                                                                                  | 0              |
| 11:0       | Fast Age Single VID | R/W        | Fast age single VID select<br>Writing bits [11:0] selects the VID to be fast-aged. | 0              |

## Page 01h: Status Registers

**Table 73: Status Registers (Page 01h)**

| Address | Bits    | Register Name                                                        |
|---------|---------|----------------------------------------------------------------------|
| 00h–01h | 16      | “Link Status Summary (Page 01h: Address 00h)” on page 164            |
| 02h–03h | 16      | “Link Status Change (Page 01h: Address 02h)” on page 164             |
| 04h–07h | 32      | “Port Speed Summary (Page 01h: Address 04h)” on page 165             |
| 08h–09h | 16      | “Duplex Status Summary (Page 01h: Address 08h)” on page 165          |
| 0Ah–0Dh | 32      | “Pause Status Summary (Page 01h: Address 0Ah)” on page 166           |
| 0Eh–0Fh | 16      | “Source Address Change Register (Page 01h: Address 0Eh)” on page 166 |
| 10h–45h | 48/port | “Last Source Address Register (Page 01h: Address 10h)” on page 166   |
| 46h–EFh | –       | Reserved                                                             |
| F0h–F7h | 8       | “SPI Data I/O Register (Global, Address F0h)” on page 294, bytes 0–7 |
| F8h–FDh | –       | Reserved                                                             |
| FEh     | 8       | “SPI Status Register (Global, Address FEh)” on page 295              |
| FFh     | 8       | “Page Register (Global, Address FFh)” on page 295                    |

### Link Status Summary (Page 01h: Address 00h)

**Table 74: Link Status Summary Register (Page 01h: Address 00h–01h)**

| Bit  | Name        | R/W | Description                                                                                                              | Default |
|------|-------------|-----|--------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved    | RO  | –                                                                                                                        | 0       |
| 8:0  | LINK_STATUS | RO  | Link status<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>0 = Link fail<br>1 = Link pass | 0       |

### Link Status Change (Page 01h: Address 02h)

**Table 75: Link Status Change Register (Page 01h: Address 02h–03h)**

| Bit  | Name     | R/W | Description | Default |
|------|----------|-----|-------------|---------|
| 15:9 | Reserved | RO  | –           | 0       |

**Table 75: Link Status Change Register (Page 01h: Address 02h–03h) (Cont.)**

| <b>Bit</b> | <b>Name</b>        | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                         | <b>Default</b> |
|------------|--------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 8:0        | LINK_STATUS_CHANGE | RO         | Link status change.<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>Upon change of link status, a bit remains set until cleared by a read operation.<br>0 = Link status constant.<br>1 = Link status change. | 0              |

## Port Speed Summary (Page 01h: Address 04h)

**Table 76: Port Speed Summary Register (Page 01h: Address 04h–07h)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | <b>Default</b> |
|------------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 31:18      | Reserved    | PO         | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0              |
| 17:0       | PORT_SPEED  | RO         | Port speed<br>Speed of each port is reported based on the mapping below: <ul style="list-style-type: none"> <li>• Bits [17:16] = IMP port</li> <li>• Bits [15:12] = Reserved</li> <li>• Bits [11:10] = Port 5</li> <li>• Bits [9:8] = Port 4</li> <li>• Bits [7:6] = Port 3</li> <li>• Bits [5:4] = Port 2</li> <li>• Bits [3:2] = Port 1</li> <li>• Bits [1:0] = Port 0</li> </ul> Bit values are as follows: <ul style="list-style-type: none"> <li>• 00 = 10 Mbps</li> <li>• 01 = 100 Mbps</li> <li>• 10 = 1000 Mbps</li> <li>• 11 = Illegal state</li> </ul> | 0              |

## Duplex Status Summary (Page 01h: Address 08h)

**Table 77: Duplex Status Summary Register (Page 01h: Address 08h–09h)**

| <b>Bit</b> | <b>Name</b>  | <b>R/W</b> | <b>Description</b>                                                                                                            | <b>Default</b> |
|------------|--------------|------------|-------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15:9       | Reserved     | RO         | —                                                                                                                             | 0              |
| 8:0        | DUPLEX_STATE | RO         | Duplex state<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>0 = Half duplex<br>1 = Full duplex | 0x1FF          |

## Pause Status Summary (Page 01h: Address 0Ah)

**Table 78: PAUSE Status Summary Register (Page 01h: Address 0Ah–0Dh)**

| Bit   | Name                 | R/W | Description                                                                                                                                       | Default |
|-------|----------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:18 | Reserved             | RO  | Reserved                                                                                                                                          | 0       |
| 17:9  | RECEIVE_PAUSE_STATE  | RO  | Pause state. Receive pause capability<br>Bit 17 = IMP port<br>Bits [14:9] correspond to ports [5:0], respectively.<br>0 = Disabled<br>1 = Enabled | 0       |
| 8:0   | TRANSMIT_PAUSE_STATE | RO  | Transmit pause capability<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>0 = Disabled<br>1 = Enabled               | –       |

## Source Address Change Register (Page 01h: Address 0Eh)

**Table 79: Source Address Change Register (Page 01h: Address 0Eh–0Fh)**

| Bit  | Name            | R/W | Description                                                                                                                                                                                                                                                                                                                                                      | Default |
|------|-----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved        | RO  | –                                                                                                                                                                                                                                                                                                                                                                | 0       |
| 8:0  | SRC_ADDR_CHANGE | RC  | Source address change<br>Bit 8 = IMP port<br>Bits [4:0] correspond to ports [4:0], respectively.<br>The value of this bit is 1 if a change in the source address is detected on the given port.<br>The bit remains set until cleared by a read operation.<br>0 = No change in source address since last read.<br>1 = Source address has changed since last read. | 0       |

## Last Source Address Register (Page 01h: Address 10h)

**Table 80: Last Source Address Register Address Summary**

| Address | Description |
|---------|-------------|
| 10h–15h | Port 0      |
| 16h–1Bh | Port 1      |
| 1Ch–21h | Port 2      |
| 22h–27h | Port 3      |

**Table 80: Last Source Address Register Address Summary (Cont.)**

| <b>Address</b> | <b>Description</b> |
|----------------|--------------------|
| 28h–2Dh        | Port 4             |
| 2Eh–33h        | Port 5             |
| 34h–39h        | Reserved           |
| 3Ah–3Fh        | Reserved           |
| 40h–45h        | IMP port           |

**Table 81: Last Source Address (Page 01h: Address 10h–45h)**

| <b>Bit</b> | <b>Name</b>     | <b>R/W</b> | <b>Description</b>                                               | <b>Default</b> |
|------------|-----------------|------------|------------------------------------------------------------------|----------------|
| 47:0       | LAST_SOURCE_ADD | RO         | The 48-bit source address detected on the last packet ingressed. | 0              |

## Page 02h: Management/Mirroring Registers

**Table 82: Aging/Mirroring Registers (Page 02h)**

| Address | Bits | Register Name                                                                  |
|---------|------|--------------------------------------------------------------------------------|
| 00h     | 8    | "Global Management Configuration Register (Page 02h: Address 00h)" on page 169 |
| 01h–02h | –    | Reserved                                                                       |
| 03h     | 8    | "Broadcom Header Control Register (Page 02h: Address 03h)" on page 169         |
| 04h–05h | 16   | "RMON MIB Steering Register (Page 02h: Address 04h)" on page 170               |
| 06h–09h | 32   | "Aging Time Control Register (Page 02h: Address 06h)" on page 170              |
| 0Ah–0Fh | –    | Reserved                                                                       |
| 10h–11h | 16   | "Mirror Capture Control Register (Page 02h: Address 10h)" on page 170          |
| 12h–13h | 16   | "Ingress Mirror Control Register (Page 02h: Address 12h)" on page 171          |
| 14h–15h | 16   | "Ingress Mirror Divider Register (Page 02h: Address 14h)" on page 172          |
| 16h–1Bh | 48   | "Ingress Mirror MAC Address Register (Page 02h: Address 16h)" on page 172      |
| 1Ch–1Dh | 16   | "Egress Mirror Control Register (Page 02h: Address 1Ch)" on page 173           |
| 1Eh–1Fh | 16   | "Egress Mirror Divider Register (Page 02h: Address 1Eh)" on page 173           |
| 20h–25h | 48   | "Egress Mirror MAC Address Register (Page 02h: Address 20h)" on page 174       |
| 26h–EFh | –    | Reserved                                                                       |
| 30h–33h | 8    | Device ID number                                                               |
| 34h–3Fh | –    | Reserved                                                                       |
| 40h     | 8    | Revision ID number                                                             |
| 41h–4Fh | –    | Reserved                                                                       |
| 50h–53h | 32   | "High-Level Protocol Control Register (Page 02h: Address 50h–53h)" on page 175 |
| F0h–F7h | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, bytes 0–7           |
| F8h–FDh | –    | Reserved                                                                       |
| FEh     | 8    | "SPI Status Register (Global, Address FEh)" on page 295                        |
| FFh     | 8    | "Page Register (Global, Address FFh)" on page 295                              |

## Global Management Configuration Register (Page 02h: Address 00h)

**Table 83: Global Management Configuration Register (Page 02h: Address 00h)**

| Bit | Name        | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Default |
|-----|-------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:6 | En_IMP_Port | R/W | IMP port enable<br>00 = No frame management port.<br>01 = Reserved<br>10 = Enable IMP port only. All traffic to CPU from LAN and WAN ports will be forwarded to IMP port.<br>11 = Enable Dual-IMP ports (both IMP port and port 5). All traffic to CPU from LAN ports will be forwarded to IMP port and all traffic from WAN ports will be forwarded to Port 5.<br>These bits are ignored when SW_FWD_MODE = Unmanaged in the <a href="#">“Switch Mode Register (Page 00h: Address 0Bh)”</a> on page 150. | 00      |
| 5   | Reserved    | R/W | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0       |
| 4   | Intrpt_En   | R/W | Link status change interrupt enable<br>0 = Disable link status change interrupt<br>1 = Enable link status change interrupt                                                                                                                                                                                                                                                                                                                                                                                | 0       |
| 3:2 | Reserved    | R/W | —                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0       |
| 1   | En_Rx_BPDU  | R/W | Receive BPDU enable<br>Enables all ports to receive BPDUs and forwards to the IMP port. This bit must be set to globally allow BPDUs to be received.                                                                                                                                                                                                                                                                                                                                                      | 0       |
| 0   | Reset MIB   | R/W | Reset MIB counters<br>Resets all MIB counters for all ports to 0 (pages 20h–28h). This bit must be set and then cleared in successive write cycles to activate the reset operation.                                                                                                                                                                                                                                                                                                                       | 0       |

## Broadcom Header Control Register (Page 02h: Address 03h)

**Table 84: Broadcom Tag Control Register (Page 02h: Address 03h)**

| Bit | Name        | R/W | Description                                                                                                                                                                                                                                                                                                                                                        | Default |
|-----|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:2 | Reserved    | RO  | —                                                                                                                                                                                                                                                                                                                                                                  | 0       |
| 1:0 | BRCM_HDR_EN | R/W | Broadcom Tag enable for IMP<br>Bit 1 = Reserved<br>Bit 0 = Enable BRCM header for IMP port.<br><ul style="list-style-type: none"> <li>1 = Additional header information is inserted into the original frame, between original SA field and Type/Length fields. The tag includes the BRCM Tag field.</li> <li>0 = Without additional header information.</li> </ul> | 11      |

## RMON MIB Steering Register (Page 02h: Address 04h)

**Table 85: RMON MIB Steering Register (Page 02h: Address 04h–05h)**

| Bit  | Name                  | R/W | Description                                                                                                                                                                                                                                                                                                                                                             | Default |
|------|-----------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved              | R/W | –                                                                                                                                                                                                                                                                                                                                                                       | 0       |
| 8:0  | Override RMON Receive | R/W | <p>Override RMON receive</p> <p>Forces the RMON packet size bucket counters from the normal default of snooping on the receive side of the MAC to the transmit side. This allows the RMON bucket counters to snoop either transmit or receive, allowing full-duplex MAC support.</p> <p>Bit 8 = IMP port</p> <p>Bits [5:0] correspond to ports [5:0], respectively.</p> | 0       |

## Aging Time Control Register (Page 02h: Address 06h)

**Table 86: Aging Time Control Register (Page 02h: Address 06h–09h)**

| Bit   | Name       | R/W | Description                                                                                                                                                                                                                                                  | Default |
|-------|------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:21 | Reserved   | RO  | –                                                                                                                                                                                                                                                            | –       |
| 20    | Age Change | R/W | <p>Age change enable</p> <p>1 = Set age time using bits [19:0]</p> <p>0 = Age time default 300 ns</p>                                                                                                                                                        | 0       |
| 19:0  | AGE_TIME   | R/W | <p>Specifies the aging time in seconds for dynamically learned addresses. Maximum age time is 1,048,575s. Setting the AGE_TIME to 0 disables the aging process. For more information on ARL table aging, see <a href="#">“Address Aging” on page 62</a>.</p> | 300d    |

## Mirror Capture Control Register (Page 02h: Address 10h)

**Table 87: Mirror Capture Control Register (Page 02h: Address 10h–11h)**

| Bit  | Name          | R/W | Description                                                                                                                                                                                                                                                 | Default |
|------|---------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | Mirror Enable | R/W | <p>Global mirror enable</p> <p>0 = Disable mirror capture feature</p> <p>1 = Enable mirror capture feature</p>                                                                                                                                              | 0       |
| 14   | BLK_NOT_MIR   | R/W | <p>When enabled, all traffic to MIRROR_CAPTURE_PORT is blocked, except for mirror traffic. Nonmirror traffic is disabled.</p> <p>0 = No traffic blocking on mirror capture port</p> <p>1 = Traffic to mirror capture port blocked unless mirror traffic</p> | 0       |
| 13:4 | Reserved      | RO  | –                                                                                                                                                                                                                                                           | 0       |

**Table 87: Mirror Capture Control Register (Page 02h: Address 10h–11h) (Cont.)**

| Bit | Name         | R/W | Description                                                                                                                                                  | Default |
|-----|--------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 3:0 | Capture Port | R/W | Mirror capture port ID<br>Binary value identifies the single unique port that is designated as the port where all ingress and/or egress traffic is mirrored. | 0       |

For additional information about port mirroring, see [“Port Mirroring” on page 47](#).

## Ingress Mirror Control Register (Page 02h: Address 12h)

**Table 88: Ingress Mirror Control Register (Page 02h: Address 12h–13h)**

| Bit   | Name             | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Default |
|-------|------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:14 | IN_MIRROR_FILTER | R/W | Ingress mirror filter<br>Filters frames to be forwarded to the mirror capture port, specified in <a href="#">“Mirror Capture Control Register (Page 02h: Address 10h)” on page 170</a> .<br>00 = Mirror all ingress frames.<br>01 = Mirror all ingress frames with DA = IN_MIRROR_MAC.<br>10 = Mirror all ingress frames with SA = IN_MIRROR_MAC.<br>11 = Reserved<br>IN_MIRROR_MAC is specified in <a href="#">“Ingress Mirror MAC Address Register (Page 02h: Address 16h)” on page 172</a> .         | 0       |
| 13    | IN_DIV_EN        | R/W | Ingress divider enable<br>The ingress divider mirrors every $n^{\text{th}}$ ingress frame that has passed through the IN_MIRROR_FILTER (n represents the IN_MIRROR_DIV defined in <a href="#">“Ingress Mirror Divider Register (Page 02h: Address 14h)” on page 172</a> ).<br>0 = Disable ingress divider feature.<br>1 = Enable ingress divider feature.                                                                                                                                               | 0       |
| 12:9  | Reserved         | R/W | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 0       |
| 8:0   | IN_MIRROR_MASK   | R/W | Ingress mirror port mask<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>Ports with the corresponding bit set to 1 have ingress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an Ingress Mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the ingress mirrored port (s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter using bits [15:14] or divider using bit 13 may be helpful. | 0       |

For additional information about port mirroring, see [“Port Mirroring” on page 47](#).

## Ingress Mirror Divider Register (Page 02h: Address 14h)

**Table 89: Ingress Mirror Divider Register (Page 02h: Address 14h–15h)**

| Bit   | Name          | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                     | Default |
|-------|---------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:10 | Reserved      | RO  | –                                                                                                                                                                                                                                                                                                                                                                                                                               | 0       |
| 9:0   | IN_MIRROR_DIV | R/W | Ingress mirror divider<br>Receive frames that have passed the IN_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the IN_DIV_EN bit in the <a href="#">“Ingress Mirror Control Register (Page 02h: Address 12h)” on page 171</a> is set, frames that pass the IN_MIRROR_FILTER rule are further divided by n, where $n = \text{IN\_MIRROR\_DIV} + 1$ . | 0       |

For additional information about port mirroring, see [“Port Mirroring” on page 47](#).

## Ingress Mirror MAC Address Register (Page 02h: Address 16h)

**Table 90: Ingress Mirror MAC Address Register (Page 02h: Address 16h–1Bh)**

| Bit  | Name          | R/W | Description                                                                                                                                                                                                                | Default |
|------|---------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 47:0 | IN_MIRROR_MAC | R/W | Ingress mirror MAC address<br>MAC address that is compared against ingress frames in accordance with the IN_MIRROR_FILTER rules in <a href="#">“Ingress Mirror Control Register (Page 02h: Address 12h)” on page 171</a> . | 0       |

For additional information about port mirroring, see [“Port Mirroring” on page 47](#).

## Egress Mirror Control Register (Page 02h: Address 1Ch)

**Table 91: Egress Mirror Control Register (Page 02h: Address 1Ch–1Dh)**

| Bit   | Name              | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Default |
|-------|-------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:14 | OUT_MIRROR_FILTER | R/W | Egress mirror filter<br>Filters egress frames that are forwarded to the mirror capture port, specified in <a href="#">“Mirror Capture Control Register (Page 02h: Address 10h)”</a> on page 170.<br>00 = Mirror all egress frames.<br>01 = Mirror all egress frames with DA = OUT_MIRROR_MAC.<br>10 = Mirror all egress frames with SA = OUT_MIRROR_MAC.<br>11 = Reserved<br>OUT_MIRROR_MAC is specified in <a href="#">“Egress Mirror MAC Address Register (Page 02h: Address 20h)”</a> on page 174. | 0       |
| 13    | OUT_DIV_EN        | R/W | Egress divider enable<br>The egress divider mirrors every $n^{\text{th}}$ egress frame that has passed through the OUT_MIRROR_FILTER ( $n$ represents the OUT_MIRROR_DIV defined in <a href="#">“Egress Mirror Divider Register (Page 02h: Address 1Eh)”</a> on page 173).<br>0 = Disable egress divider feature.<br>1 = Enable egress divider feature.                                                                                                                                               | 0       |
| 12:9  | Reserved          | R/W | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0       |
| 8:0   | OUT_MIRROR_MASK   | R/W | Egress mirror port mask<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>Ports with the corresponding bit set to 1 have egress frames mirrored to the MIRROR_CAPTURE_PORT. While multiple ports can be set as an egress mirror port, severe congestion and/or frame loss may occur if excessive bandwidth from the egress mirrored port (s) is directed to the MIRROR_CAPTURE_PORT. Setting a mirror filter using bits [15:14] or a divider using bit 13 may be helpful. | 0       |

For additional information about port mirroring, see [“Port Mirroring”](#) on page 47.

## Egress Mirror Divider Register (Page 02h: Address 1Eh)

**Table 92: Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)**

| Bit   | Name     | R/W | Description | Default |
|-------|----------|-----|-------------|---------|
| 15:10 | Reserved | RO  | –           | 0       |

**Table 92: Egress Mirror Divider Register (Page 02h: Address 1Eh–1Fh)**

| Bit | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                            | Default |
|-----|----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 9:0 | OUT_MIRROR_DIV | R/W | Egress mirror divider<br>Egressed frames that have passed the OUT_MIRROR_FILTER rule can further be pruned to reduce the overall number of frames returned to the MIRROR_CAPTURE_PORT. When the OUT_DIV_EN bit in the <a href="#">“Egress Mirror Control Register (Page 02h: Address 1Ch)”</a> on page 173 is set, frames that pass the OUT_MIRROR_FILTER rule are further divided by n, where n = OUT_MIRROR_DIV + 1. | 0       |

For additional information about port mirroring, see [“Port Mirroring”](#) on page 47.

## Egress Mirror MAC Address Register (Page 02h: Address 20h)

**Table 93: Egress Mirror MAC Address Register (Page 02h: Address 20h–25h)**

| Bit  | Name           | R/W | Description                                                                                                                                                                                                                     | Default |
|------|----------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 47:0 | OUT_MIRROR_MAC | R/W | Egress mirror MAC address<br>MAC address that is compared against egress frames in accordance with the OUT_MIRROR_FILTER rules defined in <a href="#">“Egress Mirror Control Register (Page 02h: Address 1Ch)”</a> on page 173. | 0       |

For additional information about port mirroring, see [“Port Mirroring”](#) on page 47.

## Device ID Register (Page 02h: Address 30h–33h)

**Table 94: Device ID Register (Page 02h: Address 30h–33h)**

| Bit  | Name      | R/W | Description | Default      |
|------|-----------|-----|-------------|--------------|
| 31:0 | Device_ID | RO  | Device ID   | 32'0005_3115 |

## Revision Number Register (Page 02h: Address 40h)

**Table 95: Egress Mirror MAC Address Register (Page 02h: Address 40h)**

| Bit | Name        | R/W | Description     | Default |
|-----|-------------|-----|-----------------|---------|
| 7:0 | Revision_ID | RO  | Revision number | 0       |

## High-Level Protocol Control Register (Page 02h: Address 50h–53h)

**Table 96: High-Level Protocol Control Register (Page 02h: Address 50h–53h)**

| Bit   | Name                 | R/W | Description                                                                                                                                                                                                | Default |
|-------|----------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:19 | Reserved             | R/W | Reserved                                                                                                                                                                                                   | –       |
| 18    | MLD_QRY_FWD_MODE     | R/W | MLD Query Message Forwarding Mode<br>1 = MLD Query message frames will be trapped to CPU port only.<br>0 = MLD Query message frames will be forwarded by L2 result and also copied to CPU.                 | 0       |
| 17    | MLD_QRY_EN           | R/W | MLD Query Message Snooping/Redirect Enable<br>1 = Enable MLD query message snooping/redirect<br>0 = Disable                                                                                                | 0       |
| 16    | MLD_RPTDONE_FWD_MODE | R/W | MLD Report/Done Message Forwarding Mode<br>1 = MLD report/done message frames will be trapped to CPU port only<br>0 = MLD report/done message frames will be forwarded by L2 result and also copied to CPU | 0       |
| 15    | MLD_RPTDONE_EN       | R/W | MLD Report/Done Message Snooping/Redirect Enable<br>1 = Enable MLD report/done message snooping/redirect<br>0 = Disable                                                                                    | 0       |
| 14    | IGMP_UKN_FWD_MODE    | R/W | IGMP Unknown Message Forwarding Mode<br>1 = IGMP unknown message frames will be trapped to CPU port only<br>0 = IGMP unknown message frames will be forwarded by L2 result and also copied to CPU          | 0       |
| 13    | IGMP_UKN_EN          | R/W | IGMP Unknown Message Snooping/Redirect Enable<br>1 = Enable IGMP unknown message snooping/redirect<br>0 = Disable                                                                                          | 0       |
| 12    | IGMP_QRY_FWD_MODE    | R/W | IGMP Query Message Forwarding Mode<br>1 = IGMP query message frames will be trapped to CPU port only<br>0 = IGMP query message frames will be forwarded by L2 result and also copied to CPU                | 0       |
| 11    | IGMP_QRY_EN          | R/W | IGMP Query Message Snooping/Redirect Enable<br>1 = Enable IGMP query message Snooping/Redirect<br>0 = Disable                                                                                              | 0       |

**Table 96: High-Level Protocol Control Register (Page 02h: Address 50h–53h) (Cont.)**

| <b>Bit</b> | <b>Name</b>          | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                  | <b>Default</b> |
|------------|----------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 10         | IGMP_RPTLVE_FWD_MODE | R/W        | IGMP Report/Leave Message Forwarding Mode<br>1 = IGMP report/leave message frames will be trapped to CPU port only<br>0 = IGMP report/leave message frames will be forwarded by L2 result and also copied to CPU                                                                    | 0              |
| 9          | IGMP_RPTLVE_EN       | R/W        | IGMP Report/Leave Message Snooping/Redirect Enable<br>1 = Enable IGMP report/leave message Snooping/Redirect<br>0 = Disable                                                                                                                                                         | 0              |
| 8          | IGMP_DIP_EN          | R/W        | IGMP L3 DIP checking Enable<br>In addition to the IP datagram with a protocol value of 2, IGMP will be classified by matching its DIP with the Class D IP address(224.0.0.0–239.255.255.255).                                                                                       | 0              |
| 7:6        | Reserved             | R/W        | Reserved                                                                                                                                                                                                                                                                            | 0              |
| 5          | ICMPv6_FWD_MODE      | R/W        | ICMPv6 (exclude MLD) Forwarding Mode<br>1 = ICMPv6 frames will be trapped to CPU port only.<br>0 = ICMPv6 frames will be forwarded by L2 result and also copied to CPU.                                                                                                             | 0              |
| 4          | ICMPv6_EN            | R/W        | ICMPv6 (exclude MLD) Snooping/Redirect Enable<br>ICMPv6, with a next header value of 58, will be classified by IPv6 datagram.                                                                                                                                                       | 0              |
| 3          | ICMPv4_EN            | R/W        | ICMPv4 Snooping Enable<br>ICMPv6, with a next header value of 0 and extension header next header value of 58, will be classified by IPv6 datagram.<br>1 = ICMPv4 frames will be forwarded by L2 result and also copied to CPU.<br>0 = ICMPv4 frames will be forwarded by L2 result. | 0              |
| 2          | DHCP_EN              | R/W        | DHCP Snooping Enable<br>1 = DHCP frames will be forwarded by L2 result and also copied to CPU.<br>0 = DHCP frames will be forwarded by L2 result.                                                                                                                                   | 0              |
| 1          | RARP_EN              | R/W        | RARP Snooping Enable<br>1 = RARP frames will be forwarded by L2 result and also copied to CPU.<br>0 = RARP frames will be forwarded by L2 result.                                                                                                                                   | 0              |
| 0          | ARP_EN               | R/W        | ARP Snooping Enable<br>1 = ARP frames will be forwarded by L2 result and also copied to CPU.<br>0 = ARP frames will be forwarded by L2 result.                                                                                                                                      | 0              |

## Page 04h: ARL Control Register

**Table 97: ARL Control Registers (Page 04h)**

| Address | Bits | Register Name                                                              |
|---------|------|----------------------------------------------------------------------------|
| 00h     | 8    | "Global ARL Configuration Register (Page 04h: Address 00h)" on page 178    |
| 01h–03h | –    | Reserved                                                                   |
| 04h–09h | 48   | "BPDU Multicast Address Register (Page 04h: Address 04h)" on page 178      |
| 0Ah–0Dh | –    | Reserved                                                                   |
| 0Eh–0Fh | 16   | "Multiport Control Register (Page 04h: Address 0Eh–0Fh)" on page 179       |
| 10h–17h | 64   | "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 180 |
| 18h–1Bh | 32   | "Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 181  |
| 1Ch–1Fh | –    | Reserved                                                                   |
| 20h–27h | 64   | "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 180 |
| 28h–2Bh | 32   | "Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 181  |
| 2Ch–2Fh | –    | Reserved                                                                   |
| 30h–37h | 64   | "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 180 |
| 38h–3Bh | 32   | "Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 181  |
| 3Ch–3Fh | –    | Reserved                                                                   |
| 40h–47h | 64   | "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 180 |
| 48h–4Bh | 32   | "Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 181  |
| 4Ch–4Fh | –    | Reserved                                                                   |
| 50h–57h | 64   | "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 180 |
| 58h–5Bh | 32   | "Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 181  |
| 5Ch–5Fh | –    | Reserved                                                                   |
| 60h–67h | 64   | "Multiport Address N (N=0–5) Register (Page 04h: Address 10h)" on page 180 |
| 68h–6Bh | 32   | "Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)" on page 181  |
| 6Ch–FEh | –    | Reserved                                                                   |
| F0h–F7h | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, bytes 0–7       |
| F8h–FDh | –    | Reserved                                                                   |

**Table 97: ARL Control Registers (Page 04h) (Cont.)**

| Address | Bits | Register Name                                                           |
|---------|------|-------------------------------------------------------------------------|
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a> |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>       |

## Global ARL Configuration Register (Page 04h: Address 00h)

**Table 98: Global ARL Configuration Register (Page 04h: Address 00h)**

| Bit | Name           | R/W | Description                                                                                                                                                                                                                                                                                              | Default |
|-----|----------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:5 | Reserved       | RO  | –                                                                                                                                                                                                                                                                                                        | 0       |
| 4   | Reserved       | –   | –                                                                                                                                                                                                                                                                                                        | –       |
| 3   | Reserved       | RO  | –                                                                                                                                                                                                                                                                                                        | 0       |
| 2   | AGE_Accelerate | R/W | When enabled, the aging time is reduced by 1/128. –<br>1 = Accelerate the aging 128 times<br>0 = Keep the original age process                                                                                                                                                                           | –       |
| 1   | Reserved       | RO  | –                                                                                                                                                                                                                                                                                                        | 1       |
| 0   | Hash Disable   | R/W | Hash function disable<br>Disables the hash function of the ARL table so that entries are directly mapped to the table instead of being hashed to an index.<br>1 = Disable hash function<br>0 = Enable hash function<br>For more information see <a href="#">“Address Table Organization” on page 55.</a> | 0       |

## BPDU Multicast Address Register (Page 04h: Address 04h)

**Table 99: BPDU Multicast Address Register (Page 04h: Address 04h–09h)**

| Bit  | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                 | Default           |
|------|--------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| 47:0 | BPDU_MC_ADDR | R/W | BPDU multicast address 1<br>Defaults to the IEEE 802.1 defined reserved multicast address for the bridge group address. Programming to an alternate value allows support of proprietary protocols in place of the normal spanning tree protocol. Frames with a matching DA to this address are forwarded to the designated management port. | 01-80-c2-00-00-00 |

## Multiport Control Register (Page 04h: Address 0Eh–0Fh)

**Table 100: Multiport Control Register (Page 04h: Address 0Eh–0Fh)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                            | <b>Default</b> |
|------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15         | Reserved    | R/W        | Reserved                                                                                                                                                                                                                                                                                                      | 0              |
| 14:12      | Reserved    | RO         | Reserved                                                                                                                                                                                                                                                                                                      | 0              |
| 11:10      | MPORT_CTRL5 | R/W        | Multiport 5 control<br>00 = Disable Multiport 5 Forward.<br>10 = Compare MPORT_ADD5 only; Forward based on MPORT_Vector 5 if matched.<br>01 = Compare MPORT_ETYPE5 only; Forward based on MPORT_Vector 5 if matched.<br>11 = Compare MPORT_ETYPE5 and MPORT_ADD5; Forward based on MPORT_Vector 5 if matched. | 00             |
| 9:8        | MPORT_CTRL4 | R/W        | Multiport 4 control<br>00 = Disable Multiport 4 Forward.<br>10 = Compare MPORT_ADD4 only; Forward based on MPORT_Vector 4 if matched.<br>01 = Compare MPORT_ETYPE4 only; Forward based on MPORT_Vector 4 if matched.<br>11 = Compare MPORT_ETYPE4 and MPORT_ADD4; Forward based on MPORT_Vector 4 if matched. | 00             |
| 7:6        | MPORT_CTRL3 | R/W        | Multiport 3 control<br>00 = Disable Multiport 3 Forward.<br>10 = Compare MPORT_ADD3 only; Forward based on MPORT_Vector 3 if matched.<br>01 = Compare MPORT_ETYPE3 only; Forward based on MPORT_Vector 3 if matched.<br>11 = Compare MPORT_ETYPE3 and MPORT_ADD3; Forward based on MPORT_Vector 3 if matched. | 00             |
| 5:4        | MPORT_CTRL2 | R/W        | Multiport 2 control<br>00 = Disable Multiport 2 Forward.<br>10 = Compare MPORT_ADD2 only; Forward based on MPORT_Vector 2 if matched.<br>01 = Compare MPORT_ETYPE2 only; Forward based on MPORT_Vector 2 if matched.<br>11 = Compare MPORT_ETYPE2 and MPORT_ADD2; Forward based on MPORT_Vector 2 if matched. | 00             |
| 3:2        | MPORT_CTRL1 | R/W        | Multiport 1 control<br>00 = Disable Multiport 1 Forward.<br>10 = Compare MPORT_ADD1 only; Forward based on MPORT_Vector 1 if matched.<br>01 = Compare MPORT_ETYPE1 only; Forward based on MPORT_Vector 1 if matched.<br>11 = Compare MPORT_ETYPE1 and MPORT_ADD1; Forward based on MPORT_Vector 1 if matched. | 00             |

**Table 100: Multiport Control Register (Page 04h: Address 0Eh–0Fh) (Cont.)**

| Bit | Name        | R/W | Description                                                                                                                                                                                                                                                                                                   | Default |
|-----|-------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 1:0 | MPORT_CTRL0 | R/W | Multiport 0 control<br>00 = Disable Multiport 0 Forward.<br>10 = Compare MPORT_ADD0 only; Forward based on MPORT_Vector 0 if matched.<br>01 = Compare MPORT_ETYPE0 only; Forward based on MPORT_Vector 0 if matched.<br>11 = Compare MPORT_ETYPE0 and MPORT_ADD0; Forward based on MPORT_Vector 0 if matched. | 00      |

## Multiport Address N (N=0–5) Register (Page 04h: Address 10h)

**Table 101: Multiport Address Register Address Summary**

| Address | Description               |
|---------|---------------------------|
| 10h–17h | Multiport ETYPE address 0 |
| 20h–27h | Multiport ETYPE address 1 |
| 30h–37h | Multiport ETYPE address 2 |
| 40h–47h | Multiport ETYPE address 3 |
| 50h–57h | Multiport ETYPE address 4 |
| 60h–67h | Multiport ETYPE address 5 |

**Table 102: Multiport Address Register (Page 04h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h, 50h–57h, 60h–67h)**

| Bit   | Name        | R/W | Description                                                                                                                                                                                                                                                                                                 | Default          |
|-------|-------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|
| 64:48 | MPORT_ETYPE | R/W | Multiport Ethernet type<br>Allows a frames with a matching MPORT_ETYPE to this Length Type field to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector Register.<br>Must be enabled using the MPORT_CTRL bit in the Multiport Control Register. | 0000             |
| 47:0  | MPORT_ADDR  | R/W | Multiport Address<br>Allows a frames with a matching DA to this address to be forwarded to any programmable group of ports on the chip, as defined in the bit map in the Multiport Vector Register.<br>Must be enabled using the MPORT_CTRL bit in the Multiport Control Register.                          | 0000000<br>00000 |

## Multiport Vector N (N=0–5) Register (Page 04h: Address 18h)

**Table 103: Multiport Vector Register Address Summary**

| Address | Description        |
|---------|--------------------|
| 18h–1Bh | Multiport Vector 0 |
| 28h–2Bh | Multiport Vector 1 |
| 38h–3Bh | Multiport Vector 2 |
| 48h–4Bh | Multiport Vector 3 |
| 58h–5Bh | Multiport Vector 4 |
| 68h–6Bh | Multiport Vector 5 |

**Table 104: Multiport Vector Register (Page 04h:  
Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh, 58h–5Bh, 68h–6Bh)**

| Bit  | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                     | Default |
|------|--------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:9 | Reserved     | R/O | –                                                                                                                                                                                                                                                                                                                                               | 0       |
| 8:0  | MPORT_VCTR_N | R/W | <p>Multiport Vector</p> <p>A bit mask corresponding to the physical ports on the chip.</p> <p>A frame with a DA matching the content of the Multiport Address register are forwarded to each port with a bit set in the Multiport Vector bit map.</p> <p>Bits[5:0] correspond to ports[5:0]</p> <p>Bit 8 = Management port (MII management)</p> | 0       |

## Page 05h: ARL/VTBL Access Registers

**Table 105: ARL/VTBL Access Registers (Page 05h)**

| Address | Bits | Register Name                                                                                      |
|---------|------|----------------------------------------------------------------------------------------------------|
| 00h     | 8    | <a href="#">“ARL Table Read/Write Control Register (Page 05h: Address 00h)” on page 182</a>        |
| 01h–0Fh | –    | Reserved                                                                                           |
| 02h–07h | 48   | <a href="#">“MAC Address Index Register (Page 05h: Address 02h)” on page 183</a>                   |
| 08h–09h | 16   | <a href="#">“VLAN ID Index Register (Page 05h: Address 08h)” on page 183</a>                       |
| 0Ah–0Fh | –    | Reserved                                                                                           |
| 10h–17h | 64   | <a href="#">“ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)” on page 184</a> |
| 18h–1Bh | 16   | <a href="#">“ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 184</a>    |
| 1Ch–1Fh | –    | Reserved                                                                                           |

**Table 105: ARL/VTBL Access Registers (Page 05h) (Cont.)**

| Address | Bits | Register Name                                                                            |
|---------|------|------------------------------------------------------------------------------------------|
| 20h–27h | 64   | “ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)” on page 184       |
| 28h–2Bh | 32   | “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 184          |
| 2Ch–2Fh | –    | Reserved                                                                                 |
| 30h–37h | 64   | “ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)” on page 184       |
| 38h–3Bh | 32   | “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 184          |
| 3Ch–3Fh | –    | Reserved                                                                                 |
| 40h–47h | 64   | “ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)” on page 184       |
| 48h–4Bh | 32   | “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 184          |
| 4Ch–4Fh | –    | Reserved                                                                                 |
| 50h     | 8    | “ARL Table Search Control Register (Page 05h: Address 50h)” on page 186                  |
| 51h–52h | 16   | ARL Search Address                                                                       |
| 60h–77h | 64   | “ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)” on page 187 |
| 68h–7Bh | 32   | “ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)” on page 188    |
| 7Ch–7Fh | –    | Reserved                                                                                 |
| 80h     | 8    | “VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)” on page 189       |
| 81h–82h | 16   | “VLAN Table Address Index Register (Page 05h: Address 81h)” on page 190                  |
| 83h–86h | 32   | “VLAN Table Entry Register (Page 05h: Address 83h–86h)” on page 190                      |
| 67h–EFh | –    | Reserved                                                                                 |
| F0h–F7h | 8    | “SPI Data I/O Register (Global, Address F0h)” on page 294, bytes 0–7                     |
| F8h–FDh | –    | Reserved                                                                                 |
| FEh     | 8    | “SPI Status Register (Global, Address FEh)” on page 295                                  |
| FFh     | 8    | “Page Register (Global, Address FFh)” on page 295                                        |

## ARL Table Read/Write Control Register (Page 05h: Address 00h)

**Table 106: ARL Table Read/Write Control Register (Page 05h: Address 00h)**

| Bit | Name       | R/W         | Description                                                                                                                                                   | Default |
|-----|------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | START/DONE | R/W<br>(SC) | Start/done command<br>Write as 1 to initiate a read/write command to the ARL table. The bit returns to 0 to indicate that a read/write operation is complete. | 0       |

**Table 106: ARL Table Read/Write Control Register (Page 05h: Address 00h)**

| Bit | Name     | R/W | Description                                                                                                          | Default |
|-----|----------|-----|----------------------------------------------------------------------------------------------------------------------|---------|
| 6:1 | Reserved | RO  | —                                                                                                                    | —       |
| 0   | ARL_R/W  | R/W | ARL table read/write bit<br>Specifies whether the ARL command is a read or write operation.<br>1 = Read<br>0 = Write | 0       |

For more information, see [“Accessing the ARL Table Entries” on page 61](#).

## MAC Address Index Register (Page 05h: Address 02h)

**Table 107: MAC Address Index Register (Page 05h: Address 02h–07h)**

| Bit  | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                            | Default |
|------|----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 47:0 | MAC_ADDR_INDXX | R/W | MAC address index<br>The ARL table read/write command uses this 48-bit address to index the ARL table. When IEEE 802.1Q is enabled, the ARL table is indexed by a combined hash of the MAC_ADDR_INDXX and the VID_TBL_INDXX, defined in the <a href="#">“VLAN ID Index Register (Page 05h: Address 08h)” on page 183</a> .<br>For more information, see <a href="#">“Accessing the ARL Table Entries” on page 61</a> . | 0       |

## VLAN ID Index Register (Page 05h: Address 08h)

**Table 108: VLAN ID Index Register (Page 05h: Address 08h–09h)**

| Bit   | Name      | R/W | Description                                                                                                                                                                                                                                                                                                                                                      | Default |
|-------|-----------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:12 | Reserved  | R/W | —                                                                                                                                                                                                                                                                                                                                                                | 0       |
| 11:0  | VID_INDXX | R/W | VLAN ID index<br>When IEEE 802.1Q is enabled, the VLAN ID Index is used with the MAC_ADDR_INDXX, defined in the <a href="#">“MAC Address Index Register (Page 05h: Address 02h)” on page 183</a> , to form the hash index for which status is to be read or written.<br>For more information, see <a href="#">“Accessing the ARL Table Entries” on page 61</a> . | 0       |

## ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)

**Table 109: ARL Table MAC/VID Entry N (N = 0–3) Register Address Summary**

| Address | Description               |
|---------|---------------------------|
| 10h–17h | ARL Table MAC/VID Entry 0 |
| 20h–27h | ARL Table MAC/VID Entry 1 |
| 30h–37h | ARL Table MAC/VID Entry 2 |
| 40h–47h | ARL Table MAC/VID Entry 3 |

**Table 110: ARL Table MAC/VID Entry N (N = 0–3) Register  
(Page 05h: Address 10h–17h, 20h–27h, 30h–37h, 40h–47h)**

| Bit   | Name      | R/W | Description                                                                                                                                            | Default |
|-------|-----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 63:60 | Reserved  | R/O | –                                                                                                                                                      | 0       |
| 59:48 | VID_N     | R/W | VID entry N<br>The VID field is either read from or written to the ARL table entry N.<br>The VID is a “don’t-care” field when IEEE 802.1Q is disabled. | 0       |
| 47:0  | MACADDR_N | R/W | MAC address entry N<br>The 48-bit MAC Address field to be either read from or written to the ARL table entry N.                                        | 0       |



**Note:** Together, the “ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)” on page 184 and the “ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)” on page 184 compose a complete entry in the ARL table. For more information, see “Accessing the ARL Table Entries” on page 61.

## ARL Table Data Entry N (N = 0–3) Register (Page 05h: Address 18h)

**Table 111: ARL Table Data Entry N (N = 0–3) Register Address Summary**

| Address | Description            |
|---------|------------------------|
| 18h–1Bh | ARL Table Data Entry 0 |
| 28h–2Bh | ARL Table Data Entry 1 |
| 38h–3Bh | ARL Table Data Entry 2 |
| 48h–4Bh | ARL Table Data Entry 3 |

**Table 112: ARL Table Data Entry N (N = 0–3) Register**  
**(Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh)**

| Bit   | Name     | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Default |
|-------|----------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:17 | Reserved | RO  | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0       |
| 16    | VALID_N  | R/W | Valid bit entry N<br>Write this bit to 1 to indicate that a valid MAC address is stored in the MACADDR_N field defined in the “ <a href="#">ARL Table MAC/VID Entry N (N = 0–3) Register (Page 05h: Address 10h)</a> ” on <a href="#">page 184</a> , and that the entry has not aged out. Reset when an entry is empty.<br>This information is read from or written to the ARL table during a read/write command.                                                                                                                                                                                                                                | 0       |
| 15    | STATIC_N | RW  | Static bit entry N<br>Write this bit to 1 to indicate that the entry is controlled by the external register control. When cleared, the internal learning and aging process controls the validity of the entry. This information is read from or written to the ARL table during a read/write command.                                                                                                                                                                                                                                                                                                                                            | 0       |
| 14    | AGE_N    | R/W | Age bit entry N<br>Write this bit to 1 to indicate that an address entry has been learned or accessed. This bit is set to 0 by the internal aging algorithm. If the internal aging process detects that a valid entry has remained unused for the period set by the AGE_TIME (defined in the “ <a href="#">Aging Time Control Register (Page 02h: Address 06h)</a> ” on <a href="#">page 170</a> ) and the entry has not been marked as static, the entry has the valid bit cleared.<br>The age bit is ignored if the entry has been marked as Static.<br>This information is read from or written to the ARL table during a read/write command. | 0       |
| 13:11 | TC_N     | R/W | TC bit for MAC-based QoS entry N<br>These bits define the TC field for MAC-based QoS packets.<br>This information is read from or written to the ARL table during a read/write command.                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0       |
| 10:9  | Reserved | R/W | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | –       |

**Table 112: ARL Table Data Entry N (N = 0–3) Register**  
**(Page 05h: Address 18h–1Bh, 28h–2Bh, 38h–3Bh, 48h–4Bh) (Cont.)**

| Bit | Name          | R/W | Description                                                                                                                                                                                                                                                              | Default |
|-----|---------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 8:0 | FWD_PRT_MAP_N | R/W | Multicast Group Forward portmap entry N<br>For multicast entries, these bits define the forward port map.<br>Bit 8 = CPU port/MII port<br>Bits [5:0] correspond to ports [5:0], respectively.                                                                            | 0       |
|     | PORTID_N      | –   | Unicast Forward PortID entry N<br>For unicast entries, these bits define the port number associated with the entry of the ARL table.<br>Bits [8:4] = Reserved<br>Bits [3:0] = Port ID/Port Number which identifies where the station with unique MACADDR_N is connected. | 0       |

## ARL Table Search Control Register (Page 05h: Address 50h)

**Table 113: ARL Table Search Control Register (Page 05h: Address 50h)**

| Bit | Name         | R/W         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Default |
|-----|--------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | START/DONE   | R/W<br>(SC) | Start/done<br>Write as 1 to initiate a sequential search of the ARL table. Each entry found by the search is returned to the “ <a href="#">ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)</a> ” on page 188 and the “ <a href="#">ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)</a> ” on page 187. Reading the “ <a href="#">ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)</a> ” on page 188 allows the ARL table search to continue.<br>BCM53115S clears this bit when the ARL table search is complete. | 0       |
| 6:1 | Reserved     | RO          | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0       |
| 0   | ARL_SR_VALID | RC          | ARL search result valid<br>Set by BCM53115S to indicate that an ARL entry is found by the ARL table search. The found entry is available in the “ <a href="#">ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)</a> ” on page 188.<br>This bit automatically returns to 0 after the ARL Search Result register is read.                                                                                                                                                                                                                                             | 0       |

For more information, see “[Accessing the ARL Table Entries](#)” on page 61.

## ARL Search Address Register (Page 05h: Address 51h)

**Table 114: ARL Search Address Register (Page 05h: Address 51h–52h)**

| Bit  | Name           | R/W         | Description                                                                                                                                                                                                                              | Default |
|------|----------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | ARL_ADDR_VALID | R/W<br>(SC) | ARL address valid<br>Indicates the lower 15 bits of this register contain a valid internal representation of the ARL entry that is currently being accessed. Intended for factory test/diagnostic use only.                              | 0       |
| 14:0 | ARL_ADDR       | –           | ARL address<br>14-bit internal representation of the address of the ARL entry currently being accessed by the ARL search routine. This is not a direct address of the ARL location and is intended for factory test/diagnostic use only. | 0       |

## ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h)

**Table 115: ARL Table Search MAC/VID Result N (N=0-1) Register Address Summary**

| Address | Description                       |
|---------|-----------------------------------|
| 60h–67h | ARL Table Search MAC/VID Result 0 |
| 70h–77h | ARL Table Search MAC/VID Result 1 |

**Table 116: ARL Table Search MAC/VID Result N (N=0-1) Register (Page 05h: Address 60h–67h, 70h–77h)**

| Bit   | Name         | R/W | Description                                                                                                                       | Default |
|-------|--------------|-----|-----------------------------------------------------------------------------------------------------------------------------------|---------|
| 63:60 | Reserved     | RO  | –                                                                                                                                 | 0       |
| 59:48 | ARL_SR_VID_N | RO  | ARL search VID result<br>These bits store the VID of the ARL table entry found by the ARL table search function.                  | 0       |
| 47:0  | ARL_SR_MAC_N | RO  | ARL search MAC address result.<br>These bits store the MAC address of the ARL table entry found by the ARL table search function. | N/A     |

For more information, see [“Accessing the ARL Table Entries” on page 61](#).

## ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h)

**Table 117: ARL Table Search Data Result N (N=0-1) Register Address Summary**

| Address | Description                    |
|---------|--------------------------------|
| 68h–6Bh | ARL Table Search Data Result 0 |
| 78h–7Bh | ARL Table Search Data Result 1 |

**Table 118: ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh)**

| Bit   | Name            | R/W | Description                                                                                                                                                                                                                                           | Default |
|-------|-----------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:17 | Reserved        | RO  | –                                                                                                                                                                                                                                                     | 0       |
| 16    | ARL_SR_VALID_N  | RO  | ARL search valid bit result<br>This bit stores the valid bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.   | 0       |
| 15    | ARL_SR_STATIC_N | RO  | ARL search static bit result<br>This bit stores the static bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching. | N/A     |
| 14    | ARL_SR_AGE_N    | RO  | ARL search age bit result<br>This bit stores the Age bit of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.       | –       |
| 13:11 | ARL_SR_TC_N     | RO  | ARL search TC bits result<br>These bits store the TC bits of the ARL table entry found by the ARL table search function. Reading this register clears the data from the register and allows the ARL table search function to continue searching.      | –       |
| 10:9  | Reserved        | RO  | –                                                                                                                                                                                                                                                     | 0       |

**Table 118: ARL Table Search Data Result N (N=0-1) Register (Page 05h: Address 68h–6Bh, 78h–7Bh)**

| Bit | Name          | R/W | Description                                                                                                                                                                                                                                                              | Default |
|-----|---------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 8:0 | FWD_PRT_MAP_N | R/W | Multicast Group Forward portmap entry N<br>For multicast entries, these bits define the forward port map.<br>Bit 8 = CPU port/MII port<br>Bits [5:0] correspond to ports [5:0]                                                                                           | 0       |
|     | PORTID_N      | –   | Unicast Forward PortID entry N<br>For unicast entries, these bits define the port number associated with the entry of the ARL table.<br>Bits [8:4] = Reserved<br>Bits [3:0] = Port ID/Port Number which identifies where the station with unique MACADDR_N is connected. | 0       |

For more information, see [“Accessing the ARL Table Entries” on page 61](#).

## VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)

**Table 119: VLAN Table Read/Write/Clear Control Register (Page 05h: Address 80h)**

| Bit | Name         | R/W         | Description                                                                                                                                                                                                    | Default |
|-----|--------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | START/DONE   | R/W<br>(SC) | Start/done command<br>Write as 1 to initiate a read or write or clear-table command to the VLAN table. The bit returns to 0 to indicate that the read or write or clear-table operation is complete.           | 0       |
| 6:2 | Reserved     | R/W         | –                                                                                                                                                                                                              | –       |
| 1:0 | VTBL_R/W/Clr | R/W         | Read/Write/Clear-table<br>Specifies whether the current VLAN table read/write/clear-table command is a read or write or clear-table operation.<br>11 = Reserved<br>10 = Clear-table<br>01 = Read<br>00 = Write | 0       |

See [“Programming the VLAN Table” on page 40](#) for more information.

## VLAN Table Address Index Register (Page 05h: Address 81h)

**Table 120: VLAN Table Address Index Register (Page 05h: Address 81h–82h)**

| Bit   | Name          | R/W | Description                                                                                                     | Default |
|-------|---------------|-----|-----------------------------------------------------------------------------------------------------------------|---------|
| 15:12 | Reserved      | RO  | –                                                                                                               | 0       |
| 11:0  | VTBL_ADDR_IND | R/W | VLAN table address index<br>The current VLAN table read/write uses this 12-bit address to index the VLAN table. | –       |

See “Programming the VLAN Table” on page 40 for more information.

## VLAN Table Entry Register (Page 05h: Address 83h–86h)

**Table 121: VLAN Table Entry Register (Page 05h: Address 83h–86h)**

| Bit   | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Default |
|-------|------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:22 | Reserved   | RO  | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 0       |
| 21    | FWD_MODE   | R/W | This indicates whether the packet forwarding should be based on VLAN membership or based on ARL flow.<br>1 = Based on VLAN membership (excluding Ingress port)<br>0 = Based on ARL flow.<br>Note that the VLAN membership based forwarding mode is only used for certain ISP Tagged packets received from ISP port when BCM53115S is operating in Double-Tag mode.                                                                                                   | 0       |
| 20:18 | MSPT_INDEX | R/W | Index for 8 spanning trees                                                                                                                                                                                                                                                                                                                                                                                                                                           | 0       |
| 17:9  | UNTAG_MAP  | R/W | Untagged port map<br>Bit 17 = CPU Port/MII Port<br>Bits [14:9] correspond to ports [5:0], respectively.<br>Ports written to 1 are designated as untagged VLAN ports.<br>VLAN-tagged frames destined for these ports are untagged before they are forwarded.<br>When the IEEE 802.1Q feature is enabled, frames sent using the CPU (MII port configured as a management port) are tagged.<br>Note that the packet forwarded to IMP port should always be VLAN tagged. | –       |

**Table 121: VLAN Table Entry Register (Page 05h: Address 83h–86h) (Cont.)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                         | <b>Default</b> |
|------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 8:0        | FWD_MAP     | R/W        | Forward PORT MAP<br>The VLAN-tagged Frame is allowed to be forwarded to the destination ports corresponding bits set in the Map Ports written to 1 are designated as capable of receiving VLAN-tagged frames.<br>Bit 8 = CPU Port/MII Port<br>Bits [7:6] = Reserved<br>Bits [5:0] correspond to Ports [5:0], respectively. | —              |

See [“Programming the VLAN Table” on page 40](#) for more information.

## Page 10h–14h: Internal GPHY MII Registers

**Table 122: 10/100/1000 PHY Page Summary**

| <b>Page</b> | <b>Description</b>                |
|-------------|-----------------------------------|
| 10h         | Port 0 Internal PHY MII Registers |
| 11h         | Port 1 Internal PHY MII Registers |
| 12h         | Port 2 Internal PHY MII Registers |
| 13h         | Port 3 Internal PHY MII Registers |
| 14h         | Port 4 Internal PHY MII Registers |

**Table 123: Register Map (Page 10h–14h)**

| <b>SPI Offset Address</b>                       | <b>MII Address</b> | <b># of Bits</b> | <b>Register Table</b>                                                                                    |
|-------------------------------------------------|--------------------|------------------|----------------------------------------------------------------------------------------------------------|
| <b>10BASE-T/100BASE-TX/1000BASE-T Registers</b> |                    |                  |                                                                                                          |
| 00h                                             | 00h                | 16               | Table 124: “MII Control Register (Page 10h–14h: Address 00h–01h),” on page 194                           |
| 02h                                             | 01h                | 16               | Table 125: “MII Status Register (Page 10h–14h: Address 02h–03h),” on page 195                            |
| 04h–06h                                         | 02h                | 32               | Table 126: “PHY Identifier Register MSB (Page 10h–14h: Address 04–07h),” on page 196                     |
| 08h                                             | 04h                | 16               | Table 128: “Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h),” on page 196        |
| 0Ah                                             | 05h                | 16               | Table 129: “Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh),” on page 197 |
| 0Ch                                             | 06h                | 16               | Table 129: “Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh),” on page 197 |
| 0Eh                                             | 07h                | 16               | Table 131: “Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh),” on page 199                    |
| 10h                                             | 08h                | 16               | Table 132: “Link Partner Received Next Page Register (Page 10h–14h: Address 10h–11h),” on page 200       |
| 12h                                             | 09h                | 16               | Table 133: “1000BASE-T Control Register (Page 10h–14h: Address 12h–13h),” on page 201                    |
| 14h                                             | 0Ah                | 16               | Table 134: “1000BASE-T Status Register (Page 10h–14h: Address 14h–15h),” on page 202                     |
| 16h–1Dh                                         | –                  | 16               | Reserved (Do not read from or write to a reserved register.)                                             |
| 1Eh                                             | 0Fh                | 16               | Table 135: “IEEE Extended Status Register (Page 10h–14h: Address 1Eh–1Fh),” on page 203                  |
| 20h                                             | 10h                | 16               | Table 136: “PHY Extended Control Register (Page 10h–14h: Address 20h–21h),” on page 204                  |
| 22h                                             | 11h                | 16               | Table 137: “PHY Extended Status Register (Page 10h–14h: Address 22h–23h),” on page 205                   |

**Table 123: Register Map (Page 10h–14h) (Cont.)**

| <b>SPI Offset Address</b>                                                                                                                         | <b>MI1 Address</b> | <b># of Bits</b> | <b>Register Table</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24h                                                                                                                                               | 12h                | 16               | Table 138: “Receive Error Counter Register (Page 10h–14h: Address 24h–25h),” on page 206                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 26h                                                                                                                                               | 13h                | 16               | Table 139: “False Carrier Sense Counter Register (Page 10h–14h: Address 26h–27h),” on page 206                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 28h                                                                                                                                               | 14h                | 16               | Table 141: “Receiver NOT_OK Counter Register (Page 10h–14h: Address 28h–29h),” on page 207                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2Ah–2Ch                                                                                                                                           | 15h–16h            |                  | Reserved (Do not read from or write to a reserved register except for accessing the Expansion registers through register 15h.)                                                                                                                                                                                                                                                                                                                                                                                         |
| 2Eh                                                                                                                                               | 17h                | 16               | Table 143: “Expansion Register Access Register (Page 10h–14h: Address 2Eh–2Fh),” on page 208                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 30h                                                                                                                                               | 18h                | 16               | Table 148: “Auxiliary Control Register (Page 10h–14h: Address 30h, Shadow Value 000),” on page 210<br>Table 149: “10BASE-T Register (Page 10h–14h: Address 30h, Shadow Value 001),” on page 211<br>Table 150: “Power/MI1 Control Register (Page 10h–14h: Address 30h, Shadow Value 010),” on page 212<br>Table 151: “Miscellaneous Test Register (Page 10h–14h: Address 30h, Shadow Value 100),” on page 213<br>Table 152: “Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111),” on page 213 |
| 32h                                                                                                                                               | 19h                | 16               | Table 153: “Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h),” on page 214                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 34h                                                                                                                                               | 1Ah                | 16               | Table 154: “Interrupt Status Register (Page 10h–14h: Address 34h–35h),” on page 216                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 36h                                                                                                                                               | 1Bh                | 16               | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 38h                                                                                                                                               | 1Ch                | 16               | Table 156: “Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100),” on page 217<br>Table 156: “Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100),” on page 217<br>Table 157: “Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010),” on page 218<br>Table 159: “Mode Control Register (Page 10h–14h: Address 38h, Shadow Value 11111),” on page 220                                                                                                      |
| 3Ah                                                                                                                                               | 1Dh                | 16               | Table 160: “Master/Slave Seed Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 0,” on page 221<br>Table 161: “HCD Status Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 1,” on page 222                                                                                                                                                                                                                                                                                                                            |
| 3Ch                                                                                                                                               | 1Eh                | 16               | Table 162: “Test Register 1 (Page 10h–14h: Address 3C–3Dh),” on page 223                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 3Eh                                                                                                                                               | 1Fh                | 16               | Reserved (Do not read from or write to a reserved register.)                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| <b>Expansion Registers: Read/Write through Register 2Ah (Accessed by Writing to Register 2Eh, Bits [11:0] = 1111 + Expansion Register Number)</b> |                    |                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 00h                                                                                                                                               | –                  | –                | Table 163: “Expansion Register 00h: Receive/Transmit Packet Counter,” on page 224                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 123: Register Map (Page 10h–14h) (Cont.)**

| <b>SPI Offset Address</b> | <b>MII Address</b> | <b># of Bits</b> | <b>Register Table</b>                                                                        |
|---------------------------|--------------------|------------------|----------------------------------------------------------------------------------------------|
| 01h                       | –                  | –                | <a href="#">Table 164: “Expansion Register 01h: Expansion Interrupt Status,” on page 224</a> |
| 04h                       | –                  | –                | –                                                                                            |
| 05h                       | –                  | –                | –                                                                                            |
| 07h                       | –                  | –                | –                                                                                            |
| 45h                       | –                  | –                | <a href="#">Table 165: “Expansion Register 45h: Transmit CRC,” on page 225</a>               |

## MII Control Register (Page 10h–14h: Address 00h–01h)

**Table 124: MII Control Register (Page 10h–14h: Address 00h–01h)**

| <b>Bit</b> | <b>Name</b>              | <b>R/W</b> | <b>Description</b>                                                               | <b>Default</b> |
|------------|--------------------------|------------|----------------------------------------------------------------------------------|----------------|
| 15         | Reset                    | R/W<br>SC  | 1 = PHY reset<br>0 = Normal operation                                            | 0              |
| 14         | Internal Loopback        | R/W        | 1 = Loopback mode<br>0 = Normal operation                                        | 0              |
| 13         | Speed Selection (LSB)    | R/W        | Bits [6,13]:<br>11 = Reserved<br>10 = 1000 Mbps<br>01 = 100 Mbps<br>00 = 10 Mbps | 0              |
| 12         | Auto-negotiation Enable  | R/W        | 1 = Auto-negotiation is enabled.<br>0 = Auto-negotiation is disabled.            | 1              |
| 11         | Power Down               | R/W        | 1 = Power-down<br>0 = Normal operation                                           | 0              |
| 10         | Isolate                  | R/W        | 1 = Electrically isolate PHY from GMII.<br>0 = Normal operation                  | 0              |
| 9          | Restart Auto-negotiation | R/W<br>SC  | 1 = Restarting auto-negotiation<br>0 = Auto-negotiation restart is complete.     | 0              |
| 8          | Duplex Mode              | R/W        | 1 = Full duplex<br>0 = Half duplex                                               | 1              |
| 7          | Collision Test Enable    | R/W        | 1 = Enable the collision test mode.<br>0 = Disable the collision test mode.      | 0              |
| 6          | Speed Selection (MSB)    | R/W        | Works in conjunction with bit 13                                                 | 1              |
| 5          | Reserved                 | R/W        | Write as 0, ignore on read.                                                      | 0              |
| 4          | Reserved                 | R/W        | Write as 0 ignore on read                                                        | 0              |
| 3          | Reserved                 | R/W        | Write as 0 ignore on read                                                        | 0              |
| 2          | Reserved                 | R/W        | Write as 0 ignore on read                                                        | 0              |
| 1          | Reserved                 | R/W        | Write as 0 ignore on read                                                        | 0              |

**Table 124: MII Control Register (Page 10h–14h: Address 00h–01h) (Cont.)**

| Bit | Name     | R/W | Description               | Default |
|-----|----------|-----|---------------------------|---------|
| 0   | Reserved | R/W | Write as 0 ignore on read | 0       |

## MII Status Register (Page 10h–14h: Address 02h)

**Table 125: MII Status Register (Page 10h–14h: Address 02h–03h)**

| Bit | Name                                   | R/W      | Description                                                                                 | Default |
|-----|----------------------------------------|----------|---------------------------------------------------------------------------------------------|---------|
| 15  | 100BASE-T4 Capable                     | RO<br>L  | 1 = 100BASE-T4 capable<br>0 = Not 100BASE-T4 capable                                        | 0       |
| 14  | 100BASE-X Full-Duplex Capable          | RO<br>H  | 1 = 100BASE-X full-duplex capable<br>0 = Not 100BASE-X full-duplex capable                  | 1       |
| 13  | 100BASE-X Half-Duplex Capable          | RO<br>H  | 1 = 100BASE-X half-duplex capable<br>0 = Not 100BASE-X half-duplex capable                  | 1       |
| 12  | 10BASE-T Full-Duplex Capable           | RO<br>H  | 1 = 10BASE-T full-duplex capable<br>0 = Not 10BASE-T full-duplex capable                    | 1       |
| 11  | 10BASE-T Half-Duplex Capable           | RO<br>H  | 1 = 10BASE-T half-duplex capable<br>0 = Not 10BASE-T half-duplex capable                    | 1       |
| 10  | 100BASE-T2 Full-Duplex Capable         | RO<br>L  | 1 = 100BASE-T2 full-duplex capable<br>0 = Not 100BASE-T2 full-duplex capable                | 0       |
| 9   | 100BASE-T2 Half-Duplex Capable         | RO<br>L  | 1 = 100BASE-T2 half-duplex capable<br>0 = Not 100BASE-T2 half-duplex capable                | 0       |
| 8   | Extended Status                        | RO<br>H  | 1 = Extended status information in reg 0Fh<br>0 = No extended status information in reg 0Fh | 1       |
| 7   | Reserved                               | RO       | Ignore on read.                                                                             | 0       |
| 6   | Management Frames Preamble Suppression | RO<br>H  | 1 = Preamble can be suppressed.<br>0 = Preamble always required                             | 1       |
| 5   | Auto-negotiation Complete              | RO       | 1 = Auto-negotiation is complete.<br>0 = Auto-negotiation is in progress.                   | 0       |
| 4   | Remote Fault                           | RO<br>LH | 1 = Remote fault detected.<br>0 = No remote fault detected.                                 | 0       |
| 3   | Auto-negotiation Ability               | RO<br>H  | 1 = Auto-negotiation capable<br>0 = Not auto-negotiation capable                            | 1       |
| 2   | Link Status                            | RO<br>LL | 1 = Link is up (link pass state).<br>0 = Link is down (link fail state).                    | 0       |
| 1   | Jabber Detect                          | RO<br>LH | 1 = Jabber condition detected.<br>0 = No jabber condition detected.                         | 0       |
| 0   | Extended Capability                    | RO<br>H  | 1 = Extended register capabilities<br>0 = No extended register capabilities                 | 1       |

## PHY Identifier Register (Page 10h–14h: Address 04h)

**Table 126: PHY Identifier Register MSB (Page 10h–14h: Address 04–07h)**

| Bit  | Name | R/W | Description                                     | Default    |
|------|------|-----|-------------------------------------------------|------------|
| 15:0 | OUI  | RO  | Bits 3:18 of organizationally unique identifier | 0143 (hex) |

**Table 127: PHY Identifier Register LSB (Page 10h–14h: Address 06h–07h)**

| Bit   | Name     | R/W | Description                                      | Default     |
|-------|----------|-----|--------------------------------------------------|-------------|
| 15:10 | OUI      | RO  | Bits 19:24 of organizationally unique identifier | 101111      |
| 9:4   | MODEL    | RO  | Device model number                              | 111000      |
| 3:0   | REVISION | RO  | Device revision number                           | $n^a$ (hex) |

- a. The revision number ( $n$ ) changes with each silicon revision.

The IEEE has issued an Organizationally Unique Identifier (OUI) to Broadcom Corporation. This 24-bit number allows devices developed by Broadcom to be distinguished from all other manufacturers. The OUI combined with model numbers and revision numbers assigned by Broadcom precisely identifies a device manufactured by Broadcom.

The [15:0] bits of MII register 02h (PHYID HIGH) contain OUI bits [3:18]. The [15:0] bits of MII register 03h (PHYID LOW) contain the most significant OUI bits [19:24], six manufacturer's model number bits, and four revision number bits. The two least significant OUI binary bits are not used.

Broadcom Corporation's OUI is 00-0A-F7, expressed as hexadecimal values. The binary OUI is 0000-0000-0000-1010-1111-0111. The model number for BCM53115S is 38h. Revision numbers start with 0h and increment by 1 for each chip modification.

- PHYID HIGH[15:0] = OUI[3:18]
- PHYID LOW[15:0] = OUI[19:24] + Model[5:0] + Revision [3:0]

## Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h)

**Table 128: Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h)**

| Bit | Name         | R/W | Description                                                                           | Default |
|-----|--------------|-----|---------------------------------------------------------------------------------------|---------|
| 15  | Next Page    | R/W | 1 = Next page ability is supported.<br>0 = Next page ability is not supported.        | 0       |
| 14  | Reserved     | R/W | Write as 0, ignore on read.                                                           | 0       |
| 13  | Remote Fault | R/W | 1 = Advertise remote fault is detected.<br>0 = Advertise no remote fault is detected. | 0       |

**Table 128: Auto-Negotiation Advertisement Register (Page 10h–14h: Address 08h–09h) (Cont.)**

| Bit | Name                           | R/W | Description                                                                    | Default |
|-----|--------------------------------|-----|--------------------------------------------------------------------------------|---------|
| 12  | Reserved Technology            | R/W | Write as 0, ignore on read.                                                    | 0       |
| 11  | Asymmetric Pause               | R/W | 1 = Advertise asymmetric pause<br>0 = Advertise no asymmetric pause            | 1       |
| 10  | Pause Capable                  | R/W | 1 = Capable of full-duplex pause operation<br>0 = Incapable of pause operation | 0       |
| 9   | 100BASE-T4 Capable             | R/W | 1 = 100BASE-T4 capable<br>0 = Not 100BASE-T4 capable                           | 0       |
| 8   | 100BASE-TX Full-Duplex Capable | R/W | 1 = 100BASE-TX full-duplex capable<br>0 = Not 100BASE-TX full-duplex capable   | 1       |
| 7   | 100BASE-TX Half-Duplex Capable | R/W | 1 = 100BASE-TX half-duplex capable<br>0 = Not 100BASE-TX half-duplex capable   | 1       |
| 6   | 10BASE-T Full-Duplex Capable   | R/W | 1 = 10BASE-T full-duplex capable<br>0 = Not 10BASE-T full-duplex capable       | 1       |
| 5   | 10BASE-T Half-Duplex Capable   | R/W | 1 = 10BASE-T half-duplex capable<br>0 = Not 10BASE-T half-duplex capable       | 1       |
| 4   | Protocol Selector Field        | R/W | Bits [4:0] = 00001 indicates IEEE 802.3 CSMA/CD                                | 0       |
| 3   | –                              | R/W | –                                                                              | 0       |
| 2   | –                              | R/W | –                                                                              | 0       |
| 1   | –                              | R/W | –                                                                              | 0       |
| 0   | –                              | R/W | –                                                                              | 1       |

## Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah)

**Table 129: Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh)**

| Bit | Name                          | R/W | Description                                                                                          | Default |
|-----|-------------------------------|-----|------------------------------------------------------------------------------------------------------|---------|
| 15  | Next Page                     | RO  | 1 = Link partner has next page ability.<br>0 = Link partner does not have next page ability.         | 0       |
| 14  | Acknowledge                   | RO  | 1 = Link partner has received link code word.<br>0 = Link partner has not received link code word.   | 0       |
| 13  | Remote Fault                  | RO  | 1 = Link partner has detected remote fault.<br>0 = Link partner has not detected remote fault.       | 0       |
| 12  | Reserved Technology           | RO  | Write as 0, ignore on read.                                                                          | 0       |
| 11  | Link Partner Asymmetric Pause | RO  | 1 = Link partner wants asymmetric pause.<br>0 = Link partner does not want asymmetric pause.         | 0       |
| 10  | Pause Capable                 | RO  | 1 = Link partner is capable of pause operation.<br>0 = Link partner is incapable of pause operation. | 0       |

**Table 129: Auto-Negotiation Link Partner Ability Register (Page 10h–14h: Address 0Ah–0Bh) (Cont.)**

| Bit | Name                           | R/W | Description                                                                                                    | Default |
|-----|--------------------------------|-----|----------------------------------------------------------------------------------------------------------------|---------|
| 9   | 100BASE-T4 Capable             | RO  | 1 = Link partner is 100BASE-T4 capable.<br>0 = Link partner is not 100BASE-T4 capable.                         | 0       |
| 8   | 100BASE-TX Full-Duplex Capable | RO  | 1 = Link partner is 100BASE-TX full-duplex capable.<br>0 = Link partner is not 100BASE-TX full-duplex capable. | 0       |
| 7   | 100BASE-TX Half-Duplex Capable | RO  | 1 = Link partner is 100BASE-TX half-duplex capable.<br>0 = Link partner not 100BASE-TX half-duplex capable.    | 0       |
| 6   | 10BASE-T Full-Duplex Capable   | RO  | 1 = Link partner is 10BASE-T full-duplex capable.<br>0 = Link partner is not 10BASE-T full-duplex capable.     | 0       |
| 5   | 10BASE-T Half-Duplex Capable   | RO  | 1 = Link partner is 10BASE-T half-duplex capable.<br>0 = Link partner is not 10BASE-T half-duplex capable.     | 0       |
| 4   | Protocol Selector Field        | RO  | Link partner protocol selector field                                                                           | 0       |
| 3   |                                | RO  |                                                                                                                | 0       |
| 2   |                                | RO  |                                                                                                                | 0       |
| 1   |                                | RO  |                                                                                                                | 0       |
| 0   |                                | RO  |                                                                                                                | 0       |



**Note:** As indicated by bit 5 of the 10BASE-T/100BASE-TX/1000BASE-T MII Status register, the values contained in the 10BASE-T/100BASE-TX/1000BASE-T Auto-negotiation Link Partner Ability register are only guaranteed to be valid after auto-negotiation has successfully completed.

## Next Page

BCM53115S returns a 1 in bit 15 when the link partner wants to transmit Next Page information.

## Acknowledge

BCM53115S returns a 1 in bit 14 when the link partner has acknowledged reception of the link code word; otherwise, BCM53115S returns a 0.

## Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch)

**Table 130: Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch–0Dh)**

| Bit | Name     | R/W | Description     | Default |
|-----|----------|-----|-----------------|---------|
| 15  | Reserved | RO  | Ignore on read. | 0       |
| 14  | Reserved | RO  | Ignore on read. | 0       |
| 13  | Reserved | RO  | Ignore on read. | 0       |

**Table 130: Auto-Negotiation Expansion Register (Page 10h–14h: Address 0Ch–0Dh) (Cont.)**

| Bit | Name                                  | R/W      | Description                                                                                                                                  | Default |
|-----|---------------------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 12  | Reserved                              | RO       | Ignore on read.                                                                                                                              | 0       |
| 11  | Reserved                              | RO       | Ignore on read.                                                                                                                              | 0       |
| 10  | Reserved                              | RO       | Ignore on read.                                                                                                                              | 0       |
| 9   | Reserved                              | RO       | Ignore on read.                                                                                                                              | 0       |
| 8   | Reserved                              | RO       | Ignore on read.                                                                                                                              | 0       |
| 7   | Reserved                              | RO       | Ignore on read.                                                                                                                              | 0       |
| 6   | Next Page Receive Location Able       | R/W      | 1 = Bit 5 in register 06h determines next page receive location.<br>0 = Bit 5 in register 06h does not determine next page receive location. | 1       |
| 5   | Next Page Receive Location            | R/W      | 1 = Next pages stored in register 08h.<br>0 = Next pages stored in register 05h.                                                             | 1       |
| 4   | Parallel Detection Fault              | RO<br>LH | 1 = Parallel link fault is detected.<br>0 = Parallel link fault is not detected.                                                             | 0       |
| 3   | Link Partner Next Page Ability        | RO       | 1 = Link partner has next page capability.<br>0 = Link partner does not have next page capability.                                           | 0       |
| 2   | Next Page Capable                     | RO<br>H  | 1 = BCM53115S is next page capable.<br>0 = BCM53115S is not next page capable.                                                               | 1       |
| 1   | Page Received                         | RO<br>LH | 1 = New page has been received from link partner.<br>0 = New page has not been received.                                                     | 0       |
| 0   | Link Partner Auto-negotiation Ability | RO       | 1 = Link partner has auto-negotiation capability.<br>0 = Link partner does not have auto-negotiation.                                        | 0       |

## Next Page Transmit Register (Page 10h–14h: Address 0Eh)

**Table 131: Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh)**

| Bit | Name         | R/W | Description                                                                                                        | Default |
|-----|--------------|-----|--------------------------------------------------------------------------------------------------------------------|---------|
| 15  | Next Page    | R/W | 1 = Additional next pages follow.<br>0 = Sending last next page.                                                   | 0       |
| 14  | Reserved     | RO  | Ignore on read.                                                                                                    | 0       |
| 13  | Message Page | R/W | 1 = Formatted page<br>0 = Unformatted page                                                                         | 1       |
| 12  | Acknowledge2 | R/W | 1 = Complies with message.<br>0 = Cannot comply with message.<br><b>Note:</b> Not used with 1000BASE-T next pages. | 0       |
| 11  | Toggle       | RO  | Toggles between exchanges of different next 0 pages.                                                               | 0       |

**Table 131: Next Page Transmit Register (Page 10h–14h: Address 0Eh–0Fh) (Cont.)**

| Bit | Name                           | R/W | Description                                | Default |
|-----|--------------------------------|-----|--------------------------------------------|---------|
| 10  | Message/Unformatted Code Field | R/W | Next page message code or unformatted data | 0       |
| 9   |                                | R/W |                                            | 0       |
| 8   |                                | R/W |                                            | 0       |
| 7   |                                | R/W |                                            | 0       |
| 6   |                                | R/W |                                            | 0       |
| 5   |                                | R/W |                                            | 0       |
| 4   |                                | R/W |                                            | 0       |
| 3   |                                | R/W |                                            | 0       |
| 2   |                                | R/W |                                            | 0       |
| 1   |                                | R/W |                                            | 0       |
| 0   |                                | R/W |                                            | 1       |

## Link Partner Received Next Page Register (Page 10h–14h: Address 10h)

**Table 132: Link Partner Received Next Page Register (Page 10h–14h: Address 10h–11h)**

| Bit | Name         | R/W | Description                                                                                                      | Default |
|-----|--------------|-----|------------------------------------------------------------------------------------------------------------------|---------|
| 15  | Next Page    | RO  | 1 = Additional next pages follow<br>0 = Sending last next page                                                   | 0       |
| 14  | Acknowledge  | RO  | 1 = Acknowledge<br>0 = No acknowledge                                                                            | 0       |
| 13  | Message Page | RO  | 1 = Formatted page<br>0 = Unformatted page                                                                       | 0       |
| 12  | Acknowledge2 | RO  | 1 = Complies with message<br>0 = Cannot comply with message<br><b>Note:</b> Not used with 1000BASE-T next pages. | 0       |
| 11  | Toggle       | RO  | Toggles between exchanges of different next pages                                                                | 0       |

**Table 132: Link Partner Received Next Page Register (Page 10h–14h: Address 10h–11h) (Cont.)**

| Bit | Name               | R/W | Description                                | Default |
|-----|--------------------|-----|--------------------------------------------|---------|
| 10  | Message Code field | RO  | Next page message code or unformatted data | 0       |
| 9   |                    | RO  |                                            | 0       |
| 8   |                    | RO  |                                            | 0       |
| 7   |                    | RO  |                                            | 0       |
| 6   |                    | RO  |                                            | 0       |
| 5   |                    | RO  |                                            | 0       |
| 4   |                    | RO  |                                            | 0       |
| 3   |                    | RO  |                                            | 0       |
| 2   |                    | RO  |                                            | 0       |
| 1   |                    | RO  |                                            | 0       |
| 0   |                    | RO  |                                            | 0       |

## 1000BASE-T Control Register (Page 10h–14h: Address 12h)

**Table 133: 1000BASE-T Control Register (Page 10h–14h: Address 12h–13h)**

| Bit | Name                                        | R/W | Description                                                                                             | Default |
|-----|---------------------------------------------|-----|---------------------------------------------------------------------------------------------------------|---------|
| 15  | Test Mode                                   | R/W | 1 X X = Test mode 4 — Transmitter distortion test.                                                      | 0       |
| 14  |                                             | R/W | 0 1 1 = Test mode 3 — Slave transmit jitter test.                                                       | 0       |
| 13  |                                             | R/W | 0 1 0 = Test mode 2 — Master transmit jitter test.                                                      | 0       |
|     |                                             |     | 0 0 1 = Test mode 1 — Transmit waveform test.                                                           |         |
|     |                                             |     | 0 0 0 = Normal operation                                                                                |         |
| 12  | Master/Slave Configuration Enable           | R/W | 1 = Enable master/slave manual configuration value.<br>0 = Automatic master/slave configuration         | 0       |
| 11  | Master/Slave Configuration Value            | R/W | 1 = Configure PHY as master.<br>0 = Configure PHY as slave.                                             | 1       |
| 10  | Repeater/DTE                                | R/W | 1 = Repeater/switch device port<br>0 = DTE device                                                       | 1       |
| 9   | Advertise 1000BASE-T Full-Duplex Capability | R/W | 1 = Advertise 1000BASE-T full-duplex capability.<br>0 = Advertise no 1000BASE-T full-duplex capability. | 1       |
| 8   | Advertise 1000BASE-T Half-Duplex Capability | R/W | 1 = Advertise 1000BASE-T half-duplex capability.<br>0 = Advertise no 1000BASE-T half-duplex capability. | 1       |
| 7   | Reserved                                    | RO  | Ignore on read.                                                                                         | 0       |
| 6   | Reserved                                    | RO  | Ignore on read.                                                                                         | 0       |
| 5   | Reserved                                    | RO  | Ignore on read.                                                                                         | 0       |

**Table 133: 1000BASE-T Control Register (Page 10h–14h: Address 12h–13h) (Cont.)**

| Bit | Name     | R/W | Description     | Default |
|-----|----------|-----|-----------------|---------|
| 4   | Reserved | RO  | Ignore on read. | 0       |
| 3   | Reserved | RO  | Ignore on read. | 0       |
| 2   | Reserved | RO  | Ignore on read. | 0       |
| 1   | Reserved | RO  | Ignore on read. | 0       |
| 0   | Reserved | RO  | Ignore on read. | 0       |

## Test Mode

The BCM53115S can be placed in 1 of 4 transmit test modes by writing bits [15:13] of the 1000BASE-T Control register. The transmit test modes are defined in IEEE 802.3ab. When read, these bits return the last value written. For test modes 1, 2, and 4, the PHY must have auto-negotiation disabled and forced to 1000BASE-T mode and Auto-MDIX disabled.

- Disable auto-negotiation and force to 1000BASE-T mode (write to register 00h = 0x0040)
- Disable Auto-MDIX (write to register 18h, shadow value 111, bit 9 = 0)
- Enter test modes (write to register 09h, bits [15:13] = the desired test mode)

## Master/Slave Configuration Enable

When bit 12 is set = 1, the BCM53115S master/slave mode is configured using the manual master/slave configuration value. When the bit is cleared, the master/slave mode is configured using the automatic resolution function. This bit returns a 1 when manual master/slave configuration is enabled; otherwise, it returns a 0.

## 1000BASE-T Status Register (Page 10h–14h: Address 14h)

**Table 134: 1000BASE-T Status Register (Page 10h–14h: Address 14h–15h)**

| Bit | Name                                           | R/W      | Description                                                                                                    | Default |
|-----|------------------------------------------------|----------|----------------------------------------------------------------------------------------------------------------|---------|
| 15  | Master/Slave Configuration Fault               | RO<br>LH | 1 = Master/slave configuration fault detected.<br>0 = No master/slave configuration fault detected.            | 0       |
| 14  | Master/Slave Configuration Resolution          | RO       | 1 = Local transmitter is master.<br>0 = Local transmitter is slave.                                            | 0       |
| 13  | Local Receiver Status                          | RO       | 1 = Local receiver is OK.<br>0 = Local receiver is not OK.                                                     | 0       |
| 12  | Remote Receiver Status                         | RO       | 1 = Remote receiver is OK.<br>0 = Remote receiver is not OK.                                                   | 0       |
| 11  | Link Partner 1000BASE-T Full-Duplex Capability | RO       | 1 = Link partner is 1000BASE-T full-duplex capable.<br>0 = Link partner is not 1000BASE-T full-duplex capable. | 0       |

**Table 134: 1000BASE-T Status Register (Page 10h–14h: Address 14h–15h)**

| Bit | Name                                           | R/W | Description                                                                                                 | Default |
|-----|------------------------------------------------|-----|-------------------------------------------------------------------------------------------------------------|---------|
| 10  | Link Partner 1000BASE-T Half-Duplex Capability | RO  | 1 = Link partner is 1000BASE-T half-duplex capable. 0 = Link partner is not 1000BASE-T half-duplex capable. | 0       |
| 9   | Reserved                                       | RO  | Ignore on read.                                                                                             | 0       |
| 8   | Reserved                                       | RO  | Ignore on read.                                                                                             | 0       |
| 7   | Idle Error Count                               | RO  | Number of idle errors since last read                                                                       | 0       |
|     |                                                | CR  |                                                                                                             |         |
| 6   |                                                | RO  |                                                                                                             |         |
|     |                                                | CR  |                                                                                                             |         |
| 5   |                                                | RO  |                                                                                                             |         |
|     |                                                | CR  |                                                                                                             |         |
| 4   |                                                | RO  |                                                                                                             |         |
|     |                                                | CR  |                                                                                                             |         |
| 3   |                                                | RO  |                                                                                                             |         |
|     |                                                | CR  |                                                                                                             |         |
| 2   |                                                | RO  |                                                                                                             |         |
|     |                                                | CR  |                                                                                                             |         |
| 1   |                                                | RO  |                                                                                                             |         |
|     |                                                | CR  |                                                                                                             |         |
| 0   |                                                | RO  |                                                                                                             |         |
|     |                                                | CR  |                                                                                                             |         |



**Note:** As indicated by bit 5 of the MII Status register (0h), the values contained in bits 14, 11, and 10 of the 1000BASE-T Status register are guaranteed to be valid only after auto-negotiation has successfully completed.

## IEEE Extended Status Register (Page 10h–14h: Address 1Eh)

**Table 135: IEEE Extended Status Register (Page 10h–14h: Address 1Eh–1Fh)**

| Bit | Name                           | R/W | Description                            | Default |
|-----|--------------------------------|-----|----------------------------------------|---------|
| 15  | 1000BASE-X Full-Duplex Capable | RO  | 1 = 1000BASE-X full-duplex capable     | 0       |
|     |                                | L   | 0 = Not 1000BASE-X full-duplex capable |         |
| 14  | 1000BASE-X Half-Duplex Capable | RO  | 1 = 1000BASE-X half-duplex capable     | 0       |
|     |                                | L   | 0 = Not 1000BASE-X half-duplex capable |         |
| 13  | 1000BASE-T Full-Duplex Capable | RO  | 1 = 1000BASE-T full-duplex capable     | 1       |
|     |                                | H   | 0 = Not 1000BASE-T full-duplex capable |         |

**Table 135: IEEE Extended Status Register (Page 10h–14h: Address 1Eh–1Fh)**

| Bit | Name                           | R/W     | Description                                                                  | Default |
|-----|--------------------------------|---------|------------------------------------------------------------------------------|---------|
| 12  | 1000BASE-T Half-Duplex Capable | RO<br>H | 1 = 1000BASE-T half-duplex capable<br>0 = Not 1000BASE-T half-duplex capable | 1       |
| 11  | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 10  | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 9   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 8   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 7   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 6   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 5   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 4   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 3   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 2   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 1   | Reserved                       | RO      | Ignore on read.                                                              | 0       |
| 0   | Reserved                       | RO      | Ignore on read.                                                              | 0       |

## PHY Extended Control Register (Page 10h–14h: Address 20h)

**Table 136: PHY Extended Control Register (Page 10h–14h: Address 20h–21h)**

| Bit   | Name                                         | R/W       | Description                                                                                 | Default |
|-------|----------------------------------------------|-----------|---------------------------------------------------------------------------------------------|---------|
| 15    | Reserved                                     | R/W       | Write as 0, ignore on read.                                                                 | 0       |
| 14    | Disable Automatic MDI Crossover              | R/W       | 1 = Automatic MDI crossover is disabled.<br>0 = Automatic MDI crossover is enabled.         | 0       |
| 13    | Transmit Disable                             | R/W       | 1 = Transmitter outputs are disabled.<br>0 = Normal operation                               | 0       |
| 12:11 | Reserved                                     | —         | —                                                                                           | —       |
| 10    | Bypass 4B/5B Encoder/Decoder (100BASE-T)     | R/W       | 1 = Transmit and receive 5B codes over MII pins.<br>0 = Normal MII                          | 0       |
| 9     | Bypass Scrambler/Descrambler (100BASE-T)     | R/W       | 1 = Scrambler and descrambler are disabled.<br>0 = Scrambler and descrambler are enabled.   | 0       |
| 8     | Bypass NRZI/MLT3 Encoder/Decoder (100BASE-T) | R/W       | 1 = Bypass NRZI/MLT3 encoder and decoder.<br>0 = Normal operation                           | 0       |
| 7     | Bypass Receive Symbol Alignment (100BASE-T)  | R/W       | 1 = The 5B receive symbols are not aligned.<br>0 = Receive symbols aligned to 5B boundaries | 0       |
| 6     | Reset Scrambler (100BASE-T)                  | R/W<br>SC | 1 = Reset scrambler to initial state.<br>0 = Normal scrambler operation                     | 0       |
| 5:3   | Reserved                                     | —         | —                                                                                           | —       |

**Table 136: PHY Extended Control Register (Page 10h–14h: Address 20h–21h)**

| Bit | Name                                   | R/W | Description                         | Default |
|-----|----------------------------------------|-----|-------------------------------------|---------|
| 2   | Reserved                               | R/W | Write as 0, ignore on read.         | 0       |
| 1   | Reserved                               | R/W | Write as 0, ignore on read.         | 0       |
| 0   | 1000 Mbps PCS Transmit FIFO Elasticity | R/W | 1 = High latency<br>0 = Low latency | 0       |

## PHY Extended Status Register (Page 10h–14h: Address 22h)

**Table 137: PHY Extended Status Register (Page 10h–14h: Address 22h–23h)**

| Bit | Name                                               | R/W      | Description                                                                                                                                  | Default |
|-----|----------------------------------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15  | Auto-negotiation Base Page Selector Field Mismatch | RO<br>LH | 1 = Link partner base page selector field mismatched advertised selector field since last read.<br>0 = No mismatch detected since last read. | 0       |
| 14  | Ethernet@WireSpeed Downgrade                       | RO       | 1 = Auto-negotiation advertised speed downgraded<br>0 = No advertised speed downgrade                                                        | 0       |
| 13  | MDI Crossover State                                | RO       | 1 = Crossover MDI mode<br>0 = Normal MDI mode                                                                                                | 0       |
| 12  | Interrupt Status                                   | RO       | 1 = Unmasked interrupt is currently active.<br>0 = Interrupt is cleared.                                                                     | 0       |
| 11  | Remote Receiver Status                             | RO<br>LL | 1 = Remote receiver is OK.<br>0 = Remote receiver is not OK since last read                                                                  | 0       |
| 10  | Local Receiver Status                              | RO<br>LL | 1 = Local receiver is OK.<br>0 = Local receiver is not OK since last read.                                                                   | 0       |
| 9   | Locked                                             | RO       | 1 = Descrambler is locked.<br>0 = Descrambler is unlocked.                                                                                   | 0       |
| 8   | Link Status                                        | RO       | 1 = Link pass<br>0 = Link fail                                                                                                               | 0       |
| 7   | CRC Error Detected                                 | RO<br>LH | 1 = CRC error detected.<br>0 = No CRC error since last read.                                                                                 | 0       |
| 6   | Carrier Extension Error Detected                   | RO<br>LH | 1 = Carrier extension error detected since last read.<br>0 = No carrier extension error since last read.                                     | 0       |
| 5   | Bad SSD Detected (False Carrier)                   | RO<br>LH | 1 = Bad SSD error detected since last read.<br>0 = No bad SSD error since last read.                                                         | 0       |
| 4   | Bad ESD Detected (Premature End)                   | RO<br>LH | 1 = Bad ESD error detected since last read.<br>0 = No bad ESD error since last read.                                                         | 0       |
| 3   | Receive Error Detected                             | RO<br>LH | 1 = Receive error detected since last read.<br>0 = No receive error since last read.                                                         | 0       |
| 2   | Transmit Error Detected                            | RO<br>LH | 1 = Transmit error code received since last read.<br>0 = No transmit error code received since last read.                                    | 0       |

**Table 137: PHY Extended Status Register (Page 10h–14h: Address 22h–23h) (Cont.)**

| Bit | Name                     | R/W      | Description                                                                              | Default |
|-----|--------------------------|----------|------------------------------------------------------------------------------------------|---------|
| 1   | Lock Error Detected      | RO<br>LH | 1 = Lock error detected since last read.<br>0 = No lock error since last read.           | 0       |
| 0   | MLT3 Code Error Detected | RO<br>LH | 1 = MLT3 code error detected since last read.<br>0 = No MLT3 code error since last read. | 0       |

## Receive Error Counter Register (Page 10h–14h: Address 24h)

**Table 138: Receive Error Counter Register (Page 10h–14h: Address 24h–25h)<sup>a</sup>**

| Bit  | Name                  | R/W       | Description                                                            | Default |
|------|-----------------------|-----------|------------------------------------------------------------------------|---------|
| 15:0 | Receive Error Counter | R/W<br>CR | The number of noncollision packets with receive errors since last read | 0000h   |

- a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, 1000BASE-T Receive Error Counter when register 38h, shadow value 11011, bit 9 = 0.

## Copper Receive Error Counter

When bit 9 = 0 in register 38h, shadow value 11011, this counter increments each time BCM53115S receives a 10BASE-T, 100BASE-TX, 1000BASE-T noncollision packet containing at least one receive error. This counter freezes at the maximum value of FFFFh. The counter automatically clears when read.

## False Carrier Sense Counter Register (Page 10h–14h: Address 26h)

**Table 139: False Carrier Sense Counter Register (Page 10h–14h: Address 26h–27h)<sup>a</sup>**

| Bit  | Name                        | R/W       | Description                                               | Default |
|------|-----------------------------|-----------|-----------------------------------------------------------|---------|
| 15:8 | Reserved                    | RO        | Ignore on read.                                           | 00h     |
| 7:0  | False Carrier Sense Counter | R/W<br>CR | The number of false carrier sense events since last read. | 00h     |

- a. Bits 7:0 of this register become the 10BASE-T/100BASE-TX/1000BASE-T Carrier Sense Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch, bit 14 = 0.

## Copper False Carrier Sense Counter

When bit 9 = 0 in register 1Ch, shadow value 11011 and bit 14 = 0 in register 3Ch, the False Carrier Sense Counter increments each time the BCM53115S detects a 10BASE-T, 100BASE-TX, 1000BASE-T false carrier sense on the receive input. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

## 10BASE-T/100BASE-TX/1000BASE-T Packets Received with Transmit Error Codes Counter

**Table 140: 10BASE-T/100BASE-TX/1000BASE-T Transmit Error Code Counter Register (Address 13h)<sup>a</sup>**

| Bit  | Name                        | R/W       | Description                                                               | Default |
|------|-----------------------------|-----------|---------------------------------------------------------------------------|---------|
| 15:8 | Reserved                    | RO        | Write as 0, ignore on read.                                               | 00h     |
| 7:0  | Transmit Error Code Counter | R/W<br>CR | The number of packets received with transmit error codes since last read. | 00h     |

- a. Bits 7:0 of this register become the 10BASE-T/100BASE-TX/1000BASE-T packets received with transmit error codes counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch, bit 14 = 1.

### Packets Received with Transmit Error Codes Counter

BCM53115S detects a 10BASE-T/100BASE-TX/1000BASE-T packet with a transmit error code violation when bit 9 = 0 in register 38h, shadow value 11011, and when bit 14 = 1 in register 1Eh, Packets Received with Transmit Error Codes Counter increments each time. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

## Receiver NOT\_OK Counter Register (Page 10h–14h: Address 28h)

**Table 141: Receiver NOT\_OK Counter Register (Page 10h–14h: Address 28h–29h)<sup>a</sup>**

| Bit  | Name                           | R/W       | Description                                                                                 | Default |
|------|--------------------------------|-----------|---------------------------------------------------------------------------------------------|---------|
| 15:8 | Local Receiver NOT_OK Counter  | R/W<br>CR | The number of times local receiver was NOT_OK since last read.                              | 00h     |
| 7:0  | Remote Receiver NOT_OK Counter | R/W<br>CR | The number of times BCM53115S detected that the remote receiver was NOT_OK since last read. | 00h     |

- a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, or 1000BASE-T Receiver NOT\_OK Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch bit 15 = 0.

### Copper Local Receiver NOT\_OK Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 0 in register 3Ch, this counter increments each time the 10BASE-T, 100BASE-TX, or 1000BASE-T local receiver enters the NOT\_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

### Copper Remote Receiver NOT\_OK Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 0 in register 3Ch, this counter increments each time the 1000BASE-T, 100BASE-TX, or 10BASE-T remote receiver enters the NOT\_OK state. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

## Receive CRC Counter Register (Page 10h–14h: Address 28h)

**Table 142: CRC Counter Register (Page 10h–14h: Address 28h–29h)<sup>a</sup>**

| Bit  | Name                | R/W       | Description                                           | Default |
|------|---------------------|-----------|-------------------------------------------------------|---------|
| 15:0 | Receive CRC Counter | R/W<br>CR | The number of times receive CRC errors were detected. | 00h     |

- a. Bits 15:0 of this register become the 10BASE-T, 100BASE-TX, or 1000BASE-T Receive CRC Counter when register 38h, shadow 11011, bit 9 = 0 and register 3Ch bit 15 = 1.

## Copper CRC Counter

When bit 9 = 0 in register 38h, shadow value 11011 and bit 15 = 1 in register 3Ch, this counter increments each time the 10BASE-T, 100BASE-TX, or 1000BASE-T detects a receive CRC error. This counter freezes at the maximum value of FFh. The counter automatically clears when read.

## Expansion Register Access Register (Page 10h–14h: Address 2Eh)

**Table 143: Expansion Register Access Register (Page 10h–14h: Address 2Eh–2Fh)**

| Bit | Name                        | R/W | Description                                                                  | Default |
|-----|-----------------------------|-----|------------------------------------------------------------------------------|---------|
| 15  | Reserved                    | R/W | Write as 0, ignore on read.                                                  | 0       |
| 14  | Reserved                    | R/W | Write as 0, ignore on read.                                                  | 0       |
| 13  | Reserved                    | R/W | Write as 0, ignore on read.                                                  | 0       |
| 12  | Reserved                    | R/W | Write as 0, ignore on read.                                                  | 0       |
| 11  | Expansion Register Select   | R/W | 1111 = Expansion register is selected.                                       | 0       |
| 10  |                             | R/W | 0000 = Expansion register is not selected.                                   | 0       |
| 9   |                             | R/W | All others = Reserved (Do not use)                                           | 0       |
| 8   |                             | R/W |                                                                              | 0       |
| 7   | Expansion Register Accessed | R/W | Sets the expansion register number accessed when read/write to register 2Ah. | 0       |
| 6   |                             | R/W |                                                                              | 0       |
| 5   |                             | R/W |                                                                              | 0       |
| 4   |                             | R/W |                                                                              | 0       |
| 3   |                             | R/W |                                                                              | 0       |
| 2   |                             | R/W |                                                                              | 0       |
| 1   |                             | R/W |                                                                              | 0       |
| 0   |                             | R/W |                                                                              | 0       |

## Expansion Register Select

Setting bits [11:8] to 1111 enables the reading from and writing to the Expansion registers in conjunction with register 2Ah. These bits should be cleared after the Expansion registers are accessed or when the Expansion registers are not being accessed. See [“Expansion Registers” on page 224](#) for Expansion register detail.

## Expansion Register Accessed

The Expansion registers can be accessed through register 2Ah when bits [11:8] of this register are set to 1111. The available expansion registers are listed in [Table 144](#).

**Table 144: Expansion Register Select Values**

| Expansion Register | Register Name                                                        |
|--------------------|----------------------------------------------------------------------|
| 00h                | <a href="#">“Expansion Register 01h: Expansion Interrupt Status”</a> |

## Auxiliary Control Shadow Value Access Register (Page 10h–14h: Address 30h)

Available 30h registers are listed in the [Table 145](#).

**Table 145: Auxiliary Control Shadow Values Access Register (Page 10h–14h: Address 30h)**

| Shadow Value | Register Name                                                                                              |
|--------------|------------------------------------------------------------------------------------------------------------|
| 000          | <a href="#">“Auxiliary Control Shadow Values Access Register (Page 10h–14h: Address 30h)” on page 209</a>  |
| 001          | <a href="#">“10BASE-T Register (Page 10h–14h: Address 30h, Shadow Value 001)” on page 211</a>              |
| 010          | <a href="#">“Power/MII Control Register (Page 10h–14h: Address 30h, Shadow Value 010)” on page 212</a>     |
| 100          | <a href="#">“Miscellaneous Test Register (Page 10h–14h: Address 30h, Shadow Value 100)” on page 213</a>    |
| 111          | <a href="#">“Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111)” on page 213</a> |

Read from register 30h, shadow value zzz.

**Table 146: Reading Register 30h**

| Register Reads/Writes                | Description                                                                                                                  |
|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| Write register 30h, bits [2:0] = 111 | Selects miscellaneous control register, shadow value 111: All reads must be done through the miscellaneous control register. |
| Bit 15 = 0                           | Allows only bits [14:12] and bits [2:0] to be written                                                                        |
| Bits [14:12] = zzz                   | Selects shadow value register zzz to be read                                                                                 |
| Bits [11:3] = <don't care>           | When bit 15 = 0, these bits are ignored.                                                                                     |
| Bits [2:0] = 111                     | Sets shadow register select to 111 (miscellaneous control register)                                                          |

**Table 146: Reading Register 30h (Cont.)**

| <b>Register Reads/Writes</b> | <b>Description</b>                                    |
|------------------------------|-------------------------------------------------------|
| Read register 30h            | Data read back is the value from shadow register zzz. |

Write to register 30h, shadow value yyy.

**Table 147: Writing Register 30h**

| <b>Register Writes</b>                   | <b>Description</b>                                                                                       |
|------------------------------------------|----------------------------------------------------------------------------------------------------------|
| Set Bits [15:3] = Preferred write values | Bits [15:3] contain the values to which the desired bits are written.                                    |
| Set Bits [2:0] = yyy                     | This enables shadow value register yyy to be written. For shadow value 111, bit 15 must also be written. |

**Table 148: Auxiliary Control Register (Page 10h–14h: Address 30h, Shadow Value 000)**

| <b>Bit</b> | <b>Name</b>                    | <b>R/W</b> | <b>Description</b>                                                                                             | <b>Default</b> |
|------------|--------------------------------|------------|----------------------------------------------------------------------------------------------------------------|----------------|
| 15         | External Loopback              | R/W        | 1 = External Loopback is enabled<br>0 = Normal operation                                                       | 0              |
| 14         | Receive Extended Packet Length | R/W        | 1 = Allow reception of extended length packets.<br>0 = Allow reception of normal length Ethernet packets only. | 0              |
| 13         | Edge Rate Control (1000BASE-T) | R/W        | 00 = 4.0 ns                                                                                                    | 0              |
| 12         |                                | R/W        | 01 = 5.0 ns                                                                                                    | 0              |
|            |                                |            | 10 = 3.0 ns                                                                                                    |                |
|            |                                |            | 11 = 0.0 ns                                                                                                    |                |
| 11         | Reserved                       | R/W        | Write as 0, ignore on read.                                                                                    | 0              |
| 10         | Reserved                       | R/W        | Write as 1, ignore on read.                                                                                    | 1              |
| 9          | Reserved                       | R/W        | Write as 0, ignore on read.                                                                                    | 0              |
| 8          | Reserved                       | R/W        | Write as 0, ignore on read.                                                                                    | 0              |
| 7          | Reserved                       | R/W        | Write as 0, ignore on read.                                                                                    | 0              |
| 6          | Reserved                       | R/W        | Write as 0, ignore on read.                                                                                    | 0              |
| 5          | Edge Rate Control (100BASE-TX) | R/W        | 00 = 4.0 ns                                                                                                    | 0              |
| 4          |                                | R/W        | 01 = 5.0 ns                                                                                                    | 0              |
|            |                                |            | 10 = 3.0 ns                                                                                                    |                |
|            |                                |            | 11 = 0.0 ns                                                                                                    |                |
| 3          | Reserved                       | R/W        | Write as 0, ignore on read                                                                                     | 0              |
| 2          | Shadow Register Select         | R/W        | 000 = Auxiliary control register                                                                               | 0              |
| 1          |                                | R/W        | 001 = 10BASE-T register                                                                                        | 0              |
| 0          |                                | R/W        | 010 = Power/MIU control register                                                                               | 0              |
|            |                                |            | 100 = Miscellaneous test register                                                                              |                |
|            |                                |            | 111 = Miscellaneous control register                                                                           |                |

## External Loopback

When bit 15 = 1, external loopback operation is enabled. When the bit is cleared, normal operation resumes.

## Receive Extended Packet Length

When bit 14 = 1, BCM53115S can receive packets up to 9720 bytes in length when in SGMII mode.

When the bit is cleared, the BCM53115S only receives packets up to standard maximum size in length.

## Edge Rate Control (1000BASE-T)

Bits [13:12] control the edge rate of the 1000BASE-T transmit DAC output waveform.

## Edge Rate Control (100BASE-TX)

Bits [5:4] control the edge rate of the 100BASE-TX transmit DAC output waveform.

## Shadow Register Select

See the note on [“Auxiliary Control Shadow Values Access Register \(Page 10h–14h: Address 30h\)”](#) on page 209 describing reading from and writing to register 18h.

The register set shown above is that for normal operation obtained when the lower 3 bits are 000.

## 10BASE-T Register

**Table 149: 10BASE-T Register (Page 10h–14h: Address 30h, Shadow Value 001)**

| Bit | Name                        | R/W      | Description                                                                     | Default |
|-----|-----------------------------|----------|---------------------------------------------------------------------------------|---------|
| 15  | Manchester Code Error       | RO<br>LH | 1 = Manchester code error (10BASE-T)<br>0 = No Manchester code error            | 0       |
| 14  | EOF Error                   | RO<br>LH | 1 = EOF error is detected (10BASE-T).<br>0 = No EOF error is detected.          | 0       |
| 13  | Polarity Error              | RO       | 1 = Channel polarity is inverted.<br>0 = Channel polarity is correct.           | 0       |
| 12  | Block RX_DV Extension (IPG) | R/W      | 1 = Block RX_DV for four additional RXC cycles for IPG.<br>0 = Normal operation | 0       |
| 11  | 10BASE-T TXC Invert Mode    | R/W      | 1 = Invert TXC output.<br>0 = Normal operation                                  | 0       |
| 10  | Reserved                    | R/W      | Write as 0, ignore on read                                                      | 0       |
| 9   | Jabber Disable              | R/W      | 1 = Jabber function is disabled.<br>0 = Jabber function is enabled              | 0       |
| 8   | Reserved                    | R/W      | Write as 0, ignore on read.                                                     | 0       |

**Table 149: 10BASE-T Register (Page 10h–14h: Address 30h, Shadow Value 001) (Cont.)**

| Bit | Name                   | R/W | Description                                                               | Default |
|-----|------------------------|-----|---------------------------------------------------------------------------|---------|
| 7   | Reserved               | R/W | Write as 0, ignore on read.                                               | 0       |
| 6   | 10BASE-T Echo Mode     | R/W | 1 = Echo transmit data to receive data<br>0 = Normal operation            | 0       |
| 5   | SQE Enable Mode        | R/W | 1 = Enable SQE.<br>0 = Disable SQE.                                       | 0       |
| 4   | 10BASE-T No Dribble    | R/W | 1 = Correct 10BASE-T dribble nibble.<br>0 = Normal operation              | 0       |
| 3   | Reserved               | R/W | Write as 0, ignore on read.                                               | 0       |
| 2   | Shadow Register Select | R/W | 000 = Auxiliary control register                                          | 0       |
| 1   |                        | R/W | 001 = 10BASE-T register                                                   | 0       |
| 0   |                        | R/W | 010 = Power/MIU control register                                          | 1       |
|     |                        |     | 100 = Miscellaneous test register<br>111 = Miscellaneous control register |         |

## Power/MIU Control Register (Page 10h–14h: Address 30h)

**Table 150: Power/MIU Control Register (Page 10h–14h: Address 30h, Shadow Value 010)**

| Bit  | Name                        | R/W | Description                                                               | Default |
|------|-----------------------------|-----|---------------------------------------------------------------------------|---------|
| 15   | Reserved                    | R/W | Write as 0, ignore on read.                                               | 0       |
| 14   | Reserved                    | R/W | Write as 0, ignore on read.                                               | 0       |
| 13   | Reserved                    | R/W | Write as 0, ignore on read.                                               | 0       |
| 12   | Reserved                    | R/W | Write as 0, ignore on read.                                               | 0       |
| 11   | Reserved                    | R/W | Write as 0, ignore on read.                                               | 0       |
| 10:7 | Reserved                    | —   | —                                                                         | —       |
| 6    | Reserved                    | R/W | Write as 0, ignore on read.                                               | 1       |
| 5    | Super Isolate (Copper Only) | R/W | 1 = Isolate mode with no link pulses transmitted.<br>0 = Normal operation | 1       |
| 4    | Reserved                    | R/W | Write as 0, ignore on read.                                               | 0       |
| 3    | Reserved                    | R/W | Write as 0, ignore on read.                                               | 0       |
| 2    | Shadow Register Select      | R/W | 000 = Auxiliary control register                                          | 0       |
| 1    |                             | R/W | 001 = 10BASE-T register                                                   | 1       |
| 0    |                             | R/W | 010 = Power/MIU control register                                          | 0       |
|      |                             |     | 100 = Miscellaneous test register<br>111 = Miscellaneous control register |         |

## Super Isolate (Copper Only)

Setting bit 5 = 1, places the BCM53115S into the super isolate mode.

## Shadow Register Select

See the note on “Auxiliary Control Shadow Values Access Register (Page 10h–14h: Address 30h)” on page 209 describing reading from and writing to register 30h.

## Miscellaneous Test Register (Page 10h–14h: Address 30h)

**Table 151: Miscellaneous Test Register (Page 10h–14h: Address 30h, Shadow Value 100)**

| Bit | Name                              | R/W | Description                                                               | Default |
|-----|-----------------------------------|-----|---------------------------------------------------------------------------|---------|
| 15  | Lineside [Remote] Loopback Enable | R/W | 1 = Enable lineside [remote] loopback.<br>0 = Disable loopback.           | 0       |
| 14  | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 13  | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 12  | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 11  | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 10  | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 9   | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 8   | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 7   | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 6   | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 5   | Reserved                          | R/W | Write as 0, ignore on read.                                               | 0       |
| 4   | Swap RX MDIX                      | R/W | 1 = RX and TX operate on same pair.<br>0 = Normal operation               | 0       |
| 3   | 10BASE-T Halfout                  | R/W | 1 = Transmit 10BASE-T at half amplitude.<br>0 = Normal operation          | 0       |
| 2   | Shadow Register Select            | R/W | 000 = Auxiliary control register                                          | 1       |
| 1   |                                   | R/W | 001 = 10BASE-T register                                                   | 0       |
| 0   |                                   | R/W | 010 = Power/MII control register                                          | 0       |
|     |                                   |     | 100 = Miscellaneous test register<br>111 = Miscellaneous control register |         |

## Miscellaneous Control Register (Page 10h–14h: Address 30h)

**Table 152: Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111)**

| Bit | Name         | R/W | Description                 | Default |
|-----|--------------|-----|-----------------------------|---------|
| 15  | Write Enable | R/W | 1 = Write bits [14:3]       | 0       |
|     |              | SC  | 0 = Only write bits [14:12] |         |

**Table 152: Miscellaneous Control Register (Page 10h–14h: Address 30h, Shadow Value 111) (Cont.)**

| Bit | Name                          | R/W | Description                                                                                                                                                                                                                                                                | Default |
|-----|-------------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 14  | Shadow Register Read Selector | R/W | These bits are written when bit 15 is not set. This sets the shadow value for address 18h register read.<br>000 = Normal operation<br>001 = 10BASE-T register<br>010 = Power control register<br>100 = Miscellaneous test register<br>111 = Miscellaneous control register | 0       |
| 13  |                               | R/W |                                                                                                                                                                                                                                                                            | 0       |
| 12  |                               | R/W |                                                                                                                                                                                                                                                                            | 0       |
| 11  | Packet Counter Mode           | R/W | 1 = Receive packet counter.<br>0 = Transmit packet counter.                                                                                                                                                                                                                | 0       |
| 10  | Reserved                      | R/W | Write as 0, ignore on read.                                                                                                                                                                                                                                                | 0       |
| 9   | Force Auto-MDIX Mode          | R/W | 1 = Auto-MDIX is enabled when auto-negotiation is disabled.<br>0 = Auto-MDIX is disabled when auto-negotiation is disabled.                                                                                                                                                | 0       |
| 8   | Reserved                      | R/W | Write as 0, ignore on read.                                                                                                                                                                                                                                                | 0       |
| 7   | Reserved                      | R/W | Write as 0, ignore on read.                                                                                                                                                                                                                                                | 0       |
| 6   | Reserved                      | R/W | Write as 0, ignore on read.                                                                                                                                                                                                                                                | 0       |
| 5   | Reserved                      | R/W | Write as 0, ignore on read.                                                                                                                                                                                                                                                | 0       |
| 4   | Ethernet@WireSpeed Enable     | R/W | 1 = Enable Ethernet@WireSpeed<br>0 = Disable Ethernet@WireSpeed                                                                                                                                                                                                            | 1       |
| 3   | MDIO All PHY Select           | R/W | 1 = The PHY ports accepts MDIO writes to PHY address = 00000.<br>0 = Normal operation                                                                                                                                                                                      | 0       |
| 2   | Shadow Register Select        | R/W | 000 = Auxiliary control register                                                                                                                                                                                                                                           | 1       |
| 1   |                               | R/W | 001 = 10BASE-T register                                                                                                                                                                                                                                                    | 1       |
| 0   |                               | R/W | 010 = Power/MI control register<br>100 = Miscellaneous test register<br>111 = Miscellaneous control register                                                                                                                                                               | 1       |

## Auxiliary Status Summary Register (Page 10h–14h: Address 32h)

**Table 153: Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h)**

| Bit | Name                                  | R/W      | Description                                                                                      | Default |
|-----|---------------------------------------|----------|--------------------------------------------------------------------------------------------------|---------|
| 15  | Auto-negotiation Complete             | RO       | 1 = Auto-negotiation is complete.<br>0 = Auto-negotiation is in progress.                        | 0       |
| 14  | Auto-negotiation Complete Acknowledge | RO<br>LH | 1 = Entered auto-negotiation link is good check state.<br>0 = State not entered since last read. | 0       |

**Table 153: Auxiliary Status Summary Register (Page 10h–14h: Address 32h–33h) (Cont.)**

| Bit | Name                                    | R/W      | Description                                                                                                                                                                                                                                                                | Default |
|-----|-----------------------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 13  | Auto-negotiation Acknowledge Detect     | RO<br>LH | 1 = Entered auto-negotiation acknowledge detect state.<br>0 = State not entered since last read                                                                                                                                                                            | 0       |
| 12  | Auto-negotiation Ability Detect         | RO<br>LH | 1 = Entered auto-negotiation ability detect state.<br>0 = State not entered since last read.                                                                                                                                                                               | 0       |
| 11  | Auto-negotiation Next Page Wait         | RO<br>LH | 1 = Entered auto-negotiation next page wait state.<br>0 = State not entered since last read.                                                                                                                                                                               | 0       |
| 10  | Auto-negotiation HCD                    | RO       | 111 = 1000BASE-T full-duplex <sup>a</sup>                                                                                                                                                                                                                                  | 0       |
| 9   | Current Operating Speed and Duplex Mode | RO       | 110 = 1000BASE-T half-duplex <sup>a</sup>                                                                                                                                                                                                                                  | 0       |
| 8   |                                         | RO       | 101 = 100BASE-TX full-duplex <sup>a</sup><br>100 = 100BASE-T4<br>011 = 100BASE-TX half-duplex <sup>a</sup><br>010 = 10BASE-T full-duplex <sup>a</sup><br>001 = 10BASE-T half-duplex <sup>a</sup><br>000 = No highest common denominator or auto-negotiation is incomplete. | 0       |
| 7   | Parallel Detection Fault                | RO<br>LH | 1 = Parallel link fault is detected.<br>0 = Parallel link fault is not detected.                                                                                                                                                                                           | 0       |
| 6   | Remote Fault                            | RO       | 1 = Link partner has detected a remote fault.<br>0 = Link partner has not detected a remote fault.                                                                                                                                                                         | 0       |
| 5   | Auto-negotiation Page Received          | RO<br>LH | 1 = New page has been received from the link partner.<br>0 = New page has not been received.                                                                                                                                                                               | 0       |
| 4   | Link Partner Auto-negotiation Ability   | RO       | 1 = Link partner has auto-negotiation capability.<br>0 = Link partner does not perform auto-negotiation.                                                                                                                                                                   | 0       |
| 3   | Link Partner Next Page Ability          | RO       | 1 = Link partner has next page capability.<br>0 = Link partner does not have next page capability.                                                                                                                                                                         | 0       |
| 2   | Link Status                             | RO       | 1 = Link is up (link pass state).<br>0 = Link is down (link fail state).                                                                                                                                                                                                   | 0       |
| 1   | Pause Resolution — Receive Direction    | RO       | 1 = Enable pause receive.<br>0 = Disable pause receive.                                                                                                                                                                                                                    | 0       |
| 0   | Pause Resolution — Transmit Direction   | RO       | 1 = Enable pause transmit.<br>0 = Disable pause transmit.                                                                                                                                                                                                                  | 0       |

a. Indicates the negotiated HCD when Auto-negotiation Enable = 1, or indicates the manually selected speed and duplex mode when Auto-negotiation Enable = 0.

## Interrupt Status Register (Page 10h–14h: Address 34h)

**Table 154: Interrupt Status Register (Page 10h–14h: Address 34h–35h)**

| Bit | Name                            | R/W      | Description                                                                                                            | Default |
|-----|---------------------------------|----------|------------------------------------------------------------------------------------------------------------------------|---------|
| 15  | Energy Detect Change            | RO<br>LH | 1 = Energy detect change since last read (enabled by register 1Ch, shadow 00101, bit 5 = 1).<br>0 = Interrupt cleared. | 0       |
| 14  | Illegal Pair Swap               | RO<br>LH | 1 = Illegal pair swap is detected.<br>0 = Interrupt cleared.                                                           | 0       |
| 13  | MDIX Status Change              | RO<br>LH | 1 = MDIX status changed since last read.<br>0 = Interrupt cleared.                                                     | 0       |
| 12  | Exceeded High Counter Threshold | RO       | 1 = Value in one or more counters is above 32K.<br>0 = All counters below are 32K.                                     | 0       |
| 11  | Exceeded Low Counter Threshold  | RO       | 1 = Value in one or more counters is above 128K.<br>0 = All counters below are 128K.                                   | 0       |
| 10  | Auto-negotiation Page Received  | RO<br>LH | 1 = Page received since last read.<br>0 = Interrupt cleared.                                                           | 0       |
| 9   | No HCD Link                     | RO<br>LH | 1 = Negotiated HCD, did not establish link.<br>0 = Interrupt cleared.                                                  | 0       |
| 8   | No HCD                          | RO<br>LH | 1 = Auto-negotiation returned HCD = none.<br>0 = Interrupt cleared.                                                    | 0       |
| 7   | Negotiated Unsupported HCD      | RO<br>LH | 1 = Auto-negotiation HCD is not supported by BCM53115S.<br>0 = Interrupt cleared.                                      | 0       |
| 6   | Scrambler Synchronization Error | RO<br>LH | 1 = Scrambler synchronization error occurred since last read.<br>0 = Interrupt cleared.                                | 0       |
| 5   | Remote Receiver Status Change   | RO<br>LH | 1 = Remote receiver status changed since last read.<br>0 = Interrupt cleared.                                          | 0       |
| 4   | Local Receiver Status Change    | RO<br>LH | 1 = Local receiver status changed since last read.<br>0 = Interrupt cleared.                                           | 0       |
| 3   | Duplex Mode Change              | RO<br>LH | 1 = Duplex mode changed since last read.<br>0 = Interrupt cleared.                                                     | 0       |
| 2   | Link Speed Change               | RO<br>LH | 1 = Link speed changed since last read.<br>0 = Interrupt cleared.                                                      | 0       |
| 1   | Link Status Change              | RO<br>LH | 1 = Link status changed since last read.<br>0 = Interrupt cleared.                                                     | 0       |
| 0   | Receive CRC Error               | RO<br>LH | 1 = Receive CRC error occurred since last read.<br>0 = Interrupt cleared.                                              | 0       |

The INTR LED output is asserted when any bit in 10BASE-T/100BASE-TX/1000BASE-T interrupt status register is set and the corresponding bit in the 10BASE-T/100BASE-TX/1000BASE-T interrupt mask register is cleared.

## 10BASE-T/100BASE-TX/1000BASE-T Register 38h Access

Reading from and writing to 10BASE-T/100BASE-TX/1000BASE-T register 38h is through register 38h bits [15:10]. The bits [14:10] set the shadow value of register 38h, and bit 15 enables the writing of the bits [9:0]. Setting bit 15 allows writing to bits [9:0] of register 38h. Before reading register 38h shadow zzzzz, writes to register 38h should be set with bit 15 = 0, and bits [14:10] to zzzzz. The subsequent register read from register 38h contains the shadow zzzzz register value. [Table 155](#) lists all the register 38h shadow values.

**Table 155: 10BASE-T/100BASE-TX/1000BASE-T Register 38h Shadow Values**

| Shadow Value | Register Name                                                                          |
|--------------|----------------------------------------------------------------------------------------|
| 00100        | "Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100)" on page 217 |
| 00101        | –                                                                                      |
| 01000        | –                                                                                      |
| 01001        | –                                                                                      |
| 01010        | "Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010)" on page 218 |
| 01101        | –                                                                                      |
| 01110        | "LED Selector 2 Register (Page 10h–14h: Address 38h, Shadow Value 01110)" on page 219  |
| 11111        | "Mode Control Register (Page 10h–14h: Address 38h, Shadow Value 11111)" on page 220    |

## Spare Control 2 Register (Page 10h–14h: Address 38h)

**Table 156: Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100)**

| Bit | Name                     | R/W | Description                                 | Default |
|-----|--------------------------|-----|---------------------------------------------|---------|
| 15  | Write Enable             | R/W | 1 = Write bits [9:0]<br>0 = Read bits [9:0] | 0       |
| 14  | Shadow Register Selector | R/W | 00100 = Spare control 2 register            | 0       |
| 13  |                          | R/W |                                             | 0       |
| 12  |                          | R/W |                                             | 1       |
| 11  |                          | R/W |                                             | 0       |
| 10  |                          | R/W |                                             | 0       |
| 9   | Reserved                 | R/W | Write as 0, ignore when read.               | 0       |
| 8   | Reserved                 | –   | –                                           | –       |
| 7   | Reserved                 | R/W | Write as 0, ignore when read.               | 0       |
| 6   | Reserved                 | R/W | Write as 0, ignore when read.               | 0       |
| 5   | Reserved                 | R/W | Write as 0, ignore when read.               | 0       |

**Table 156: Spare Control 2 Register (Page 10h–14h: Address 38h, Shadow Value 00100) (Cont.)**

| Bit | Name                              | R/W | Description                                                                                                                                                                          | Default |
|-----|-----------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 4   | Ethernet@WireSpeed<br>Retry Limit | RO  | 000 = Downgrade after 2 failed auto-negotiation attempts.                                                                                                                            | 0       |
| 3   |                                   |     | 001 = Downgrade after 3 failed auto-negotiation attempts.                                                                                                                            | 1       |
| 2   |                                   |     | 010 = Downgrade after 4 failed auto-negotiation attempts.                                                                                                                            | 1       |
|     |                                   |     | 011 = Downgrade after 5 failed auto-negotiation attempts.                                                                                                                            |         |
|     |                                   |     | 100 = Downgrade after 6 failed auto-negotiation attempts.                                                                                                                            |         |
|     |                                   |     | 101 = Downgrade after 7 failed auto-negotiation attempts.                                                                                                                            |         |
|     |                                   |     | 110 = Downgrade after 8 failed auto-negotiation attempts.                                                                                                                            |         |
|     |                                   |     | 111 = Downgrade after 9 failed auto-negotiation attempts.                                                                                                                            |         |
| 1   | Energy Detect on INTR LED Pin     | R/W | 1 = Routes energy detect to interrupt signal. Use LED selectors (register 38h shadow 01101 and 01110) and program to INTR mode.<br>0 = INTR LED pin performs the Interrupt function. | 0       |
| 0   | Reserved                          | R/W | Write as 0, ignore when read.                                                                                                                                                        | 0       |

## Auto Power-Down Register (Page 10h–14h: Address 38h)

**Table 157: Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010)**

| Bit | Name                     | R/W | Description                                                                   | Default |
|-----|--------------------------|-----|-------------------------------------------------------------------------------|---------|
| 15  | Write Enable             | R/W | 1 = Write bits [9:0]<br>0 = Read bits [9:0]                                   | 0       |
| 14  | Shadow Register Selector | R/W | 01010 = Auto power-down register                                              | 0       |
| 13  |                          | R/W |                                                                               | 1       |
| 12  |                          | R/W |                                                                               | 0       |
| 11  |                          | R/W |                                                                               | 1       |
| 10  |                          | R/W |                                                                               | 0       |
| 9   | Reserved                 | R/W | Write as 0, ignore when read.                                                 | 0       |
| 8   | Reserved                 | R/W | Write as 0, ignore when read.                                                 | 0       |
| 7   | Reserved                 | R/W | Write as 0, ignore when read.                                                 | 0       |
| 6   | Reserved                 | R/W | Write as 0, ignore when read.                                                 | 0       |
| 5   | Auto Power-Down Mode     | R/W | 1 = Auto power-down mode is enabled.<br>0 = Auto power-down mode is disabled. | 0       |
| 4   | Sleep Timer Select       | R/W | 1 = Sleep timer is 5.4 seconds.<br>0 = Sleep timer is 2.7 seconds.            | 0       |

**Table 157: Auto Power-Down Register (Page 10h–14h: Address 38h, Shadow Value 01010) (Cont.)**

| Bit | Name                 | R/W | Description                                 | Default |
|-----|----------------------|-----|---------------------------------------------|---------|
| 3   | Wake-up Timer Select | R/W | Counter for wake-up timer in units of 84 ms | 0       |
| 2   |                      | R/W | 0001 = 84 ms                                | 0       |
| 1   |                      | R/W | 0010 = 168 ms                               | 0       |
| 0   |                      | R/W | ...<br>1111 = 1.26 sec.                     | 1       |

## LED Selector 2 Register (Page 10h–14h: Address 38h)

**Table 158: LED Selector 2 Register (Page 10h–14h: Address 38h, Shadow Value 01110)**

| Bit | Name                     | R/W | Description                                 | Default |
|-----|--------------------------|-----|---------------------------------------------|---------|
| 15  | Write Enable             | R/W | 1 = Write bits [9:0]<br>0 = Read bits [9:0] | 0       |
| 14  | Shadow Register Selector | R/W | 01110 = LED status register                 | 0       |
| 13  |                          | R/W |                                             | 1       |
| 12  |                          | R/W |                                             | 1       |
| 11  |                          | R/W |                                             | 1       |
| 10  |                          | R/W |                                             | 0       |
| 9   | Reserved                 | R/W | Write as 0, ignore when read.               | 0       |
| 8   | Reserved                 | R/W | Write as 0, ignore when read.               | 0       |
| 7   | LED4 Selector            | R/W | 0000 = <u>LINKSPD[1]</u>                    | 0       |
| 6   |                          | R/W | 0001 = <u>LINKSPD[2]</u>                    | 1       |
| 5   |                          | R/W | 0010 = <u>XMITLED</u>                       | 1       |
| 4   |                          | R/W | 0011 = <u>ACTIVITY</u>                      | 0       |
|     |                          |     | 0100 = <u>FDXLED</u>                        |         |
|     |                          |     | 0101 = <u>SLAVE</u>                         |         |
|     |                          |     | 0110 = <u>INTR</u>                          |         |
|     |                          |     | 0111 = <u>QUALITY</u>                       |         |
|     |                          |     | 1000 = <u>RCVLED</u>                        |         |
|     |                          |     | 1001 = <u>WIRESPD_DOWNGRADE</u>             |         |
|     |                          |     | 1010 = <u>MULTICOLOR[2]</u>                 |         |
|     |                          |     | 1011 = <u>CABLE DIAGNOSTIC OPEN/SHORT</u>   |         |
|     |                          |     | 1100 = <u>RESERVED</u>                      |         |
|     |                          |     | 1101 = <u>CRS (SGMII mode)</u>              |         |
|     |                          |     | 1110 = <u>Off (high)</u>                    |         |
|     |                          |     | 1111 = <u>On (low)</u>                      |         |

**Table 158: LED Selector 2 Register (Page 10h–14h: Address 38h, Shadow Value 01110) (Cont.)**

| Bit | Name          | R/W | Description                        | Default |
|-----|---------------|-----|------------------------------------|---------|
| 3   | LED3 Selector | R/W | 0000 = LINKSPD[1]                  | 0       |
| 2   |               | R/W | 0001 = LINKSPD[2]                  | 0       |
| 1   |               | R/W | 0010 = XMITLED                     | 1       |
| 0   |               | R/W | 0011 = ACTIVITY                    | 1       |
|     |               |     | 0100 = FDXLED                      |         |
|     |               |     | 0101 = SLAVE                       |         |
|     |               |     | 0110 = INTR                        |         |
|     |               |     | 0111 = QUALITY                     |         |
|     |               |     | 1000 = RCVLED                      |         |
|     |               |     | 1001 = WIRESPD_DOWNGRADE           |         |
|     |               |     | 1010 = MULTICOLOR[1]               |         |
|     |               |     | 1011 = CABLE DIAGNOSTIC OPEN/SHORT |         |
|     |               |     | 1100 = RESERVED                    |         |
|     |               |     | 1101 = CRS (SGMII mode)            |         |
|     |               |     | 1110 = Off (high)                  |         |
|     |               |     | 1111 = On (low)                    |         |

## Mode Control Register (Page 10h–14h: Address 38h)

**Table 159: Mode Control Register (Page 10h–14h: Address 38h, Shadow Value 11111)**

| Bit | Name                     | R/W | Description                                                                                      | Default |
|-----|--------------------------|-----|--------------------------------------------------------------------------------------------------|---------|
| 15  | Write Enable             | R/W | 1 = Write bits [9:0]<br>0 = Read bits [9:0]                                                      | 0       |
| 14  | Shadow Register Selector | R/W | 11111 = LED status register                                                                      | 1       |
| 13  |                          | R/W |                                                                                                  | 1       |
| 12  |                          | R/W |                                                                                                  | 1       |
| 11  |                          | R/W |                                                                                                  | 1       |
| 10  |                          | R/W |                                                                                                  | 1       |
| 9   | Reserved                 | RO  | Ignore on read.                                                                                  | 0       |
| 8   | Reserved                 | –   | –                                                                                                | –       |
| 7   | Copper Link              | RO  | 1 = Link is good on the copper interface.<br>0 = Copper link is down.                            | 0       |
| 6   | Reserved                 | –   | –                                                                                                | –       |
| 5   | Copper Energy Detect     | RO  | 1 = Energy detected on the copper interface.<br>0 = Energy not detected on the copper interface. | 0       |
| 4   | Reserved                 | RO  | Ignore on read.                                                                                  | 0       |
| 3   | Reserved                 | RO  | Ignore on read.                                                                                  | 1       |

**Table 159: Mode Control Register (Page 10h–14h: Address 38h, Shadow Value 11111) (Cont.)**

| Bit | Name        | R/W | Description   | Default |
|-----|-------------|-----|---------------|---------|
| 2   | Mode Select | R/W | 00 = GMII     | 0       |
| 1   |             |     | 01 = Reserved | 0       |
|     |             |     | 10 = Reserved |         |
|     |             |     | 11 = Reserved |         |
| 0   | Reserved    | –   | –             | –       |

## Master/Slave Seed Register (Page 10h–14h: Address 3Ah)

**Table 160: Master/Slave Seed Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 0**

| Bit | Name                                                  | R/W      | Description                                                                                                                       | Default |
|-----|-------------------------------------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------|---------|
| 15  | Enable Shadow Register                                | R/W      | 1 = Select shadow register.<br>0 = Normal operation<br>Writes to the selected register are done on a single cycle.                | 0       |
| 14  | Master/Slave Seed Match                               | RO<br>LH | 1 = Seeds match<br>0 = Seeds do not match                                                                                         | 0       |
| 13  | Link Partner Repeater/DTE Bit                         | RO       | 1 = Link partner is a repeater/switch device.<br>0 = Link partner is a DTE device.                                                | 0       |
| 12  | Link Partner Manual Master/Slave Configuration Value  | RO       | 1 = Link partner is configured as master.<br>0 = Link partner is configured as slave.                                             | 0       |
| 11  | Link Partner Manual Master/Slave Configuration Enable | RO       | 1 = Link partner manual master/slave configuration is enabled.<br>0 = Link partner manual master/slave configuration is disabled. | 0       |
| 10  | Local Master/Slave Seed Value                         | R/W      | Returns the automatically generated master/slave random seed.                                                                     | 0       |
| 9   |                                                       | R/W      |                                                                                                                                   | 0       |
| 8   |                                                       | R/W      |                                                                                                                                   | 0       |
| 7   |                                                       | R/W      |                                                                                                                                   | 0       |
| 6   |                                                       | R/W      |                                                                                                                                   | 0       |
| 5   |                                                       | R/W      |                                                                                                                                   | 0       |
| 4   |                                                       | R/W      |                                                                                                                                   | 0       |
| 3   |                                                       | R/W      |                                                                                                                                   | 0       |
| 2   |                                                       | R/W      |                                                                                                                                   | 0       |
| 1   |                                                       | R/W      |                                                                                                                                   | 0       |
| 0   |                                                       | R/W      |                                                                                                                                   | 0       |

## HCD Status Register (Page 10h–14h: Address 3Ah)

**Table 161: HCD Status Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 1**

| Bit | Name                                                  | R/W      | Description                                                                                                    | Default |
|-----|-------------------------------------------------------|----------|----------------------------------------------------------------------------------------------------------------|---------|
| 15  | Enable Shadow Register                                | R/W      | 1 = Select Shadow register.<br>0 = Normal operation                                                            | 0       |
| 14  | Ethernet@WireSpeed<br>Disable Gigabit<br>Advertising  | RO       | 1 = Disable advertising gigabit.<br>0 = Advertise gigabit based on register 09h.                               | 0       |
| 13  | Ethernet@WireSpeed<br>Disable 100TX<br>Advertising    | RO       | 1 = Disable advertising 100TX.<br>0 = Advertise 100TX based on register 04h.                                   | 0       |
| 12  | Ethernet@WireSpeed<br>Downgrade                       | RO<br>LH | 1 = Ethernet@WireSpeed downgrade occurred since last read.<br>0 = Ethernet@WireSpeed downgrade cleared.        | 0       |
| 11  | HCD 1000BASE-T<br>Full-Duplex                         | RO<br>LH | 1 = Gigabit full-duplex occurred since last read.<br>0 = HCD cleared.                                          | 0       |
| 10  | HCD 1000BASE-T<br>Half-Duplex                         | RO<br>LH | 1 = Gigabit half-duplex occurred since last read.<br>0 = HCD cleared.                                          | 0       |
| 9   | HCD 100BASE-TX<br>Full-Duplex                         | RO<br>LH | 1 = 100BASE-TX full-duplex occurred since last read.<br>0 = HCD cleared.                                       | 0       |
| 8   | HCD 100BASE-T<br>Half-Duplex                          | RO<br>LH | 1 = 100BASE-TX half-duplex occurred since last read.<br>0 = HCD cleared.                                       | 0       |
| 7   | HCD 10BASE-T<br>Full-Duplex                           | RO<br>LH | 1 = 10BASE-T full-duplex occurred since last read<br>0 = HCD cleared.                                          | 0       |
| 6   | HCD 10BASE-T<br>Half-Duplex                           | RO<br>LH | 1 = 10BASE-T half-duplex occurred since last read.<br>0 = HCD cleared.                                         | 0       |
| 5   | HCD 1000BASE-T<br>Full-Duplex<br>(Link Never Came Up) | RO<br>LH | 1 = Gigabit full-duplex HCD and <i>link never came up</i> occurred since the last read.<br>0 = HCD cleared.    | 0       |
| 4   | HCD 1000BASE-T<br>Half-Duplex<br>(Link Never Came Up) | RO<br>LH | 1 = Gigabit half-duplex HCD and <i>link never came up</i> occurred since the last read.<br>0 = HCD cleared.    | 0       |
| 3   | HCD 100BASE-TX<br>Full-Duplex<br>(Link Never Came Up) | RO<br>LH | 1 = 100BASE-TX full-duplex HCD and <i>link never came up</i> occurred since the last read.<br>0 = HCD cleared. | 0       |
| 2   | HCD 100BASE-T<br>Half-Duplex<br>(Link Never Came Up)  | RO<br>LH | 1 = 100BASE-TX half-duplex HCD and <i>link never came up</i> occurred since the last read.<br>0 = HCD cleared. | 0       |
| 1   | HCD 10BASE-T<br>Full-Duplex<br>(Link Never Came Up)   | RO<br>LH | 1 = 10BASE-T full-duplex HCD and <i>link never came up</i> occurred since the last read.<br>0 = HCD cleared.   | 0       |

**Table 161: HCD Status Register (Page 10h–14h: Address 3Ah–3Bh) Bit 15 = 1 (Cont.)**

| Bit | Name                                          | R/W      | Description                                                                                                  | Default |
|-----|-----------------------------------------------|----------|--------------------------------------------------------------------------------------------------------------|---------|
| 0   | HCD 10BASE-T Half-Duplex (Link Never Came Up) | RO<br>LH | 1 = 10BASE-T half-duplex HCD and <i>link never came up</i> occurred since the last read.<br>0 = HCD cleared. | 0       |



**Note:** Bits [12:0] are also cleared when auto-negotiation is disabled using the MII register 00h, bit 12 = 1, or restarted using the MII register 00h, bit 9 = 1.

## Test Register 1 (Page 10h–14h: Address 3Ch)

**Table 162: Test Register 1 (Page 10h–14h: Address 3C–3Dh)**

| Bit | Name                           | R/W | Description                                                                                                                                                                                                                                                 | Default |
|-----|--------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15  | CRC Error Counter Selector     | R/W | 1 = Receiver NOT_OK counters (register 14h) becomes 16-bit CRC error counter (CRC errors are counted only after this bit is set).<br>0 = Normal operation                                                                                                   | 0       |
| 14  | Transmit Error Code Visibility | R/W | 1 = False carrier sense counters (register 13h) counts packets received with transmit error codes.<br>0 = Normal operation                                                                                                                                  | 0       |
| 13  | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 12  | Force Link 10/100/1000BASE-T   | R/W | 1 = Force link state machine into link pass state.<br>0 = Normal operation                                                                                                                                                                                  | 0       |
| 11  | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 10  | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 9   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 8   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 7   | Manual Swap MDI State          | R/W | 1 = Manually swap MDI state.<br>0 = Normal operation<br><br><b>Note:</b> To change the MDI state when in forced 100BASE-TX mode, the PHY must first be put into a nonlink condition, then set bit 7 = 1 and finally set the PHY into force 100BASE-TX mode. | 0       |
| 6   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 5   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 4   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 3   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 2   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 1   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |
| 0   | Reserved                       | R/W | Write as 0, ignore when read.                                                                                                                                                                                                                               | 0       |



**Note:** Preamble is still required on the first read or write. Preamble suppression cannot be disabled.

## Expansion Registers

### Expansion Register 00h: Receive/Transmit Packet Counter

Expansion register 00h is enabled by writing to “[Expansion Register Access Register \(Page 10h–14h: Address 2Eh–2Fh\)](#)” bits [11:0] = ‘F00’h, and read/write access is through register 2Ah.

**Table 163: Expansion Register 00h: Receive/Transmit Packet Counter**

| Bit  | Name                         | R/W       | Description                                   | Default |
|------|------------------------------|-----------|-----------------------------------------------|---------|
| 15:0 | Packet Counter (Copper Only) | R/W<br>CR | Returns transmitted and received packet count | 0000h   |

#### Packet Counter (Copper Only)

The mode of this counter is set by bit 11 of “[Miscellaneous Control Register \(Page 10h–14h: Address 30h, Shadow Value 111\)](#)”. When bit 11 = 1, then receive packets (both good and bad CRC error packets) are counted. When bit 11 = 0, then transmit packets (both good and bad CRC error packets) are counted. This counter is cleared on read and freezes at FFFFh.

### Expansion Register 01h: Expansion Interrupt Status

Expansion register 01h is enabled by writing to “[Expansion Register Access Register \(Page 10h–14h: Address 2Eh–2Fh\)](#)” bits [11:0] = ‘F01’h, and read/write access is through register 2Ah.

**Table 164: Expansion Register 01h: Expansion Interrupt Status**

| Bit  | Name               | R/W      | Description                                                                             | Default |
|------|--------------------|----------|-----------------------------------------------------------------------------------------|---------|
| 15:1 | Reserved           | RO       | Write as 0, ignore on read                                                              | 0       |
| 0    | Transmit CRC Error | RO<br>LH | 1 = Transmit CRC error detected since last read.<br>0 = No transmit CRC error detected. | 0       |

#### Transmit CRC Error

This bit indicates that a transmit CRC error has been detected since the last read.

## Expansion Register 45h: Transmit CRC Enable

Expansion register 00h is enabled by writing to “[Expansion Register Access Register \(Page 10h–14h: Address 2Eh–2Fh\)](#)” bits [11:0] = ‘F45’h, and read/write access is through register 2Ah.

**Table 165: Expansion Register 45h: Transmit CRC**

| <b>Bit</b> | <b>Name</b>         | <b>R/W</b> | <b>Description</b>                                                                                                                  | <b>Default</b> |
|------------|---------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15:13      | Reserved            | R/W        | Write as 0, ignore on read.                                                                                                         | 000            |
| 12         | Transmit CRC enable | R/W        | 1 = Enable transmit CRC checker.<br>0 = Disable transmit CRC checker.<br>Register 18h, shadow value 100, bit 15 must be set to a 1. | 0              |
| 11:0       | Reserved            | R/W        | Write as 0, ignore on read.                                                                                                         | 0              |

### Transmit CRC Checker

When register 30h, Shadow Value 100, bit 15 = 1 and Expansion Register 45h, bit 12 = 1, the transmit CRC checker is enabled. When a transmit CRC error occurs, Expansion Register 01h, bit 0 = 1.

## Page 15h: Internal SerDes Port (Port 5) Register

The register is broken into two blocks:

- Block 0 is for IEEE and non-IEEE controls.
- Blocks 0, 2, and 3 are non-IEEE blocks where the analog section or the SerDes is controlled.

To access block 0, 2, or 3, write to the block number in the Block Address register at MII address 0x1F SPI offset address 3Eh.

**Table 166: Page 15h Register Map**

| <b>SPI Offset<br/>Address</b> | <b>MI<br/>Address</b> | <b>Block</b> | <b>Bits</b> | <b>Register Name</b>                                                                 |
|-------------------------------|-----------------------|--------------|-------------|--------------------------------------------------------------------------------------|
| 00h                           | 00h                   | 0            | 16          | "MII Control Register (Page 15h: Address 00h)" on page 227                           |
| 02h                           | 01h                   | 0            | 16          | "MII Status Register (Page 15h: Address 02h)" on page 228                            |
| 04h–06h                       | 02h–03h               | 0            | –           | Reserved                                                                             |
| 08h                           | 04h                   | 0            | 16          | "Auto-Negotiation Advertisement Register (Page 15h: Address 08h)" on page 229        |
| 0Ah                           | 05h                   | 0            | 16          | "Auto-Negotiation Link Partner Ability Register (Page 15h: Address 0Ah)" on page 230 |
| 0Ch                           | 06h                   | 0            | 16          | "Auto-Negotiation Expansion Register (Page 15h: Address 0Ch)" on page 231            |
| 0Eh                           | 07h–0Eh               | 0            | –           | Reserved                                                                             |
| 1Eh                           | 0Fh                   | 0            | 16          | "Extended Status Register (Page 15h: Address 1Eh)" on page 231                       |
| 20h                           | 10h                   | 0            | 16          | "SerDes/SGMII Control 1 Register (Page 15h: Address 20h, Block 0)" on page 232       |
| 22h                           | 11h                   | 0            | 16          | "SerDes/SGMII Control 2 Register (Page 15h: Address 22h, Block 0)" on page 233       |
| 24h                           | 12h                   | 0            | 16          | "SerDes/SGMII Control 3 Register (Page 15h: Address 24h, Block 0)" on page 235       |
| 28h                           | 14h                   | 0            | 16          | "SerDes/SGMII Status 1 Register (Page 15h: Address 28h, Block 0)" on page 236        |
| 2Ah                           | 15h                   | 0            | 16          | "SerDes/SGMII Status 2 Register (Page 15h: Address 2Ah, Block 0)" on page 238        |
| 2Ch                           | 16h                   | 0            | 16          | "SerDes/SGMII Status 3 Register (Page 15h: Address 2Ch, Block 0)" on page 239        |
| 2Eh                           | 17h–1Eh               | 0            | –           | Reserved                                                                             |
| 20h                           | 10h                   | 2            | 16          | "100FX Enabling Control Register (Page 15h: Address 20h, Block 2)" on page 239       |
| 22h                           | 11h                   | 2            | 16          | "100FX Extended Packet Size Register (Page 15h: Address 22h, Block 2)" on page 240   |
| 24h                           | 12h                   | 2            | 16          | "100FX Control Register (Page 15h: Address 24h, Block 2)" on page 241                |
| 26h                           | 13h                   | 2            | 16          | "100FX Link Status Register (Page 15h: Address 26h, Block 2)" on page 241            |

**Table 166: Page 15h Register Map (Cont.)**

| <b>SPI Offset Address</b> | <b>MII Address</b> | <b>Block</b> | <b>Bits</b> | <b>Register Name</b>                                                                 |
|---------------------------|--------------------|--------------|-------------|--------------------------------------------------------------------------------------|
| 28h                       | 14h–1Eh            | 2            | –           | Reserved                                                                             |
| 20h                       | 10h                | 3            | 16          | <a href="#">“Analog TX1 Register (Page 15h: Address 20h, Block 3)” on page 242</a>   |
| 22h                       | 11h                | 3            | 16          | <a href="#">“Analog TX2 Register (Page 15h: Address 22h, Block 3)” on page 243</a>   |
| 24h                       | 12h                | 3            | 16          | <a href="#">“Analog TXAMP Register (Page 15h: Address 24h, Block 3)” on page 243</a> |
| 26h                       | 13h                | 3            | 16          | <a href="#">“Analog RX1 Register (Page 15h: Address 26h, Block 3)” on page 244</a>   |
| 28h                       | 14h                | 3            | 16          | <a href="#">“Analog RX2 Register (Page 15h: Address 28h, Block 3)” on page 244</a>   |
| 30h                       | 18h                | 3            | 16          | <a href="#">“Analog PLL Register (Page 15h: Address 30h, Block 3)” on page 245</a>   |
| 3Eh                       | 1Fh                | –            | –           | <a href="#">“Block Address Number (Page 010h–017h: Address 03Eh)” on page 245</a>    |

## MII Control Register (Page 15h: Address 00h)

**Table 167: MII Control Register (Page 15h: Address 00h-01h)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                | <b>Default</b> |
|-------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15          | RST_SW      | R/W        | PHY Reset<br>0 = Normal Operation<br>1 = Reset                                                                                                    | 0              |
| 14          | LOOPBACK    | R/W        | Local loopback, data is looping back at the PHY before going out to the wire.<br>0 = Normal operation<br>1 = Loopback enable                      | 0              |
| 13          | SPD[0]      | R/W        | Bit[0] of manual Speed[1:0] in SGMII mode only. This field is ignored in 1000Base-X operation.<br>1X = 1000 Mbps<br>01 = 100 Mbps<br>00 = 10 Mbps | 0x0            |
| 12          | AN_EN       | R/W        | Auto-negotiation enable<br>0 = Disable<br>1 = Enable AN                                                                                           | 1              |
| 11          | PWRDN       | R/W        | Power down GE SerDes<br>0 = Normal operation<br>1 = Power down the SerDes PHY                                                                     | 0              |
| 10          | RESERVED    | RO         | Reserved write 0, ignore read                                                                                                                     | 0              |
| 9           | RESTART_AN  | R/W        | Restart Auto-negotiation process<br>0 = Normal operation<br>1 = Restart AN                                                                        | 0              |

**Table 167: MII Control Register (Page 15h: Address 00h-01h) (Cont.)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                | <b>Default</b> |
|-------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 8           | FDX         | R/W        | Duplex mode<br>0 = Half duplex<br>1 = Full duplex                                                                                                 | 1              |
| 7           | COL_TEST_EN | R/W        | Collision test enable<br>0 = Normal operation<br>1 = Collision test                                                                               | 0              |
| 6           | SPD[1]      | R/W        | Bit[1] of manual Speed[1:0] in SGMII mode only. This field is ignored in 1000Base-X operation.<br>1X = 1000 Mbps<br>01 = 100 Mbps<br>00 = 10 Mbps | 1              |
| 5:0         | RESERVED    | RO         | Reserved write 0, ignore read.                                                                                                                    | 0x0            |

## MII Status Register (Page 15h: Address 02h)

**Table 168: MII Status Register (Page 15h: Address 02h-03h)**

| <b>Bits</b> | <b>Name</b>             | <b>R/W</b> | <b>Description</b>                                                                                                                 | <b>Default</b> |
|-------------|-------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15          | 100BASE_T4              | RO         | 0 = Incapable.<br>1 = 100Base-T4 capable.                                                                                          | 0              |
| 14          | 100BASEX_FDX            | RO         | 0 = Incapable.<br>1 = 100BASE-X full-duplex capable.                                                                               | 0              |
| 13          | 100BASEX_HDX            | RO         | 0 = Incapable.<br>1 = 100BASE-X half-duplex capable.                                                                               | 0              |
| 12          | 10BASE_T_FDX            | RO         | 0 = Incapable.<br>1 = 10BASE-T full-duplex capable.                                                                                | 0              |
| 11          | 10BASE_T_HDX            | RO         | 0 = Incapable.<br>1 = 10BASE-T half-duplex capable.                                                                                | 0              |
| 10          | 10BASE2_T_FDX           | RO         | 0 = Incapable.<br>1 = 10BASE-T2 full-duplex capable.                                                                               | 0              |
| 9           | 10BASE2_T_HDX           | RO         | 0 = Incapable.<br>1 = 10BASE-T2 half-duplex capable.                                                                               | 0              |
| 8           | EXT_STATUS              | RO         | 0 = No extended status.<br>1 = Extended status in register 0x0F.                                                                   | 1              |
| 7           | RESERVED                | RO         | Reserved write 0, ignore read.                                                                                                     | 0              |
| 6           | MF_PREAMBLE_SUPPRESSION | RO         | 0 = PHY does not accept management frames with preamble suppressed.<br>1 = PHY accepts management frames with preamble suppressed. | 1              |

**Table 168: MII Status Register (Page 15h: Address 02h-03h) (Cont.)**

| <b>Bits</b> | <b>Name</b>    | <b>R/W</b> | <b>Description</b>                                                                                          | <b>Default</b> |
|-------------|----------------|------------|-------------------------------------------------------------------------------------------------------------|----------------|
| 5           | AN_COMPLETE    | RO         | Auto-negotiation complete.<br>0 = Not done<br>1 = AN complete                                               | 0              |
| 4           | RF             | RO         | Remote fault.<br>0 = No fault detected<br>1 = Remote fault detected                                         | 0              |
| 3           | AN_ABILITY     | RO         | Auto-negotiation ability.<br>0 = Incapable of AN<br>1 = AN capable                                          | 1              |
| 2           | LINK_STATUS    | RO         | Link status.<br>0 = Link fail<br>1 = Good link                                                              | 0              |
| 1           | JABBER_DETECT  | RO         | Jabber detect<br>0 = Not detected<br>1 = Jabber detected                                                    | 0              |
| 0           | EXT_CAPABILITY | RO         | Extended capability<br>0 = Supports basic register set only<br>1 = Extended register capabilities supported | 1              |

## Auto-Negotiation Advertisement Register (Page 15h: Address 08h)

**Table 169: Auto-Negotiation Advertisement Register (Page 15h: Address 08h-09h)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                          | <b>Default</b> |
|-------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15          | NEXT_PG     | RO         | Next page                                                                                                                                                                   | 0              |
| 14          | RESERVED    | RO         | Reserved write 0, ignore read                                                                                                                                               | 0              |
| 13:12       | RF          | R/W        | Remote fault<br>2'b00 = No fault<br>2'b01 = Link failure<br>2'b10 = Offline<br>2'b11 = Auto-negotiation error                                                               | 0x0            |
| 11:9        | RESERVED    | RO         | Reserved write 0, ignore read                                                                                                                                               | 0x0            |
| 8:7         | PAUSE       | R/W        | Pause<br>2'b00 = No pause<br>2'b01 = Asymmetric pause<br>2'b10 = Asymmetric pause towards link partner<br>2'b11 = Both symmetric and asymmetric pause, towards local device | 0x11           |

**Table 169: Auto-Negotiation Advertisement Register (Page 15h: Address 08h-09h) (Cont.)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                           | <b>Default</b> |
|-------------|-------------|------------|------------------------------------------------------------------------------|----------------|
| 6           | HDX         | R/W        | Half duplex<br>0 = Do not advertise half duplex<br>1 = Advertise half duplex | 1              |
| 5           | FDX         | R/W        | Full duplex<br>0 = Do not advertise full duplex<br>1 = Advertise full duplex | 1              |
| 4:0         | RESERVED    | RO         | Reserved write 0, ignore read.                                               | 0x0            |

## Auto-Negotiation Link Partner Ability Register (Page 15h: Address 0Ah)

**Table 170: Auto-Negotiation Link Partner Ability Register (Page 15h: Address 0Ah-0Bh)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                          | <b>Default</b> |
|-------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15          | NEXT_PG     | RO         | Next page                                                                                                                                                                   | 0              |
| 14          | ACK         | RO         | 0 = Link partner has not received link code word<br>1 = Link partner has received link code word                                                                            | 0              |
| 13:12       | RF          | RO         | Remote fault<br>2'b00 = No fault<br>2'b01 = Link failure<br>2'b10 = Offline<br>2'b11 = Auto-negotiation error                                                               | 0x0            |
| 11:9        | RESERVED    | RO         | Reserved write 0, ignore read                                                                                                                                               | 0x0            |
| 8:7         | PAUSE       | RO         | Pause<br>2'b00 = No pause<br>2'b01 = Asymmetric pause<br>2'b10 = Asymmetric pause towards link partner<br>2'b11 = Both symmetric and asymmetric pause, towards local device | 0x0            |
| 6           | HDX         | RO         | Half duplex<br>0 = Do not advertise half duplex<br>1 = Advertise half duplex                                                                                                | 0              |
| 5           | FDX         | RO         | Full duplex<br>0 = Do not advertise full duplex<br>1 = Advertise full duplex                                                                                                | 0              |
| 4:1         | RESERVED    | RO         | Reserved write 0, ignore read.                                                                                                                                              | 0x0            |

**Table 170: Auto-Negotiation Link Partner Ability Register (Page 15h: Address 0Ah-0Bh) (Cont.)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                             | <b>Default</b> |
|-------------|-------------|------------|------------------------------------------------|----------------|
| 0           | SGMII       | RO         | SGMII mode<br>0 = Fiber mode<br>1 = SGMII mode | 0              |

## Auto-Negotiation Expansion Register (Page 15h: Address 0Ch)

**Table 171: Auto-Negotiation Expansion Register (Page 15h: Address 0Ch-0Dh)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                        | <b>Default</b> |
|-------------|-------------|------------|-----------------------------------------------------------------------------------------------------------|----------------|
| 15:3        | RESERVED    | RO         | Reserved                                                                                                  | 0x000          |
| 2           | NP_ABILITY  | RO         | Next page ability<br>0 = Local device is not next page capable.<br>1 = Local device is next page capable. | 0              |
| 1           | PG_REC      | RO         | Page received<br>0 = New link code word has not been received.<br>1 = Received new link code word.        | 0              |
| 0           | RESERVED    | RO         | Reserved write 0, ignore read.                                                                            | 0              |

## Extended Status Register (Page 15h: Address 1Eh)

**Table 172: Extended Status Register (Page 15h: Address 1Eh-1Fh)**

| <b>Bits</b> | <b>Name</b>   | <b>R/W</b> | <b>Description</b>                                                           | <b>Default</b> |
|-------------|---------------|------------|------------------------------------------------------------------------------|----------------|
| 15          | 1000BASEX_FDX | RO         | 0 = 1000Base-X full duplex incapable.<br>1 = 1000Base-X full duplex capable. | 1              |
| 14          | 1000BASEX_HDX | RO         | 0 = 1000Base-X half duplex incapable.<br>1 = 1000Base-X half duplex capable. | 1              |
| 13          | 1000BASET_FDX | RO         | 0 = 1000Base-T full duplex incapable.<br>1 = 1000Base-T full duplex capable. | 0              |
| 12          | 1000BASET_HDX | RO         | 0 = 1000Base-T half duplex incapable.<br>1 = 1000Base-T half duplex capable. | 0              |
| 11:0        | RESERVED      | RO         | Reserved write 0, ignore read.                                               | 0x000          |

## SerDes/SGMII Control 1 Register (Page 15h: Address 20h, Block 0)

**Table 173: SerDes/SGMII Control 1 Register (Page 15h: Address 20h-21h, Block 0)**

| Bits | Name                        | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                    | Default |
|------|-----------------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | RESERVED                    | RO  | Reserved write 0, ignore read                                                                                                                                                                                                                                                                                                                                                                  | 0       |
| 14   | DIS_SD_FILTER               | R/W | 0 = Filter signal detect from pin before using for synchronization.<br>1 = Disable filter for signal detect.                                                                                                                                                                                                                                                                                   | 0       |
| 13   | MSTR_MDIO_PHY_SEL           | R/W | 0 = Normal operation.<br>1 = All MDIO write accesses to PHY address "00000" will write this PHY in addition to its own PHY address.                                                                                                                                                                                                                                                            | 0       |
| 12   | SERDES_TX_AMPL_OV<br>ERRIDE | R/W | 0 = If SGMII mode, use analog txCntrl Reg. (reg. 3*10h and reg. 3*11h), if Fiber mode, use analog txAmp Reg. (reg. 3*12h).<br>1 = use analog txCntrl Reg. (reg. 3*10h and reg. 3*11h).                                                                                                                                                                                                         | 0       |
| 11   | SEL_RX_PKTS_FOR_CN<br>TS    | R/W | 0 = Select CRC errors for 0*17h counter.<br>1 = Select received packets for 0*17h counter.                                                                                                                                                                                                                                                                                                     | 0       |
| 10   | REMOTE_LOOPBACK             | R/W | 0 = Normal operation.<br>1 = Enable remote loopback (operates in 10/100/1000) speed.                                                                                                                                                                                                                                                                                                           | 0       |
| 9    | ZERO_COMMA_DET_P<br>HASE    | R/W | 0 = Normal operation.<br>1 = Force comma detector phase to zero.                                                                                                                                                                                                                                                                                                                               | 0       |
| 8    | COMMA_DET_EN                | R/W | 0 = Disable comma detection.<br>1 = Enable comma detection.                                                                                                                                                                                                                                                                                                                                    | 1       |
| 7    | CRC_CHECKER_DIS             | R/W | 0 = Enable CRC checker.<br>1 = Disable CRC checker by gating the clock to save power.                                                                                                                                                                                                                                                                                                          | 1       |
| 6    | DISABLE_PLL_PWRDW<br>N      | R/W | 0 = Pll will be powered down when register 0.11 is set.<br>1 = Pll will never be powered down. (use this when the mac/switch uses the pll_clk125 output).                                                                                                                                                                                                                                      | 0       |
| 5    | SGMII_MSTR_MODE             | R/W | 0 = Normal operation.<br>1 = SGMII mode operates in "PHY mode". If auto-neg is enabled, then the local device will send out the following auto-neg code word:<br>[15] = 1<br>[14] = ACK<br>[13] = 0<br>[12] = Register 0.8<br>[11] = Register 0.6<br>[10] = Register 0.13<br>[9:0] = "0000000001"<br>To disable the link, set register 0.11 = 1.<br>To enable the link, set register 0.11 = 0. | 0       |

**Table 173: SerDes/SGMII Control 1 Register (Page 15h: Address 20h-21h, Block 0) (Cont.)**

| <b>Bits</b> | <b>Name</b>      | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                 | <b>Default</b> |
|-------------|------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 4           | AUTODET_EN       | R/W        | 0 = Disable auto detection (fiber or SGMII mode is set according to bit 0 of this register.)<br>1 = Enable auto-detection (fiber and SGMII mode will switch each time a auto-negotiation page is received with the wrong selector field in bit 0.) | 1              |
| 3           | INVERT_SIG_DET   | R/W        | 0 = Use signal detect from pin.<br>1 = Invert signal detect from pin.                                                                                                                                                                              | 0              |
| 2           | SIGNAL_DETECT_EN | R/W        | 0 = Ignore signal detect from pin.<br>1 = Signal detect from pin must be set in order to achieve synchronization. In SGMII the signal detect is always ignored regardless of the setting of this bit.                                              | 0              |
| 1           | TBI_INTERFACE    | R/W        | 0 = GMII interface<br>1 = Ten-bit interface.                                                                                                                                                                                                       | 0              |
| 0           | FIBER_MODE_1000X | R/W        | 0 = SGMII mode<br>1 = Fiber mode (1000X)                                                                                                                                                                                                           | 0              |

## SerDes/SGMII Control 2 Register (Page 15h: Address 22h, Block 0)

**Table 174: SerDes/SGMII Control 2 Register (Page 15h: Address 22h-23h, Block 0)**

| <b>Bits</b> | <b>Name</b>          | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                             | <b>Default</b> |
|-------------|----------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15          | DIS_EXTEND_FDX       | R/W        | 0 = Normal operation<br>1 = In full duplex mode, disable carrier extension in pcs receive when bit[7] of this register is set and disable TRRR generation in pcs transmit when bit[8] of this register is set.                                 | 0              |
| 14          | CLR_BER_CNTR         | R/W        | 0 = Normal operation<br>1 = Clear bit-error-rate counter (register 0*17h bits[15:8])                                                                                                                                                           | 0              |
| 13          | TX_IDLE_JAM_SEQ_TEST | R/W        | Register 0*1dh bits[9:0] will override k28.5 for stage 5 (17Ch).<br>Register 0*1eh bits[9:0] will override D16.2 for stage 6 (289h).<br>0 = Normal operation.<br>1 = Enable 16-stage 10-bit idle transmit test sequence to SerDes transmitter. | 0              |
| 12          | TX_PKT_SEQ_TEST      | R/W        | Stage 1-4, 13-16 = idle.<br>Stage 5-12 = data packet.<br>0 = Normal operation.<br>1 = Enable 16-stage 10-bit idle transmit test sequence to SerDes transmitter.                                                                                | 0              |

**Table 174: SerDes/SGMII Control 2 Register (Page 15h: Address 22h-23h, Block 0) (Cont.)**

| <b>Bits</b> | <b>Name</b>               | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                          | <b>Default</b> |
|-------------|---------------------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 11          | TEST_CNTR                 | R/W        | 0 = Normal operation.<br>1 = Increment bits[7:0] of register 0*17h counter for each clock cycle.                                                                                                                                                                                                            | 0              |
| 10          | BYPASS_PCS_TX             | R/W        | 0 = Normal operation<br>1 = Bypass pcs transmit operation                                                                                                                                                                                                                                                   | 0              |
| 9           | BYPASS_PCS_RX             | R/W        | 0 = Normal operation<br>1 = Bypass pcs receive operation                                                                                                                                                                                                                                                    | 0              |
| 8           | DISABLE_TRRR_GEN          | R/W        | 0 = Normal operation<br>1 = Disable TRRR generation in pcs transmit                                                                                                                                                                                                                                         | 0              |
| 7           | DISABLE_CARRIER_EXTEND    | R/W        | 0 = Normal operation<br>1 = Disable carrier extension in pcs receive                                                                                                                                                                                                                                        | 0              |
| 6           | AUTONEG_FAST_TIMERS       | R/W        | 0 = Normal operation<br>1 = Speed up timers during auto-negotiation for testing                                                                                                                                                                                                                             | 0              |
| 5           | FORCE_XMIT_DATA_ON_TXSIDE | R/W        | 0 = Normal operation<br>1 = Allow packets to be transmitted regardless of the condition of the link or synchronization                                                                                                                                                                                      | 0              |
| 4           | DIS_REMOTE_FAULT_SENSING  | R/W        | 0 = Automatically detect remote faults and send remote fault status to link partner using auto-negotiation when Fiber mode is selected. (SGMII does not support remote faults)<br>1 = Disable automatic sensing of remote faults, such as auto-negotiation error                                            | 0              |
| 3           | ENABLE_AUTONEG_ERR_TIMER  | R/W        | 0 = Normal operation<br>1 = Enable auto-negotiation error timer. Error occurs when timer expires in ability-detect, ack-detect, or idle-detect. When the error occurs, config words of all zeros are sent until an ability match occurs, then the autoneg-enable state is entered.                          | 0              |
| 2           | FILTER_FORCE_LINK         | R/W        | 0 = Normal operation<br>1 = Sync-status must be set for a solid 10ms before a valid link will be established when auto-negotiation is disabled. (This is useful in fiber applications where the user does not have the signal detect pin connected to the fiber module and auto-negotiation is turned off.) | 1              |
| 1           | DISABLE_FALSE_LINK        | R/W        | 0 = Normal operation<br>1 = Do not allow link to be established when auto-negotiation is disabled and receiving auto-negotiation code words. The link will only be established in this case after idles are received. (This bit does not need to be set, if bit 0 below is set.)                            | 1              |

**Table 174: SerDes/SGMII Control 2 Register (Page 15h: Address 22h-23h, Block 0) (Cont.)**

| Bits | Name                      | R/W | Description                                                                                                                                                                                                                                                                | Default |
|------|---------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 0    | ENABLE_PARALLEL_DETECTION | R/W | 0 = Disable parallel detection<br>1 = Enable parallel detection. (This will turn auto-negotiation on and off as needed to properly link up with the link partner. The idles and auto-negotiation code words received from the link partner are used to make this decision) | 1       |

## SerDes/SGMII Control 3 Register (Page 15h: Address 24h, Block 0)

**Table 175: SerDes/SGMII Control 3 Register (Page 15h: Address 24h-25h, Block 0)**

| Bits | Name                   | R/W | Description                                                                                                                                                                                                                                                | Default |
|------|------------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | DISABLE_PKT_ALIGNMENT  | R/W | 0 = Normal operation.<br>1 = Disable packet misalignment by carrier extend and removing preamble.                                                                                                                                                          | 0       |
| 14   | RXFIFO_GMII_RST        | R/W | 0 = Normal operation.<br>1 = Reset receive FIFO and data_out_1000. FIFO remains in reset until this bit is cleared with a software write.                                                                                                                  | 0       |
| 13   | DISABLE_TX_CRIS        | R/W | 0 = Normal operation.<br>1 = Disable generating CRS from transmitting in half-duplex mode. Only receiving will generate CRS.                                                                                                                               | 0       |
| 12   | INVERT_EXT_PHY_CRIS    | R/W | 0 = Use "receive CRS from PHY" pin.<br>1 = Invert "receive CRS from PHY" pin                                                                                                                                                                               | 0       |
| 11   | EXT_PHY_CRIS_MODE      | R/W | 0 = Normal operation.<br>1 = Use external pin for the PHY's receive-only CRS output. (Useful in SGMII 10/100 half-duplex applications in order to reduce the collision domain latency. Requires a PHY which generates a receive-only CRS output to a pin.) | 0       |
| 10   | JAM_FALSE_CARRIER_MODE | R/W | 0 = Normal operation.<br>1 = Change false carriers received into packets with preamble only. (Not necessary if MAC uses CRS to determine collision)                                                                                                        | 0       |
| 9    | BLOCK_TXEN_MODE        | R/W | 0 = Normal operation.<br>1 = Block TXEN when necessary to guarantee an IPG of at least 6.5 bytes in 10/100 mode, 7 bytes in 1000 mode.                                                                                                                     | 0       |
| 8    | FORCE_TXFIFO_ON        | R/W | 0 = Normal operation.<br>1 = Force transmit FIFO to free-run in gigabit mode (Requires clk_in and pll_clk125 to be frequency locked.)                                                                                                                      | 0       |

**Table 175: SerDes/SGMII Control 3 Register (Page15h: Address 24h-25h, Block 0) (Cont.)**

| Bits | Name                    | R/W | Description                                                                                                                                                                                                                                                                                                     | Default |
|------|-------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7    | BYPASS_TXFIFO1000       | R/W | 0 = Normal operation.<br>1 = Bypass transmit FIFO in gigabit mode. (Useful for fiber or gigabit only applications where the MAC is using the pll_clk125 as the clk_in port. User must meet timing to the pll_clk125 domain)                                                                                     | 0       |
| 6    | FREQ_LOCK_ELASTICITY_TX | R/W | 0 = Normal operation.<br>1 = Minimum FIFO latency to properly handle a clock which is frequency locked, but out of phase. (overrides bits [2:1] of this register).<br><b>Note:</b> pll_clk125 and clk_in must be using the same crystal.                                                                        | 1       |
| 5    | FREQ_LOCK_ELASTICITY_RX | R/W | 0 = Normal operation<br>1 = Minimum FIFO latency to properly handle a clock which is frequency locked, but out of phase. (Not necessary if MAC uses CRS to determine collision; overrides bits [2:1] of this register).<br><b>Note:</b> MAC and PHY must be using the same crystal for this mode to be enabled. | 0       |
| 4    | EARLY_PREAMBLE_RX       | R/W | 0 = Normal operation<br>1 = Send extra bytes of preamble to avoid FIFO latency. (Not necessary if MAC uses CRSCRS to determine collision)                                                                                                                                                                       | 0       |
| 3    | EARLY_PREAMBLE_TX       | R/W | 0 = Normal operation<br>1 = Send extra bytes of preamble to avoid FIFO latency. (Used in half-duplex applications to reduce collision domain latency. MAC must send 5 bytes of preamble or less to avoid noncompliant behavior.)                                                                                | 0       |
| 2:1  | FIFO_ELASTICITY_TX_RX   | R/W | 00 = Supports packets up to 5 KB<br>01 = Supports packets up to 10 KB<br>1X = Supports packets up to 13.5 KB                                                                                                                                                                                                    | 01      |
| 0    | TX_FIFO_RST             | R/W | 0 = Normal operation<br>1 = Reset transmit FIFO. FIFO remains in reset until this bit is cleared with a software write.                                                                                                                                                                                         | 0       |

## SerDes/SGMII Status 1 Register (Page 15h: Address 28h, Block 0)

**Table 176: SerDes/SGMII Status 1 Register (Page 15h: Address 28h-29h, Block 0)**

| Bits | Name                | R/W | Description                                                                                               | Default |
|------|---------------------|-----|-----------------------------------------------------------------------------------------------------------|---------|
| 15   | TXFIFO_ERR_DETECTED | RO  | 1 = Transmit FIFO error detected since last read.<br>0 = No transmit FIFO error detected since last read. | 0       |
| 14   | RXFIFO_ERR_DETECTED | RO  | 1 = Receive FIFO error detected since last read.<br>0 = No receive FIFO error detected since last read.   | 0       |

**Table 176: SerDes/SGMII Status 1 Register (Page 15h: Address 28h-29h, Block 0) (Cont.)**

| <b>Bits</b> | <b>Name</b>              | <b>R/W</b> | <b>Description</b>                                                                                                                                            | <b>Default</b> |
|-------------|--------------------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 13          | FALSE_CARRIER_DETECTED   | RO         | 1 = False carrier detected since last read.<br>0 = No false carrier detected since last read.                                                                 | 0              |
| 12          | CRC_ERR_DETECTED         | RO         | 1 = CRC error detected since last read.<br>0 = No CRC error detected since last read or detection is disabled using register 0*10h bit [7].                   | 0              |
| 11          | TX_ERR_DETECTED          | RO         | 1 = Transmit error code detected since last read (rx_data_error state in pcs receive fsm).<br>0 = No transmit error code detected since last read.            | 0              |
| 10          | RX_ERR_DETECTED          | RO         | 1 = Receive error since last read (early_end state in pcs receive fsm)<br>0 = No receive error since last read                                                | 0              |
| 9           | CARRIER_EXT_ERR_DETECTED | RO         | 1 = Carrier extend error since last read (extend_err in pcs receive fsm)<br>0 = No carrier extend error since last read                                       | 0              |
| 8           | EARLY_END_EXT_DETECTED   | RO         | 1 = Early end extension since last read (early_end_ext in pcs receive fsm)<br>0 = No early end extension since last read                                      | 0              |
| 7           | LINK_STATUS_CHG          | RO         | 1 = Link status has changed since last read<br>0 = Link status has not changed since last read                                                                | 0              |
| 6           | PAUSE_RESOLUTION_RXSIDE  | RO         | 1 = Enable pause receive<br>0 = Disable pause receive                                                                                                         | 0              |
| 5           | PAUSE_RESOLUTION_TXSIDE  | RO         | 1 = Enable pause transmit<br>0 = Disable pause transmit                                                                                                       | 0              |
| 4:3         | SPEED_STATUS             | RO         | 1X = Gigabit<br>01 = 100 Mbps<br>00 = 10 Mbps                                                                                                                 | 10             |
| 2           | DUPLEX_STATUS            | RO         | 1 = Full duplex<br>0 = Half duplex<br><b>Note:</b> When the ten bit interface is selected with Fiber mode (1000-X), then half-duplex will always be reported. | 0              |
| 1           | LINK_STATUS              | RO         | 1 = Link is up.<br>0 = Link is down.<br><b>Note:</b> When the ten-bit interface is selected with Fiber mode (1000-X), then link will always be down           | 0              |
| 0           | SGMII_MODE               | RO         | 1 = SGMII mode<br>0 = Fiber mode (1000-X)                                                                                                                     | 1              |

## SerDes/SGMII Status 2 Register (Page15h: Address 2Ah, Block 0)

**Table 177: SerDes/SGMII Status 2 Register (Page15h: Address 2Ah-2Bh, Block 0)**

| Bits | Name                    | R/W | Description                                                                                                                                                                                                                                                     | Default |
|------|-------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15   | SGMII_MODE_CHG          | RO  | 1 = SGMII mode has changed since last read (SGMII mode enabled or disabled).<br><b>Note:</b> This bit is useful when the auto-detection is enabled in register 0*10h bit [4].<br>0 = SGMII mode has not changed since last read (fixed in SGMII or Fiber mode). | 0       |
| 14   | CONSISTENCY_MISMATCH    | RO  | 1 = Consistency mismatch detected since last read.<br>0 = Consistency mismatch has not been detected since last read.                                                                                                                                           | 0       |
| 13   | AUTONEG_RES_ERR         | RO  | 1 = Auto-negotiation HCD error detected since last read (HCD is none in Fiber mode).<br>0 = Auto-negotiation HCD error has not been detected since last read.                                                                                                   | 0       |
| 12   | SGMII_SELECTOR_MISMATCH | RO  | 1 = SGMII selector mismatch detected since last read (auto-negotiation page received from link partner with bit [0] = 0 while local device is in SGMII mode).<br>0 = SGMII selector mismatch not detected since last read.                                      | 0       |
| 11   | SYNC_STATUS_FAIL        | RO  | 1 = Sync_status has failed since last read (synchronization has been lost).<br>0 = Sync_status has not failed since last read.                                                                                                                                  | 1       |
| 10   | SYNC_STATUS_OK          | RO  | 1 = Sync_status ok detected since last read (synchronization has been achieved).<br>0 = Sync_status ok has not been detected since last read.                                                                                                                   | 0       |
| 9:7  | RESERVED                | RO  | Reserved                                                                                                                                                                                                                                                        | 3'b001  |
| 6    | LINK_DOWN_SYNC_LOSS     | RO  | 1 = Valid link went down due to a loss of synchronization for over 10 ms.<br>0 = Failure condition has not been detected since last read.                                                                                                                       | 0       |
| 5:1  | RESERVED                | RO  | Reserved                                                                                                                                                                                                                                                        | 0       |
| 0    | ANEG_ENABLE_STATE       | RO  | 1 = An_enable state in auto-negotiation fsm entered since last read.<br>0 = An_enable state has not been entered since last read.                                                                                                                               | 1       |

## SerDes/SGMII Status 3 Register (Page 15h: Address 2Ch, Block 0)

**Table 178: SerDes/SGMII Status 3 Register (Page 15h: Address 2Ch–2Dh, Block 0)**

| Bits  | Name           | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                          | Default |
|-------|----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:11 | RESERVED       | RO  | Reserved                                                                                                                                                                                                                                                                                                                                                                                             | 0x00    |
| 10    | LATCH_LINKDOWN | RO  | 1 = Link has been down since register 0*13h bit [9] has been written a '1'<br>0 = Link has not been down since register 0*13h bit [9] has been written a '1'                                                                                                                                                                                                                                         | 0       |
| 9     | SD_FILTER      | RO  | 1 = Output of signal detect filter is set<br>0 = Output of signal detect is not set<br><b>Note:</b> This signal is used for the PCS synchronization. When register 0*10h bit [2] is 0, then the output of the filter will be forced high. This status signal is still valid when register 0*10h bit [14] is 1. Noise pulses less than 16 ns wide are still removed when even the filter is disabled. | 0       |
| 8     | SD_MUX         | RO  | 1 = Output of signal detect filter is set<br>0 = Output of signal detect is not set<br><b>Note:</b> This is the only SD status bit that will be valid when the SerDes is powered down from register 0.11. This status signal is the “signal detect” input port when register 0*10h bit [3] is 0, otherwise it is the “signal detect” input port inverted.                                            | 0       |
| 7     | SD_FILTER_CHG  | RO  | 1 = Signal detect has changed since last read<br>0 = Signal detect has not changed since last read<br><b>Note:</b> The signal detect change is based on a change in bit [9] of this register                                                                                                                                                                                                         | 0       |
| 6     | SIGNAL_DETECT  | RO  | Signal detect directly from pin                                                                                                                                                                                                                                                                                                                                                                      | 0       |
| 5     | ANA_SIGNAL_DET | RO  | Analog signal detect status bit. This status signal is the analog signal detect status if register 0*13h bit [0] is set, otherwise it is the value based on register 0*13h bit [1].                                                                                                                                                                                                                  | 0       |
| 4     | ANA_SIGDET_CHG | RO  | 1 = Analog signal detect has changed since last read<br>0 = Analog signal detect has not changed since last read<br><b>Note:</b> The analog signal detect change is based on a change in bit [5] of this register.                                                                                                                                                                                   | 0       |
| 3:0   | RESERVED       | RO  | Reserved                                                                                                                                                                                                                                                                                                                                                                                             | 0       |

## 100FX Enabling Control Register (Page 15h: Address 20h, Block 2)

**Table 179: 100FX Enabling Control Register (Page 15h: Address 20h, Block 2)**

| Bits | Name                    | R/W | Description                                                                               | Default |
|------|-------------------------|-----|-------------------------------------------------------------------------------------------|---------|
| 15   | RESERVED                | R/W | Reserved                                                                                  | 0       |
| 14   | FIBER_AUTOPWRDWN_WAKEUP | R/W | 1 = Wake up for 250 ms before powering down<br>0 = Wake up for 42 ms before powering down | 0       |

**Table 179: 100FX Enabling Control Register (Page 15h: Address 20h, Block 2) (Cont.)**

| <b>Bits</b> | <b>Name</b>              | <b>R/W</b> | <b>Description</b>                                                                                                                                                                             | <b>Default</b> |
|-------------|--------------------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 13          | FIBER_AUTOPWRDWN_SLEEP   | R/W        | 1 = Power down for 3 seconds before waking up<br>0 = Power down for 5 seconds before waking up                                                                                                 | 0              |
| 12          | FIBER_AUTOPWRDWN_ENABLE  | R/W        | 1 = Power down fiber when signal detect is inactive (wake up for 42 ms every 5 seconds to transmit code words; see register 2*10h[13:12] for different time options).<br>0 = Normal operation. | 0              |
| 11          | FIBER_AUTOPWRDWN_DISABLE | R/W        | 1 = Disable 1000-X power down from fiber auto-power down (register 0[11] powerdown not affected).<br>0 = Normal operation                                                                      | 0              |
| 10          | FX100_AUTODET_TIMER_SEL  | R/W        | 1 = 125 ms–166 ms (do not use if fiber auto-power down is enabled; register 2*10h[12]).<br>0 = 31 ms–42 ms                                                                                     | 0              |
| 9:6         | FX100_RXDATA_SEL         | R/W        | Selects the sample bit out of 10 bits for FX100 RX data                                                                                                                                        | 0x9            |
| 5           | FX100_DISABLE_RX_QUAL    | R/W        | 1 = Always use sample bit without filtering<br>0 = Normal operation                                                                                                                            | 0              |
| 4           | FX100_FORCE_RX_QUAL      | R/W        | 1 = Always compare 2 surrounding bits with sample to filter noise<br>0 = Normal operation                                                                                                      | 0              |
| 3           | FX100_FAREND_FAULT_EN    | R/W        | 1 = Enable far-end fault<br>0 = Disable far-end fault                                                                                                                                          | 1              |
| 2           | FX100_AUTODET_EN         | R/W        | 1 = Auto-detect between 100FX mode and 1000-X mode<br>0 = Disable auto-detection                                                                                                               | 0              |
| 1           | FX100_FULL_DUPLEX        | R/W        | 1 = 100-FX SerDes full-duplex<br>0 = 100-FX SerDes half-duplex                                                                                                                                 | 1              |
| 0           | FX100_ENABLE             | R/W        | 1 = Select 100-FX mode<br>0 = Select 1000-X mode                                                                                                                                               | 0              |

## 100FX Extended Packet Size Register (Page 15h: Address 22h, Block 2)

**Table 180: 100FX Extended Packet Size Register (Page 15h: Address 22h, Block 2)**

| <b>Bits</b> | <b>Name</b>     | <b>R/W</b> | <b>Description</b>                                                                              | <b>Default</b> |
|-------------|-----------------|------------|-------------------------------------------------------------------------------------------------|----------------|
| 15:1        | RESERVED        | R/W        | Reserved                                                                                        | 0x000          |
| 0           | EXTEND_PKT_SIZE | R/W        | 1 = Allow reception of extended length packets<br>0 = Allow normal length Ethernet packets only | 0              |

## 100FX Control Register (Page 15h: Address 24h, Block 2)

**Table 181: 100FX Control Register (Page 15h: Address 24h, Block 2)**

| Bits | Name                    | R/W | Description                                                                                                     | Default |
|------|-------------------------|-----|-----------------------------------------------------------------------------------------------------------------|---------|
| 15:7 | RESERVED                | R/W | Reserved                                                                                                        | 0x000   |
| 6    | FX100_BYPASS_NRZ        | R/W | 1 = Bypass NRZ encoder in 100FX mode<br>0 = Normal operation                                                    | 0       |
| 5    | FX100_BYPASS_ENCODER    | R/W | 1 = Bypass 4B5B encoder in 100FX mode<br>0 = Normal operation                                                   | 0       |
| 4    | FX100_BYPASS_ALIGNMENT  | R/W | 1 = Bypass 5B code group alignment in 100FX mode<br>0 = Normal operation                                        | 0       |
| 3    | FX100_FORCE_LINK        | R/W | 1 = Force link in 100FX mode<br>0 = Normal operation                                                            | 0       |
| 2    | FX100_FORCE_LOCK        | R/W | 1 = Force lock in 100FX mode<br>0 = Normal operation                                                            | 0       |
| 1    | FX100_FAST_UNLOCK_TIMER | R/W | 1 = Speed up unlock timer in 100FX mode<br>0 = Normal operation                                                 | 0       |
| 0    | FX100_FAST_TIMER        | R/W | 1 = Speed up timer to acquire lock and link (test vectors and simulation) in 100FX mode<br>0 = Normal operation | 0       |

## 100FX Link Status Register (Page 15h: Address 26h, Block 2)

**Table 182: 100FX Link Status Register (Page 15h: Address 26h, Block 2)**

| Bits  | Name                         | R/W   | Description                                                                                                                                           | Default |
|-------|------------------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:10 | RESERVED                     | R/W   | Reserved                                                                                                                                              | 0x00    |
| 9     | FX100_LINK_STATUS_CHG        | RO/LH | 1 = 100-FX mode link status change since last read<br>0 = 100-FX mode link status has not changed since last read                                     | 0       |
| 8     | FX100_BAD_ESD_DETECTED       | RO/LH | 1 = 100-FX mode bad ESD error detected since last read (premature end)<br>0 = No 100-FX mode bad ESD error detected since last read                   | 0       |
| 7     | FX100_FALSE_CARRIER_DETECTED | RO/LH | 1 = 100-FX mode false carrier detected since last read<br>0 = No 100-FX mode false carrier detected since last read                                   | 0       |
| 6     | FX100_TX_ERR_DETECTED        | RO/LH | 1 = 100-FX mode received packet with txer code detected since last read<br>0 = No 100-FX mode received packet with txer code detected since last read | 0       |

**Table 182: 100FX Link Status Register (Page 15h: Address 26h, Block 2) (Cont.)**

| Bits | Name                     | R/W   | Description                                                                                                                       | Default |
|------|--------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------|---------|
| 5    | FX100_RX_ERR_DETECTED    | RO/LH | 1 = 100-FX mode receive coding error detected since last read<br>0 = No 100-FX mode receive coding error detected since last read | 0       |
| 4    | FX100_LOCK_TIMER_EXPIRED | RO/LH | 1 = Unable to lock within 730us since last read<br>0 = Condition not detected since last read                                     | 0       |
| 3    | FX100_LOST_LOCK          | RO/LH | 1 = Lost lock since last read<br>0 = Lock has not been lost since last read                                                       | 0       |
| 2    | FX100_FAULTING           | RO/LH | 1 = Far end fault detected since last read<br>0 = No far end fault detected since last read                                       | 0       |
| 1    | FX100_LOCKED             | RO    | 1 = Enough idles are properly detected to lock<br>0 = Not locked                                                                  | 0       |
| 0    | FX100_LINK               | RO    | 1 = 100-FX mode link is up<br>0 = 100-FX mode link is down                                                                        | 0       |

## Analog TX1 Register (Page 15h: Address 20h, Block 3)

**Table 183: Analog TX1 Register (Page 15h: Address 20h, Block 3)**

| Bits  | Name           | R/W | Description                                                                                           | Default |
|-------|----------------|-----|-------------------------------------------------------------------------------------------------------|---------|
| 15:12 | DRIVER_CURRENT | R/W | Setting the output amplitude of the SerDes ranging from 700 mV to 1280 mV.                            | 0xa     |
| 11    | RESERVED       | R/W | Reserved                                                                                              | 0       |
| 10:7  | PREEMPH_COEF   | R/W | Setting the preemphasis level for the SerDes driver, ranging from 0% to 60%.                          | 0       |
| 6     | RX_CLKP        | R/W | Reserved for factory use only.<br>1 = Select RX clock<br>0 = Do not select RX clock                   | 0       |
| 5     | REG_EDGE_SEL   | R/W | Reserved for factory use only.<br>1 = Capture on rising edge<br>0 = Capture on falling edge           | 1       |
| 4     | BOOST_MODE     | R/W | Reserved for factory use only<br>1 = Enable boost output current for preamp driver<br>0 = Normal mode | 0       |
| 3     | DRIVER_IDLE    | R/W | 1 = Enable transmit driver idle<br>0 = Disable transmit driver idle                                   | 0       |

**Table 183: Analog TX1 Register (Page 15h: Address 20h, Block 3) (Cont.)**

| <b>Bits</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                          | <b>Default</b> |
|-------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 2           | LOOPBACK    | R/W        | 1 = Enable remote loopback. The far end sends the data to the device and the data is looped back to the wire at the analog block prior of reaching to the deserializer. The data will not reach the device MAC block. In order to use the remote loopback, both loopback bits must be set in the ANALOG_TX and ANALOG_RX registers.<br>0 = Normal operation | 0              |
| 1           | RESET       | R/W        | 1 = SerDes is in reset<br>0 = SerDes is not in reset                                                                                                                                                                                                                                                                                                        | 0              |
| 0           | IDDQ        | R/W        | 1 = Power down the driver<br>0 = Normal operation                                                                                                                                                                                                                                                                                                           | 0              |

## Analog TX2 Register (Page 15h: Address 22h, Block 3)

**Table 184: Analog TX2 Register (Page 15h: Address 22h, Block 3)**

| <b>Bits</b> | <b>Name</b>       | <b>R/W</b> | <b>Description</b>                                                        | <b>Default</b> |
|-------------|-------------------|------------|---------------------------------------------------------------------------|----------------|
| 15:4        | RESERVED          | R/W        | Reserved                                                                  | 0x300          |
| 3:0         | PREDRIVER_CURRENT | R/W        | Controls output driving amplitude: set in conjunction with DRIVER_CURRENT | 0x7            |

## Analog TXAMP Register (Page 15h: Address 24h, Block 3)

**Table 185: Analog TXAMP Register (Page 15h: Address 24h, Block 3)**

| <b>Bits</b> | <b>Name</b>           | <b>R/W</b> | <b>Description</b>                                                                                                              | <b>Default</b> |
|-------------|-----------------------|------------|---------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15          | DRIVER_FULL_RANGE     | R/W        | Reserved for factory use only.<br>1 = Enable TX driver full output range<br>0 = Disable TX driver full output range             | 0              |
| 14          | PREDRIVER_SWING_BOOST | R/W        | Reserved for factory use only.<br>1 = Enable final stage predriver swing boost<br>0 = Disable final stage predriver swing boost | 0              |
| 13:10       | RESERVED              | R/W        | Reserved                                                                                                                        | 0x0            |
| 9           | BMODE                 | R/W        | Reserved for factory use only.<br>1 = Enable transmit boost mode<br>0 = Normal operation                                        | 0              |
| 8:5         | PREDRIVER_CURRENT     | R/W        | This is to control the output driving amplitude. This is set in conjunction with the DRIVER_CURRENT                             | 0x1            |
| 4:1         | DRIVER_CURRENT        | R/W        | Setting the output amplitude of the SerDes ranging from 700 mV to 1280 mV.                                                      | 0x3            |
| 0           | RESERVED              | R/W        | Reserved                                                                                                                        | 0              |

## Analog RX1 Register (Page 15h: Address 26h, Block 3)

**Table 186: Analog RX1 Register (Page 15h: Address 26h, Block 3)**

| Bits  | Name            | R/W | Description                                                                                                                                                                                    | Default |
|-------|-----------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:13 | RESERVED        | R/W | Reserved                                                                                                                                                                                       | 3'b001  |
| 12:10 | SD_THRESHOLD    | R/W | Controls when signal detect should be asserted, based on energy level.<br>000 = 10 mV<br>001 = 20 mV<br>011 = 30 mV<br>010 = 40 mV<br>110 = 50 mV<br>111 = 60 mV<br>101 = 70 mV<br>100 = 80 mV | 3'b010  |
| 9     | SIGDET_EN       | R/W | 1 = Enable signal detect<br>0 = Disable signal detect                                                                                                                                          | 1       |
| 8     | LOOPBACK        | R/W | Set to enable remote loopback. This must be set in conjunction with the loopback bit under ANALOG_TX1 register.<br>1 = Enable loopback<br>0 = Normal operation                                 | 0       |
| 7     | REG_EDGE_SELECT | R/W | Reserved for factory use only.<br>1 = Use rising edge of rx_wclk<br>0 = Use falling edge of rx_wclk                                                                                            | 1       |
| 6:1   | RESERVED        | R/W | Reserved                                                                                                                                                                                       | 0x00    |
| 0     | IDDQ            | R/W | Set to power down analog receiver block<br>1 = Power down RX<br>0 = Normal operation                                                                                                           | 0       |

## Analog RX2 Register (Page 15h: Address 28h, Block 3)

**Table 187: Analog RX2 Register (Page 15h: Address 28h, Block 3)**

| Bits | Name         | R/W | Description                                                             | Default |
|------|--------------|-----|-------------------------------------------------------------------------|---------|
| 15:4 | RESERVED     | R/W | Reserved                                                                | 0x000   |
| 3    | 100FX_ENABLE | R/W | Enables SerDes in 100-FX mode<br>1 = FX100 mode<br>0 = Normal operation | 0       |
| 2:0  | RESERVED     | R/W | Reserved                                                                | 0x0     |

## Analog PLL Register (Page 15h: Address 30h, Block 3)

*Table 188: Analog PLL Register (Page 15h: Address 30h, Block 3)*

| <i>Bits</i> | <i>Name</i>    | <i>R/W</i> | <i>Description</i>                         | <i>Default</i> |
|-------------|----------------|------------|--------------------------------------------|----------------|
| 15:1        | RESERVED       | R/W        | Reserved                                   | 0x4040         |
| 0           | PLL_POWER_DOWN | R/W        | 1 = PLL power down<br>0 = Normal operation | 0              |

## Block Address Number (Page 010h–017h: Address 03Eh)

*Table 189: Block Address Number (Page 010h-017h: Address 03Eh-03Fh)*

| <i>Bits</i> | <i>Name</i> | <i>R/W</i> | <i>Description</i>                                                                                                                                                                                                                                            | <i>Default</i> |
|-------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 15:4        | RESERVED    | R/W        | Reserved write 0, ignore read                                                                                                                                                                                                                                 | 0x000          |
| 3:0         | BLK_NO      | R/W        | MII address registers 00-0Fh and 1Fh do not use the block addressing and are fixed. Block 0, 2, or 3 selected using these bits:<br>0000 = Valid (block0)<br>0010 = Valid (block2)<br>0011 = Valid (block3)<br>0001, 1111 = reserved for future implementation | 0x0            |

## Page 20h–28h: Port MIB Registers

**Table 190: Port MIB Registers Page Summary**

| <b>Page</b> | <b>Description</b> |
|-------------|--------------------|
| 20h         | Port 0             |
| 21h         | Port 1             |
| 22h         | Port 2             |
| 23h         | Port 3             |
| 24h         | Port 4             |
| 25h         | Port 5             |
| 26h         | Reserved           |
| 27h         | Reserved           |
| 28h         | IMP port           |

**Table 191: Page 20h–28h Port MIB Registers**

| <b>ADDR</b> | <b>Bits</b> | <b>Name</b>          | <b>Description</b>                                                                                                                                                                                                                                         |
|-------------|-------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00h–07h     | 64          | TxOctets             | Total number of good bytes of data transmitted by a port (excluding preamble, but including FCS)                                                                                                                                                           |
| 08h–0Bh     | 32          | TxDropPkts           | This counter is incremented every time a transmit packet is dropped due to lack of resources (such as transmit FIFO underflow), or an internal MAC sublayer transmit error not counted by either the TxLateCollision or the TxExcessiveCollision counters. |
| 0Ch–0Fh     | 32          | TxQOPKT              | Total number of good packets transmitted on CoS0, specified in MIB queue select register when QoS is enabled                                                                                                                                               |
| 10h–13h     | 32          | TxBroadcastPkts      | Number of good packets transmitted by a port that are directed to a broadcast address. This counter does not include errored broadcast packets or valid multicast packets.                                                                                 |
| 14h–17h     | 32          | TxMulticastPkts      | Number of good packets transmitted by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.                                                                                 |
| 18h–1Bh     | 32          | TxUnicastPkts        | Number of good packets transmitted by a port that are addressed to a unicast address.                                                                                                                                                                      |
| 1Ch–1Fh     | 32          | TxCollisions         | Number of collisions experienced by a port during packet transmissions.                                                                                                                                                                                    |
| 20h–23h     | 32          | TxSingleCollision    | Number of packets successfully transmitted by a port that experienced exactly one collision.                                                                                                                                                               |
| 24h–27h     | 32          | TxMultiple Collision | Number of packets successfully transmitted by a port that experienced more than one collision.                                                                                                                                                             |
| 28h–2Bh     | 32          | TxDeferredTransmit   | Number of packets transmitted by a port for which the first transmission attempt is delayed because the medium is busy.                                                                                                                                    |

**Table 191: Page 20h–28h Port MIB Registers (Cont.)**

| <b>ADDR</b> | <b>Bits</b> | <b>Name</b>          | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------------|-------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2Ch–2Fh     | 32          | TxLateCollision      | Number of times that a collision is detected later than 512 bit-times into the transmission of a packet.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 30h–33h     | 32          | TxExcessiveCollision | Number of packets that are not transmitted from a port because the packet experienced 16 transmission attempts.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 34h–37h     | 32          | TxFramelnDisc        | Number of valid packets received that are discarded by the forwarding process due to lack of space on an output queue. (Not maintained or reported in the MIB counters and located in the congestion management registers [Page 0Ah].) This attribute only increments if a network device is not acting in compliance with a flow-control request or the BCM53115S internal flow control/buffering scheme has been misconfigured.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 38h–3Bh     | 32          | TxPausePkts          | Number of PAUSE events on a given port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 3Ch–3Fh     | 32          | TxQ1PKT              | Total number of good packets transmitted on CoS1, which is specified in MIB queue select register when QoS is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 40h–43h     | 32          | TxQ2PKT              | Total number of good packets transmitted on CoS2, which is specified in MIB queue select register when QoS is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 44h–47h     | 32          | TxQ3PKT              | Total number of good packets transmitted on CoS3, which is specified in MIB queue select register when QoS is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 48h–4Bh     | 32          | Reserved             | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 4Ch–4Fh     | 32          | Reserved             | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 50h–57h     | 64          | RxOctets             | Number of bytes of data received by a port (excluding preamble, but including FCS), including bad packets.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 58h–5Bh     | 32          | RxUndersizePkts      | Number of good packets received by a port that are less than 64 bytes in length (excluding framing bits, but including the FCS).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 50h–5Fh     | 32          | RxPausePkts          | Number of PAUSE frames received by a port. The PAUSE frame must have a valid MAC control frame EtherType field (88–08h), have a destination MAC address of either the MAC control frame reserved multicast address (01-80-C2-00-00-01) or the unique MAC address associated with the specific port, a valid PAUSE Opcode (00–01), be a minimum of 64 bytes in length (excluding preamble, but including FCS), and have a valid CRC. Although an IEEE 802.3-compliant MAC is only permitted to transmit PAUSE frames when in full-duplex mode with flow control enabled and with the transfer of PAUSE frames determined by the result of auto-negotiation, an IEEE 802.3 MAC receiver is required to count all received PAUSE frames, regardless of its half/full-duplex status. An indication that a MAC is in half-duplex with the RxPausePkts incrementing indicates a noncompliant transmitting device on the network. |
| 60h–63h     | 32          | Pkts64Octets         | Number of packets (including error packets) that are 64 bytes long.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 64h–67h     | 32          | Pkts65to127Octets    | Number of packets (including error packets) that are between 65 and 127 bytes long.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

**Table 191: Page 20h–28h Port MIB Registers (Cont.)**

| <b>ADDR</b> | <b>Bits</b> | <b>Name</b>            | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                 |
|-------------|-------------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 68h–6Bh     | 32          | Pkts128to255Octets     | Number of packets (including error packets) that are between 128 and 255 bytes long.                                                                                                                                                                                                                                                                                                               |
| 6Ch–6Fh     | 32          | Pkts256to511Octets     | Number of packets (including error packets) that are between 256 and 511 bytes long.                                                                                                                                                                                                                                                                                                               |
| 70h–73h     | 32          | Pkts512to1023Octets    | Number of packets (including error packets) that are between 512 and 1023 bytes long.                                                                                                                                                                                                                                                                                                              |
| 74h–77h     | 32          | Pkts1024toMaxPktOctets | Number of packets (including error packets) that are between 1024 and MaxPacket bytes long.                                                                                                                                                                                                                                                                                                        |
| 78h–7Bh     | 32          | RxOversizePkts         | Number of good packets received by a port that are greater than standard max frame size.                                                                                                                                                                                                                                                                                                           |
| 7Ch–7Fh     | 32          | RxJabbers              | Number of packets received by a port that are longer than 1522 bytes and have either an FCS error or an alignment error.                                                                                                                                                                                                                                                                           |
| 80h–83h     | 32          | RxAlignmentErrors      | Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with a nonintegral number of bytes.                                                                                                                                                                                      |
| 84h–87h     | 32          | RxFCSErrors            | Number of packets received by a port that have a length (excluding framing bits, but including FCS) between 64 and standard max frame size, inclusive, and have a bad FCS with an integral number of bytes.                                                                                                                                                                                        |
| 88h–8Fh     | 64          | RxGoodOctets           | Total number of bytes in all good packets received by a port (excluding framing bits but including FCS)                                                                                                                                                                                                                                                                                            |
| 90h–93h     | 32          | RxDropPkts             | Number of good packets received by a port that were dropped due to lack of resources (such as lack of input buffers) or were dropped due to lack of resources before a determination of the validity of the packet was able to be made (such as receive FIFO overflow). The counter is only incremented if the receive error was not counted by the RxAlignmentErrors or the RxFCSErrors counters. |
| 94h–97h     | 32          | RxUnicastPkts          | Number of good packets received by a port that are addressed to a unicast address.                                                                                                                                                                                                                                                                                                                 |
| 98h–9Bh     | 32          | RxMulticastPkts        | Number of good packets received by a port that are directed to a multicast address. This counter does not include errored multicast packets or valid broadcast packets.                                                                                                                                                                                                                            |
| 9Ch–9Fh     | 32          | RxBroadcastPkts        | Number of good packets received by a port that are directed to the broadcast address. This counter does not include errored broadcast packets or valid multicast packets.                                                                                                                                                                                                                          |
| A0h–A3h     | 32          | RxSACHanges            | Number of times the SA of good receive packets has changed from the previous value. A count greater than 1 generally indicates the port is connected to a repeater-based network.                                                                                                                                                                                                                  |
| A4h–A7h     | 32          | RxFragments            | Number of packets received by a port that are less than 64 bytes (excluding framing bits) and have either an FCS error or an alignment error.                                                                                                                                                                                                                                                      |

**Table 191: Page 20h–28h Port MIB Registers (Cont.)**

| <b>ADDR</b> | <b>Bits</b> | <b>Name</b>                                                          | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                            |
|-------------|-------------|----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A8h–ABh     | 32          | JumboPkt                                                             | Number of frames received with frame size greater than the Standard Maximum Size and less than or equal to the Jumbo Frame Size, regardless of CRC or Alignment errors.<br><b>Note:</b> InFrame count should count “the JumboPkt count with good CRC.”                                                                                                                        |
| ACH–AFh     | 32          | RXSymbolError                                                        | Total number of times a valid length packet was received at a port and at least one invalid data symbol was detected. Counter only increments once per carrier event and does not increment on detection of collision during the carrier event.                                                                                                                               |
| B0h–B3h     | 32          | InRangeErrors                                                        | Number of frames received with good CRC and the following conditions.<br>The value of Length/Type field is between 46 and 1500 inclusive, and does not match the number or (MAC Client Data + PAD) data octets received,<br>OR<br>The value of Length/Type field is less than 46, and the number of data octets received is greater than 46 (which does not require padding). |
| B4h–B7h     | 32          | OutOfRangeErrors                                                     | Number of frames received with good CRC and the value of Length/Type field is greater than 1500 and less than 1536.                                                                                                                                                                                                                                                           |
| C0h–C3h     | 32          | RxDiscard                                                            | Number of good packets received by a port that were discarded by the Forwarding Process.                                                                                                                                                                                                                                                                                      |
| F0h–F7h     | 64          | “SPI Data I/O Register (Global, Address F0h)” on page 294, bytes 0–7 | –                                                                                                                                                                                                                                                                                                                                                                             |
| F8h–FDh     | –           | Reserved                                                             | –                                                                                                                                                                                                                                                                                                                                                                             |
| FEh         | 8           | “SPI Status Register (Global, Address FEh)” on page 295              | –                                                                                                                                                                                                                                                                                                                                                                             |
| FFh         | 8           | “Page Register (Global, Address FFh)” on page 295                    | –                                                                                                                                                                                                                                                                                                                                                                             |

## Page 30h: QoS Registers

**Table 192: Page 30h QoS Registers**

| <b>Address</b> | <b>Bits</b> | <b>Description</b>                                                                         |
|----------------|-------------|--------------------------------------------------------------------------------------------|
| 00h            | 8           | <a href="#">“QoS Global Control Register (Page 30h: Address 00h)” on page 251</a>          |
| 01h–02h        | 16          | Reserved                                                                                   |
| 03h            | –           | Reserved                                                                                   |
| 04h–05h        | 16          | <a href="#">“QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)” on page 251</a>      |
| 06h–07h        | 16          | <a href="#">“QoS DiffServ Enable Register (Page 30h: Address 06h)” on page 252</a>         |
| 08h–0Fh        | –           | Reserved                                                                                   |
| 10h–2Bh        | 32/port     | <a href="#">“Port N (N=0-5, 8) PCP To TC Register (Page 30h: Address 10h)” on page 252</a> |
| 2Ch–2Fh        | –           | Reserved                                                                                   |
| 30h–35h        | 48          | <a href="#">“DiffServ Priority Map 0 Register (Page 30h: Address 30h)” on page 253</a>     |
| 36h–3Bh        | 48          | <a href="#">“DiffServ Priority Map 1 Register (Page 30h: Address 36h)” on page 253</a>     |
| 3Ch–41h        | 48          | <a href="#">“DiffServ Priority Map 2 Register (Page 30h: Address 3Ch)” on page 254</a>     |
| 42h–47h        | 48          | <a href="#">“DiffServ Priority Map 3 Register (Page 30h: Address 42h)” on page 255</a>     |
| 48h–61h        | –           | Reserved                                                                                   |
| 62h–63h        | 16          | <a href="#">“TC To CoS Mapping Register (Page 30h: Address 62h–63h)” on page 255</a>       |
| 64h–67h        | 32          | <a href="#">“CPU To CoS Map Register (Page 30h: Address 64h–67h)” on page 256</a>          |
| 68h–7Fh        | –           | Reserved                                                                                   |
| 80h            | 8           | <a href="#">“TX Queue Control Register (Page 30h: Address 80h)” on page 256</a>            |
| 81h            | 8           | <a href="#">“TX Queue Weight Register (Page 30h: Address 81h)” on page 257, Queue 0</a>    |
| 82h            | 8           | <a href="#">“TX Queue Weight Register (Page 30h: Address 81h)” on page 257, Queue 1</a>    |
| 83h            | 8           | <a href="#">“TX Queue Weight Register (Page 30h: Address 81h)” on page 257, Queue 2</a>    |
| 84h            | 8           | <a href="#">“TX Queue Weight Register (Page 30h: Address 81h)” on page 257, Queue 3</a>    |
| 85h–86h        | 16          | Reserved                                                                                   |
| 87h–9Fh        | –           | Reserved                                                                                   |
| A0h            | –           | Reserved                                                                                   |
| A1h            | –           | Reserved                                                                                   |
| A2h–EFh        | –           | Reserved                                                                                   |
| F0h–F7h        | 8           | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294, bytes 0–7</a>       |
| F8h–FDh        | –           | Reserved                                                                                   |
| FEh            | 8           | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>                    |
| FFh            | 8           | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                          |

## QoS Global Control Register (Page 30h: Address 00h)

**Table 193: QoS Global Control Register (Page 30h: Address 00h)**

| Bit | Name             | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                            | Default |
|-----|------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Aggregation Mode | R/W | When enable this bit, the IMP operated as the uplink port to the upstream network processor and the CoS is decided from the TC based on the normal packet classification flow. Otherwise, the IMP operated as the interface to the management CPU, and the CoS is decided based on the reasons for forwarding the packet to the CPU.                                                                                                   | 0       |
| 6   | PORT_QOS_EN      | R/W | Port-based QoS enable<br>When port-based QoS is enabled, ingress frames are assigned a priority ID value based on the PORT_QOS_PRI bits in the <a href="#">“Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)” on page 267</a> . IEEE 802.1p and DiffServ priorities are disregarded.<br>0 = Disable port-based QoS.<br>1 = Enable port-based QoS.<br>See <a href="#">“Quality of Service” on page 34</a> for more information. | 0       |
| 5:4 | Reserved         | R/W | –                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0       |
| 3:2 | QOS_LAYER_SEL    | R/W | QoS priority selection<br>These bits determine which QoS priority scheme is associated with the frame. See <a href="#">Table 1 on page 37</a> for more information.                                                                                                                                                                                                                                                                    | 0       |
| 1:0 | Reserved         | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               | 0       |

## QoS IEEE 802.1p Enable Register (Page 30h: Address 04h)

**Table 194: QoS.1P Enable Register (Page 30h: Address 04h–05h)**

| Bit  | Name      | R/W | Description                                                                                                                                                                                                                                                                                        | Default |
|------|-----------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved  | RO  | –                                                                                                                                                                                                                                                                                                  | 0       |
| 8:0  | 802_1P_EN | R/W | QoS IEEE 802.1p port mask<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>0 = Disable IEEE 802.1p priority for individual ports.<br>1 = Enable IEEE 802.1p priority for individual ports.<br>See <a href="#">“IEEE 802.1Q VLAN” on page 39</a> for more information. | 0       |

## QoS DiffServ Enable Register (Page 30h: Address 06h)

**Table 195: QoS DiffServ Enable Register (Page 30h: Address 06h–07h)**

| Bit  | Name        | R/W | Description                                                                                                                                                                                                | Default |
|------|-------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved    | RO  | –                                                                                                                                                                                                          | 0       |
| 8:0  | DIFFSERV_EN | R/W | DiffServ port mask<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>0 = Disable DiffServ priority for individual ports.<br>1 = Enable DiffServ priority for individual ports. | 0       |

See “Quality of Service” on page 34 for more information.

## Port N (N=0-5, 8) PCP\_To\_TC Register (Page 30h: Address 10h)

**Table 196: Port N (N=0-5,8) PCP\_To\_TC Register Address Summary**

| Address | Description |
|---------|-------------|
| 10h–13h | Port 0      |
| 14h–17h | Port 1      |
| 18h–1Bh | Port 2      |
| 1Ch–1Fh | Port 3      |
| 20h–23h | Port 4      |
| 24h–27h | Port 5      |
| 28h–2Bh | IMP Port    |

These bits map the IEEE 802.1p priority level to one of the eight priority ID levels in the [“TC To CoS Mapping Register \(Page 30h: Address 62h–63h\)” on page 255](#).

**Table 197: Port N (N=0-5,8) PCP\_To\_TC Register (Page 30h: Address 10h–2Bh)**

| Bit   | Name       | R/W | Description                        | Default |
|-------|------------|-----|------------------------------------|---------|
| 31:24 | Reserved   | RO  | –                                  | 0       |
| 23:21 | 1P_111_MAP | R/W | IEEE 802.1p priority tag field 111 | 111     |
| 20:18 | 1P_110_MAP | R/W | IEEE 802.1p priority tag field 110 | 110     |
| 17:15 | 1P_101_MAP | R/W | IEEE 802.1p priority tag field 101 | 101     |
| 14:12 | 1P_100_MAP | R/W | IEEE 802.1p priority tag field 100 | 100     |
| 11:9  | 1P_011_MAP | R/W | IEEE 802.1p priority tag field 011 | 011     |
| 8:6   | 1P_010_MAP | R/W | IEEE 802.1p priority tag field 010 | 010     |
| 5:3   | 1P_001_MAP | R/W | IEEE 802.1p priority tag field 001 | 001     |
| 2:0   | 1P_000_MAP | R/W | IEEE 802.1p priority tag field 000 | 000     |

See “Quality of Service” on page 34 for more information.

## DiffServ Priority Map 0 Register (Page 30h: Address 30h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the [“TC To CoS Mapping Register \(Page 30h: Address 62h–63h\)” on page 255](#).

**Table 198: DiffServ Priority Map 0 Register (Page 30h: Address 30h–35h)**

| Bit   | Name                | R/W | Description                             | Default |
|-------|---------------------|-----|-----------------------------------------|---------|
| 47:45 | DIFFSERV_001111_MAP | R/W | DiffServ DSCP priority tag field 001111 | 0       |
| 44:42 | DIFFSERV_001110_MAP | R/W | DiffServ DSCP priority tag field 001110 | 0       |
| 41:39 | DIFFSERV_001101_MAP | R/W | DiffServ DSCP priority tag field 001101 | 0       |
| 38:36 | DIFFSERV_001100_MAP | R/W | DiffServ DSCP priority tag field 001100 | 0       |
| 35:33 | DIFFSERV_001011_MAP | R/W | DiffServ DSCP priority tag field 001011 | 0       |
| 32:30 | DIFFSERV_001010_MAP | R/W | DiffServ DSCP priority tag field 001010 | 0       |
| 29:27 | DIFFSERV_001001_MAP | R/W | DiffServ DSCP priority tag field 001001 | 0       |
| 26:24 | DIFFSERV_001000_MAP | R/W | DiffServ DSCP priority tag field 001000 | 0       |
| 23:21 | DIFFSERV_000111_MAP | R/W | DiffServ DSCP priority tag field 000111 | 0       |
| 20:18 | DIFFSERV_000110_MAP | R/W | DiffServ DSCP priority tag field 000110 | 0       |
| 17:15 | DIFFSERV_000101_MAP | R/W | DiffServ DSCP priority tag field 000101 | 0       |
| 14:12 | DIFFSERV_000100_MAP | R/W | DiffServ DSCP priority tag field 000100 | 0       |
| 11:9  | DIFFSERV_000011_MAP | R/W | DiffServ DSCP priority tag field 000011 | 0       |
| 8:6   | DIFFSERV_000010_MAP | R/W | DiffServ DSCP priority tag field 000010 | 0       |
| 5:3   | DIFFSERV_000001_MAP | R/W | DiffServ DSCP priority tag field 000001 | 0       |
| 2:0   | DIFFSERV_000000_MAP | R/W | DiffServ DSCP priority tag field 000000 | 0       |

See “Quality of Service” on page 34 for more information.

## DiffServ Priority Map 1 Register (Page 30h: Address 36h)

These bits map the DiffServ priority level to one of the eight Priority ID levels in the [“TC To CoS Mapping Register \(Page 30h: Address 62h–63h\)” on page 255](#).

**Table 199: DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh)**

| Bit   | Name                | R/W | Description                             | Default |
|-------|---------------------|-----|-----------------------------------------|---------|
| 47:45 | DIFFSERV_011111_MAP | R/W | DiffServ DSCP priority tag field 011111 | 0       |
| 44:42 | DIFFSERV_011110_MAP | R/W | DiffServ DSCP priority tag field 011110 | 0       |
| 41:39 | DIFFSERV_011101_MAP | R/W | DiffServ DSCP priority tag field 011101 | 0       |
| 38:36 | DIFFSERV_011100_MAP | R/W | DiffServ DSCP priority tag field 011100 | 0       |
| 35:33 | DIFFSERV_011011_MAP | R/W | DiffServ DSCP priority tag field 011011 | 0       |

**Table 199: DiffServ Priority Map 1 Register (Page 30h: Address 36h–3Bh) (Cont.)**

| Bit   | Name                | R/W | Description                             | Default |
|-------|---------------------|-----|-----------------------------------------|---------|
| 32:30 | DIFFSERV_011010_MAP | R/W | DiffServ DSCP priority tag field 011010 | 0       |
| 29:27 | DIFFSERV_011001_MAP | R/W | DiffServ DSCP priority tag field 011001 | 0       |
| 26:24 | DIFFSERV_011000_MAP | R/W | DiffServ DSCP priority tag field 011000 | 0       |
| 23:21 | DIFFSERV_010111_MAP | R/W | DiffServ DSCP priority tag field 010111 | 0       |
| 20:18 | DIFFSERV_010110_MAP | R/W | DiffServ DSCP priority tag field 010110 | 0       |
| 17:15 | DIFFSERV_010101_MAP | R/W | DiffServ DSCP priority tag field 010101 | 0       |
| 14:12 | DIFFSERV_010100_MAP | R/W | DiffServ DSCP priority tag field 010100 | 0       |
| 11:9  | DIFFSERV_010011_MAP | R/W | DiffServ DSCP priority tag field 010011 | 0       |
| 8:6   | DIFFSERV_010010_MAP | R/W | DiffServ DSCP priority tag field 010010 | 0       |
| 5:3   | DIFFSERV_010001_MAP | R/W | DiffServ DSCP priority tag field 010001 | 0       |
| 2:0   | DIFFSERV_010000_MAP | R/W | DiffServ DSCP priority tag field 010000 | 0       |

See “Quality of Service” on page 34 for more information.

## DiffServ Priority Map 2 Register (Page 30h: Address 3Ch)

These bits map the DiffServ priority level to one of the eight priority ID levels in the [“TC To CoS Mapping Register \(Page 30h: Address 62h–63h\)” on page 255](#).

**Table 200: DiffServ Priority Map 2 Register (Page 30h: Address 3Ch–41h)**

| Bit   | Name                | R/W | Description                             | Default |
|-------|---------------------|-----|-----------------------------------------|---------|
| 47:45 | DIFFSERV_101111_MAP | R/W | DiffServ DSCP priority tag field 101111 | 0       |
| 44:42 | DIFFSERV_101110_MAP | R/W | DiffServ DSCP priority tag field 101110 | 0       |
| 41:39 | DIFFSERV_101101_MAP | R/W | DiffServ DSCP priority tag field 101101 | 0       |
| 38:36 | DIFFSERV_101100_MAP | R/W | DiffServ DSCP priority tag field 101100 | 0       |
| 35:33 | DIFFSERV_101011_MAP | R/W | DiffServ DSCP priority tag field 101011 | 0       |
| 32:30 | DIFFSERV_101010_MAP | R/W | DiffServ DSCP priority tag field 101010 | 0       |
| 29:27 | DIFFSERV_101001_MAP | R/W | DiffServ DSCP priority tag field 101001 | 0       |
| 26:24 | DIFFSERV_101000_MAP | R/W | DiffServ DSCP priority tag field 101000 | 0       |
| 23:21 | DIFFSERV_100111_MAP | R/W | DiffServ DSCP priority tag field 100111 | 0       |
| 20:18 | DIFFSERV_100110_MAP | R/W | DiffServ DSCP priority tag field 100110 | 0       |
| 17:15 | DIFFSERV_100101_MAP | R/W | DiffServ DSCP priority tag field 100101 | 0       |
| 14:12 | DIFFSERV_100100_MAP | R/W | DiffServ DSCP priority tag field 100100 | 0       |
| 11:9  | DIFFSERV_100011_MAP | R/W | DiffServ DSCP priority tag field 100011 | 0       |
| 8:6   | DIFFSERV_100010_MAP | R/W | DiffServ DSCP priority tag field 100010 | 0       |
| 5:3   | DIFFSERV_100001_MAP | R/W | DiffServ DSCP priority tag field 100001 | 0       |
| 2:0   | DIFFSERV_100000_MAP | R/W | DiffServ DSCP priority tag field 100000 | 0       |

See [“Quality of Service” on page 34](#) for more information.

## DiffServ Priority Map 3 Register (Page 30h: Address 42h)

These bits map the DiffServ priority level to one of the eight priority ID levels in the [“TC To CoS Mapping Register \(Page 30h: Address 62h–63h\)” on page 255](#).

**Table 201: DiffServ Priority Map 3 Register (Page 30h: Address 42h–47h)**

| Bit   | Name                | R/W | Description                             | Default |
|-------|---------------------|-----|-----------------------------------------|---------|
| 47:45 | DIFFSERV_111111_MAP | R/W | DiffServ DSCP priority tag field 111111 | 0       |
| 44:42 | DIFFSERV_111110_MAP | R/W | DiffServ DSCP priority tag field 111110 | 0       |
| 41:39 | DIFFSERV_111101_MAP | R/W | DiffServ DSCP priority tag field 111101 | 0       |
| 38:36 | DIFFSERV_111100_MAP | R/W | DiffServ DSCP priority tag field 111100 | 0       |
| 35:33 | DIFFSERV_111011_MAP | R/W | DiffServ DSCP priority tag field 111011 | 0       |
| 32:30 | DIFFSERV_111010_MAP | R/W | DiffServ DSCP priority tag field 111010 | 0       |
| 29:27 | DIFFSERV_111001_MAP | R/W | DiffServ DSCP priority tag field 111001 | 0       |
| 26:24 | DIFFSERV_111000_MAP | R/W | DiffServ DSCP priority tag field 111000 | 0       |
| 23:21 | DIFFSERV_110111_MAP | R/W | DiffServ DSCP priority tag field 110111 | 0       |
| 20:18 | DIFFSERV_110110_MAP | R/W | DiffServ DSCP priority tag field 110110 | 0       |
| 17:15 | DIFFSERV_100101_MAP | R/W | DiffServ DSCP priority tag field 100101 | 0       |
| 14:12 | DIFFSERV_110100_MAP | R/W | DiffServ DSCP priority tag field 110100 | 0       |
| 11:9  | DIFFSERV_110011_MAP | R/W | DiffServ DSCP priority tag field 110011 | 0       |
| 8:6   | DIFFSERV_110010_MAP | R/W | DiffServ DSCP priority tag field 110010 | 0       |
| 5:3   | DIFFSERV_110001_MAP | R/W | DiffServ DSCP priority tag field 110001 | 0       |
| 2:0   | DIFFSERV_110000_MAP | R/W | DiffServ DSCP priority tag field 110000 | 0       |

See [“Quality of Service” on page 34](#) for more information.

## TC\_To\_CoS Mapping Register (Page 30h: Address 62h–63h)

All the bits in [Table 202](#) map the priority ID to one of the TX queues.

**Table 202: TC\_To\_CoS Mapping Register (Page 30h: Address 62h–63h)**

| Bit   | Name        | R/W | Description                           | Default |
|-------|-------------|-----|---------------------------------------|---------|
| 15:14 | PRI_111_QID | R/W | Priority ID 111 mapped to TX Queue ID | 00      |
| 13:12 | PRI_110_QID | R/W | Priority ID 110 mapped to TX Queue ID | 00      |
| 11:10 | PRI_101_QID | R/W | Priority ID 101 mapped to TX Queue ID | 00      |
| 9:8   | PRI_100_QID | R/W | Priority ID 100 mapped to TX Queue ID | 00      |
| 7:6   | PRI_011_QID | R/W | Priority ID 011 mapped to TX Queue ID | 00      |
| 5:4   | PRI_010_QID | R/W | Priority ID 010 mapped to TX Queue ID | 00      |

**Table 202: TC\_To\_CoS Mapping Register (Page 30h: Address 62h–63h) (Cont.)**

| Bit | Name        | R/W | Description                           | Default |
|-----|-------------|-----|---------------------------------------|---------|
| 3:2 | PRI_001_QID | R/W | Priority ID 001 mapped to TX Queue ID | 00      |
| 1:0 | PRI_000_QID | R/W | Priority ID 000 mapped to TX Queue ID | 00      |

See “Quality of Service” on page 34 for more information.

## CPU\_To\_CoS Map Register (Page 30h: Address 64h–67h)

**Table 203: CPU\_To\_CoS Map Register (Page 30h: Address 64h–67h)**

| Bit   | Name                                         | R/W | Description                                                                                                                                                             | Default |
|-------|----------------------------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:18 | Reserved                                     | RO  | –                                                                                                                                                                       | 0       |
| 17:15 | Exception/Flooding Processing to CPU CoS Map | R/W | The packet forwarded to the CPU for Exception Processing/Flooding reason.<br>The CoS selection is based on the highest CoS values among all the reasons for the packet. | 0       |
| 14:12 | Protocol Snooping to CPU CoS Map             | R/W | The packet forwarded to the CPU for Protocol Snooping reason.<br>The CoS selection is based on the highest CoS values among all the reasons for the packet.             | 0       |
| 11:9  | Protocol Termination to CPU CoS Map          | R/W | The packet forwarded to the CPU for Protocol Termination reason.<br>The CoS selection is based on the highest CoS values among all the reasons for the packet.          | 0       |
| 8:6   | Switching to CPU CoS Map                     | R/W | The packet forwarded to the CPU for Switching reason.<br>The CoS selection is based on the highest CoS values among all the reasons for the packet.                     | 0       |
| 5:3   | SA Learning to CPU CoS Map                   | R/W | The packet forwarded to the CPU for SA Learning reason.<br>The CoS selection is based on the highest CoS among all the reasons for the packet.                          | 0       |
| 2:0   | Mirror to CPU CoS Map                        | R/W | The packet forwarded to the CPU for mirroring reason.<br>The CoS selection is based on the highest CoS values among all the reasons for the packet.                     | 0       |

## TX Queue Control Register (Page 30h: Address 80h)

**Table 204: TX Queue Control Register (Page 30h: Address 80h)**

| Bit | Name     | R/W | Description | Default |
|-----|----------|-----|-------------|---------|
| 7:4 | Reserved | R/W | –           | 0       |

**Table 204: TX Queue Control Register (Page 30h: Address 80h) (Cont.)**

| Bit | Name             | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Default |
|-----|------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 3:2 | Reserved         | R/W | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | –       |
| 1:0 | QOS_PRIORITY_CTL | R/W | <p>Best Effort Queues Priority Control</p> <p>This field controls the best effort queues' scheduling priority.</p> <p>00 = All queues are weighted round robin</p> <p>01 = CoS 3 is strict priority, CoS2-CoS0 are weighted round robin.</p> <p>10 = CoS3 and CoS2 is strict priority, CoS1-CoS0 are weighted round robin.</p> <p>11 = CoS3, CoS2, CoS1 and CoS0 are in strict priority.</p> <p>Strict priority: When it is in strict priority, the priority is CoS3 &gt; CoS2 &gt; CoS1 &gt; CoS0.</p> <p>The G_TXPORT will serve the higher queue first if it is not empty.</p> <p>In this mode, the service weight are don't care.</p> <p>Weighted round robin: When it is in weighted round robin mode, the queues are scheduled in a round robin way according to the service weight of each queue.</p> | 00      |

See [“Quality of Service” on page 34](#) for more information.

## TX Queue Weight Register (Page 30h: Address 81h)

**Table 205: TX Queue Weight Register Queue[0:3] (Page 30h: Address 81h–84h)**

| Bit | Name         | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Default                                                                       |
|-----|--------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|
| 7:0 | QSERV_WEIGHT | R/W | <p>Queue weight register</p> <p>The binary value of these bits sets the service weight of the given queue. The value of 1 allows the queue to send one packet for every round; the value of 4 allows the queue to send four packets for every round. It is suggested that the weight of each queue be <math>Q3 &gt; Q2 &gt; Q1 &gt; Q0 &gt; 0</math>.</p> <p><b>Note:</b> The maximum allowable transmit queue weight is 31h. Programming a higher weight than 31h can yield unexpected results. This field must not be programmed as zero.</p> | <p>Queue:</p> <p>0 = 0001</p> <p>1 = 0010</p> <p>2 = 0100</p> <p>3 = 1000</p> |

See [“Quality of Service” on page 34](#) for more information.

## Page 31h: Port-Based VLAN Registers

**Table 206: Page 31h VLAN Registers**

| Address | Bits    | Description                                                                            |
|---------|---------|----------------------------------------------------------------------------------------|
| 00h–11h | 16/port | <a href="#">“Port-Based VLAN Control Register (Page 31h: Address 00h)” on page 258</a> |
| 1Fh–EFh | –       | Reserved                                                                               |
| F0h–F7h | 8       | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294</a> , bytes 0–7  |
| F8h–FDh | –       | Reserved                                                                               |
| FEh     | 8       | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>                |
| FFh     | 8       | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                      |

## Port-Based VLAN Control Register (Page 31h: Address 00h)

**Table 207: Port-Based VLAN Control Register Address Summary**

| Address | Description              |
|---------|--------------------------|
| 00h–01h | <a href="#">Port 0</a>   |
| 02h–03h | <a href="#">Port 1</a>   |
| 04h–05h | <a href="#">Port 2</a>   |
| 06h–07h | <a href="#">Port 3</a>   |
| 08h–09h | <a href="#">Port 4</a>   |
| 0Ah–0Bh | Port 5                   |
| 0Ch–0Dh | Reserved                 |
| 0Eh–0Fh | Reserved                 |
| 10h–11h | <a href="#">IMP port</a> |

**Table 208: Port VLAN Control Register (Page 31h: Address 00h–11h)**

| Bit  | Name         | R/W | Description                                                                                                                                                                                  | Default |
|------|--------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved     | RO  | –                                                                                                                                                                                            | –       |
| 8:0  | FORWARD_MASK | R/W | VLAN forwarding mask<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>0 = Disable VLAN forwarding to egress port.<br>1 = Enable VLAN forwarding to egress port. | 1FFh    |

For more information, see [“Port-Based VLAN” on page 38](#).

## Page 32h: Trunking Registers

**Table 209: Page 32h Trunking Registers**

| Address | Bits | Description                                                                           |
|---------|------|---------------------------------------------------------------------------------------|
| 00h     | 8    | <a href="#">“MAC Trunking Control Register (Page 32h: Address 00h)” on page 259</a>   |
| 01h–0Fh | –    | Reserved                                                                              |
| 10h–11h | 16   | Trunk group 0 register                                                                |
| 12h–13h | 16   | Trunk group 1 register                                                                |
| 14h–15h | –    | Reserved                                                                              |
| 16h–17h | –    | Reserved                                                                              |
| 18h–EFh | –    | Reserved                                                                              |
| F0h–F7h | 8    | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294</a> , bytes 0–7 |
| F8h–FDh | –    | Reserved                                                                              |
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>               |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                     |

## MAC Trunking Control Register (Page 32h: Address 00h)

**Table 210: MAC Trunk Control Register (Page 32h: Address 00h)**

| Bit | Name             | R/W | Description                                                                                                                                                                   | Default |
|-----|------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:4 | Reserved         | RO  | –                                                                                                                                                                             | –       |
| 3   | MAC_BASE_TRNK_EN | –   | Enable MAC base trunking                                                                                                                                                      | –       |
| 2   | Reserved         | –   | –                                                                                                                                                                             | –       |
| 1:0 | TRK_HASH_INDX    | R/W | Trunk hash index selector<br>00 = Use hash [DA,SA] to generate index.<br>01 = Use hash [DA] to generate index.<br>10 = Use hash [SA] to generate index.<br>11 = Illegal state | 0       |

See [“Port Trunking/Aggregation” on page 43](#) for more information.

## Trunking Group 0 Register (Page 32h: Address 10h)

**Table 211: Trunk Group 0 Register (Page 32h: Address 10h–11h)**

| Bit  | Name     | R/W | Description | Default |
|------|----------|-----|-------------|---------|
| 15:9 | Reserved | R/W | –           | 0       |

**Table 211: Trunk Group 0 Register (Page 32h: Address 10h–11h)**

| Bit | Name               | R/W | Description                                                                                                                                          | Default |
|-----|--------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 8:0 | Trunk Group Enable | R/W | Trunk group enable<br>1 = Enable trunk group.<br>0 = Disable trunk group.<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively. | 0       |

See [“Port Trunking/Aggregation” on page 43](#) for more information.

## Trunking Group 1 Register (Page 32h: Address 12h)

**Table 212: Trunk Group 1 Register (Page 32h: Address 12h–13h)**

| Bit  | Name               | R/W | Description                                                                                                                                          | Default |
|------|--------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved           | R/W | —                                                                                                                                                    | 0       |
| 8:0  | Trunk Group Enable | R/W | Trunk group enable<br>1 = Enable trunk group.<br>0 = Disable trunk group.<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively. | 0       |

## Page 34h: IEEE 802.1Q VLAN Registers

**Table 213: Page 34h IEEE 802.1Q VLAN Registers**

| Address  | Bits    | Description                                                                                      |
|----------|---------|--------------------------------------------------------------------------------------------------|
| 00h      | 8       | <a href="#">“Global IEEE 802.1Q Register (Pages 34h: Address 00h)” on page 261</a>               |
| 01h      | 8       | <a href="#">“Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)” on page 262</a> |
| 02h      | 8       | <a href="#">“Global VLAN Control 2 Register (Page 34h: Address 02h)” on page 263</a>             |
| 03h–04h  | 16      | <a href="#">“Global VLAN Control 3 Register (Page 34h: Address 03h)” on page 263</a>             |
| 05h      | 8       | <a href="#">“Global VLAN Control 4 Register (Page 34h: Address 05h)” on page 264</a>             |
| 06h      | 8       | <a href="#">“Global VLAN Control 5 Register (Page 34h: Address 06h)” on page 265</a>             |
| 07h      | 8       | Reserved                                                                                         |
| 0Ah–0Bh  | 16      | <a href="#">“” on page 266</a>                                                                   |
| Reserved | 32      | Reserved                                                                                         |
| 10h–21h  | 16/port | <a href="#">“Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)” on page 267</a>           |
| 20h–2Fh  | —       | Reserved                                                                                         |
| 30h–31h  | 16      | <a href="#">“Double Tagging TPID Register (Page 34h: Address 30h–31h)” on page 268</a>           |

**Table 213: Page 34h IEEE 802.1Q VLAN Registers (Cont.)**

| Address | Bits | Description                                                                                   |
|---------|------|-----------------------------------------------------------------------------------------------|
| 32h–33h | 16   | <a href="#">“ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)” on page 268</a> |
| 34h–3Fh | –    | Reserved                                                                                      |
| 40h–43h | 32   | Reserved                                                                                      |
| 44h–48h | 32   | Reserved                                                                                      |
| 49h–EFh | –    | –                                                                                             |
| F0h–F7h | 8    | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294, bytes 0–7</a>          |
| F8h–FDh | –    | Reserved                                                                                      |
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>                       |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                             |

## Global IEEE 802.1Q Register (Pages 34h: Address 00h)

**Table 214: Global IEEE 802.1Q Register (Pages 34h: Address 00h)**

| Bit | Name               | R/W | Description                                                                                                                                                                                                                                                                                                                                                        | Default |
|-----|--------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Enable IEEE 802.1Q | R/W | Enable IEEE 802.1Q VLAN<br>0 = Disable IEEE 802.1Q VLAN.<br>1 = Enable IEEE 802.1Q VLAN.<br>See <a href="#">“Programming the VLAN Table” on page 40</a> for more information.<br><b>Note:</b> This bit must be set if Double-Tagging mode enable (En_DT_Mode = 01 or 10) in <a href="#">“Global VLAN Control 4 Register (Page 34h: Address 05h)” on page 264</a> . | 0       |
| 6:5 | VLAN Learning Mode | R/W | VLAN learning mode<br>00 = SVL (Shared VLAN learning mode) (MAC hash ARL table)<br>11 = IVL (Individual VLAN learning mode) (MAC and VID hash ARL table)<br>10 = Illegal setting<br>01 = Illegal setting<br><b>Note:</b> Applied to 802.1Q enable, DT_Mode.                                                                                                        | 11      |
| 4   | Reserved           | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                           | 0       |
| 3   | Change_1Q_VID      | R/W | Change 1Q VID to PVID<br>1 =<br><ul style="list-style-type: none"> <li>For a single-tag frame with VID not = 0, change the VID to PVID.</li> <li>For a double-tag frame with outer VID not = 0, change outer VID to PVID.</li> </ul> 0 = No change for 1Q/ISP tag if VID is not 0.                                                                                 | 0       |

**Table 214: Global IEEE 802.1Q Register (Pages 34h: Address 00h) (Cont.)**

| Bit | Name     | R/W | Description | Default |
|-----|----------|-----|-------------|---------|
| 2   | Reserved | R/W | Reserved    | 0       |
| 1   | Reserved | R/W | Reserved    | 1       |
| 0   | Reserved | R/W | Reserved    | 1       |

See “IEEE 802.1Q VLAN” on page 39 for more information.

## Global IEEE 802.1Q VLAN Control 1 Register (Page 34h: Address 01h)

**Table 215: Global VLAN Control 1 Register (Page 34h: Address 01h)**

| Bit | Name                             | R/W | Description                                                                                                                                                                                                                                                                                                                     | Default |
|-----|----------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Reserved                         | R/W | Reserved                                                                                                                                                                                                                                                                                                                        | 0       |
| 6   | Multicast Untag Check            | R/W | Multicast VLAN untagged map check bypass<br>1 = Multicast frames are not checked against the VLAN untagged map.<br>0 = Multicast frames are checked against the VLAN untagged map. Does not apply to the frame management port.                                                                                                 | 0       |
| 5   | Multicast Forward Check          | R/W | Multicast VLAN forward map check bypass<br>1 = Multicast frames are not checked against the VLAN forward map.<br>0 = Multicast frames are checked against the VLAN forward map.<br><b>Note:</b> Applied to 802.1Q enable, DT_Mode.                                                                                              | 0       |
| 4   | Reserved                         | R/W | It is illegal to set 1.                                                                                                                                                                                                                                                                                                         | 0       |
| 3   | Reserved Multicast Untag Check   | R/W | Reserved multicast (except GMRP and GVRP) VLAN untagged map check bit<br>1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN untagged map.<br>0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN untagged map. Does not apply to the frame management port.    | 0       |
| 2   | Reserved Multicast Forward Check | R/W | Reserved multicast (except GMRP and GVRP) VLAN forward map check bit<br>1 = Reserved multicast (except GMRP and GVRP) frames are checked against the VLAN forward map.<br>0 = Reserved multicast (except GMRP and GVRP) frames are not checked against the VLAN forward map.<br><b>Note:</b> Applied to 802.1Q enable, DT_Mode. | 0       |
| 1   | Reserved                         | R/W | It is illegal to set 0.                                                                                                                                                                                                                                                                                                         | 1       |
| 0   | Reserved                         | R/W | Reserved                                                                                                                                                                                                                                                                                                                        | 0       |

For more information, see [“IEEE 802.1Q VLAN” on page 39](#).

## Global VLAN Control 2 Register (Page 34h: Address 02h)

**Table 216: Global VLAN Control 2 Register (Page 34h: Address 02h)**

| Bit | Name                     | R/W | Description                                                                                                                                                                                                                                                                           | Default |
|-----|--------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Reserved                 | R/W | Reserved                                                                                                                                                                                                                                                                              | 0       |
| 6   | GMRP/GVRP Untag Check    | R/W | GMRP or GVRP VLAN untag map check bit<br>1 = GMRP or GVRP frames are checked against the VLAN untagged map.<br>0 = GMRP or GVRP frames are not checked against the VLAN untagged map.<br><b>Note:</b> Does not apply to the frame management port.                                    | 0       |
| 5   | GMRP/GVRP Forward Check  | R/W | GMRP or GVRP VLAN forward map check bit<br>1 = GMRP or GVRP frames are checked against the VLAN forward map.<br>0 = GMRP or GVRP frames are not checked against the VLAN forward map.<br><b>Note:</b> Does not apply to the frame management port. Applied to 802.1Q enable, DT_Mode. | 0       |
| 4   | Reserved                 | R/W | Reserved                                                                                                                                                                                                                                                                              | 1       |
| 3   | Reserved                 | R/W | Reserved                                                                                                                                                                                                                                                                              | 0       |
| 2   | IMP Frame Forward Bypass | R/W | IMP Frame VLAN forward map check bit<br>1 = IMP frames are not checked against the VLAN forward map.<br>0 = IMP frames are checked against the VLAN forward map.<br><b>Note:</b> Applied to 802.1Q enable, DT_Mode.                                                                   | 0       |
| 1:0 | Reserved                 | R/W | Reserved                                                                                                                                                                                                                                                                              | 00      |

For more information, see [“IEEE 802.1Q VLAN” on page 39](#).

## Global VLAN Control 3 Register (Page 34h: Address 03h)

**Table 217: Global VLAN Control 3 Register (Page 34h: Address 03h–04h)**

| Bit  | Name     | R/W | Description | Default |
|------|----------|-----|-------------|---------|
| 15:9 | Reserved | RO  | —           | —       |

**Table 217: Global VLAN Control 3 Register (Page 34h: Address 03h–04h)**

| Bit | Name              | R/W | Description                                                                                                                                                                                                                                                                                                                                                                          | Default |
|-----|-------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:0 | Drop Non1Q Frames | R/W | Drop non1Q frames<br>When enabled, any frame without an IEEE 802.1Q tag is dropped by this port.<br>This field does not apply to IMP port (includes Port 5 if Dual-IMP ports enabled, En_IMP_PORT = 11 in <a href="#">“Global Management Configuration Register (Page 02h: Address 00h)”</a> on page 169.<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively. | 0       |

## Global VLAN Control 4 Register (Page 34h: Address 05h)

**Table 218: Global VLAN Control 4 Register (Page 34h: Address 05h)**

| Bit | Name                       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Default |
|-----|----------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:6 | Source Membership Check    | R/W | Source membership check bit<br>Frames with a VID matching a corresponding entry in the VLAN table can be checked for source membership. The source is a member only when the source address of the frame is included as a member in the corresponding VLAN entry.<br>00 = Forward frame, but do not learn the SA into the ARL table.<br>01 = Drop frame.<br>10 = Forward frame, and learn the SA into the ARL table.<br>11 = Forward frame to IMP, but not learn.<br><b>Note:</b> Does not apply to IMP port (includes Port 5 if Dual-IMP ports enabled, En_IMP_PORT = 11 in <a href="#">“Global Management Configuration Register (Page 02h: Address 00h)”</a> on page 169). | 11      |
| 5   | Forward GVRP to Management | R/W | Forward all GVRP frames to the frame management port bit.<br>1 = GVRP frames are forwarded to the management port.<br>0 = GVRP frames are not forwarded to the management port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0       |
| 4   | Forward GMRP to Management | R/W | Forward All GMRP Frames to the frame management port bit.<br>1 = GMRP frames are forwarded to the management port.<br>0 = GMRP frames are not forwarded to the management port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0       |

**Table 218: Global VLAN Control 4 Register (Page 34h: Address 05h) (Cont.)**

| <b>Bit</b> | <b>Name</b>     | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                              | <b>Default</b> |
|------------|-----------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 3:2        | En_DT_Mode      | R/W        | 00 = Disable Double-Tagging mode<br>01 = Enable DT_Mode (Double-Tagging mode)<br>10 = Reserved<br>11 = Reserved                                                                                                                                                                                 | 2'b00          |
| 1          | RSV_MCAST_FLOOD | R/W        | This is used when the BCM53115S is configured to operate in double-tag feature (DT_Mode) and management mode.<br>1 = Flood (including all data port and CPU), reserved mcast is based on the VLAN rule.<br>0 = Trap reserved mcast to CPU.<br>Reserved mcast include: 01-80-C2-00-00-(00,02–2F) |                |
| 0          | Reserved        | R/W        | –                                                                                                                                                                                                                                                                                               | 0              |

For more information, see [“IEEE 802.1Q VLAN” on page 39](#).

## Global VLAN Control 5 Register (Page 34h: Address 06h)

**Table 219: Global VLAN Control 5 Register (Page 34h: Address 06h)**

| <b>Bit</b> | <b>Name</b>         | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                         | <b>Default</b> |
|------------|---------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 7          | Reserved            | R/W        | Reserved                                                                                                                                                                                                                                   | 0              |
| 6          | Tag Status Preserve | R/W        | IEEE 802.1Q tag/untag status preserved at egress.<br>1 = Regardless of untag map in VLAN table, non-1Q frames (including 802.1p frames) will not be changed at TX (egress).<br>This field has no effect in Double-Tagging mode (DT_Mode).  | 0              |
| 5          | Reserved            | R/W        | Reserved                                                                                                                                                                                                                                   | 0              |
| 4          | Trunk Check Bypass  | R/W        | Trunk check bypass<br>1 = Egress directed frames issued from the IMP port bypass trunk checking.<br>0 = Egress directed frames issued from the IMP port are subject to trunk checking and redirection.                                     | 1              |
| 3          | Drop Invalid VID    | R/W        | Drop frames with invalid VID.<br>Frames with an invalid VID do not have a corresponding entry in the VLAN table.<br>1 = Ingress frames with invalid VID are dropped.<br>0 = Ingress frames with invalid VID are forwarded to the IMP port. | 0              |
| 2          | VID_FFF_Fwding      | R/W        | Enable VID FFF forward<br>1 = Forward frame<br>0 = Comply with standard, drop frame                                                                                                                                                        | 0              |

**Table 219: Global VLAN Control 5 Register (Page 34h: Address 06h) (Cont.)**

| Bit | Name                        | R/W | Description                                                                             | Default |
|-----|-----------------------------|-----|-----------------------------------------------------------------------------------------|---------|
| 1   | Reserved                    | R/W | Reserved                                                                                | 0       |
| 0   | Management CRC Check Bypass | R/W | Bypass CRC check at the frame management port.<br>1 = Ignore CRC check<br>0 = Check CRC | 0       |

For more information, see [“IEEE 802.1Q VLAN” on page 39](#).

## VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)

**Table 220: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh)**

| Bit   | Name               | R/W | Description                                                                                                                 | Default |
|-------|--------------------|-----|-----------------------------------------------------------------------------------------------------------------------------|---------|
| 15:12 | Reserved           | RO  | –                                                                                                                           | 0       |
| 11    | EN_MPORT5_untagmap | R/W | When set to 1, MPORT_ADD5 is checked by VLAN untag map.<br><b>Note:</b> Does not apply to the frame management port.        | 0       |
| 10    | EN_MPORT5_fwdmap   | R/W | When set to 1, MPORT_ADD5 is checked by VLAN forward map.<br><b>Note:</b> Does not apply to the frame management port.      | 0       |
| 9     | EN_MPORT4_untagmap | R/W | When set to 1, MPORT_ADD4 will be checked by VLAN untag map.<br><b>Note:</b> Does not apply to the frame management port.   | 0       |
| 8     | EN_MPORT4_fwdmap   | R/W | When set to 1, MPORT_ADD4 will be checked by VLAN forward map.<br><b>Note:</b> Does not apply to the frame management port. | 0       |
| 7     | EN_MPORT3_untagmap | R/W | When set to 1, MPORT_ADD3 will be checked by VLAN untag map.<br><b>Note:</b> Does not apply to the frame management port.   | 0       |
| 6     | EN_MPORT3_fwdmap   | R/W | When set to 1, MPORT_ADD3 will be checked by VLAN forward map.<br><b>Note:</b> Does not apply to the frame management port. | 0       |
| 5     | EN_MPORT2_untagmap | R/W | When set to 1, MPORT_ADD2 will be checked by VLAN untag map.<br><b>Note:</b> Does not apply to the frame management port.   | 0       |

**Table 220: VLAN Multiport Address Control Register (Page 34h: Address 0Ah–0Bh) (Cont.)**

| <b>Bit</b> | <b>Name</b>        | <b>R/W</b> | <b>Description</b>                                                                                                          | <b>Default</b> |
|------------|--------------------|------------|-----------------------------------------------------------------------------------------------------------------------------|----------------|
| 4          | EN_MPORT2_fwdmap   | R/W        | When set to 1, MPORT_ADD2 will be checked by VLAN forward map.<br><b>Note:</b> Does not apply to the frame management port. | 0              |
| 3          | EN_MPORT1_untagmap | R/W        | When set to 1, MPORT_ADD1 will be checked by VLAN untag map.<br><b>Note:</b> Does not apply to the frame management port.   | 0              |
| 2          | EN_MPORT1_fwdmap   | R/W        | When set to 1, MPORT_ADD1 will be checked by VLAN forward map.<br><b>Note:</b> Does not apply to the frame management port. | 0              |
| 1          | EN_MPORT0_untagmap | R/W        | When set to 1, MPORT_ADD0 will be checked by VLAN untag map.<br><b>Note:</b> Does not apply to the frame management port.   | 0              |
| 0          | EN_MPORT0_fwdmap   | R/W        | When set to 1, MPORT_ADD0 will be checked by VLAN forward map.<br><b>Note:</b> Does not apply to the frame management port. | 0              |

## Default IEEE 802.1Q Tag Register (Page 34h: Address 10h)

**Table 221: Default IEEE 802.1Q Tag Register Address Summary**

| <b>Address</b> | <b>Description</b> |
|----------------|--------------------|
| 10h–11h        | Port 0             |
| 12h–13h        | Port 1             |
| 14h–15h        | Port 2             |
| 16h–17h        | Port 3             |
| 18h–19h        | Port 4             |
| 1Ah–1Bh        | Port 5             |
| 1Ch–1Dh        | Reserved           |
| 1Eh–1Fh        | Reserved           |
| 20h–21h        | IMP port           |

**Table 222: Default IEEE 802.1Q Tag Register (Page 34h: Address 10h–21h)**

| Bit   | Name                         | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Default |
|-------|------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:13 | DEFAULT_PRI/<br>PORT_QOS_PRI | R/W | Default IEEE 802.1Q priority<br>If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q frame, these bits are the default priority value for the new tag. See <a href="#">“IEEE 802.1Q VLAN” on page 39</a> for more information.<br>Port-based QoS priority map bits<br>When port-based QoS is enabled in the <a href="#">Table : “QoS Global Control Register (Page 30h: Address 00h),” on page 251</a> , these bits represent the TC for the ingress port. The TC determines the TX queue for each frame based on the <a href="#">“TC_To_CoS Mapping Register (Page 30h: Address 62h–63h)” on page 255</a> . | 000     |
| 12    | CFI                          | R/W | Conical form indicator                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0       |
| 11:0  | DEFAULT_VID                  | R/W | Default IEEE 802.1Q VLAN ID<br>If an IEEE 802.1Q tag is added to an incoming non-IEEE 802.1Q frame, then these bits are the default VID for the new tag. See <a href="#">“IEEE 802.1Q VLAN” on page 39</a> for more information.                                                                                                                                                                                                                                                                                                                                                                                      | 001     |

## Double Tagging TPID Register (Page 34h: Address 30h–31h)

**Table 223: Double Tagging TPID Register (Page 34h: Address 30h–31h)**

| Bit  | Name     | R/W | Description                                    | Default |
|------|----------|-----|------------------------------------------------|---------|
| 15:0 | ISP_TPID | R/W | The TPID used to identify double-tagged frame. | 9100    |

## ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)

**Table 224: ISP Port Selection Portmap Register (Page 34h: Address 32h–33h)**

| Bit  | Name        | R/W | Description                                                                                                                                                                                                                    | Default |
|------|-------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:8 | RESERVED    | –   | –                                                                                                                                                                                                                              | 0       |
| 7:0  | ISP_Portmap | R/W | Bitmap that defines which port is designated as the ISP port.<br>Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>0 = Indicates that it is not an ISP port.<br>1 = Indicates that it is an ISP port. | –       |

## Page 36h: DOS Prevent Register

**Table 225: DOS Prevent Register**

| Address | Bits | Description                                                            |
|---------|------|------------------------------------------------------------------------|
| 00h–03h | 32   | “DOS Control Register (Page 36h: Address 00h–03h)” on page 269         |
| 04h     | 8    | “Minimum TCP Header Size Register (Page 36h: Address 04h)” on page 271 |
| 08h–0Bh | 32   | “Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)” on page 271 |
| 0Ch–0Fh | 32   | “Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)” on page 272 |
| 10h     | 8    | “DOS Disable Learn Register (Page 36h: Address 10h)” on page 272       |
| F0h–F7h | 8    | “SPI Data I/O Register (Global, Address F0h)” on page 294              |
| F8h–FDh | –    | Reserved                                                               |
| FEh     | 8    | “SPI Status Register (Global, Address FEh)” on page 295                |
| FFh     | 8    | “Page Register (Global, Address FFh)” on page 295                      |

## DOS Control Register (Page 36h: Address 00h–03h)

**Table 226: DOS Control Register (Page 36h: Address 00h–03h)**

| Bit   | Name                    | R/W | Description                                                                                                                                                                                                                | Default |
|-------|-------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:14 | Reserved                | RO  | –                                                                                                                                                                                                                          | 0       |
| 13    | ICMPv6_LongPing_DROP_EN | R/W | The ICMPv6 ping (echo request) protocol data unit carried in an unfragmented IPv6 datagram with its payload length indicating a value greater than the MAX_ICMPv6_Size.<br>1 = Drop<br>0 = Do not drop                     | 0       |
| 12    | ICMPv4_LongPing_DROP_EN | R/W | The ICMPv4 ping (echo request) protocol data unit carried in an unfragmented IPv4 datagram with its Total Length indicating a value greater than the MAX_ICMPv4_Size + size of IPv4 header.<br>1 = Drop<br>0 = Do not drop | 0       |

**Table 226: DOS Control Register (Page 36h: Address 00h–03h) (Cont.)**

| <b>Bit</b> | <b>Name</b>             | <b>R/W</b> | <b>Description</b>                                                                                                                                                                     | <b>Default</b> |
|------------|-------------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 11         | ICMPv6_Fragment_DROP_EN | R/W        | The ICMPv6 protocol data unit carried in a fragmented IPv6 datagram.<br>1 = Drop<br>0 = Do not drop                                                                                    | 0              |
| 10         | ICMPv4_Fragment_DROP_EN | R/W        | The ICMPv4 protocol data unit carried in a fragmented IPv4 datagram.<br>1 = Drop<br>0 = Do not drop                                                                                    | 0              |
| 9          | TCP_FragError_DROP_EN   | R/W        | The Fragment_Offset = 1 in any fragment of a fragmented IP datagram carrying part of TCP data.<br>1 = Drop<br>0 = Do not drop                                                          | 00             |
| 8          | TCP_ShortHDR_DROP_EN    | R/W        | The length of a TCP header carried in an unfragmented IP datagram or the first fragment of a fragmented IP datagram is less than MIN_TCP_Header_Size.<br>1 = Drop<br>0 = Do not drop   | 00             |
| 7          | TCP_SYNErrror_DROP_EN   | R/W        | SYN = 1, ACK = 0, and SRC_Port < 1024 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.<br>1 = Drop<br>0 = Do not drop      | 0              |
| 6          | TCP_SYNFINScan_DROP_EN  | R/W        | SYN = 1 and FIN = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.<br>1 = Drop<br>0 = Do not drop                        | 0              |
| 5          | TCP_XMASScan_DROP_EN    | R/W        | Seq_Num = 0, FIN = 1, URG = 1, and PSH = 1 in a TCP header carried in an unfragmented IP datagram or in the first fragment of a fragmented IP datagram.<br>1 = Drop<br>0 = Do not drop | 0              |

**Table 226: DOS Control Register (Page 36h: Address 00h–03h) (Cont.)**

| Bit | Name                 | R/W | Description                                                                                                                                                                                 | Default |
|-----|----------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 4   | TCP_NULLScan_DROP_EN | R/W | Seq_Num = 0 and all TCP_FLAGS = 0 0<br>in a TCP header carried in an<br>unfragmented IP datagram or in the<br>first fragment of a fragmented IP<br>datagram.<br>1 = Drop<br>0 = Do not drop | 0       |
| 3   | UDP_BLAT_DROP_EN     | R/W | DPort = SPort in a UDP header<br>carried in an unfragmented IP<br>datagram or in the first fragment of<br>a fragmented IP datagram.<br>1 = Drop<br>0 = Do not drop                          | 0       |
| 2   | TCP_BLAT_DROP_EN     | R/W | DPort = SPort in a TCP header<br>carried in an unfragmented IP<br>datagram or in the first fragment of<br>a fragmented IP datagram.<br>1 = Drop<br>0 = Do not drop                          | 0       |
| 1   | IP_LAN_DRIP_EN       | R/W | IPDA = IPSA in an IPv4/v6 datagram. 0<br>1 = Drop<br>0 = Do not drop                                                                                                                        | 0       |
| 0   | RESERVED             | R/W | Reserved                                                                                                                                                                                    | 1       |

## Minimum TCP Header Size Register (Page 36h: Address 04h)

**Table 227: Minimum TCP Header Size Register (Page 36h: Address 04h)**

| Bit | Name           | R/W | Description                                   | Default |
|-----|----------------|-----|-----------------------------------------------|---------|
| 7:0 | MIN_TCP_HDR_SZ | R/W | Minimum TCP header size allowed (0–256 bytes) | 8'h14   |

## Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)

**Table 228: Maximum ICMPv4 Size Register (Page 36h: Address 08h–0Bh)**

| Bit  | Name            | R/W | Description                            | Default |
|------|-----------------|-----|----------------------------------------|---------|
| 31:0 | MAX_ICMPv4_SIZE | R/W | Maximum ICMPv4 size allowed (0–9.6 KB) | 32'd512 |

## Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)

*Table 229: Maximum ICMPv6 Size Register (Page 36h: Address 0Ch–0Fh)*

| Bit  | Name            | R/W | Description                            | Default |
|------|-----------------|-----|----------------------------------------|---------|
| 31:0 | MAX_ICMPv6_SIZE | R/W | Maximum ICMPv6 size allowed (0–9.6 KB) | 32'd512 |

## DOS Disable Learn Register (Page 36h: Address 10h)

*Table 230: DOS Disable Learn Register (Page 36h: Address 08h–0Bh)*

| Bit | Name            | R/W | Description                                                                     | Default |
|-----|-----------------|-----|---------------------------------------------------------------------------------|---------|
| 7:1 | RESERVED        | R/W | Reserved                                                                        | –       |
| 0   | DOS Disable Lrn | R/W | When this bit enabled, all frames dropped by DOS 0 prevent will not be learned. |         |

## Page 40h: Jumbo Frame Control Register

*Table 231: Page 40h Jumbo Frame Control Register*

| Address | Bits | Description                                                                                |
|---------|------|--------------------------------------------------------------------------------------------|
| 00h     | –    | Reserved                                                                                   |
| 01h–04h | 32   | <a href="#">“Jumbo Frame Port Mask Register (Page 40h: Address 01h)” on page 272</a>       |
| 05h–06h | 16   | <a href="#">“Standard Maximum Frame Size Register (Page 40h: Address 05h)” on page 273</a> |
| 07h–EFh | –    | Reserved                                                                                   |
| F0h–F7h | 8    | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294</a> , bytes 0–7      |
| F8h–FDh | –    | Reserved                                                                                   |
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>                    |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                          |

## Jumbo Frame Port Mask Register (Page 40h: Address 01h)

*Table 232: Jumbo Frame Port Mask Registers (Page 40h: Address 01h–04h)*

| Bit   | Name     | R/W | Description | Default |
|-------|----------|-----|-------------|---------|
| 31:25 | Reserved | RO  | –           | 0       |
| 24:9  | Reserved | R/W | –           | 0       |

**Table 232: Jumbo Frame Port Mask Registers (Page 40h: Address 01h–04h) (Cont.)**

| Bit | Name            | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Default |
|-----|-----------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 8:0 | JUMBO_PORT_MASK | R/W | <p>Jumbo frame port mask</p> <p>Bit 8 = IMP port</p> <p>Bits [5:0] correspond to ports [5:0], respectively.</p> <p>0 = Disable jumbo frame capability on the port.</p> <p>1 = Enable jumbo frame capability on the port.</p> <p>Jumbo frames can be ingressed and egressed only to the ports enabled using this port mask. Jumbo frame port mask has no effect on the traffic of normal sized frames. See <a href="#">“Jumbo Frame Support” on page 43</a> for more information.</p> | 0       |



**Note:** When the Jumbo Frame feature is enabled, the assigned Weight value for the WRR scheduling cannot be applied fairly over the queues. This is due to the internal Packet Buffer Memory size limitation.

**Note:** The Jumbo Frame feature is only supported in 1000 Mbps mode.

## Standard Maximum Frame Size Register (Page 40h: Address 05h)

**Table 233: Standard Maximum Frame Size Registers (Page 40h: Address 05h–06h)**

| Bit   | Name     | R/W | Description | Default |
|-------|----------|-----|-------------|---------|
| 15:14 | Reserved | RO  | –           | 0       |

**Table 233: Standard Maximum Frame Size Registers (Page 40h: Address 05h–06h) (Cont.)**

| Bit  | Name                        | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Default |
|------|-----------------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 13:0 | Standard Maximum Frame Size | R/W | <p>Defines the standard maximum frame size for MAC and MIB counter.</p> <p>This register only allowed to be configured as 14'd1518 or 14'd2000. When jumbo is disabled, the content of this register is used to define good frame length.</p> <ul style="list-style-type: none"> <li>If it is configured as 1518, the tagged frames will be dropped if the frame length is larger than 1522 bytes; and the untagged frames will be dropped if the frame length is larger than 1518 bytes.</li> <li>If it is configured as 2000, both tagged and untagged frames will be dropped if the frame length is larger than 2000 bytes.</li> </ul> <p>When jumbo is enabled, all frames will be dropped if the frame length is larger than 9720 bytes.</p> <p>The register setting affects the following MIB parameters:</p> <ul style="list-style-type: none"> <li>RxSACChange</li> <li>RxGoodOctets</li> <li>RxUnicastPkts</li> <li>RxMulticastPkts</li> <li>RxBroadcastPkts</li> <li>RxOverSizePkts</li> </ul> | 'd2000  |

## Page 41h: Broadcast Storm Suppression Register

**Table 234: Broadcast Storm Suppression Register (Page 41h)**

| Address | Bits    | Description                                                                                                                |
|---------|---------|----------------------------------------------------------------------------------------------------------------------------|
| 00h–03h | 32      | <a href="#">“Ingress Rate Control Configuration Register (Page 41h: Address 00h)” on page 275</a>                          |
| 04h–0Fh | –       | Reserved                                                                                                                   |
| 10h–33h | 32/port | <a href="#">“Port Receive Rate Control Register (Page 41h: Address 10h)” on page 276</a>                                   |
| 34h–4Fh | –       | Reserved                                                                                                                   |
| 50h–73h | –       | Reserved                                                                                                                   |
| 74h–7Fh | –       | Reserved                                                                                                                   |
| 80h–91h | 16/port | <a href="#">“Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)” on page 279</a>                  |
| 92h–BFh | –       | Reserved                                                                                                                   |
| C0h–C1h | 8       | <a href="#">“IMP Port (IMP/Port 5) Egress Rate Control Configuration Register (Page 41h: Address C0h–C1h)” on page 279</a> |

**Table 234: Broadcast Storm Suppression Register (Page 41h)**

| Address | Bits | Description                                                                           |
|---------|------|---------------------------------------------------------------------------------------|
| C2h–EFh | –    | Reserved                                                                              |
| F0h–F7h | 8    | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294</a> , bytes 0–7 |
| F8h–FDh | –    | Reserved                                                                              |
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>               |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                     |

## Ingress Rate Control Configuration Register (Page 41h: Address 00h)

**Table 235: Global Rate Control Register (Page 41h: Address 00h–03h)**

| Bit   | Name               | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Default |
|-------|--------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:19 | Reserved           | RO  | –                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0       |
| 18    | XLENEN             | R/W | Packet Length Selection<br>0 = Ingress/Egress Rate excludes IPG.<br>1 = Ingress/Egress rate includes IPG.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0       |
| 17    | BUCK1_BRM_SEL      | R/W | Bit rate mode selection<br>0 = Absolute bit rate mode — The rate count in the <a href="#">“Port Receive Rate Control Register (Page 41h: Address 10h)” on page 276</a> represents the incoming bit rate as an absolute data rate.<br>1 = Bit rate normalized to link speed mode — The rate count in the <a href="#">“Port Receive Rate Control Register (Page 41h: Address 10h)” on page 276</a> represents the incoming bit rate normalized with respect to the link speed mode.<br>See <a href="#">“Rate Control” on page 44</a> for more details.                                   | 0       |
| 16    | Reserved           | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1       |
| 15:9  | BUCK1_PACKET_TY PE | R/W | Suppressed packet type mask.<br>This bit mask determines the type of packets to be monitored by bucket 1.<br>0 = Disable suppression for the corresponding packet type.<br>1 = Enable suppression for the corresponding packet type.<br>The bits in this bit field are defined as follows:<br>Bit 9 = Unicast lookup hit<br>Bit 10 = Multicast lookup hit<br>Bit 11 = Reserved MAC Address Frame<br>Bit 12 = Broadcast<br>Bit 13 = Multicast lookup failure<br>Bit 14 = Unicast lookup failure<br>Bit 15 = Reserved<br>See <a href="#">“Rate Control” on page 44</a> for more details. | 0       |

**Table 235: Global Rate Control Register (Page 41h: Address 00h–03h) (Cont.)**

| Bit | Name               | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Default                                   |
|-----|--------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
| 8   | BUCKO_BRM_SEL      | R/W | Bit rate mode selection<br>0 = Absolute bit rate mode — The rate count in the “ <a href="#">Port Receive Rate Control Register (Page 41h: Address 10h)</a> ” on <a href="#">page 276</a> represents the incoming bit rate as an absolute data rate.<br>1 = Bit rate normalized to link speed mode — The rate count in the “ <a href="#">Port Receive Rate Control Register (Page 41h: Address 10h)</a> ” on <a href="#">page 276</a> represents the incoming bit rate normalized with respect to the link speed mode.<br>See “ <a href="#">Rate Control</a> ” on <a href="#">page 44</a> for more details. | BC_SUPP_EN                                |
| 7   | Reserved           | R/W | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1                                         |
| 6:0 | BUCKO_PACKET_TY PE | R/W | Suppressed packet type mask.<br>This bit mask determines the type of packets to be monitored by bucket 0.<br>0 = Disable suppression for the corresponding packet type.<br>1 = Enable suppression for the corresponding packet type.<br>The bits in this bit field are defined as follows:<br>Bit 0 = Unicast lookup hit<br>Bit 1 = Multicast lookup hit<br>Bit 2 = Reserved MAC address frame<br>Bit 3 = Broadcast<br>Bit 4 = Multicast lookup failure<br>Bit 5 = Unicast lookup failure<br>Bit 6 = Reserved<br>See “ <a href="#">Rate Control</a> ” on <a href="#">page 44</a> for more details.         | BC_SUPP_EN:<br>1 = 0001000<br>0 = 0000000 |

## Port Receive Rate Control Register (Page 41h: Address 10h)

**Table 236: Port Rate Control Register Address Summary**

| Address | Description            |
|---------|------------------------|
| 10h–13h | Port 0                 |
| 14h–17h | Port 1                 |
| 18h–1Bh | Port 2                 |
| 1Ch–1Fh | Port 3                 |
| 20h–23h | Port 4                 |
| 24h–27h | Port 5                 |
| 28h–2Bh | Reserved               |
| 2Ch–2Fh | Reserved               |
| 30h–33h | IMP port for BCM53115S |

**Table 237: Port Rate Control Register (Page 41h: Address 10h–33h)**

| <b>Bit</b> | <b>Name</b>    | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                  | <b>Default</b>                    |
|------------|----------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
| 31:29      | Reserved       | RO         | –                                                                                                                                                                                                                                                                                                   | 0                                 |
| 28         | STRM_SUPR_EN   | R/W        | Enable storm suppression (Supported by bucket1).<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                       | Reflects the strap pin BC_SUPP_EN |
| 27         | RsvMC_SUPR_EN  | R/W        | Enable reserved mulitcast storm suppression.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                           | 0                                 |
| 26         | BC_SUPR_EN     | R/W        | Enable broadcast storm suppression.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                                    | 0                                 |
| 25         | MC_SUPR_EN     | R/W        | Enable multicast storm suppression.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                                    | 0                                 |
| 24         | DLF_SUPR_EN    | R/W        | Enable DLF storm suppression.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                                          | 0                                 |
| 23         | Enable Bucket1 | R/W        | Enable rate control of the ingress port, bucket 1.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                     | 0                                 |
| 22         | Enable Bucket0 | R/W        | Enable rate control of the ingress port, bucket 0.<br>0 = Disable<br>1 = Enable                                                                                                                                                                                                                     | Reflects the strap pin BC_SUPP_EN |
| 21:19      | BUCK1_SIZE     | R/W        | Bucket size<br>This bit determines the maximum size of bucket 1. This is specified on a per port basis.<br>000 = 4 KB<br>001 = 8 KB<br>010 = 16 KB<br>011 = 32 KB<br>100 = 64 KB<br>101 = 500 KB<br>110 = 500 KB<br>111 = 500 KB<br>See <a href="#">“Rate Control” on page 44</a> for more details. | 000                               |

**Table 237: Port Rate Control Register (Page 41h: Address 10h–33h) (Cont.)**

| <b>Bit</b> | <b>Name</b>    | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | <b>Default</b> |
|------------|----------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 18:11      | BUCK1_Rate_Cnt | R/W        | <p>Rate count</p> <p>The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the <a href="#">“Ingress Rate Control Configuration Register (Page 41h: Address 00h)”</a> on page 275 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the suppressed packet type mask in the <a href="#">“Ingress Rate Control Configuration Register (Page 41h: Address 00h)”</a> on page 275. See <a href="#">“Rate Control”</a> on page 44 for more details.</p> <p>Values written to these bits must be with the ranges specified by <a href="#">Table 3 on page 46</a>. Values outside these ranges are not valid.</p> | 10h            |
| 10:8       | BUCK0_SIZE     | R/W        | <p>Bucket size</p> <p>This bit determines the maximum size of bucket 0. This is specified on a per port basis.</p> <p>000 = 4 KB<br/> 001 = 8 KB<br/> 010 = 16 KB<br/> 011 = 32 KB<br/> 100 = 64 KB<br/> 101 = 500 KB<br/> 110 = 500 KB<br/> 111 = 500 KB</p> <p>See <a href="#">“Rate Control”</a> on page 44 for more details.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 000            |
| 7:0        | BUCK0_Rate_Cnt | R/W        | <p>Rate count</p> <p>The rate count is an integer that increments the rate at which traffic can ingress the given port without being suppressed. This value is specified on a per port basis. The programmed values of the rate count and the bit rate mode of the <a href="#">“Ingress Rate Control Configuration Register (Page 41h: Address 00h)”</a> on page 275 determine the bucket bit rate in kilobytes. The bucket bit rate represents the average upper limit for incoming packets selected in the Suppressed packet type mask in the <a href="#">“Ingress Rate Control Configuration Register (Page 41h: Address 00h)”</a> on page 275. See <a href="#">“Rate Control”</a> on page 44 for more details.</p>                                                                                                                                                         | 10h            |

## Port Egress Rate Control Configuration Register (Page 41h: Address 80h–91h)

**Table 238: Port Egress Rate Control Configuration Register Address Summary**

| Address | Description |
|---------|-------------|
| 80h–81h | Port 0      |
| 82h–83h | Port 1      |
| 84h–85h | Port 2      |
| 86h–87h | Port 3      |
| 88h–89h | Port 4      |
| 8Ah–8Bh | Port 5      |
| 8Ch–8Dh | Reserved    |
| 8Eh–8Fh | Reserved    |
| 90h–91h | IMP port    |

**Table 239: Port Egress Rate Control Configuration Registers (Page 41h: Address 80h–91h)**

| Bit   | Name     | R/W | Description                                                                                                                                                                                                                                                                                         | Default |
|-------|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:12 | Reserved | RO  | –                                                                                                                                                                                                                                                                                                   | 0       |
| 11    | ERC_EN   | R/W | Egress rate control enable ((Absolute Bit Rate)                                                                                                                                                                                                                                                     | 0       |
| 10:8  | BKT_SIZE | R/W | Bucket size<br>This bit determines the maximum size of bucket 0. This is specified on a per port basis.<br>000 = 4 KB<br>001 = 8 KB<br>010 = 16 KB<br>011 = 32 KB<br>100 = 64 KB<br>101 = 500 KB<br>110 = 500 KB<br>111 = 500 KB<br>See <a href="#">“Rate Control” on page 44</a> for more details. | 0       |
| 7:0   | RFSH_CNT | R/W | Refresh count for bucket                                                                                                                                                                                                                                                                            | 0       |

## IMP Port (IMP/Port 5) Egress Rate Control Configuration Register (Page 41h: Address C0h–C1h)

**Table 240: IMP Port (IMP/Port 5) Egress Rate Control Configuration Register Address Summary**

| Address | Description |
|---------|-------------|
| C0h     | IMP Port    |

**Table 240: IMP Port (IMP/Port 5) Egress Rate Control Configuration Register Address Summary**

| Address | Description                                                                                                                                      |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| C1h     | Port 5: Enable dual-IMP ports, EN_IMP_PORT=11 in <a href="#">“Global Management Configuration Register (Page 02h: Address 00h)”</a> on page 169. |

**Table 241: IMP Port (IMP/Port 5) Egress Rate Control Configuration Registers (Page 41h: Address C0h–C1h)**

| Bit | Name       | R/W | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Default |
|-----|------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:6 | RESERVED   | RO  | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 0       |
| 5:0 | Rate_Index | R/W | <p>Rate_Index is used to configure different egress rates for IMP in packet per second (pps). See <a href="#">Table 242: “Using Rate_Index to Configure Different Egress Rates for IMP in pps,”</a> on page 280.</p> <p>When set to 0, the egress rate is limited to a maximum of 384 pps.</p> <p>When set to 63, the egress rate control function is disabled and all packets are transmitted at wire-speed.</p> <p><b>Note:</b> If the Rate_Index is configured as a certain value, the egress rate is limited to the corresponding speed whether the switch is running at 10 Mbps, 100 Mbps, or 1 Gbps.</p> <p><b>Note:</b> The Rate_Index should be a reasonable value under the corresponding network speed configuration. It does not make sense to set a value of 63 with the network configuration at 10 Mbps. In that case, the egress rate is limited up to 10 Mbps.</p> | 6'd63   |

**Table 242: Using Rate\_Index to Configure Different Egress Rates for IMP in pps**

| Rate_Index | pps  | Rate_Index | pps   | Rate_Index | pps   | Rate_Index | pps     |
|------------|------|------------|-------|------------|-------|------------|---------|
| 0          | 384  | 16         | 5376  | 32         | 25354 | 48         | 357143  |
| 1          | 512  | 17         | 5887  | 33         | 27382 | 49         | 423729  |
| 2          | 639  | 18         | 6400  | 34         | 29446 | 50         | 500000  |
| 3          | 768  | 19         | 6911  | 35         | 31486 | 51         | 568182  |
| 4          | 1024 | 20         | 7936  | 36         | 35561 | 52         | 641026  |
| 5          | 1280 | 21         | 8960  | 37         | 39682 | 53         | 714286  |
| 6          | 1536 | 22         | 9984  | 38         | 42589 | 54         | 781250  |
| 7          | 1791 | 23         | 11008 | 39         | 56818 | 55         | 862069  |
| 8          | 2048 | 24         | 12030 | 40         | 71023 | 56         | 925926  |
| 9          | 2303 | 25         | 13054 | 41         | 85324 | 57         | 1000000 |
| 10         | 2559 | 26         | 14076 | 42         | 99602 | 58         | 1086957 |

**Table 242: Using Rate\_Index to Configure Different Egress Rates for IMP in pps (Cont.)**

| <b>Rate_Index</b> | <b>pps</b> | <b>Rate_Index</b> | <b>pps</b> | <b>Rate_Index</b> | <b>pps</b> | <b>Rate_Index</b> | <b>pps</b> |
|-------------------|------------|-------------------|------------|-------------------|------------|-------------------|------------|
| 11                | 2815       | 27                | 15105      | 43                | 113636     | 59                | 1136364    |
| 12                | 3328       | 28                | 17146      | 44                | 127551     | 60                | 1190476    |
| 13                | 3840       | 29                | 19201      | 45                | 142045     | 61                | 1250000    |
| 14                | 4352       | 30                | 21240      | 46                | 213675     | 62                | 1315789    |
| 15                | 4863       | 31                | 23299      | 47                | 284091     | 63                | 1388889    |

## Page 42h: EAP Register

**Table 243: Broadcast Storm Suppression Register (Page 42h)**

| Address | Bits | Description                                                                  |
|---------|------|------------------------------------------------------------------------------|
| 00h     | 8    | "EAP Global Control Register (Page 42h: Address 00h)" on page 282            |
| 01h     | 8    | "EAP Multiport Address Control Register (Page 42h: Address 01h)" on page 283 |
| 02h–09h | 64   | "EAP Destination IP Register 0 (Page 42h: Address 02h)" on page 283          |
| 0Ah–12h | 64   | "EAP Destination IP Register 1 (Page 42h: Address 0Ah)" on page 284          |
| 20h–4Fh | 64   | "Port EAP Configuration Register (Page 42h: Address 20h)" on page 284        |
| 50h–57h | 64   | Reserved                                                                     |
| 58h–5Fh | 64   | Reserved                                                                     |
| 60h–EFh | –    | Reserved                                                                     |
| F0h–F7h | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, bytes 0–7         |
| F8h–FDh | –    | Reserved                                                                     |
| FEh     | 8    | "SPI Status Register (Global, Address FEh)" on page 295                      |
| FFh     | 8    | "Page Register (Global, Address FFh)" on page 295                            |

## EAP Global Control Register (Page 42h: Address 00h)

**Table 244: EAP Global Control Registers (Page 42h: Address 00h)**

| Bit | Name     | R/W | Description                                                                                                                       | Default |
|-----|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | Reserved | –   | –                                                                                                                                 | 0       |
| 6   | EN_RARP  | –   | When EAP_BLK_MODE is set:<br>1 = Allow RARP to pass.<br>0 = Drop RARP                                                             | 0       |
| 5   | EN_BPDU  | –   | When EAP_BLK_MODE is set:<br>1 = BPDU Addresses are allowed to pass.<br>0 = Drop                                                  | –       |
| 4   | EN_RMC   | –   | When EAP_BLK_MODE is set:<br>1 = Allows DA = 01-80-C2-00-00-02, 04-0F to pass.<br>0 = Drop DA = 01-80-C2-00-00-02, 04-0F to pass. | –       |
| 3   | EN_DHCP  | –   | When EAP_BLK_MODE is set:<br>1 = Allows DHCP to pass<br>0 = Drop DHCP                                                             | –       |
| 2   | EN_ARP   | –   | When EAP_BLK_MODE is set:<br>1 = Allows ARP to pass<br>0 = Drop ARP                                                               | –       |

**Table 244: EAP Global Control Registers (Page 42h: Address 00h) (Cont.)**

| Bit | Name     | R/W | Description                                                                                                                                   | Default |
|-----|----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 1   | EN_2DIP  | R/W | When EAP_BLK_MODE bit is set:<br>1 = Two subnet IP addresses defined in EAP destination IP registers 0 and 1 are allowed to pass.<br>0 = Drop | 0       |
| 0   | Reserved | —   | —                                                                                                                                             | 0       |

## EAP Multiport Address Control Register (Page 42h: Address 01h)

**Table 245: EAP Multiport Address Control Register (Page 42h: Address 01h)**

| Bit | Name      | R/W | Description                                                                                                                                   | Default |
|-----|-----------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 7:6 | Reserved  | RO  | —                                                                                                                                             | —       |
| 5   | EN_MPORT5 | R/W | 1 = Allow Multiport ETYPE Address 5 define at “Multiport Address N (N=0–5) Register (Page 04h: Address 10h)” on page 180 to pass.<br>0 = Drop | —       |
| 4   | EN_MPORT4 | R/W | 1 = Allow Multiport ETYPE Address 4 define at “Multiport Address N (N=0–5) Register (Page 04h: Address 10h)” on page 180 to pass.<br>0 = Drop | —       |
| 3   | EN_MPORT3 | R/W | 1 = Allow Multiport ETYPE Address 3 define at “Multiport Address N (N=0–5) Register (Page 04h: Address 10h)” on page 180 to pass.<br>0 = Drop | —       |
| 2   | EN_MPORT2 | R/W | 1 = Allow Multiport ETYPE Address 2 define at “Multiport Address N (N=0–5) Register (Page 04h: Address 10h)” on page 180 to pass.<br>0 = Drop | —       |
| 1   | EN_MPORT1 | R/W | 1 = Allow Multiport ETYPE Address 1 define at “Multiport Address N (N=0–5) Register (Page 04h: Address 10h)” on page 180 to pass.<br>0 = Drop | —       |
| 0   | EN_MPORT0 | R/W | 1 = Allow Multiport ETYPE Address 0 define at “Multiport Address N (N=0–5) Register (Page 04h: Address 10h)” on page 180 to pass.<br>0 = Drop | —       |

## EAP Destination IP Register 0 (Page 42h: Address 02h)

**Table 246: EAP Destination IP Registers 0 (Page 42h: Address 02h–09h)**

| Bit   | Name      | R/W | Description                          | Default |
|-------|-----------|-----|--------------------------------------|---------|
| 63:32 | DIP_SUB 0 | R/W | EAP destination IP subnet register 0 | 0       |

**Table 246: EAP Destination IP Registers 0 (Page 42h: Address 02h–09h) (Cont.)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                 | <b>Default</b> |
|------------|-------------|------------|------------------------------------|----------------|
| 31:0       | DIP_MSK 0   | R/W        | EAP destination IP mask register 0 | 0              |

## EAP Destination IP Register 1 (Page 42h: Address 0Ah)

**Table 247: EAP Destination IP Registers 1 (Page 42h: Address 0Ah–12h)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                   | <b>Default</b> |
|------------|-------------|------------|--------------------------------------|----------------|
| 63:32      | DIP_SUB 1   | R/W        | EAP destination IP subnet register 1 | 0              |
| 31:0       | DIP_MSK 1   | R/W        | EAP destination IP mask register 1   | 0              |

## Port EAP Configuration Register (Page 42h: Address 20h)

**Table 248: Port EAP Configuration Register Address Summary**

| <b>Address</b> | <b>Description</b> |
|----------------|--------------------|
| 20h–27h        | Port 0             |
| 28h–2Fh        | Port 1             |
| 30h–37h        | Port 2             |
| 38h–3Fh        | Port 3             |
| 40h–47h        | Port 4             |
| 48h–4Fh        | Port 5             |

**Table 249: Port EAP Configuration Registers (Page 42h: Address 20h–47h)**

| <b>Bit</b> | <b>Name</b>  | <b>R/W</b> | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                            | <b>Default</b> |
|------------|--------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 63:55      | Reserved     | RO         | –                                                                                                                                                                                                                                                                                                                                                                                             | 0              |
| 52:51      | EAP_MODE     | R/W        | 00 = Basic mode, do not check SA.<br>01 = Reserved<br>10 = Extend mode, check SA and port number, drop if SA is unknown.<br>11 = Simplified mode, check SA and port number trap to management port if SA is unknown.                                                                                                                                                                          | 0              |
| 50:49      | EAP_BLK_MODE | R/W        | 00 = Do not check EAP_BLK_MODE.<br>01 = To check EAP_BLK MODE on ingress port, only the frame defined in EAP_GCFCG will be forwarded. Otherwise, the frame will be dropped.<br>10 = reserved<br>11 = To check EAP_BLK MODE on both ingress and egress port, only the frame defined in EAP_GCFCG will be forwarded. The forwarding process will verify that each egress port is at block mode. | 0              |

**Table 249: Port EAP Configuration Registers (Page 42h: Address 20h–47h) (Cont.)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>       | <b>Default</b>        |
|------------|-------------|------------|--------------------------|-----------------------|
| 48         | EAP_EN_DA   | R/W        | Enable EAP frame with DA | 0                     |
| 47:0       | EAP_DA      | R/W        | EAP frame DA register    | 00-00-00-<br>00-00-00 |

## Page 43h: MSPT Register

**Table 250: Broadcast Storm Suppression Register (Page 43h)**

| Address | Bits | Description                                                                                             |
|---------|------|---------------------------------------------------------------------------------------------------------|
| 00h     | 8    | MSPT control register                                                                                   |
| 01h     | —    | Reserved                                                                                                |
| 02h–05h | 32   | <a href="#">“MSPT Aging Control Register (Page 43h: Address 02h)” on page 286</a>                       |
| 06h–0Fh | —    | Reserved                                                                                                |
| 10h–2Fh | 32   | <a href="#">“MSPT Table Register (Page 43h: Address 10h)” on page 287</a>                               |
| 30h–4Ah | —    | Reserved                                                                                                |
| 50h–51h | 16   | <a href="#">“SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)” on page 287</a> |
| 52h–EFh | —    | Reserved                                                                                                |
| F0h–F7h | 8    | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294, bytes 0–7</a>                    |
| F8h–FDh | —    | Reserved                                                                                                |
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>                                 |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                                       |

## MSPT Control Register (Page 43h: Address 00h)

**Table 251: MSPT Control Registers (Page 43h: Address 00h–01h)**

| Bit | Name      | R/W | Description               | Default |
|-----|-----------|-----|---------------------------|---------|
| 7:1 | Reserved  | —   | —                         | 0       |
| 0   | EN_802.1S | R/W | 0 = Disable<br>1 = Enable | 0       |

## MSPT Aging Control Register (Page 43h: Address 02h)

**Table 252: MSPT Aging Control Registers (Page 43h: Address 02h–05h)**

| Bit  | Name         | R/W | Description                    | Default |
|------|--------------|-----|--------------------------------|---------|
| 31:8 | Reserved     | R/W | —                              | 0       |
| 7:0  | MSPT_AGE_MAP | R/W | Per spanning tree aging enable | 0       |

## MSPT Table Register (Page 43h: Address 10h)

**Table 253: MSPT Table Register Address Summary**

| Address | Description |
|---------|-------------|
| 10h–13h | MSPT 0      |
| 14h–17h | MSPT 1      |
| 18h–1Bh | MSPT 2      |
| 1Ch–1Fh | MSPT 3      |
| 20h–23h | MSPT 4      |
| 24h–27h | MSPT 5      |
| 28h–2Bh | MSPT 6      |
| 2Ch–2Fh | MSPT 7      |

**Table 254: MSPT Table Registers (Page 43h: Address 10h–2Fh)**

| Bit   | Name     | R/W | Description                                                                                                                                           | Default |
|-------|----------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 31:27 | Reserved | RO  | –                                                                                                                                                     | 0       |
| 26:24 | Reserved | R/W | –                                                                                                                                                     | 0       |
| 23:21 | Reserved | R/W | –                                                                                                                                                     | 0       |
| 20:18 | Reserved | R/W | –                                                                                                                                                     | 0       |
| 17:15 | SPT_STA5 | R/W | Spanning tree state for port 5                                                                                                                        | 0       |
| 14:12 | SPT_STA4 | R/W | Spanning tree state for port 4<br>000 = No spanning tree<br>001 = Disabled<br>010 = Blocking<br>011 = Listening<br>100 = Learning<br>101 = Forwarding | 0       |
| 11:9  | SPT_STA3 | R/W | Spanning tree state for Port 3                                                                                                                        | 0       |
| 8:6   | SPT_STA2 | R/W | Spanning tree state for Port 2                                                                                                                        | 0       |
| 5:3   | SPT_STA1 | R/W | Spanning tree state for Port 1                                                                                                                        | 0       |
| 2:0   | SPT_STA0 | R/W | Spanning tree state for Port 0                                                                                                                        | 0       |

## SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)

**Table 255: SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h)**

| Bit  | Name     | R/W | Description | Default |
|------|----------|-----|-------------|---------|
| 15:6 | Reserved | RO  | –           | –       |

**Table 255: SPT Multiport Address Bypass Control Register (Page 43h: Address 50h–51h) (Cont.)**

| Bit | Name                 | R/W | Description                                                                                                                                                                             | Default |
|-----|----------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 5   | EN_MPORT5_BYPASS_SPT | R/W | 1 = The MPORT_ADD_5 of “Multiport Address N – (N=0–5) Register (Page 04h: Address 10h)” on page 180 is not checked by SPT status.<br>0 = The MPORT_ADD_5 is checked by SPT status.      |         |
| 4   | EN_MPORT4_BYPASS_SPT | R/W | 1 = The MPORT_ADD_4 of “Multiport Address N – (N=0–5) Register (Page 04h: Address 10h)” on page 180 is not checked by SPT status.<br>0 = The MPORT_ADD_4 will be checked by SPT status. |         |
| 3   | EN_MPORT3_BYPASS_SPT | R/W | 1 = The MPORT_ADD_3 of “Multiport Address N – (N=0–5) Register (Page 04h: Address 10h)” on page 180 is not checked by SPT status.<br>0 = The MPORT_ADD_3 is checked by SPT status.      |         |
| 2   | EN_MPORT2_BYPASS_SPT | R/W | 1 = The MPORT_ADD_2 of “Multiport Address N – (N=0–5) Register (Page 04h: Address 10h)” on page 180 is not checked by SPT status.<br>0 = The MPORT_ADD_2 is checked by SPT status.      |         |
| 1   | EN_MPORT1_BYPASS_SPT | R/W | 1 = The MPORT_ADD_1 of “Multiport Address N – (N=0–5) Register (Page 04h: Address 10h)” on page 180 is not checked by SPT status.<br>0 = The MPORT_ADD_1 is checked by SPT status.      |         |
| 0   | EN_MPORT0_BYPASS_SPT | R/W | 1 = The MPORT_ADD_0 of “Multiport Address N – (N=0–5) Register (Page 04h: Address 10h)” on page 180 is not checked by SPT status.<br>0 = The MPORT_ADD_0 is checked by SPT status.      |         |

## Page 70h: MIB Snapshot Control Register

**Table 256: MIB Snapshot Control Register**

| Address | Bits | Description                                                         |
|---------|------|---------------------------------------------------------------------|
| 00h     | 8    | “MIB Snapshot Control Register (Page 70h: Address 00h)” on page 289 |
| 01h–EFh | –    | Reserved                                                            |
| F0h–F7h | 8    | “SPI Data I/O Register (Global, Address F0h)” on page 294 bytes 0-7 |
| F8h–FDh | –    | Reserved                                                            |
| FEh     | 8    | “SPI Status Register (Global, Address FEh)” on page 295             |
| FFh     | 8    | “Page Register (Global, Address FFh)” on page 295                   |

## MIB Snapshot Control Register (Page 70h: Address 00h)

**Table 257: MIB Snapshot Control Register (Page 70h: Address 00h)**

| Bit | Name                | R/W       | Description                                                                                                              | Default |
|-----|---------------------|-----------|--------------------------------------------------------------------------------------------------------------------------|---------|
| 7   | SNAPSHOT_START/DONE | R/W<br>SC | Write 1'b1 to initiate MIB snapshot access, clear to 1'b0 when MIB snapshot access is done                               | 0       |
| 6   | SNAPSHOT_MIRROR     | R/W       | 1'b1 = enable read address to port MIB, but data from MIB snapshot memory.<br>1'b0 = enable to read from port MIB memory | 0       |
| 5:4 | Reserved            | R/W       | —                                                                                                                        | —       |
| 3:0 | SNAPSHOT_PORT       | R/W       | Port number for MIB snapshot function                                                                                    | 0       |

## Page 71h: Port Snapshot MIB Control Register

**Table 258: Port Snapshot MIB Control Register**

| Address | Bits | Description                                                                                                                         |
|---------|------|-------------------------------------------------------------------------------------------------------------------------------------|
| 71h     | —    | The Port Snapshot MIB Registers are same as registers in <a href="#">“MII Control Register (Page 15h: Address 00h)” on page 227</a> |

## Page 72h: Loop Detection Register

**Table 259: Loop Detection Control Register (Page 72h)**

| Address | Bits | Description                                                                                  |
|---------|------|----------------------------------------------------------------------------------------------|
| 00h–01h | 16   | <a href="#">“Loop Detection Control Register (Page 72h: Address 00h)” on page 290</a>        |
| 02h     | 8    | <a href="#">“Discovery Frame Timer Control Register (Page 72h: Address 02h)” on page 290</a> |
| 03h–04h | 16   | <a href="#">“LED Warning Port Map Register (Page 72h: Address 03h)” on page 291</a>          |
| 05h–0Ah | 48   | Module ID 0                                                                                  |
| 0Bh–10h | 48   | Module ID 1                                                                                  |
| 11h–16h | 48   | Loop detect frame SA                                                                         |
| 17h–EFh | —    | Reserved                                                                                     |
| F0h–F7h | 8    | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294</a> , bytes 0–7        |
| F8h–FDh | —    | Reserved                                                                                     |

**Table 259: Loop Detection Control Register (Page 72h) (Cont.)**

| Address | Bits | Description                                                             |
|---------|------|-------------------------------------------------------------------------|
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a> |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>       |

## Loop Detection Control Register (Page 72h: Address 00h)

**Table 260: Loop Detection Control Registers (Page 72h: Address 00h–01h)**

| Bit   | Name                      | R/W | Description                                                                                                               | Default     |
|-------|---------------------------|-----|---------------------------------------------------------------------------------------------------------------------------|-------------|
| 15:13 | Reserved                  | R/W | –                                                                                                                         | 0           |
| 12    | EN_LOOP_DETECT            | R/W | Enable loop detection feature.<br>0 = Disable<br>1 = Enable                                                               | Strap       |
| 11    | LOOP_IMP_SEL              | R/W | Enable IMP loop detection feature.<br>0 = Disable<br>1 = Enable                                                           | Strap       |
| 10:3  | LED_RST_TIMR_CTRL         | R/W | Number of missed discovery time before LED warning portmap to be reset                                                    | 8'b00000100 |
| 2     | OV_PAUSE_ON               | R/W | 1 = Transmit frame in highest queue even if the port is in pause state<br>0 = Transmit frame follows the pause state rule | 1'b1        |
| 1:0   | DISCOVERY_FRAME_QUEUE_SEL | R/W | Specifies which queue to be put for the received discovery frame                                                          | 2'b01       |

## Discovery Frame Timer Control Register (Page 72h: Address 02h)

**Table 261: Discovery Frame Timer Control Registers (Page 72h: Address 02h)**

| Bit | Name                 | R/W | Description                                                                                                    | Default |
|-----|----------------------|-----|----------------------------------------------------------------------------------------------------------------|---------|
| 7:4 | Reserved             | R/W | –                                                                                                              | 0       |
| 3:0 | DISCOVER_FRAME_TIMER | R/W | From 1 second (default) to 15 seconds. Scale = 1s.<br>0000 = 1s<br>0001 = 2s<br>0002 = 3s<br>...<br>1110 = 15s | 0       |

## LED Warning Port Map Register (Page 72h: Address 03h)

**Table 262: LED Warning Port Map Registers (Page 72h: Address 03h–04h)**

| Bit  | Name                | R/W | Description                                                                                                                                      | Default |
|------|---------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------|---------|
| 15:9 | Reserved            | R/O | –                                                                                                                                                | 0       |
| 8:0  | LED_WARNING_PORTMAP | R/O | Bit 8 = IMP port<br>Bits [5:0] correspond to ports [5:0], respectively.<br>Each bit shows the status of Loop Detected on the corresponding port. | 0       |

## Module ID 0 Register (Page 72h: Address 05h)

**Table 263: Module ID 0 Registers (Page 72h: Address 05h–0Ah)**

| Bit  | Name         | R/W | Description | Default |
|------|--------------|-----|-------------|---------|
| 47:0 | Module_ID_SA | RO  | –           | 0       |

## Module ID 1 Register (Page 72h: Address 0Bh)

**Table 264: Module ID 1 Registers (Page 72h: Address 0Bh–10h)**

| Bit   | Name                | R/W | Description                                                                                   | Default |
|-------|---------------------|-----|-----------------------------------------------------------------------------------------------|---------|
| 47    | Module_ID_AVAILABLE | RO  | Module ID is available when the first packet is received.<br>0 = Unavailable<br>1 = Available | 0       |
| 46:40 | Reserved            | RO  | –                                                                                             | 0       |
| 39:32 | MODULE_ID_PORT_NO   | RO  | This is an 8-bit port number for module ID.                                                   | 0       |
| 31:0  | MODULE_ID_CRC       | RO  | This is an 32-bit CRC for module ID.                                                          | 0       |

## Loop Detect Source Address Register (Page 72h: Address 11h)

**Table 265: Loop Detect Source Address Registers (Page 72h: Address 11h–16h)**

| Bit  | Name  | R/W | Description             | Default           |
|------|-------|-----|-------------------------|-------------------|
| 47:0 | LD_SA | R/W | Loop detection frame SA | 01-80-C2-00-00-01 |

## Page 85h: WAN Interface (Port 5) External PHY MII Registers

**Table 266: WAN Interface (Port 5) External PHY MII Registers**

| Address | Bits | Description                                                                                                                                                                |
|---------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 85h     | –    | MII address from 00h to 0Ah are IEEE standard registers and the descriptions for the registers are <a href="#">“Page 10h–14h: Internal GPHY MII Registers” on page 192</a> |

## Page 88h: IMP Port External PHY MII Registers Page Summary

**Table 267: IMP Port External PHY MII Registers Page Summary**

| Address | Bits | Description                                                                                                                                                                |
|---------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 88h     | –    | MII address from 00h to 0Ah are IEEE standard registers and the descriptions for the registers are <a href="#">“Page 10h–14h: Internal GPHY MII Registers” on page 192</a> |

## Page 91h: Traffic Remarking Register

**Table 268: Traffic Remarking Register**

| Address | Bits | Description                                                                                    |
|---------|------|------------------------------------------------------------------------------------------------|
| 00h–03h | 32   | <a href="#">“Traffic Remarking Control Register (Page 91h: Address 00h)” on page 292</a>       |
| 04h–0Fh | –    | Reserved                                                                                       |
| 10h–57h | 32   | <a href="#">“Egress Packet TC to PCP Mapping Register (Page 91h: Address 10h)” on page 293</a> |
| 58h–EFh | –    | Reserved                                                                                       |
| F0h–F7h | 8    | <a href="#">“SPI Data I/O Register (Global, Address F0h)” on page 294</a> , bytes 0–7          |
| F8h–FDh | –    | Reserved                                                                                       |
| FEh     | 8    | <a href="#">“SPI Status Register (Global, Address FEh)” on page 295</a>                        |
| FFh     | 8    | <a href="#">“Page Register (Global, Address FFh)” on page 295</a>                              |

## Traffic Remarking Control Register (Page 91h: Address 00h)

**Table 269: Traffic Remarking Control Register (Page 91h: Address 00h)**

| Bit   | Name     | R/W | Description | Default |
|-------|----------|-----|-------------|---------|
| 31:25 | Reserved | RO  | Reserved    | 0       |

**Table 269: Traffic Remarking Control Register (Page 91h: Address 00h)**

| Bit   | Name             | R/W | Description                                                                                      | Default |
|-------|------------------|-----|--------------------------------------------------------------------------------------------------|---------|
| 24:16 | PCP_REMARKING_EN | R/W | PCP Remarking Enable<br>Bit 24 = IMP port<br>Bits[21:16] correspond to ports [5:0], respectively | 0       |
| 15:9  | Reserved         | R/W | Reserved                                                                                         | –       |
| 8:0   | CFI_REMARKING_EN | R/W | CFI Remarking Enable<br>Bit 8 = IMP port<br>Bits[5:0] correspond to ports [5:0], respectively    | 0       |

## Egress Packet TC to PCP Mapping Register (Page 91h: Address 10h)

**Table 270: Egress Packet TC to PCP Mapping Register Address Summary**

| Address | Description |
|---------|-------------|
| 10h-17h | Port 0      |
| 18h-1Fh | Port 1      |
| 20h-27h | Port 2      |
| 28h-2Fh | Port 3      |
| 30h-37h | Port 4      |
| 38h-3Fh | Port 5      |
| 40h-47h | Reserved    |
| 48h-4Fh | Reserved    |
| 50h-57h | IMP         |

**Table 271: Egress Packet TC to PCP Mapping Register**  
**(Page 91h: Address 10h–17h, 18h–1Fh, 20h–27h, 28h–2Fh, 30h–37h, 38h–3Fh, 50h–57h)**

| Bit   | Name                 | R/W | Description                    | Default |
|-------|----------------------|-----|--------------------------------|---------|
| 63:60 | Reserved             | R/W | Reserved                       | 4'b1111 |
| 59:56 | Reserved             | R/W | Reserved                       | 4'b1110 |
| 55:52 | Reserved             | R/W | Reserved                       | 4'b1101 |
| 51:48 | Reserved             | R/W | Reserved                       | 4'b1100 |
| 47:44 | Reserved             | R/W | Reserved                       | 4'b1011 |
| 43:40 | Reserved             | R/W | Reserved                       | 4'b1010 |
| 39:36 | Reserved             | R/W | Reserved                       | 4'b1001 |
| 35:32 | Reserved             | R/W | Reserved                       | 4'b1000 |
| 31:28 | {CFI,PCP} for TC = 7 | R/W | The {CFI,PCP} field for TC = 7 | 4'b0111 |
| 27:24 | {CFI,PCP} for TC = 6 | R/W | The {CFI,PCP} field for TC = 6 | 4'b0110 |

**Table 271: Egress Packet TC to PCP Mapping Register**  
**(Page 91h: Address 10h–17h, 18h–1Fh, 20h–27h, 28h–2Fh, 30h–37h, 38h–3Fh, 50h–57h) (Cont.)**

| Bit   | Name                 | R/W | Description                    | Default |
|-------|----------------------|-----|--------------------------------|---------|
| 23:20 | {CFI,PCP} for TC = 5 | R/W | The {CFI,PCP} field for TC = 5 | 4'b0101 |
| 19:16 | {CFI,PCP} for TC = 4 | R/W | The {CFI,PCP} field for TC = 4 | 4'b0100 |
| 15:12 | {CFI,PCP} for TC = 3 | R/W | The {CFI,PCP} field for TC = 3 | 4'b0011 |
| 11:8  | {CFI,PCP} for TC = 2 | R/W | The {CFI,PCP} field for TC = 2 | 4'b0010 |
| 7:4   | {CFI,PCP} for TC = 1 | R/W | The {CFI,PCP} field for TC = 1 | 4'b0001 |
| 3:0   | {CFI,PCP} for TC = 0 | R/W | The {CFI,PCP} field for TC = 0 | 4'b0000 |

## Global Registers

**Table 272: Global Registers (Maps to All Pages)**

| Address | Bits | Description                                                  |
|---------|------|--------------------------------------------------------------|
| F0h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 0 |
| F1h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 1 |
| F2h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 2 |
| F3h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 3 |
| F4h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 4 |
| F5h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 5 |
| F6h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 6 |
| F7h     | 8    | "SPI Data I/O Register (Global, Address F0h)" on page 294, 7 |
| F8–FDh  | —    | Reserved                                                     |
| FEh     | 8    | "SPI Status Register (Global, Address FEh)" on page 295      |
| FFh     | 8    | "Page Register (Global, Address FFh)" on page 295            |

## SPI Data I/O Register (Global, Address F0h)

**Table 273: SPI Data I/O Register (Maps to All Registers, Address F0h–F7h)**

| Bit | Name         | R/W | Description          | Default |
|-----|--------------|-----|----------------------|---------|
| 7:0 | SPI Data I/O | R/W | SPI data bytes [7:0] | 0       |

## SPI Status Register (Global, Address FEh)

**Table 274: SPI Status Register (Maps to All Registers, Address FEh)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                  | <b>Default</b> |
|------------|-------------|------------|-----------------------------------------------------|----------------|
| 7          | SPIF        | RO         | SPI read/write complete flag                        | 0              |
| 6          | Reserved    | RO         | —                                                   | 0              |
| 5          | RACK        | RO<br>(SC) | SPI read data ready acknowledgement (self-clearing) | 0              |
| 4:2        | Reserved    | RO         | —                                                   | 0              |
| 1          | Reserved    | RO         | —                                                   | 0              |
| 0          | Reserved    | RO         | —                                                   | 0              |

## Page Register (Global, Address FFh)

**Table 275: Page Register (Maps to All Registers, Address FFh)**

| <b>Bit</b> | <b>Name</b> | <b>R/W</b> | <b>Description</b>                                                   | <b>Default</b> |
|------------|-------------|------------|----------------------------------------------------------------------|----------------|
| 7:0        | PAGE_REG    | R/W        | The binary value determines the value of the accessed register page. | 0              |

## Section 8: Electrical Characteristics

### Absolute Maximum Ratings

**Table 276: Absolute Maximum Ratings**

| Symbol    | Parameter and Pins                                       | Minimum | Maximum | Units |
|-----------|----------------------------------------------------------|---------|---------|-------|
| –         | Supply voltage: PLL_AVDD, DVDD, AVDDL, SDVDD, SD_PLLAVDD | GND–0.3 | 1.32    | V     |
| –         | Supply voltage: OVDD2, AVDDH, OVDD, OVDD3, SD_PLLAVDD33  | GND–0.3 | 3.63    | V     |
| $I_I$     | Input current                                            | –       | –       | mA    |
| $T_{STG}$ | Storage temperature                                      | –40     | +125    | °C    |
| $V_{ESD}$ | Electrostatic discharge                                  | –       | 1000    | V     |
| –         | Input voltage: digital input pins                        | –       | –       | V     |

**Note:** These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

### Recommended Operating Conditions

**Table 277: Recommended Operating Conditions**

| Symbol   | Parameter                     | Pins                                     | Minimum | Maximum | Units |
|----------|-------------------------------|------------------------------------------|---------|---------|-------|
| VDD      | Supply voltage                | AVDDL, DVDD, PLL_AVDD, SDVDD, SD_PLLAVDD | 1.14    | 1.26    | V     |
|          |                               | OVDD2, AVDDH, SD_PLLAVDD33               | 3.14    | 3.47    | V     |
|          |                               | OVDD, OVDD3 (RGMII mode)                 | 2.38    | 2.63    | V     |
|          |                               | OVDD, OVDD3 (GMII/RvMII mode)            | 3.14    | 3.47    | V     |
| $V_{IH}$ | High-level input voltage      | All digital inputs                       | 2.0     | –       | V     |
| $V_{IL}$ | Low-level input voltage       | All digital inputs                       | –       | 0.8     | V     |
| $T_A$    | Ambient operating temperature | –                                        | 0       | 70      | °C    |

## Electrical Characteristics

**Table 278: Electrical Characteristics**

| Symbol     | Parameter                                                    | Pins                                    | Conditions                                                   | Minimum | Typical | Maximum   | Units         |
|------------|--------------------------------------------------------------|-----------------------------------------|--------------------------------------------------------------|---------|---------|-----------|---------------|
| $I_{DD}$   | Maximum supply current (for GMII/RvMII/MII operation)        | 1.2V power rail                         | —                                                            | —       | 952     | —         | mA            |
|            |                                                              | 3.3V power rail                         | —                                                            | —       | 332     | —         | mA            |
|            |                                                              | OVDD (3.3V for GMII/RvMII/MII)          | —                                                            | —       | 27      | —         | mA            |
| $I_{DD}$   | Maximum supply current (for RGMII operation)                 | 1.2V power rail                         | —                                                            | —       | 952     | —         | mA            |
|            |                                                              | 3.3V power rail                         | —                                                            | —       | 332     | —         | mA            |
|            |                                                              | OVDD (2.5V for RGMII)                   | —                                                            | —       | 29      | —         | mA            |
| $V_{OH}^*$ | High-level output voltage                                    | Digital output pins                     | $I_{OH} = -8\text{ mA}$<br>$I_{OH} = -16\text{ mA}$          | 2.4     | —       | —         | V             |
| $V_{OL}$   | Low-level output voltage                                     | Digital output pins                     | $I_{OL} = +8\text{ mA}$<br>$I_{OL} = +16\text{ mA}$          | —       | —       | 0.4       | V             |
| $V_{IH}$   | High-level input voltage                                     | Digital input pins                      | —                                                            | 2.0     | —       | —         | V             |
|            |                                                              | XTALI                                   | —                                                            | 2.0     | —       | —         | V             |
| $V_{IL}$   | Low-level input voltage                                      | Digital input pins                      | —                                                            | -0.3    | —       | 0.8       | V             |
|            |                                                              | XTALI                                   | —                                                            | -0.3    | —       | 0.8       | V             |
| $I_I$      | Input current                                                | Digital inputs with pull-up resistors   | $V_I = OVDD2$                                                | —       | —       | +100      | $\mu\text{A}$ |
|            |                                                              | Digital inputs with pull-up resistors   | $V_I = \text{GND}$                                           | —       | —       | -10       | $\mu\text{A}$ |
|            |                                                              | Digital inputs with pull-down resistors | $V_I = OVDD2$                                                | —       | —       | +100      | $\mu\text{A}$ |
|            |                                                              | Digital inputs with pull-down resistors | $V_I = \text{GND}$                                           | —       | —       | +10       | $\mu\text{A}$ |
|            |                                                              | All other digital inputs                | $\text{GND} \leq V_I \leq \text{OVDD2}$                      | —       | —       | $\pm 100$ | $\mu\text{A}$ |
| $V_{ID}$   | Receiver Input Voltage Differential Peak-to-Peak, AC-Coupled | SerDes input pins                       | The receiver differential pair has built-in AC coupling caps | 100     | —       | 2000      | mV            |
| $R_{IN}$   | Receiver Input Impedance                                     | SerDes input pins                       | Differential, integrated on-chip                             | 80      | 100     | 120       | $\Omega$      |
| $V_{OD}$   | Transmitter Output Voltage Differential Peak-to-Peak         | SerDes output pins                      | Programmable                                                 | —       | 700     | 1100      | mV            |

**Table 278: Electrical Characteristics (Cont.)**

| <b>Symbol</b>  | <b>Parameter</b>             | <b>Pins</b>        | <b>Conditions</b> | <b>Minimum</b> | <b>Typical</b> | <b>Maximum</b> | <b>Units</b> |
|----------------|------------------------------|--------------------|-------------------|----------------|----------------|----------------|--------------|
| R <sub>O</sub> | Transmitter Output Impedance | SerDes output pins | Differential      | 80             | 100            | 120            | Ω            |

**Note:** For RGMII digital output pins, VOH minimum is 2.0V.

# Section 9: Timing Characteristics

## Reset and Clock Timing

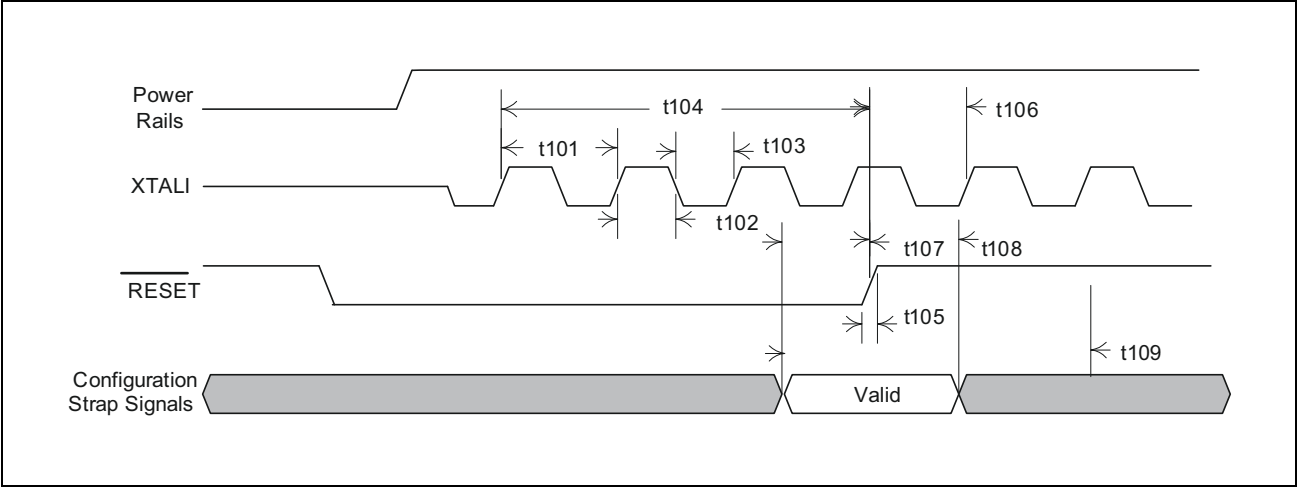


Figure 47: Reset and Clock Timing

Table 279: Reset and Clock Timing

| Description                                                                                                             | Parameter | Minimum                               | Typical | Maximum   |
|-------------------------------------------------------------------------------------------------------------------------|-----------|---------------------------------------|---------|-----------|
| XTALI period                                                                                                            | t101      | 39.998 ns                             | 40 ns   | 40.002 ns |
| XTALI high time                                                                                                         | t102      | 18 ns                                 | –       | 22 ns     |
| XTALI low time                                                                                                          | t103      | 18 ns                                 | –       | 22 ns     |
| RESET low pulse duration                                                                                                | t104      | 20 ms                                 | 80 ms   | –         |
| RESET rise time                                                                                                         | t105      | –                                     | –       | 25 ns     |
| Configuration valid setup to RESET rising                                                                               | t107      | 100 ns                                | –       | –         |
| Configuration valid hold from RESET rising                                                                              | t108      | –                                     | –       | 0 ns      |
| Hardware initialization is complete.<br>All strap pin values are clocked in and the internal registers can be accessed. | t109      | 5 ms before registers can be accessed |         |           |

# MII Interface Timing

The following specifies timing information regarding the MII Interface pins.

## MII Input Timing

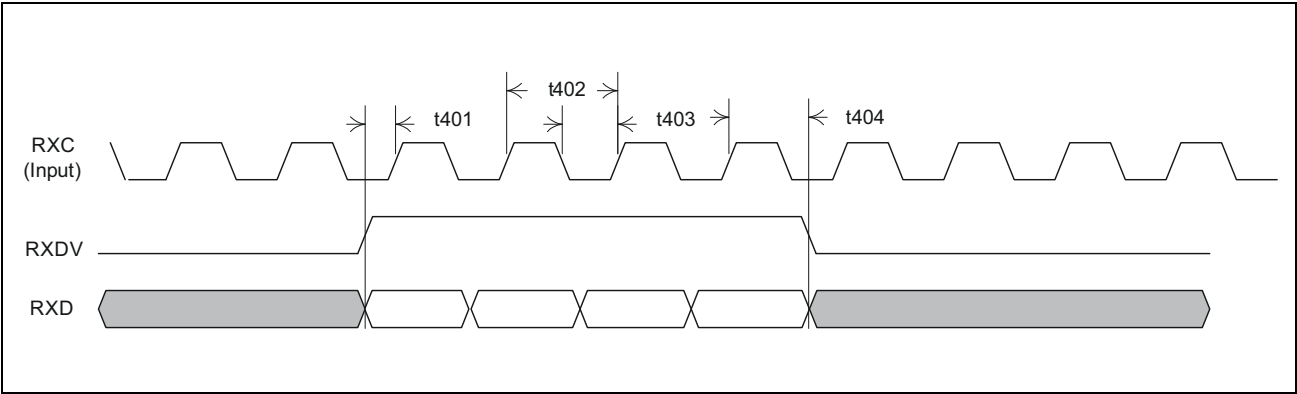


Figure 48: MII Input

Table 280: MII Input Timing

| Parameter | Description                         | Minimum | Typical | Maximum |
|-----------|-------------------------------------|---------|---------|---------|
| t401      | RXDV, RXD to RXC rising setup time  | 10 ns   | –       | –       |
| t402      | RXC clock period (10BASE-T mode)    | –       | 400 ns  | –       |
|           | RXC clock period (100BASE-TX mode)  | –       | 40 ns   | –       |
| t403      | RXC high/low time (10BASE-T mode)   | 160 ns  | –       | 240 ns  |
|           | RXC high/low time (100BASE-TX mode) | 16 ns   | –       | 24 ns   |
| t404      | RXDV, RXD to RXC rising hold time   | 10 ns   | –       | –       |
| –         | Duty cycle                          | –       | –       | –       |

MII Output Timing

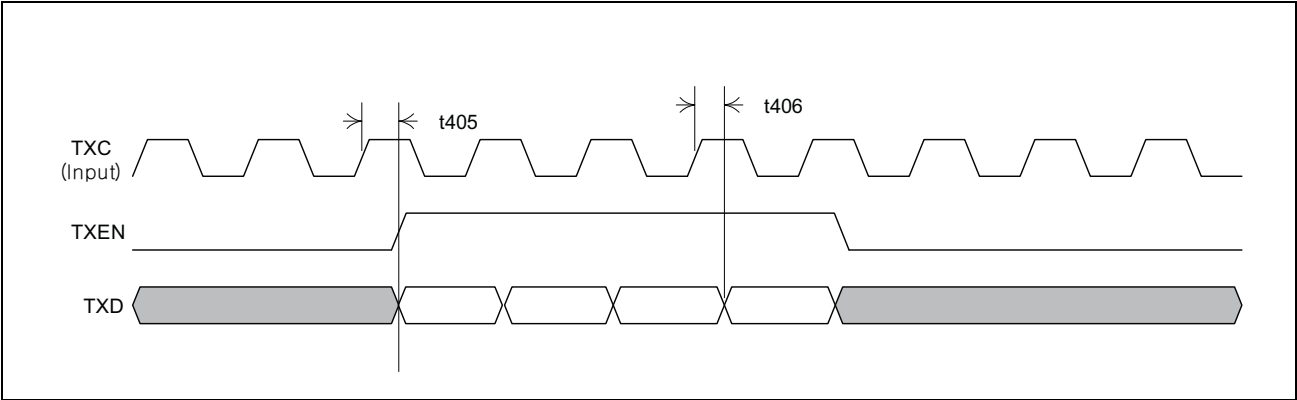


Figure 49: MII Output Timing

Table 281: MII Output Timing

| Parameter | Description                          | Minimum | Typical | Maximum |
|-----------|--------------------------------------|---------|---------|---------|
| t405      | TXC high to TXEN, TXD valid          | 0 ns    | –       | 25 ns   |
| t406      | TXC high to TXEN, TXD invalid (hold) | 0 ns    | –       | –       |

# TMII Interface Timing

## TMII Input Timing

The following specifies timing information regarding the TMII Interface pins.

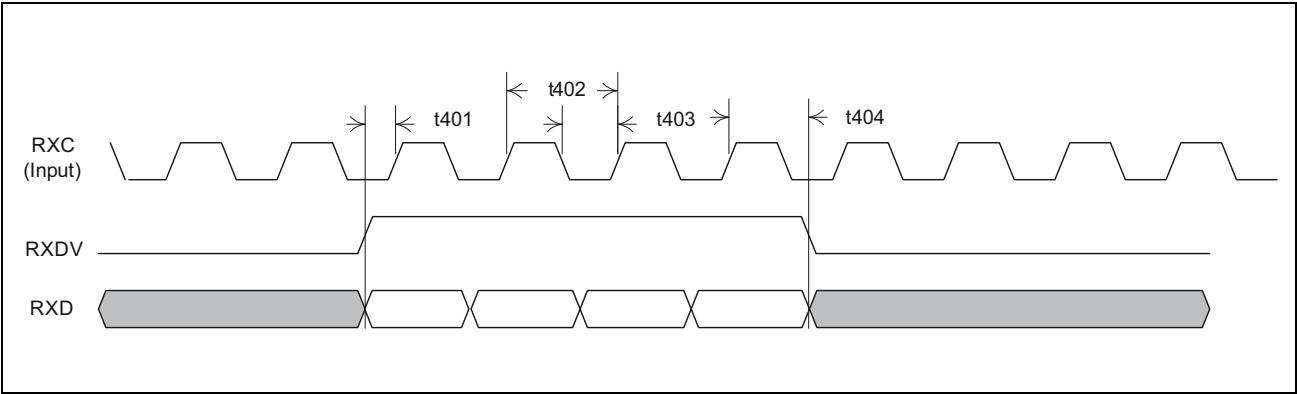


Figure 50: TMII Input

Table 282: TMII Input Timing

| Parameter | Description                         | Minimum | Typical | Maximum |
|-----------|-------------------------------------|---------|---------|---------|
| t401      | RXDV, RXD to RXC rising setup time  | 5 ns    | –       | –       |
| t402      | RXC clock period (100BASE-TX mode)  | –       | 20 ns   | –       |
| t403      | RXC high/low time (100BASE-TX mode) | 8 ns    | –       | 12 ns   |
| t404      | RXDV, RXD to RXC rising hold time   | 8 ns    | –       | –       |
| –         | Duty cycle                          | –       | –       | –       |

TMII Output Timing

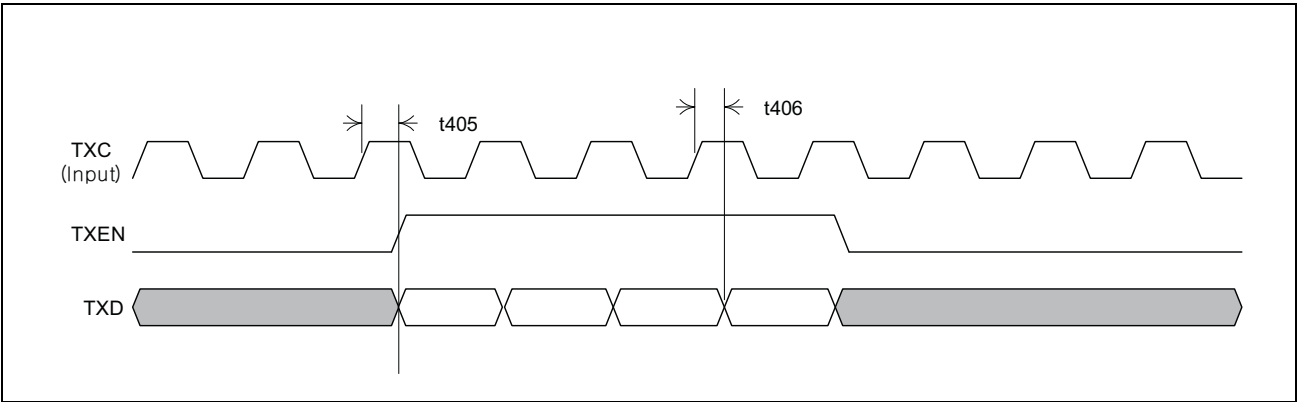


Figure 51: TMII Output Timing

Table 283: TMII Output Timing

| Parameter | Description                          | Minimum | Typical | Maximum |
|-----------|--------------------------------------|---------|---------|---------|
| t405      | TXC high to TXEN, TXD valid          | 0 ns    | –       | 12.5 ns |
| t406      | TXC high to TXEN, TXD invalid (hold) | 0 ns    | –       | –       |

# Reverse MII Interface Timing

The following specifies timing information regarding the Reverse MII Interface pins.

## Reverse MII Input Timing

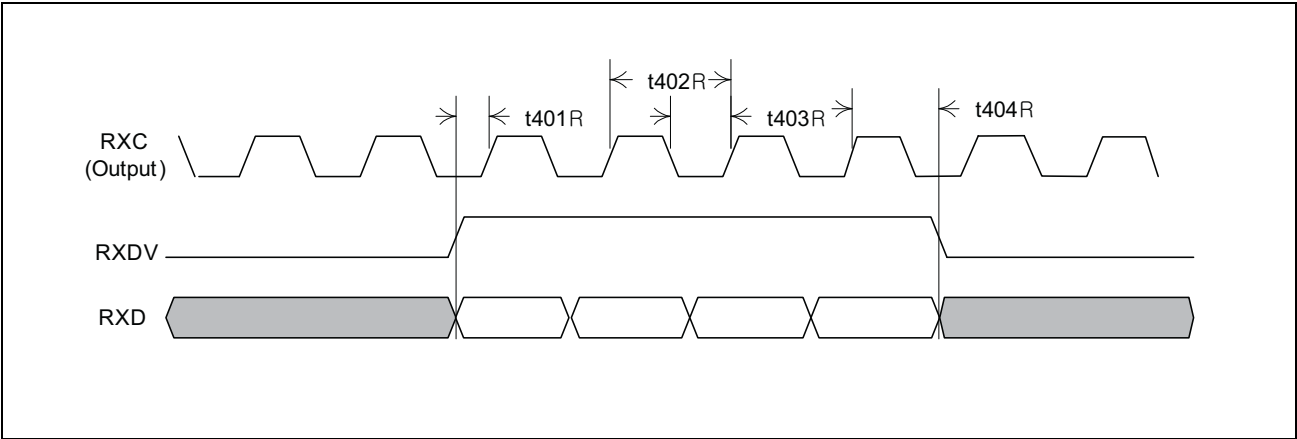


Figure 52: Reverse MII Input Timing

Table 284: Reverse MII Input Timing

| Description                               | Parameter | Minimum | Typical | Maximum | Units |
|-------------------------------------------|-----------|---------|---------|---------|-------|
| RXDV, RXD to RXC rising setup time        | t401R     | 10      | –       | –       | ns    |
| RXC (output) clock period (10BASE-T mode) | t402R     | –       | 400     | –       | ns    |
| RXC clock period (100BASE-TX mode)        |           | –       | 40      | –       | ns    |
| RXC high/low time (10BASE-T mode)         | t403R     | 160     | –       | 240     | ns    |
| RXC high/low time (100BASE-TX mode)       |           | 16      | –       | 24      | ns    |
| RXDV, RXD to RXC rising hold time         | t404R     | 0       | –       | –       | ns    |

Reverse MII Output Timing

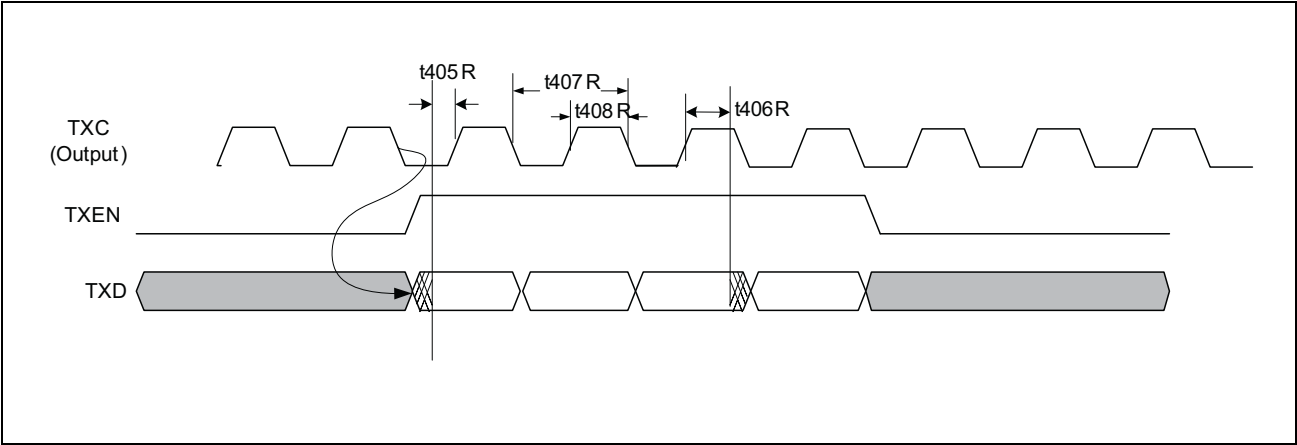


Figure 53: Reverse MII Output Timing

Table 285: Reverse MII Output Timing

| Description                              | Parameter | Minimum | Typical | Maximum | Units |
|------------------------------------------|-----------|---------|---------|---------|-------|
| Output (TXD, TX_EN) setup to TXC rising  | t405R     | 15      | –       | 25      | ns    |
| Output (TXD, TX_EN) hold from TXC rising | t406R     | 11      | –       | –       | ns    |
| TXC clock period                         | t407R     | –       | 40      | –       | ns    |
| TXC high/low time                        | t408R     | 15      | –       | 22      | ns    |

# RGMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in RGMII mode.

## RGMII Output Timing (Normal Mode)

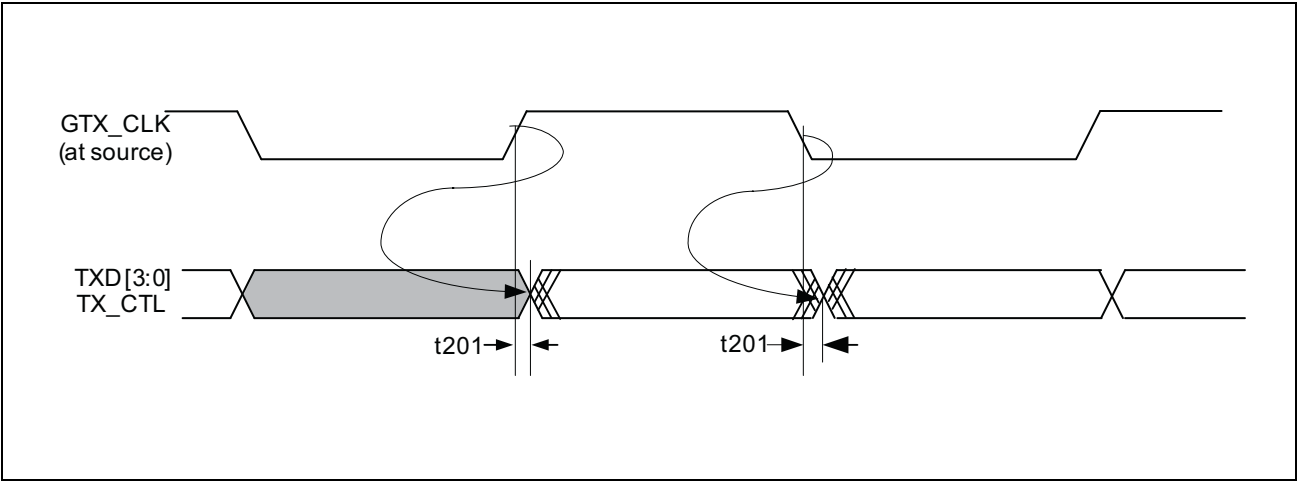


Figure 54: RGMII Output Timing (Normal Mode)

Table 286: RGMII Output Timing (Normal Mode)

| Description                       | Parameter | Minimum      | Typical | Maximum      | Units |
|-----------------------------------|-----------|--------------|---------|--------------|-------|
| GTX_CLK clock period (1000M mode) | –         | 7.2          | 8       | 8.8          | ns    |
| GTX_CLK clock period (100M mode)  | –         | 36           | 40      | 44           | ns    |
| GTX_CLK clock period (10M mode)   | –         | 360          | 400     | 440          | ns    |
| TskewT: data to clock output skew | t201      | –500 (1000M) | 0       | +500 (1000M) | ps    |
| Duty cycle for 1000M (GE)         | –         | 45           | 50      | 55           | %     |
| Duty cycle for 10/100M (FE)       | –         | 40           | 50      | 60           | %     |

 **Note:** The output timing in 10/100M operation is always as specified in the delayed mode.

## RGMII Output Timing (Delayed Mode)

RGMII output timing defaults to the delayed mode when the TXC\_DELAY pin is pulled high at power-on reset.

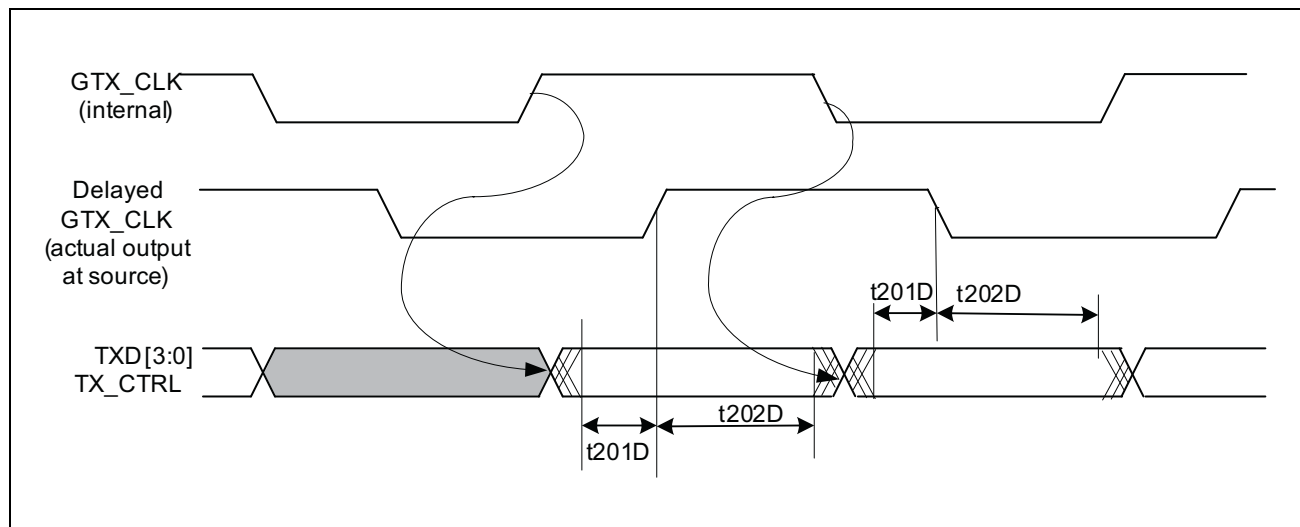


Figure 55: RGMII Output Timing (Delayed Mode)

Table 287: RGMII Output Timing (Delayed Mode)

| Description                                                                                               | Parameter | Minimum             | Typical | Maximum | Units |
|-----------------------------------------------------------------------------------------------------------|-----------|---------------------|---------|---------|-------|
| GTX_CLK clock period (1000M mode)                                                                         | –         | 7.2                 | 8       | 8.8     | ns    |
| GTX_CLK clock period (100M mode)                                                                          | –         | 36                  | 40      | 44      | ns    |
| GTX_CLK clock period (10M mode)                                                                           | –         | 360                 | 400     | 440     | ns    |
| TsetupT<br>Data valid to clock transition:<br>Available setup time at the output<br>source (delayed mode) | t201D     | 1.2 (all<br>speeds) | 2.0     | –       | ns    |
| TholdT<br>Clock transition to data valid:<br>Available hold time at the output<br>source (delayed mode)   | t202D     | 1.2                 | 2.0     | –       | ns    |
| Duty cycle for 1000M (GE)                                                                                 | –         | 45                  | 50      | 55      | %     |
| Duty cycle for 10/100M (FE)                                                                               | –         | 40                  | 50      | 60      | %     |

## RGMI Input Timing (Normal Mode)

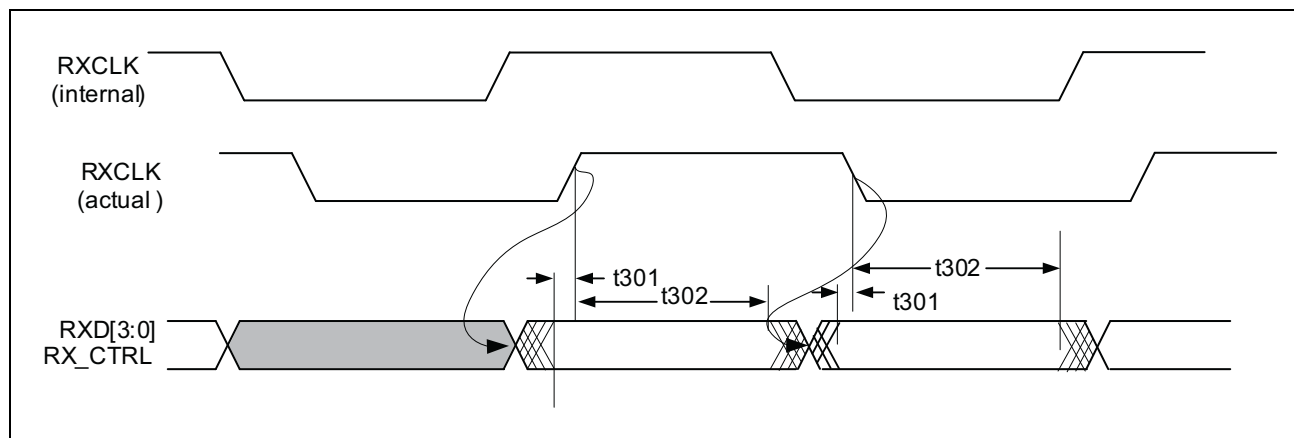


Figure 56: RGMI Input Timing (Normal Mode)

Table 288: RGMI Input Timing (Normal Mode)

| Description                                      | Parameter | Minimum | Typical | Maximum | Units |
|--------------------------------------------------|-----------|---------|---------|---------|-------|
| RXCLK clock period (1000M mode)                  | —         | 7.2     | 8       | 8.8     | ns    |
| RXCLK clock period (100M mode)                   | —         | 36      | 40      | 44      | ns    |
| RXCLK clock period (10M mode)                    | —         | 360     | 400     | 440     | ns    |
| TsetupR<br>Input setup time: valid data to clock | t301      | 1.0     | 2.0     | —       | ns    |
| TholdR<br>Input hold time: clock to valid data   | t302      | 1.0     | 2.0     | —       | ns    |
| Duty cycle for 1000M (GE)                        | —         | 45      | 50      | 55      | %     |
| Duty cycle for 10/100M (FE)                      | —         | 40      | 50      | 60      | %     |

RGMII Input Timing (Delayed Mode)

RGMII Input Timing defaults to the delayed mode when the RXC\_DELAY pin is pulled high at power-on reset.

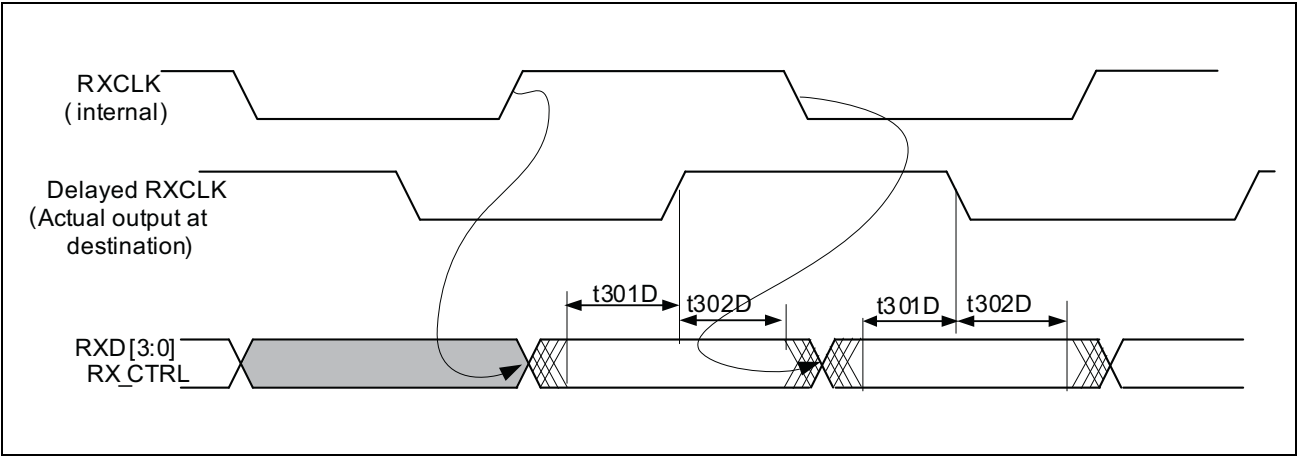


Figure 57: RGMII Input Timing (Delayed Mode)

Table 289: RGMII Input Timing (Delayed Mode)

| Description                     | Parameter | Minimum        | Typical | Maximum | Units |
|---------------------------------|-----------|----------------|---------|---------|-------|
| TsetupR                         | t301D     | −1.0 (1000M)   | –       | –       | ns    |
| Input setup time (delayed mode) |           | −1.0 (10/100M) | –       | –       | ns    |
| TholdR                          | t302D     | 3.0 (1000M)    | –       | –       | ns    |
| Input hold time (delayed mode)  |           | 9.0 (10/100M)  | –       | –       | ns    |

# GMII Interface Timing

The following specifies timing information regarding the IMP interface pins when configured in GMII mode.

## GMII Interface Output Timing

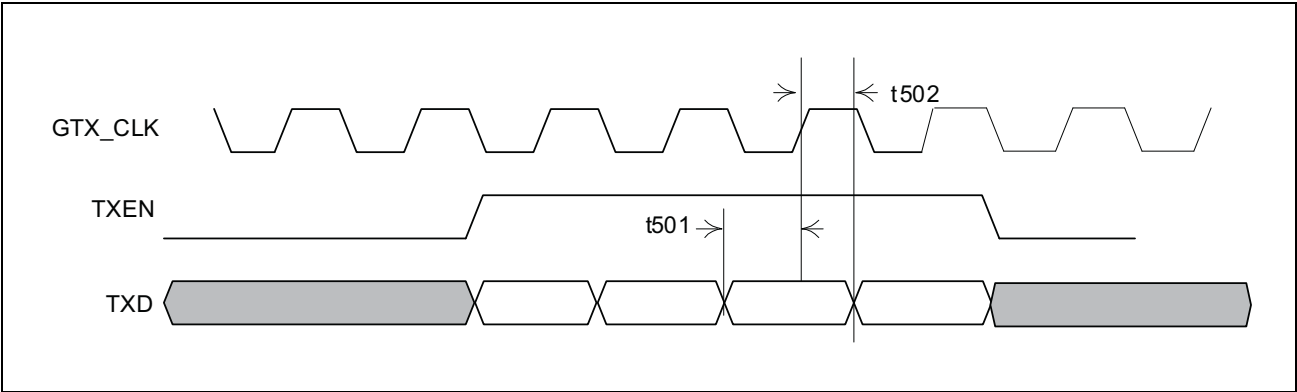


Figure 58: GMII Output Timings

Table 290: GMII Output Timing

| Description                                  | Parameter | Minimum | Typical | Maximum | Units |
|----------------------------------------------|-----------|---------|---------|---------|-------|
| GTX_CLK clock period (1000M mode)            | –         | 7.5     | 8       | 8.5     | ns    |
| Output (TXD, TX_EN) setup to GTX_CLK rising  | t501      | 2.5     | –       | –       | ns    |
| Output (TXD, TX_EN) hold from GTX_CLK rising | t502      | 0.5     | –       | 5.5     | ns    |
| Duty cycle for 1000M (GE)                    | –         | 45      | 50      | 55      | %     |
| Duty cycle for 10/100M (FE)                  | –         | 40      | 50      | 60      | %     |

GMII Interface Input Timing

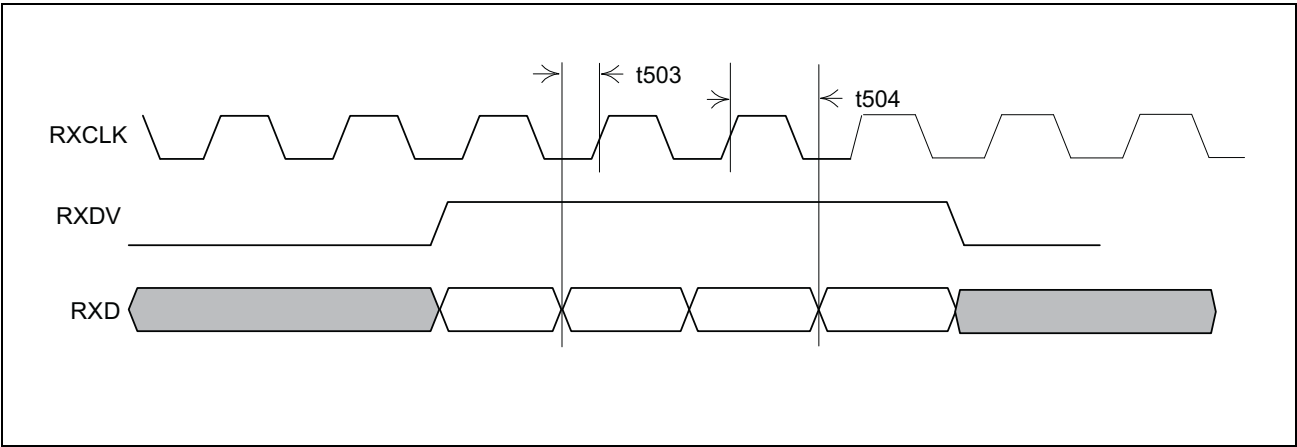


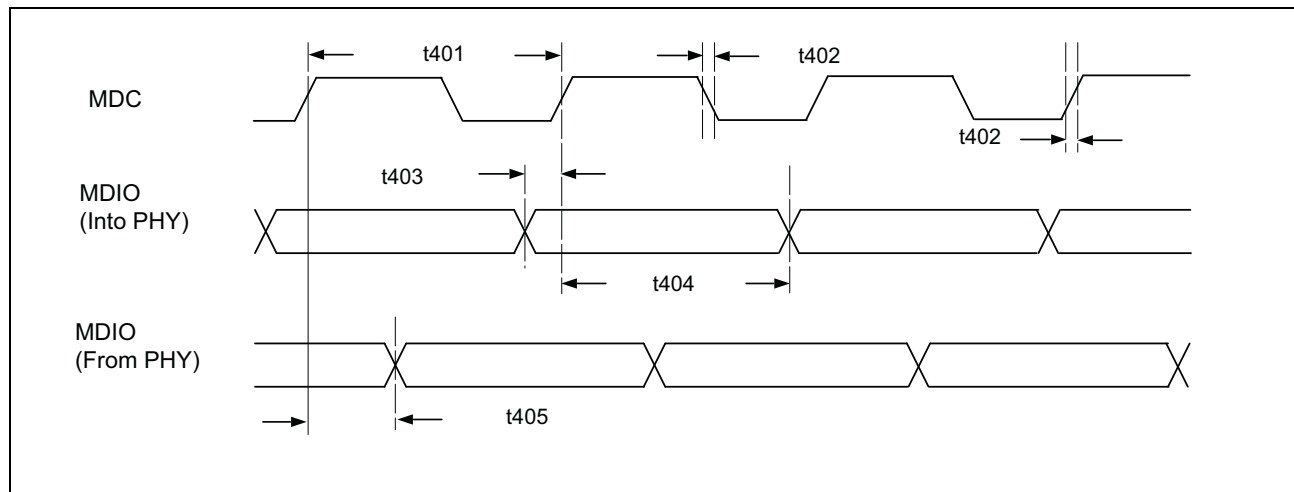
Figure 59: GMII Input Timings

Table 291: GMII Input Timing

| Description                        | Parameter | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------|---------|---------|---------|-------|
| RXCLK clock period (1000M mode)    | –         | –       | 8       | –       | ns    |
| RXD, RX_DV Setup to RX_CLK rising  | t503      | 2.0     | –       | –       | ns    |
| RXD, RX_DV Hold from RX_CLK rising | t504      | 0.0     | –       | –       | ns    |

## MDC/MDIO Timing

The following specifies timing information regarding the MDC/MDIO interface pins.



**Figure 60: MDC/MDIO Timing (Slave Mode)**

**Table 292: MDC/MDIO Timing (Slave Mode)**

| Description                          | Parameter | Minimum | Typical | Maximum | Units |
|--------------------------------------|-----------|---------|---------|---------|-------|
| MDC cycle time                       | t401      | 80      | —       | —       | ns    |
| MDC high/low                         | —         | 30      | —       | —       | ns    |
| MDC rise/fall time                   | t402      | —       | —       | 10      | ns    |
| MDIO input setup time to MDC rising  | t403      | 7.5     | —       | —       | ns    |
| MDIO input hold time from MDC rising | t404      | 7.5     | —       | —       | ns    |
| MDIO output delay from MDC rising    | t405      | 0       | —       | 45      | ns    |

**Table 293: MDC/MDIO Timing (Master Mode)**

| Description                          | Parameter | Minimum | Typical | Maximum | Units |
|--------------------------------------|-----------|---------|---------|---------|-------|
| MDC cycle time                       | t401      | 400     | —       | —       | ns    |
| MDC high/low                         | —         | 160     | —       | 240     | ns    |
| MDC rise/fall time                   | t402      | —       | —       | 10      | ns    |
| MDIO input setup time to MDC rising  | t403      | 20      | —       | —       | ns    |
| MDIO input hold time from MDC rising | t404      | 0       | —       | —       | ns    |
| MDIO output delay from MDC rising    | t405      | 15      | —       | 90      | ns    |

# Serial LED Interface Timing

The following specifies timing information regarding the LED interface pins.

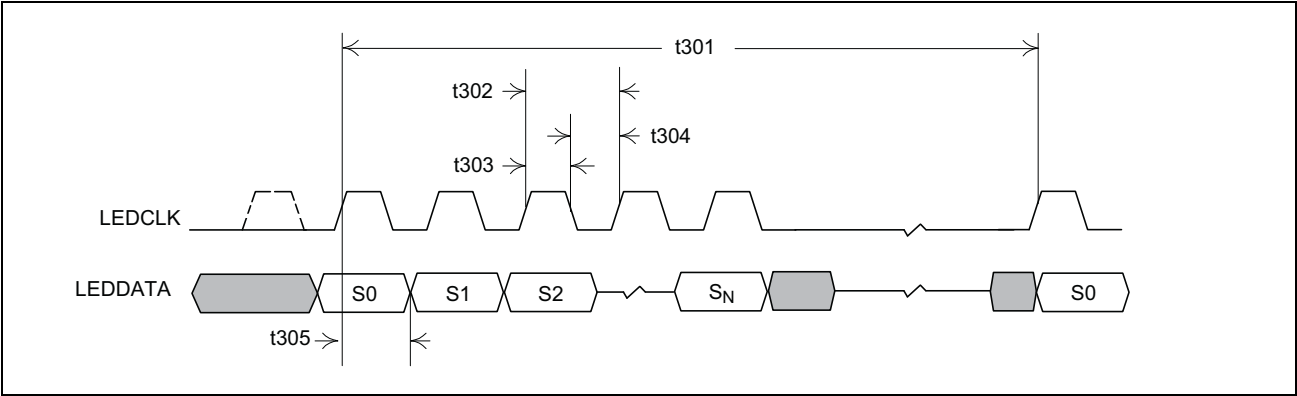


Figure 61: Serial LED Interface Timing

Table 294: Serial LED Interface Timing

| Description                   | Parameter | Minimum | Typical | Maximum | Units |
|-------------------------------|-----------|---------|---------|---------|-------|
| LED update cycle period       | t301      | –       | 42      | –       | ms    |
| LEDCLK period                 | t302      | –       | 320     | –       | ns    |
| LEDCLK high-pulse width       | t303      | 150     | –       | 170     | ns    |
| LEDCLK low-pulse width        | t304      | 150     | –       | 170     | ns    |
| LEDCLK to LEDDATA output time | t305      | 140     | –       | 180     | ns    |

## SPI Timings

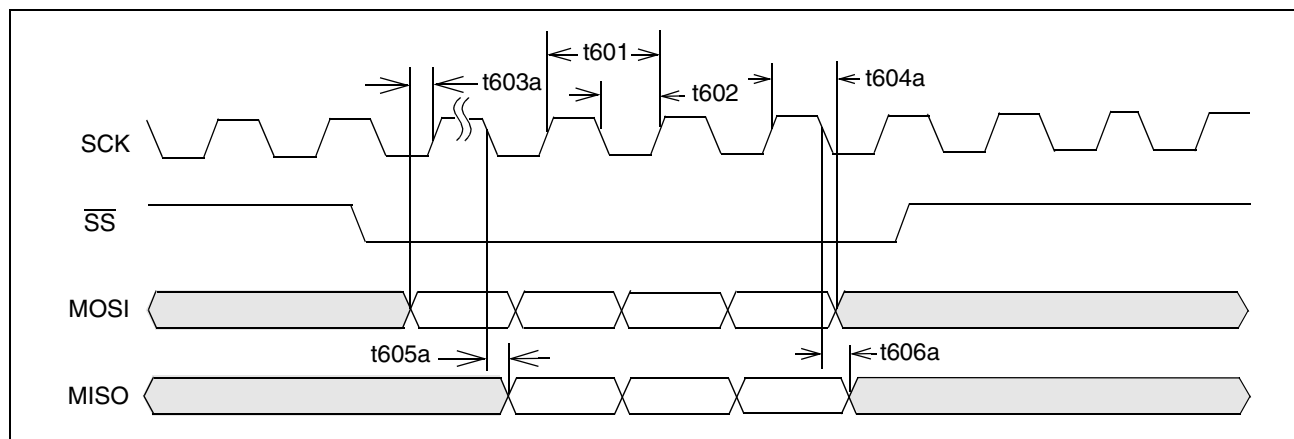


Figure 62: SPI Timings,  $\overline{SS}$  Asserted During SCK High

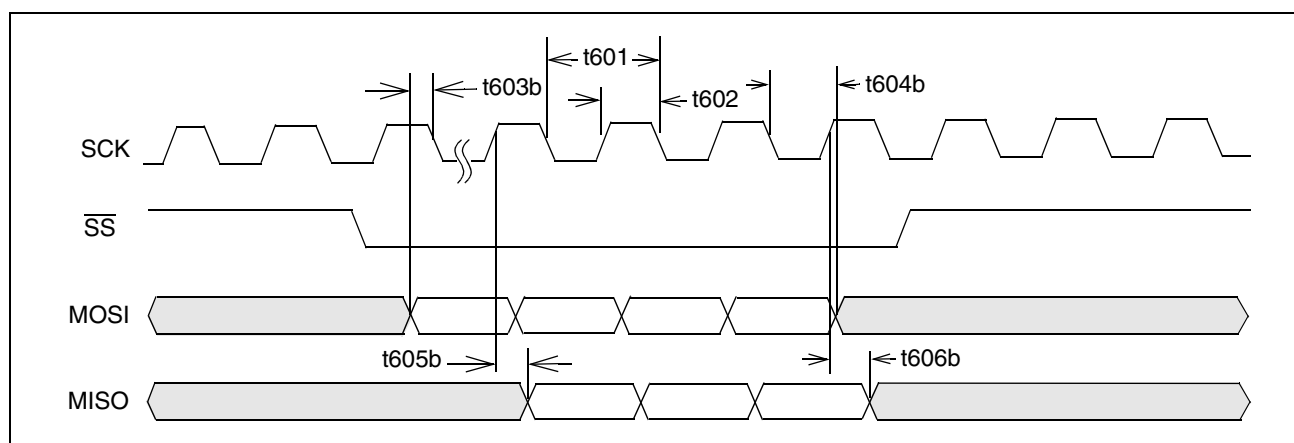


Figure 63: SPI Timings,  $\overline{SS}$  Asserted During SCK Low

Table 295: SPI Timings

| Description            | Parameter    | Minimum | Typical | Maximum |
|------------------------|--------------|---------|---------|---------|
| SCK clock period       | t601         | –       | 500 ns  | –       |
| SCK high/low time      | t602         | 200 ns  | –       | 300 ns  |
| MOSI to SCK setup time | t603a, t603b | 5 ns    | –       | –       |
| MOSI to SCK hold time  | t604a, t604b | 12 ns   | –       | –       |
| SCK to MISO valid      | t605a, t605b | –       | –       | 25 ns   |
| SCK to MISO invalid    | t606a, t606b | 0 ns    | –       | –       |



**Note:** BCM53115S behaves only as slave devices.  $\overline{SS}$  is asynchronous. If  $\overline{SS}$  is asserted during SCK high, then the BCM53115S samples data on the rising edge of SCK and references the falling edge to output data. Otherwise, the BCM53115S samples data on the falling edge and outputs data on the rising edge of SCK.

EEPROM Timing

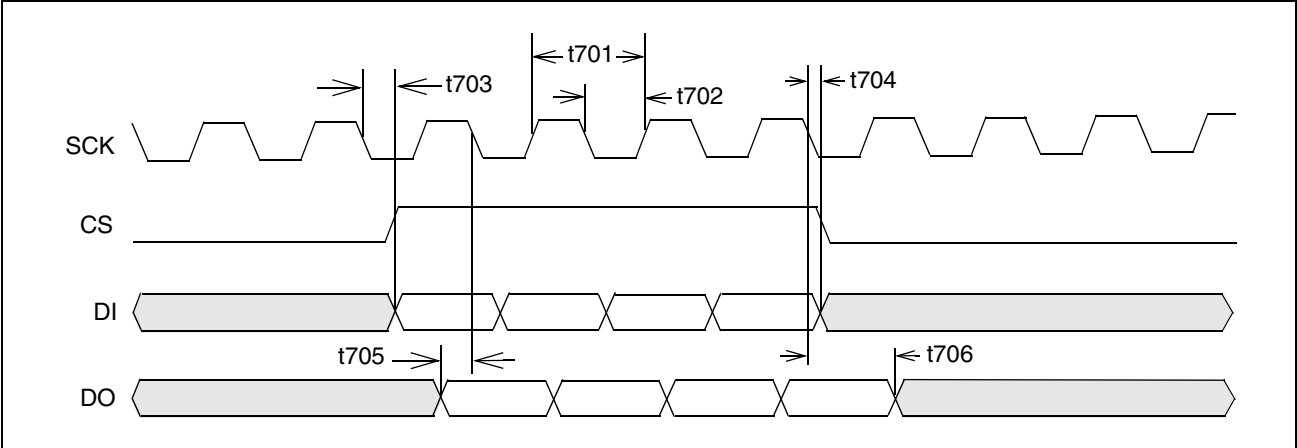


Figure 64: EEPROM Timing

Table 296: EEPROM Timing

| Description                  | Parameter | Minimum | Typical   | Maximum |
|------------------------------|-----------|---------|-----------|---------|
| SCK clock frequency          | t701      | –       | 100 kHz   | –       |
| SCK high/low time            | t702      | –       | 5 $\mu$ s | –       |
| SCK low to CS, DI valid      | t703      | –       | –         | 500 ns  |
| SCK low to CS, DI invalid    | t704      | 500 ns  | –         | –       |
| DO to SCK falling setup time | t705      | 200 ns  | –         | –       |
| DO to SCK falling hold time  | t706      | 200 ns  | –         | –       |

## Section 10: Thermal Characteristics

**Table 297: BCM53115SKFB Package with Heat Sink<sup>a</sup>**

| <b>AirFlow</b>               | <b>0 fpm, 0 mps</b> | <b>100 fpm,<br/>0.508 mps</b> | <b>200 fpm,<br/>1.016 mps</b> | <b>400 fpm,<br/>2.032 mps</b> | <b>600 fpm,<br/>3.048 mps</b> |
|------------------------------|---------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|
| Theta-JA (°C/W)              | 19.57               | 14.96                         | 13.39                         | 12.55                         | 12.22                         |
| Theta-JB (°C/W)              | 8.98                | —                             | —                             | —                             | —                             |
| Theta-JC (°C/W)              | 9.67                | —                             | —                             | —                             | —                             |
| ψT (°C/W)                    | 7.46                | 7.97                          | 8.16                          | 8.24                          | 8.26                          |
| Maximum junction temperature | 125                 | —                             | —                             | —                             | —                             |

a. With heat sink, Ta = 70°C. This is an estimation based on 4-layer PCB and P = 2.6W.  
Heat sink: 35 mm x 35 mm x 15 mm extruded Al, k = 180 (W/m x K).  
Thermal Interface: 0.23 Mm thick tape, k = 0.277 (W/m x K)

**Table 298: BCM53115SIPB Package with Heat Sink<sup>a</sup>**

| <b>AirFlow</b>               | <b>0 fpm, 0 mps</b> | <b>100 fpm,<br/>0.508 mps</b> | <b>200 fpm,<br/>1.016 mps</b> | <b>400 fpm,<br/>2.032 mps</b> | <b>600 fpm,<br/>3.048 mps</b> |
|------------------------------|---------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|
| Theta-JA (°C/W)              | 17.37               | 14.56                         | 13.79                         | 13.20                         | 12.93                         |
| Theta-JB (°C/W)              | 11.55               | —                             | —                             | —                             | —                             |
| Theta-JC (°C/W)              | 10.20               | —                             | —                             | —                             | —                             |
| ψT (°C/W)                    | 8.95                | 9.17                          | 9.23                          | 9.27                          | 9.28                          |
| Maximum junction temperature | —                   | 125                           | —                             | —                             | —                             |

a. With Heat sink, Ta = 85°C. This is an estimation based on 4-layer PCB and P=2.6W.  
Heat sink: 35 mm x 35 mm x 15 mm, k = 180 (W/m x K), blade-fin.  
Thermal Interface: 19.5 mm x 19.5 mm x 0.37 mm, k = 1.3 (W/m x K)

Section 11: Mechanical Information

Package Dimensions

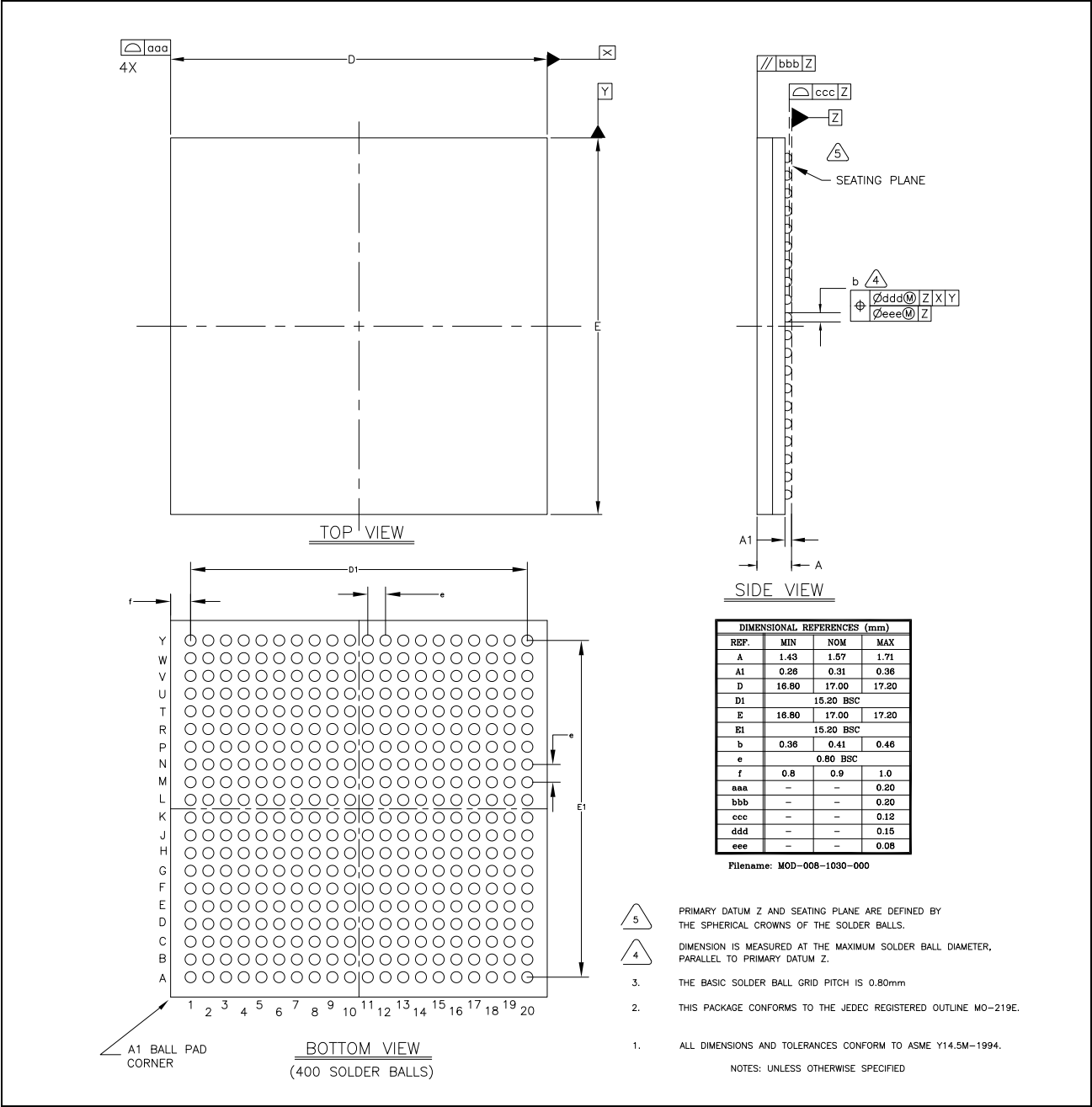


Figure 65: 400-Pin Packaging Diagram

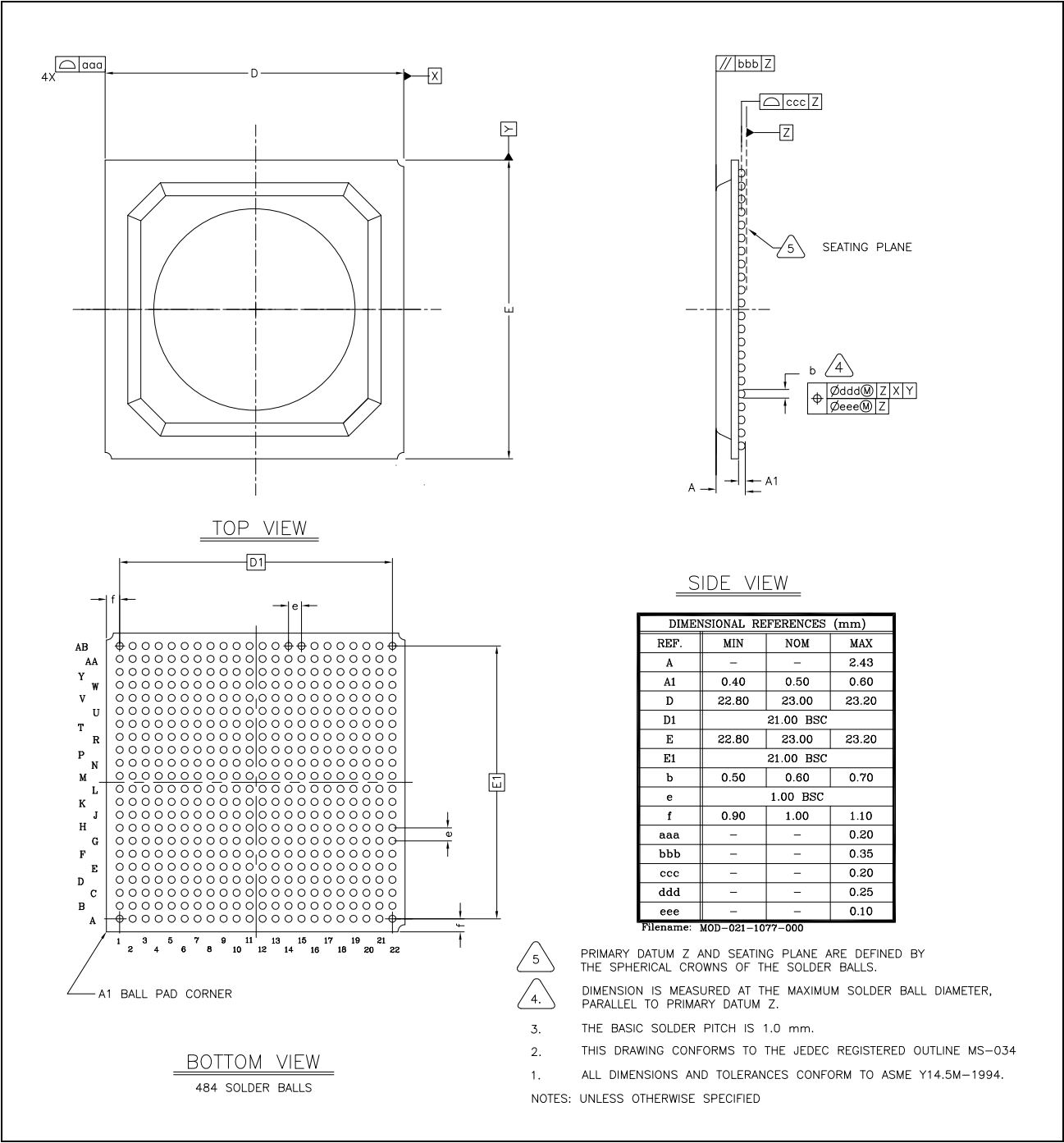
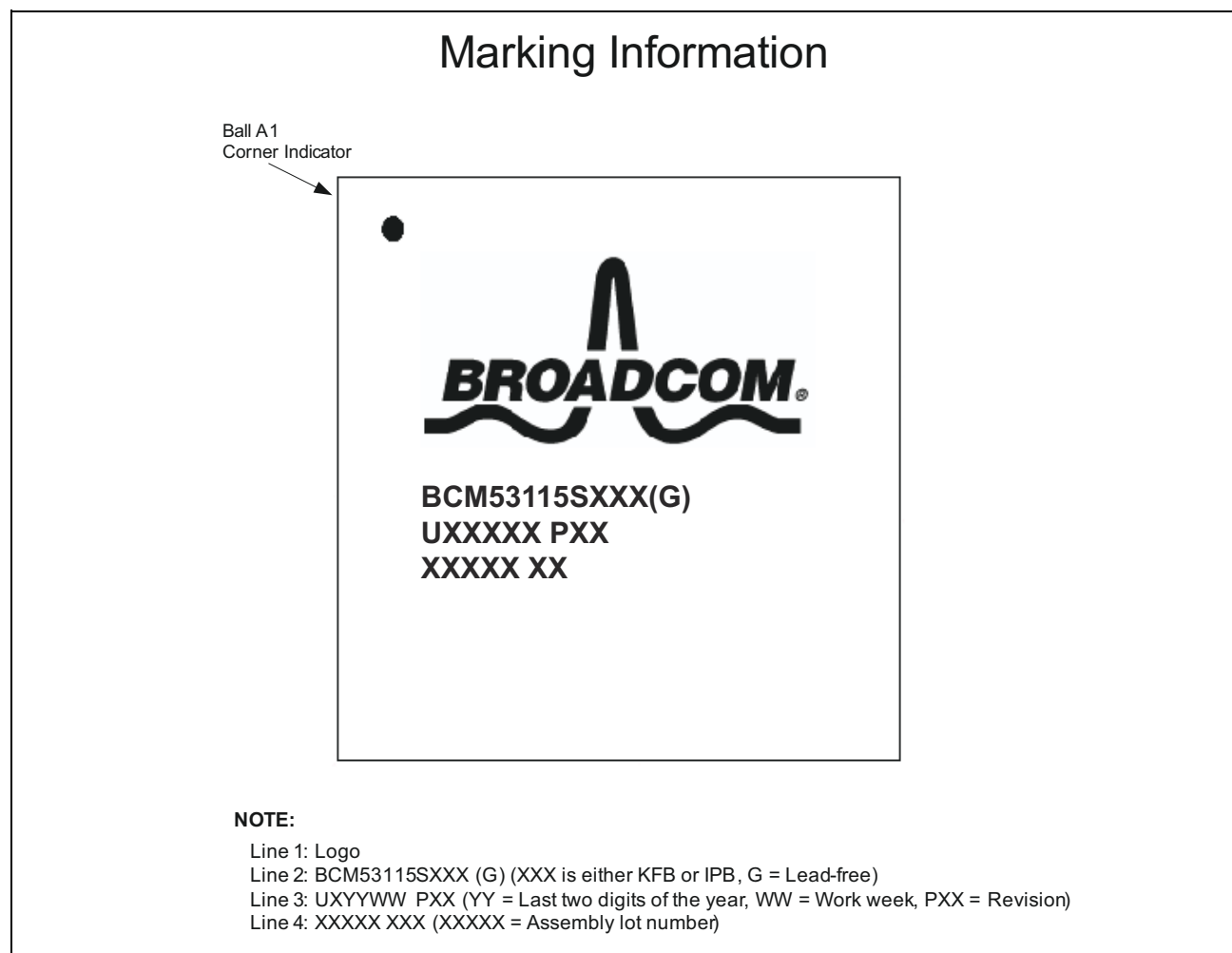


Figure 66: 484-Pin Packaging Diagram

## Marking Information



**Figure 67: Marking Information**

## Section 12: Ordering Information

| <i><b>Part Number</b></i> | <i><b>Package</b></i> | <i><b>Ambient Temperature</b></i> |
|---------------------------|-----------------------|-----------------------------------|
| BCM53115SKFB(G)           | 400 FBGA              | 0°C to 70°C                       |
| BCM53115SIPB(G)           | 484 PBGA              | –40°C to 85°C                     |
| BCM53115SKPB(G)           | 484 PBGA              | 0°C to 70°C                       |



**Note:** (G) represents the lead-free package option.

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