Preliminary Data Sheet

BCM56780

8.0-Tb/s Compiler-Programmable Multilayer Switch

Overview

The Broadcom® BCM56780 family is a class of high-performance, non-blocking network switching devices supporting compiler-based programmability of forwarding and instrumentation functions. The device family features up to 160 lanes of 50G PAM4 SerDes. Port speeds of 10, 25, 40, 50, 100, 200, and 400GbE can be simultaneously supported without the need for external PHYs. The BCM56780 delivers high bandwidth, glueless network connectivity up to 8.0 Tb/s on a single chip.

The BCM56780 is a family of Ethernet switches designed to address performance, capacity, and service requirements for next-generation datacenter and cloud computing environments, as well as high-bandwidth enterprise and mobile network applications. The BCM56780 architecture delivers complete, user-programmable forwarding and instrumentation capabilities at a very high port density, while maintaining minimum power, latency, and board footprint. SDK6 APIs and Broadcom's advanced SDKLT are provided to simplify customer designs and reduce customer time-to-market.

The BCM56780 has extensive features to address the rapidly increasing scale of datacenter network deployments and distributed computing applications. These include flexible in-band and streaming telemetry, large-scale forwarding databases with flexible allocations to allow tailoring to the required application, and support for the latest in datacenter protocol technologies with hooks to allow for future proofing. To achieve high-network utilization, the BCM56780 features advanced multipathing with highly flexible member selection schemes.

With the BCM56780 device, customers can build datacenters with higher node counts and greater levels of server utilization, while simultaneously improving per-port power efficiency. The BCM56780 is built using state-of-the-art silicon process technology and incorporates advanced power management features, such as automatic and compiler-driven power-down of internal-chip resources and adaptive-voltage scaling.

Applications

- Datacenter programmable Top-of-Rack (ToR) switch
- Datacenter leaf/spine
- Core aggregation
- Switch blade in a server chassis
- Line card and fabric in a switch chassis
- Border/DCI switch
- Gateway

Features

- 160 × 50G PAM4 SerDes configuration.
- Flexible port configurations: 10GbE to 400GbE support with runtime reconfigurability (Flexport™).
- Oversubscription to balance power with bandwidth requirements.
- Low pin-to-pin latency in cut-through and store-and-forward modes.
- Multistage field processor processing using flexible tiles.
- Large-scale forwarding and lookup tables are flexibly allocated.

Buffering and Traffic Management Features

- Integrated high-performance fully shared SmartBuffer memory for maximum burst absorption and service guarantees.
- Quality-of-Service (QoS) support: Weighted Random Early Detection (WRED), srTCM, and trTCM color marking and metering.
- ECN for congestion management.
- Packetized MMU statistics.
- Send mirror packet on buffer drops.
- Dynamic Load Balancing (DLB).
- Elephant Trap and DLB monitors.
- Support for jumbo frames up to 9416 bytes.
- High-speed vector-based scheduler with 12 queues per port and scheduling algorithms: SP, RR, WRR, and WDRR.

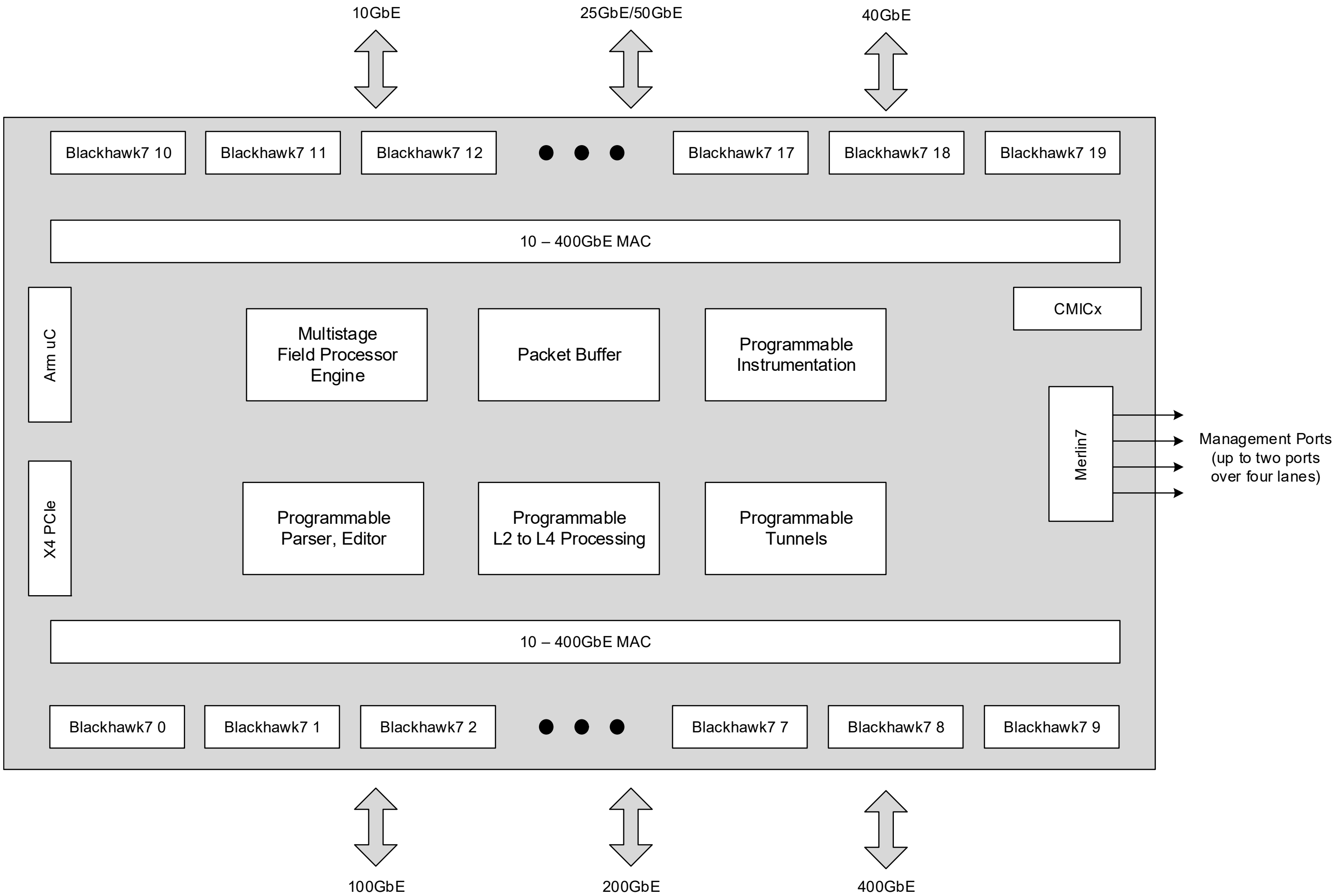
Programmable Packet Processing

- Compiler-programmable packet processing.
- Tile-based architecture.
- Programmed using advanced Network Programming Language (NPL).
- Pre-verified images provided by Broadcom.
- Compiler toolchain available for customer-defined NPL.
- Fully flexible parser and editor.
- NPL-programmable in-band instrumentation for packet trace, packet drop, counters, monitors, and flex state.

Additional Features

- Hooks for IEEE 1588 support.
- Extensive state visibility and instrumentation capabilities.
- High-performance CPU Management Interface Controller (CMICx).
- iProc with two real-time subsystems for multiple embedded application support.
- Two dedicated 1G/10G management Ethernet ports.
- x4 PCI Express (PCIe) Gen 3.0 interface to support a local CPU.
- Adaptive Voltage Scaling (AVS) for reduced average and peak power.

Figure 1: Functional Block Diagram



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Chapter 1: Introduction

The BCM56780 is an efficient, fully programmable switch chip that allows extensive flexibility in protocols and instrumentation where the data plane processing is specified with the Network Programming Language (NPL). This document covers the hardware features of this device, such as I/O bandwidth, SerDes, device interfaces, and the memory management unit.

The Broadcom BCM56780 device family consists of two products that differ in the peak I/O bandwidth and features. The peak I/O bandwidth is a function of the number of SerDes cores that are available for use, and the maximum operating rate of each of those cores. The following two tables summarize the differences in capabilities between the devices in the BCM56780 device family. Any items not listed in these tables are considered to be identical in functionality between all of the devices in the family.

Table 1: BCM56780 Device Family

Device	I/O Bandwidth (Tb/s)	Blackhawk7 Core Instances	Dedicated Management Ports (10 Gb/s)	Package
BCM56780	8.0	20	2	55 mm × 55 mm FCBGA
BCM56784	5.6	16	2	55 mm × 55 mm FCBGA

NOTE: BCM56784 supports 16 Blackhawk7 Cores. Blackhawk7 Cores 0, 9, 10, and 19 are disabled, and Blackhawk7 Cores 1, 8, 11, and 18 can only support up to 25 Gb/s per lane.

Table 2: BCM56780 Device Family Port Configurations

Device	400-Gb/s Ports (Maximum)	200-Gb/s Ports (Maximum)	100-Gb/s Ports (2 Lanes/Port)	50-Gb/s Ports (1 Lane/Port)	40-Gb/s Ports (2 Lanes/Port)	25-Gb/s Ports (Maximum)	10-Gb/s Ports (Maximum)
BCM56780	20	40	72	72	72	72	72
BCM56784	12	24	56 (note)	72	64	72	72

NOTE: BCM56784 supports 48-port 100G with 2 × 50 Gb/s and 8-port 100G with 4 × 25 Gb/s, for a total of fifty-six 100 Gb/s ports.

Table 3: Port Speed to Supported Lane Configuration

Port Speed	Number of SerDes Lanes
400 Gb/s	8 × 50 Gb/s (PAM4)
200 Gb/s	4 × 50 Gb/s (PAM4)
100 Gb/s	2 × 50 Gb/s (PAM4) or 4 × 25 Gb/s
50 Gb/s	1 × 50 Gb/s (PAM4) or 2 × 25 Gb/s
40 Gb/s	4 × 10 Gb/s or 2 × 20 Gb/s
25 Gb/s	1 × 25 Gb/s
10 Gb/s	1 × 10 Gb/s

Chapter 2: Device Overview

The BCM56780 device family has a modular, high-performance pipelined packet switching architecture. This lends itself to the following features:

- Flexible port configurations
- Scalable throughput
- Scalable and programmable packet processing features
- Low pin-to-pin latency

Table 4: Minimum Frame Size for Line-Rate Forwarding at 100% Offered Load

Device SKU	I/O BW (Tb/s)	Core Clock (MHz)	PP Clock (MHz)	Line Rate Frame Size (Bytes)
BCM56780	8.0	1350	1350	364
BCM56784	5.6	1350	1350	251

2.1 Integrated Processor Block

The BCM56780 device family contains the iProc, a full CPU subsystem. The iProc subsystem has the following feature set:

- Two real-time subsystems (RTSs)
  - Each RTS contains Cortex-R5 processors
  - Each RTS has a dedicated SRAM
  - Used to run embedded applications
- Four Cortex-M0 processors
  - Used for Broadcom firmware, such as LED processing and linkscan handling
- Four-lane PCIe Gen3 interface operating as endpoint only
- CMIC-X
  - High-performance packet and table DMA engine
- Sixteen general-purpose I/Os (GPIOs) – six for timestamping and 10 for general use
- QSPI flash
  - Supports BSPI/RAF/MSPI
  - MSPI: supports single-lane, 3B addressing
  - BSPI/RAF: supports single/dual/quad lane, 3B/4B addressing
- Serial peripheral interface (SPI) interface
- Two BroadSync® interfaces are supported
- Low-speed interfaces:
  - Broadcom Serial Connection (BSC)
  - Media Independent Interface Management (MIIM)
  - Universal Asynchronous Receiver/Transmitter (UART)
  - General purpose input/output (GPIO)

2.2 Feature List

Hardware features are listed in the following table.

Table 5: BCM56780 Device Family Features

Feature	Description
Port Configuration	■ 10GbE/25GbE/40GbE/50GbE/100GbE/200GbE/400GbE multilayer Ethernet switch ■ All ports operate in oversubscription mode. ■ Flexible SerDes contains eight SerDes lanes per Blackhawk7 SerDes, configured to operate in any of the following configurations: – 400G: 400GAUI-8, 400GBASE-CR8/KR8 – 200G: 200GAUI-4, 200GBASE-CR4/KR4 – 100G: 100GAUI-2,100GBASE-CR2/KR2, 100GAUI-4, CAUI-4, 100GBASE-CR4/KR4 – 50G: 50GAUI, 50GBASE-CR/KR, 50GAUI-2, 50GBASE-CR2/KR2 – 40G: XLAUI, XLPPI, 40GBASE-CR4/KR4, XLAUI2 – 25G: 25GAUI, 25GBASE-CR/CR-S/CR/KR – 10G: 10GBASE-KR, XFI, SFI **NOTE:** Blackhawk7 Cores 1, 8, 11, and 18 of BCM56784 support up to 25 Gb/s per lane.
Compiler-Programmable Packet Processing	■ Tile-based architecture with large, fungible tables ■ Programmed using advanced NPL language ■ Pre-verified applications provided by Broadcom ■ Compiler toolchain for customer-defined NPL applications ■ Advanced, programmable instrumentation capabilities (in-band, streaming)
iProc Subsystem	■ RTS for embedded applications ■ Four-lane PCIe Gen3 ■ CMIC-X ■ BroadSync ■ External interfaces such as QSPI/GPIO/MIIM
QoS	■ Support for up to 12 queues per port, UC or MC queue types ■ VLAN shaping support ■ 48 CoS queues for CPU ■ Per-port, per-CoS drop profiles ■ Minimum and maximum bandwidth guarantee (shaping) per CoS, per port ■ Traffic shaping available on CPU queues: bandwidth based and packets-per-second based ■ Programmable priority to CoS queue mapping ■ Explicit congestion notification (ECN) support ■ Strict priority (SP), weighted round robin (WRR), and weighted deficit round robin (WDRR) mechanism for shaped queue selection ■ Priority-based flow control (PFC) ■ Linear programming of bucket size of egress port shaping and CoS shaping ■ Supports ingress port rate-based policing and pause flow control. ■ Mapping of incoming priority, CFI to outgoing priority and drop precedence
Memory Management Unit	■ Fully shared buffer ■ Transition cut-through switching for low latency ■ Static and dynamic memory allocation ■ Programmable transmit queue thresholds ■ Ingress cell triggers for back pressure ■ Cell and packet thresholds for triggering HOL prevention ■ WRED congestion control

Table 5: BCM56780 Device Family Features (Continued)

Feature	Description
IEEE 802.1bb Priority Flow Control (PFC)	■ Enables per priority back pressure so that a low-priority application that is causing congestion can be throttled without impacting high-priority or loss-sensitive applications.
Network Time Sync	■ Packet-based time synchronization (IEEE 1588 and IEEE 802.1AS): – Integrated processor for running IEEE 1588v2 stack and clock recovery servo – 1-step and 2-step timestamping – High-precision frequency synthesizer – Synchronous Ethernet layer-one clock recovery ■ Precision Time Protocol (PTP): – Transparent clock – Boundary clock
Management Information Base	■ sFlow support, Broadcom sFlow Shim v2 (requires Remote Agent software) ■ SMON MIB, IETF RFC 2613 ■ RMON statistics group, IETF RFC 2819 ■ SNMP interface group, IETF RFC 1213, 2836 ■ Ethernet-like MIB, IETF RFC 1643 ■ Ethernet MIB, IEEE 802.3u ■ Bridge MIB, IETF RFC 1493

2.3 Target Applications

Datacenter Switch 100GbE/200GbE/400GbE

Datacenter switching represents a fast growing segment of the Ethernet switching market, and it is the primary driver behind 10GbE, 40GbE, up to 400GbE port growth. The datacenter is a facility where computer resources (servers or blade chassis) are centralized and managed in a structured way with high-efficiency Ethernet connectivity. A 20 × 400GbE, 40 × 200GbE, or 72 × 100GbE aggregation switch may be built using a single BCM56780 device as seen in the following figure. The device family is also well suited for a ToR or spine switch as shown in Figure 3 and Figure 4.

The BCM56780 family with its high concurrency, flexible tunneling, high capacity links, programmability, and large table sizes supports ToR-to-Core in the datacenter. Gateway and border devices require flexible tunneling and large ACL lists. Spine devices require high-capacity links. These devices can be used in MSDC virtual chassis environments due to their HiGig3™ feature.

Figure 2: 20 × 400GbE Aggregation Switch

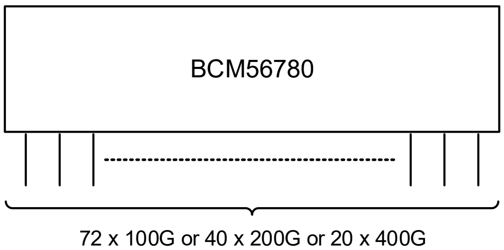


Figure 3: 48 × 100G (Downlinks) + 8 × 400G (Uplinks) ToR Switch

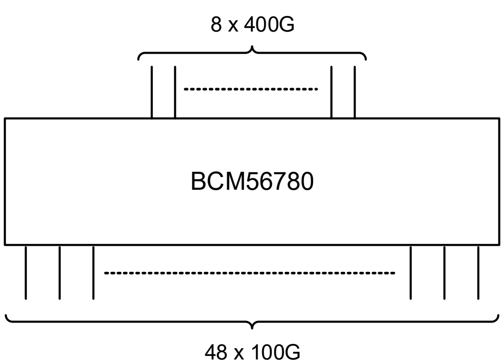
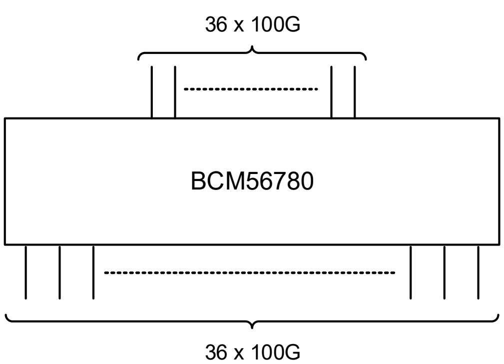


Figure 4: 36 × 100G (Downlinks) + 36 × 100G (Uplinks) Spine Switch



Chapter 3: System Interfaces

The BCM56780 device family external interfaces are described in the following table.

Table 6: BCM56780 Device Family External Interfaces

Interface	Description
Blackhawk7 SerDes	■ Integrated octal 50G SerDes core for front-panel and uplink ports: – 400G: 400GAUI-8, 400GBASE-CR8/KR8 – 200G: 200GAUI-4, 200GBASE-CR4/KR4 – 100G: 100GAUI-2,100GBASE-CR2/KR2, 100GAUI-4, CAUI-4, 100GBASE-CR4/KR4 – 50G: 50GAUI, 50GBASE-CR/KR, 50GAUI-2, 50GBASE-CR2/KR2 – 40G: XLAUI, XLPPI, 40GBASE-CR4/KR4, XLAUI2 – 25G: 25GAUI, 25GBASE-CR/CR-S/CR/KR – 10G: 10GBASE-KR, XFI, SFI ■ Support for 25GbE and 50GbE per the 25G Ethernet Consortium Specification ■ Supports speeds ranging from 10GbE to 400GbE ■ Full-duplex operation is supported (half-duplex is not supported at any speed) **NOTE:** Blackhawk7 Cores 1, 8, 11, and 18 of BCM56784 support up to 25 Gb/s per lane.
Merlin7 SerDes	■ Integrated SerDes core for management ports. Supports up to two ports ■ 10GbE: XFI, SFI, KR, CR, XAUI, RXAUI ■ 2.5GbE: 2500BASE-X ■ 1GbE: SGMII, 1000BASE-X ■ Does not support a mix of 2500BASE-X with 10G ports; see Section 3.2, 10G Quad Merlin7 SerDes ■ Supports full-duplex operation (half-duplex is not supported at any speed) ■ In single lane mode, only lane0 and lane2 can be used to support two management ports. But in 2-lane mode, lane0/1 can be used for one port and lane2/3 can be used for other port.
PCIe (iProc)	■ x4 PCIE Express (PCIe) Gen3 interface ■ Scatter-gather DMA for packet transfer to CPU ■ Table DMA: For copying any switch table into system memory ■ Statistics DMA: For gathering on-chip statistics counters ■ Packet DMA: For transferring packets from/to the CPU
LED (iProc)	■ Dedicated Arm Cortex-M0 for serial LED stream creation ■ Low-cost two-wire interface to system LEDs ■ Direct access to per-port speed, duplex state, flow control state, link state, transmit and receive activity, and collision activity
MIIM (iProc)	■ IEEE 802.3u-compliant MIIM interface for communication with external PHY devices ■ 2.5-MHz operation ■ Compliant to CL45
BSC (iProc)	■ BSC[1:0] support CPU-controlled master mode to communicate with other NXP I^2C-compatible devices
QSPI (iProc)	■ Quad Serial Peripheral Interface used by the iProc CPU subsystem for boot and nonvolatile storage
SPI (iProc)	■ SPI used by the iProc CPU subsystem for general communication. This device cannot boot from this interface
UART (iProc)	■ Four UART interfaces. Two may be used for general purpose. These are used by the embedded applications.
GPIO (iProc)	■ Sixteen General Purpose I/O: 6 for timestamping, 10 for general use
JTAG	■ JTAG-compliant interface supports boundary scan operations
BroadSync (iProc)	■ Packet-based time synchronization support: IEEE 802.1AS, IEEE 1588 ■ Provides time-of-day synchronization to grand master clock source ■ Master mode to accept time-of-day information from a grand master clock source ■ Slave mode to externalize the time-of-day information to an external device

Table 6: BCM56780 Device Family External Interfaces (Continued)

Interface	Description
Adaptive Voltage Scaling (AVS)	■ AVS pins. This interface is designed to connect to system power supply control pins to scale core input voltage to the device at the appropriate level to optimize device's power consumption

3.1 Blackhawk7 SerDes

The Blackhawk7 (TSC-BH7) SerDes is the versatile physical layer interface for the BCM56780, and is specifically designed to support up to 400 Gb/s. This serial interface supports the following features:

- Octal SerDes block supporting eight serial lanes.
- Support for data rates of 10.3125 Gb/s up to 53.125 Gb/s per serial lanes.

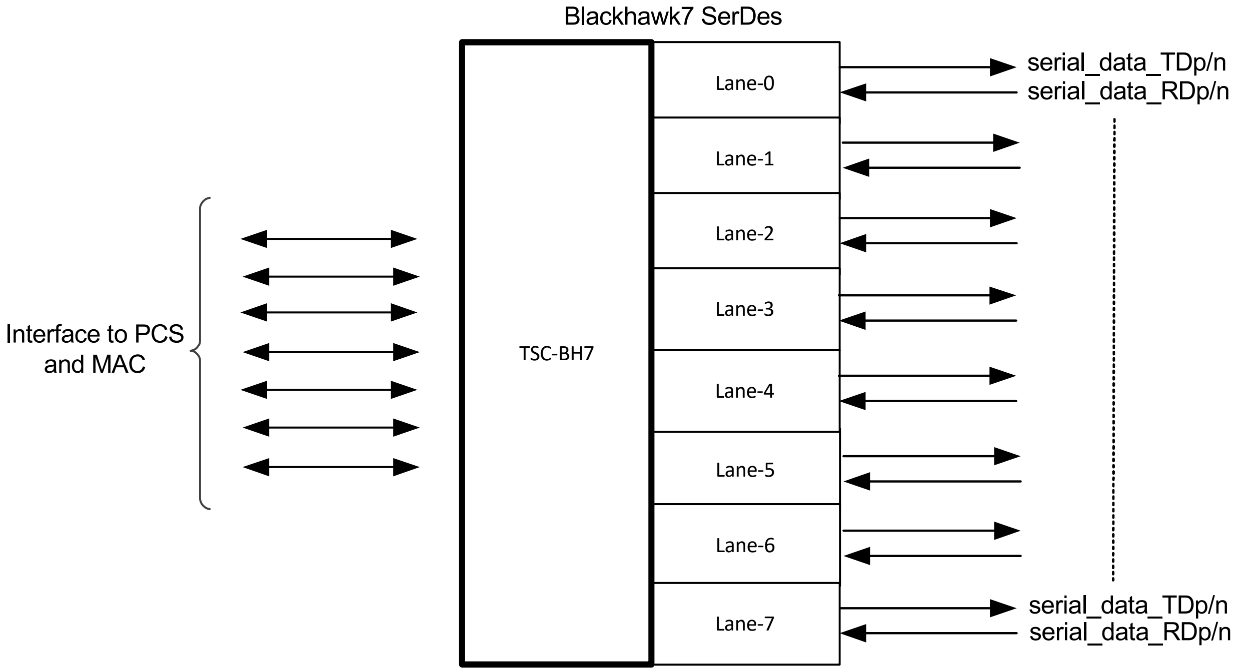
The BCM56780 device family incorporates PAM4-based SerDes Core. This macro allows the device to support low-latency throughput, oversubscription capability, and Flexport configuration. The TSC-BH7 macro consists of the digital control logic and a Blackhawk7 analog block. The terms Blackhawk7 or TSC-BH7 are used interchangeably in this document.

The BCM56780 device family has up to 20 Blackhawk7 SerDes. Each Blackhawk7 SerDes contains eight SerDes lanes. Each Blackhawk7 SerDes lane can be configured as a single individual port, or multiple lanes can be aggregated into a single port.

3.1.1 Blackhawk7 SerDes Supported Modes

The following figure is a conceptual view of the relation of the Blackhawk7 SerDes block within the device.

Figure 5: Conceptual View for Blackhawk7 Eight SerDes Lanes



Each SerDes lane operates in a range from 10.3125 Gb/s to 53.125 Gb/s.

50GBASE-KR is supported in a single lane, and each Blackhawk7 SerDes instance can support 8 × 50GBASE-KR ports.

The following table shows the different Blackhawk7 configurations including supported port speeds and interface types in the BCM56780 family of devices.

Table 7: Blackhawk7 Configurations

Port Speed	Interface Type	Logical Lane Type	Physical Lanes	FEC	Signaling Mode	VCO Frequency (Hz)
400G	400GAUI-8 (C2C, C2M) 400GBASE-KR8 400GBASE-CR8	FEC	8	RS544	53.125G PAM4	26.5625G
		FEC	8	RS272	53.125G PAM4	26.5625G
200G	200GAUI-4 (C2C, C2M) 200GBASE-KR4 200GBASE-CR4	FEC	4	RS544	53.125G PAM4	26.5625G
		FEC	4	RS272	53.125G PAM4	26.5625G
		PCS/VIRTUAL	4	NONE	51.5625G PAM4	25.78125G
100G	100GAUI-2 (C2C, C2M) 100GBASE-KR2 100GBASE-CR2	FEC	2	RS544	53.125G PAM4	26.5625G
		FEC	2	RS272	53.125G PAM4	26.5625G
		PCS/Virtual	2	NONE	51.5625G PAM4	25.78125G
		FEC	2	RS528	51.5625G PAM4	25.78125G
	100GAUI-4 (C2C, C2M) 100GBASE-KR4 100GBASE-CR4	FEC	4	RS544	26.5625G NRZ	26.5625G
		FEC	4	RS528	25.78125G NRZ	25.78125G
		PCS/VIRTUAL	4	NONE	25.78125G NRZ	25.78125G
50G	50GAUI-1 (C2C, C2M) 50GBASE-KR 50GBASE-CR	FEC	1	RS544	53.125G PAM4	26.5625G
		FEC	1	RS272	53.125G PAM4	26.5625G
		PCS/VIRTUAL	1	NONE	51.5625G PAM4	25.78125G
		FEC	1	RS528	51.5625G PAM4	25.78125G
	LAUI-2 (C2C, C2M) 50GAUI-2 (C2C, C2M) 50GBASE-KR2 50GBASE-CR2	FEC	2	RS544	26.5625G NRZ	26.5625G
		FEC	2	RS528	25.78125G NRZ	25.78125G
		PCS/VIRTUAL	2	NONE	25.78125G NRZ	25.78125G
40G	XLAUI XLPPI 40GBASE-KR4 40GBASE-CR4	PCS/VIRTUAL	4	BASE-R	10.3125G NRZ	20.625G (OSx2)
		PCS/VIRTUAL	4	NONE	10.3125G NRZ	20.625G (OSx2)
		PCS/VIRTUAL	4	BASE-R	10.3125G NRZ	25.78125G (OSx2.5)
		PCS/VIRTUAL	4	NONE	10.3125G NRZ	25.78125G (OSx2.5)
	XLAUI2	PCS/VIRTUAL	2	NONE	20.625G NRZ	20.625G
25G	25GAUI (C2C, C2M) 25GBASE-C 25GBASE-CR-S 25GBASE-CR 25GBASE-KR	FEC	1	RS528	25.78125G NRZ	25.78125G
		PCS/VIRTUAL	1	BASE-R	25.78125G NRZ	25.78125G
		PCS/VIRTUAL	1	NONE	25.78125G NRZ	25.78125G
10G	10GBASE-KR SFI XFI	PCS/VIRTUAL	1	BASE-R	10.3125G NRZ	20.625G (OSx2)
		PCS/VIRTUAL	1	NONE	10.3125G NRZ	20.625G (OSx2)
		PCS/VIRTUAL	1	BASE-R	10.3125G NRZ	25.78125G (OSx2.5)
		PCS/VIRTUAL	1	NONE	10.3125G NRZ	25.78125G (OSx2.5)

NOTE:

– Lane swapping mode is configurable.
– For PAM4 modes without FEC (single-lane 50G, dual-lane 100G and 200G) or using RS528 FEC (single-lane 50G, dual-lane 100G), the lane speed is 51.5625G.

3.1.2 Blackhawk7 Octal SerDes Configuration Guidelines

A physical port consists of one or more SerDes lanes in the device. There are up to 20 Blackhawk7 SerDes cores, each with eight physical SerDes lanes.

A logical port is defined as a front-panel, CPU, Management, or internal loopback port. The total number of logical ports on the BCM56780 is 80. Out of 80, up to 72 ports can be assigned as front-panel ports. The remaining logical ports are used as CPU, Management, and internal loopback ports. There are physical port-to-logical port numbering limitations across pipes that are integrated into the SDK software. Users must take into account these system constraints when designing their system.

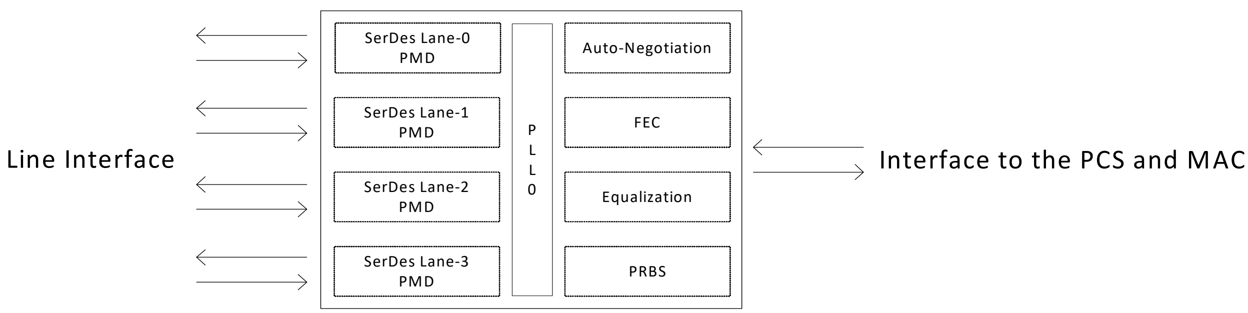
3.1.3 Flexport Configuration

The Blackhawk7 SerDes core supports the ability to change a port configuration (speed and number of lanes per port) at runtime without affecting the operation of the other ports or requiring the device to be reset. If all the SerDes lanes continue to be associated with the same logical ports, the Flexport configuration amounts to a speed change and is handled automatically by the Blackhawk7 SerDes driver. Logical ports can be added, removed, or associated with a different number of SerDes lanes through user API calls. The configuration of two SerDes lanes within a Blackhawk7 can be changed without affecting the ports using the remaining SerDes lanes.

3.2 10G Quad Merlin7 SerDes

The Merlin7 (TSC-M7) SerDes is the management-port physical-layer interface for the BCM56780 specifically designed to support up to two 10-Gb/s management ports on the single Merlin7 SerDes core.

Figure 6: Merlin7 SerDes Core Block Diagram



This serial interface supports the following features:

- The Merlin7 SerDes has four serial lanes that support the following:
  - Two ports in single-lane mode. Only Lane0 and Lane2 are used in case of single-lane mode usage.
  - Two ports in RXAUI mode.
  - One port in XAUI mode.
- Single-lane mode supports 1000BASE-X, SGMII, 2500BASE-X, SFI, XFI, or 10GBASE-KR.
- Two-lane mode supports RXAUI.
- Four-lane mode supports XAUI.
- All single-lane port types can be mixed.

NOTE: When a 2500BASE-X port is mixed with an SFI, an XFI, or a 10GBASE-KR port, the transmit jitter on the 2500BASE-X port violates the IEEE specification. These mixed modes are not supported.

3.3 PCIe

The PCIe interface provided by the BCM56780 switch conforms to the PCIe Gen3 specifications. The BCM56780 supports a four-lane PCIe interface (maximum of 8 Gb/s on each lane with a 128b/130b encoding overhead). No external glue logic is required to support this interface. The protocols and electrical requirements of the PCIe specifications are strictly implemented.

The device provides strap signals to limit the maximum link speed and link width of the PCIe interface. The internal pulls on the strap signals cause the device to default to allowing a maximum link width of x4 and PCIe Gen3 link speeds.

For all PCIe speeds, it is a design requirement that a QSPI flash memory programmed with Broadcom-provided firmware be connected to the QSPI interface on the device, and the device be strapped to perform a download from this memory. This is required, because the firmware is used to configure the PCIe interface into a mode that is functional and compliant to the PCIe specification.

3.4 LED

The BCM56780 device family has four integrated Arm Cortex-M0 microcontrollers, one of which is dedicated just for LED processor usage. This microcontroller has access to the status of all of the SerDes cores and can be used to form serial bitstreams that can be shifted out of the device in a user programmable manner.

The device provides five serial LED output interfaces. The microcontroller has control of all five interfaces, allowing the user to select which interfaces are used to provide serial LED bitstreams. The output frequency is user-configurable. This parameter is common across all five of the LED status interface outputs.

3.5 MIIM

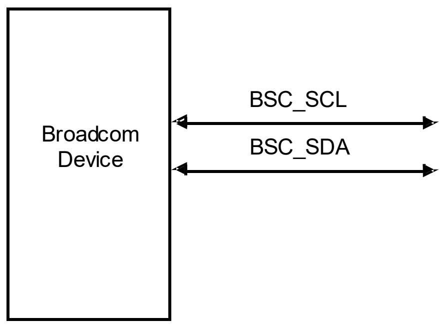
The device provides 12 independent, external MIIM interfaces for management and control of external PHYs. Each interface can be independently configured to operate using the IEEE 802.3 Clause 45 protocol.

Each MDIO interface can be configured as an MDIO master interface.

3.6 Broadcom Serial Controller

The BCM56780 switch provides a Broadcom Serial Control (BSC) interface to communicate with other devices that support a similar interface. This interface is a NXP I^2C-compatible interface. The supported signals are shown in Figure 8.

Figure 7: BSC Interface



The BSC 0 and 1 interfaces support master mode only. The BSC 2 interface supports slave mode only. The supported BSC data protocol format is big endian, which is consistent with the NXP I^2C protocol supported by other vendors.

3.7 QSPI External Microcontroller Interface

The iProc block contains three different QSPI controllers: BSPI (Boot SPI), MSPI (Master SPI), and Read Ahead FIFO (RAF).

The BSPI controller is capable of sequential read operations only. This QSPI core allows code to be downloaded from an external SPI ROM when the system is strapped to use an SPI ROM as the boot device. During boot, the BSPI interface operates at 62.5 MHz in a single-lane mode. The type of addressing (3-byte or 4-byte) is selected using a strap option. BSPI booting always occurs in single-lane mode, later, after boot, it can be used in single-lane, dual-lane, or quad-lane mode by register configuration. After register access has been established, the BSPI controller can be configured to one of four frequencies and can change between single-lane or dual-lane or quad-lane modes. Only single-lane mode is supported in MSPI mode.

The MSPI controller allows for raw bytes to be read from and written to the QSPI bus. This means that it is capable of performing any kind of operation required by the user. MSPI mode supports single-lane, dual-lane, and quad-lane modes. The operating frequency of the MSPI controller is set using a programmable divider.

The BSPI controller only supports FAST_READ commands and supports the following programmable frequencies: 25 MHz, 31.25 MHz, 50 MHz, and 62.5 MHz.

The MSPI controller has a lower maximum frequency than the BSPI controller. For this reason, all read operations are performed using the BSPI controller, and all other operations are performed using the MSPI controller. The QSPI controller selection is configured through a register and can be changed dynamically during runtime.

The RAF mode provides a DMA-like module to provide efficient SPI accesses without violating latency requirements. When programmed, it appears like a FIFO to the underlying software agent. This module fetches a chunk of data from a given address and dumps it into a buffer.

3.8 SPI External Microcontroller Interface

The Serial Peripheral Interface can act as either a master or a slave interface. The default mode is slave.

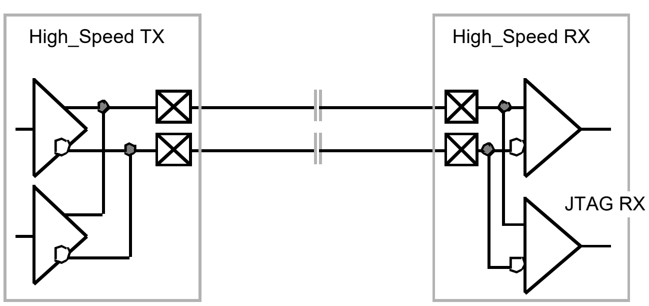
The SPI is a full-duplex synchronous interface used to transfer data to and from the device. When configured in slave mode, the master can send data to and read data from various parts of the chip. When in master mode, the SPI can contact various peripherals, such as temperature sensors, flash memory, and other devices.

3.9 JTAG

A standard JTAG interface is provided for boundary scan operations. This interface uses a standard 5-pin interface.

Traditional JTAG provides the capability to test for opens and shorts when the device is mounted on the PCB. Because current technology requires that most high-speed differential signals must be AC-coupled, the traditional DC test for opens/shorts can produce false results. To provide a means of testing high-speed differential signals, the BCM56780 family supports the latest JTAG specification IEEE Standard 1149.6 (also known as AC-JTAG). AC-JTAG can enable the detection of manufacturing faults on high-speed differential lines on the PCB. The device incorporates independent transceivers with low-load capacitance to avoid any adverse effect on the high-speed differential signals. The signals supported are shown in the following figure.

Figure 8: AC JTAG Test Block



3.10 BroadSync

The BroadSync interface provides a way to externalize the timing information and clock signals generated by the Global Timing Module, an internal clock adjustment block. The interface can also be used to receive timing from an external source or synchronize timing information within a multichip system when used as an input. The BroadSync interface is used by ordinary clocks (OCs) in either a master or slave role. When the OC is a slave, the BroadSync interface is configured as an input, accepting timing information from external hardware. When the OC is a master, BroadSync is configured as an output providing timing information to external hardware.

The BroadSync interface consists of three bidirectional signals that can be configured as slave mode (see Section 3.10.1, Slave Mode: BroadSync Signals as Inputs*)* or master mode (Section 3.10.2, Master Mode: BroadSync Signals as Outputs).

- IP_BS[1:0]_HB – Heartbeat clock: Signals the start of the transmission of the synchronized time value.
- IP_BS[1:0]_CLK – Bit clock: Used for the data transfer of the synchronized time value.
- IP_BS[1:0]_TC – Time code or synchronized time value.

3.10.1 Slave Mode: BroadSync Signals as Inputs

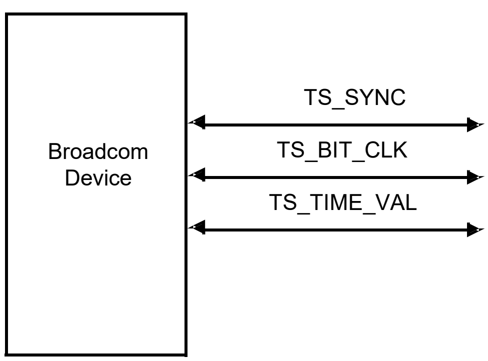
In this mode, the external hardware provides the bit clock and heartbeat clock signals. During each heartbeat period, the external hardware also shifts in the time code values. The time value shifted in corresponds to the time of the most recent rising edge of the heartbeat signal. The heartbeat and time code signals are sampled off the negative edge of the bit clock.

3.10.2 Master Mode: BroadSync Signals as Outputs

In this mode, the device provides the bit clock, heartbeat, and time code signals and enables the external devices to synchronize their behavior with that of the master.

The supported signals are shown in the following figure.

Figure 9: BroadSync Interface



3.11 Out-of-Band Flow Control

Out-of-Band Flow Control (OOBFC) provides a means of transmitting congestion information to a link partner so that the link partner can take the necessary actions to reduce the congestion. The BCM56780 family of devices supports only the generation of OOB Flow Control frames. The devices do not support reception of OOBFC frames.

Chapter 4: Signal Descriptions

This section describes the device hardware signals. The following table lists conventions that are used in the Type column of the following signal description tables.

Table 8: Signal Types

Abbreviation	Description
B	Bidirectional signal
B_{OD}	Open drain bidirectional signal
B_{PD}	Bidirectional signal with internal pull-down
B_{PU}	Bidirectional signal with internal pull-up
I	Input
I_{PD}	Input with internal pull-down
I_{PU}	Input with internal pull-up
N	Positive leg
NC	No connect
O	Output
O_{OD}	Output with open drain
P	Negative leg
PWR/GND	Power/ground plane

4.1 Signal Descriptions

NOTE: The signal description is preliminary and is subject to change. A schematic design for Broadcom AE review is required.

Table 9: Signal Descriptions

Names	Qty	I/O	Voltage	Description
System Signals				
SYS_RST_L	1	I_{PU}	1.8V	Device reset (active low)
AVS[7:0]	8	O	1.8V	Adaptive Voltage Scaling output. These outputs are expected to be connected to a VRM 11.1-compliant module to configure the appropriate core supply voltage for this part.
RESCAL[4:0]_REXT	5	I	—	For each RESCAL pin, and a nearest GND pin, connect a 4.53-kΩ resistor through a low-impedance path to ground. Each resistor calibrates the impedance of the SerDes cores in the device. Five separate resistors are required.
PCIE_INTR_L	1	O_{OD}	1.8V	Active low interrupt signal that asserts whenever the PCIe core sends an interrupt using an in-band mechanism like INT-X or MSI.
Subtotal	15	—	—	—
Required Clocks				
CORE_PLL_FREFP/N	2	I	1.8V Diff CML	50-MHz differential clock to drive core logic.
PCIE_REFCLKP/N	2	I	0.75V Diff CML	100-MHz PCIe differential reference clock. External AC-coupling capacitor and termination resistor are required.
BC_0_REFCLKP/N BC_9_REFCLKP/N BC_10_REFCLKP/N BC_19_REFCLKP/N	8	I	0.75V Diff CML	156.25-MHz differential reference clock for the BlackhawkCore. **NOTE:** Although BC_0, BC_9, BC_10, and BC_19 are disabled on the BCM56784 , these clock sources are still needed to drive other Blackhawk7 Cores.
MGMT_REFCLKP/N	2	I	0.75V Diff CML	156.25-MHz differential reference clock for the MerlinCore. AC-coupling capacitor and termination resistor are required.
Subtotal	14	—	—	—
Optional Clocks				
BS_PLL0_FREFP/N	2	I	1.8V	12.8-MHz, 20-MHz, 25-MHz, 32-MHz, or 50-MHz differential reference clock used for the BroadSync0 logic. This is an alternate clock source. By default, reference clock source is derived from a buffered version of CORE_PLL_FREFP/N inputs.
BS_PLL1_FREFP/N	2	I	1.8V	12.8-MHz, 20-MHz, 25-MHz, 32-MHz, or 50-MHz differential reference clock used for the BroadSync1 logic. This is an alternate clock source. By default, reference clock source is derived from a buffered version of CORE_PLL_FREFP/N inputs.
TS_PLL_FREFP/N	2	I	1.8V	50-MHz differential reference clock used for the TimeSync logic. This is an alternate clock source. By default, reference clock source is derived from a buffered version of CORE_PLL_FREFP/N inputs.
Subtotal	6	—	—	—

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
Strap Signals				
PCIE_FORCE_GEN[1:0]	2	I_{PD}	1.8V	Selects the maximum operating rate of the PCIe interface: ■ 2'b00: Interface can operate at PCIe Gen1, Gen2, or Gen3 speeds (functional mode) ■ 2'b01: Interface can operate at PCIe Gen1 speed (for bring-up use only) ■ 2'b10: Interface can operate at PCIe Gen1 or Gen2 speeds (for bring-up use only) ■ (Others): Reserved **NOTE:** When the PCIe interface is configured to support Gen3 speeds, it is a requirement that the MHOST0_BOOT_DEV strap signal is pulled high, the BOOT_DEV[2:0] signals are all pulled low, and a QSPI flash memory is connected to the QSPI interface and contains the Broadcom-provided PCIe Gen3 microcode.
PCIE_FORCE_LANE[1:0]	2	I_{PD}	1.8V	Selects the maximum link width of the PCIe interface: ■ 2'b00: Interface can operate at x1, x2, or x4 link widths ■ 2'b01: Interface can operate at x1 link width only ■ 2'b10: Interface can operate at x1 or x2 link widths ■ (others): Reserved
MHOST0_BOOT_DEV	1	I_{PD}	1.8V	Selects the way that mHost0 (the first internal Arm R5) is brought out of reset: ■ 1'b0: mHost0 is held in reset ■ 1'b1: mHost0 comes out of reset and begins executing code based on the setting of the BOOT_DEV[2:0] strap signals **NOTE:** This signal must be pulled high during normal operation due to the requirement of using the PCIe firmware.
MHOST1_BOOT_DEV	1	I_{PD}	1.8V	■ 1'b0: Tightly Coupled Memory or TCM in iProc (default) ■ 1'b1: Boot ROM inside iProc (Reserved) **NOTE:** This signal must be pulled low during normal operation.
BOOT_DEV[2:0]	3	I_{PD}	1.8V	Selects the boot flow for mHost0 (the first internal Arm R5): ■ 3'b000: Load all necessary code from QSPI flash attached to QSPI interface and begin execution ■ (Others): Reserved **NOTE:** It is a requirement that these signals are set to 3'b000.
IP_QSPI_4BYTE_ADDR	1	I_{PD}	1.8V	Selects the operating mode of the QSPI flash device connected to the QSPI interface: ■ 1'b0: QSPI flash is operating in 3-byte address mode ■ 1'b1: QSPI flash is operating in 4-byte address mode
IP_QSPI_ADDR_BPC_MODE	1	I_{PD}	1,8V	Selects the mode that is used for sending commands and addresses to the QSPI flash device connected to the QSPI interface: ■ 1'b0: Commands and addresses are sent serially, data is sent in parallel ■ 1'b1: Commands, addresses, and data are sent in parallel
IP_QSPI_DUAL_LANE	1	I_{PD}	1.8V	Selects the QSPI interface's operating mode: ■ 1'b0: QSPI interface operates using a serial interface ■ 1'b1: QSPI interface operates using a 2-bit parallel interface **NOTE:** If this signal is pulled high, the IP_QSPI_QUAD_LANE signal must be pulled low.

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
IP_QSPI_QUAD_LANE	1	I_{PD}	1.8V	Selects the QSPI interface's operating mode: ■ 1'b0: QSPI interface operates using a serial interface ■ 1'b1: QSPI interface operates using a 4-bit parallel interface **NOTE:** If this signal is pulled high, the IP_QSPI_DUAL_LANE signal must be pulled low.
Subtotal	13	—	—	—
PCIe Interface				
PCIE_RDN[3:0]	4	I	0.75V	PCIe receive serial data. Four-lanes of 2.5-Gb/s / 5-Gb/s differential interface negative leg of lanes 3, 2, 1, and 0.
PCIE_RDP[3:0]	4	I	0.75V	PCIe receive serial data. Four-lanes of 2.5-Gb/s / 5-Gb/s differential interface positive leg of lanes 3, 2, 1, and 0.
PCIE_TDN[3:0]	4	O	0.75V	PCIe transmit serial data. Four-lanes of 2.5-Gb/s / 5-Gb/s differential interface negative leg of lanes 3, 2, 1, and 0.
PCIE_TDP[3:0]	4	O	0.75V	PCIe transmit serial data. Four-lanes of 2.5-Gb/s / 5-Gb/s differential interface positive leg of lanes 3, 2, 1, and 0.
PCIE_PERST_L	1	I_{PU}	1.8V	PCIe reset signal. Connect this pin to PCIe_PERST_L from Root Complex if PCIe hot swap is implemented. Otherwise, it can be No Connect if RC PCIe_PERST_L is combined with SYS_RST_L pin.
PCIE_WAKE_L	1	O_{OD}	1.8V	Bi-directional Open Drain, active-low PCIe interface wake signal. Need external pull-up.
Subtotal	18	—	—	
JTAG Signals				
JTRST_L	1	I_{PU}	1.8V	JTAG test controller reset (active low). When asserted, the test controller is held in reset. This signal should be made accessible for JTAG debugging. For normal operation, this signal should be pulled low.
JTCE[1:0]	2	I_{PD}	1.8V	JTAG test controller mode: ■ 2'b00: Functional mode/Arm R5 debug mode ■ 2'b10: Non-functional mode/Logicvision TAP mode ■ (Others): Reserved These signals should be brought to pads with the ability to stuff a pull-up resistor. These resistors should not be stuffed for normal operation.
JTCK	1	I_{PD}	1.8V	JTAG test clock.
JTDI	1	I_{PU}	1.8V	JTAG test data in.
JTDO	1	O	1.8V	JTAG test data out.
JTMS	1	I_{PU}	1.8V	JTAG test mode select.
Subtotal	7	—	—	—
BSC Signals				
IP_BSC[2:0]_SCL	3	B_{OD}	1.8V	Broadcom Serial Controller interface clocks (100 kHz/400 kHz). BSC[1:0] runs in master mode only and BSC2 runs in slave mode only. These signals requires an external pull-up to 1.8V, even if the interface is unused.
IP_BSC[2:0]_SDA	3	B_{OD}	1.8V	Broadcom Serial Controller interface data. BSC[1:0] runs in master mode only and BSC2 runs in slave mode only. These signals require an external pull-up to 1.8V, even if the interface is unused.

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
BSC_SA[1:0]	2	B_{OD}	1.8V	Broadcom Serial Controller interface slave address selects the lower 2 bits of the BSC slave address used on the BSC2 interface.
Subtotal	8	—	—	—
LED Interface				
IP_LED[4:0]_CLK	5	O_{PD}	1.8V	Clocks for serial bit streams for port status LEDs. Each clock corresponds to the associated IP_LED[4:0]_DATA data signal.
IP_LED[4:0]_DATA	5	O_{PD}	1.8V	Data signals for serial bit streams for port status LEDs. Each data signal corresponds to the associated IP_LED[4:0]_CLK clock.
Subtotal	10	—	—	—
Network Timing Signals				
IP_BS[1:0]_CLK	2	B_{PD}	1.8V	BroadSync clocks. Synchronizes time code data transfer with the associated IP_BS[1:0]_HB and IP_BS[1:0]_TC signals. When configured as outputs, the BroadSync heartbeat and time code signals are driven off the rising edge of the bit clock. When configured as inputs, the heartbeat and time code signals are sampled off the negative edge of the bit clock.
IP_BS[1:0]_HB	2	B_{PD}	1.8V	BroadSync heartbeat clock that signals start of the synchronized time value transmission. Each signal is configurable as an output or an input through a register. When configured as output, this signal is driven off the rising edge of the bit clock. When configured as input, this signal is sampled off the negative edge of the bit clock.
IP_BS[1:0]_TC	2	B_{PD}	1.8V	BroadSync synchronized time code. Serially shifts time value, 1 bit per rising edge of bit clock. Each signal is configurable as an output or an input using a register. When configured as output, this signal is driven off the rising edge of the bit clock. When configured as input, this signal is sampled off the negative edge of the bit clock.
IP_TS_GPIO[5:0]	6	B_{PU}	1.8V	General-purpose I/O signals with the ability to trigger internal timestamp capture in input mode or be automatically controlled by the TimeSync logic in output mode. These signals can also be configured as general-purpose outputs or inputs (with interrupt generation capability). When configured as an input, a weak internal pull-up or pull-down resistor can be enabled. By default, these signals are configured as inputs with an internal pull-up resistor enabled. These signals return to the default state when the SYS_RST_N signal is asserted.
L1_RCVRD_CLK	1	O	1.8V	Primary recovered clock from a user-selectable Ethernet SerDes receiver. This is primarily used to enable L1 clock synchronization. The output clock frequency is user configurable through a fractional divider and supports frequencies from 25 MHz to 156.25 MHz.
L1_RCVRD_CLK_VALID	1	O	1.8V	Status signal associated with the L1_RCVRD_CLK clock output. When this signal is high, it is an indication that the output clock is valid and is usable. When this signal is low, the output clock should not be used.

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
L1_RCVRD_CLK_BKUP	1	O	1.8V	Secondary recovered clock from a user-selectable Ethernet SerDes receiver. This is primarily used to enable L1 clock synchronization. The output clock frequency is user configurable through a fractional divider and supports frequencies from 25 MHz to 156.25 MHz.
L1_RCVRD_CLK_VALID_BKUP	1	O	1.8V	Status signal associated with the L1_RCVRD_CLK_BKUP clock output. When this signal is high, it is an indication that the output clock is valid and is usable. When this signal is low, the output clock should not be used.
Subtotal	16	—	—	—
General Purpose I/Os				
IP_G_GPIO[9:0]	10	B_{PU}	1.8V 8 mA	General-purpose I/O signals. These signals can be configured as outputs or inputs (with interrupt generation capability). When configured as an input, a weak internal pull-up or pull-down resistor can be enabled. By default, these signals are configured as inputs with an internal pull-up resistor enabled. These signals are reset back to inputs upon the assertion of the SYS_RST_L signal.
Subtotal	10	—	—	—
QSPI Signals				
IP_QSPI_CS_L	1	O	1.8V	QSPI slave select (active low).
IP_QSPI_HOLD_L	1	B_{PD}	1.8V	When the QSPI interface is operating in single- or dual-lane mode, this is the QSPI pause active low output signal. When operating in quad-lane mode, this is a bidirectional signal used as DQ[3].
IP_QSPI_MISO	1	B_{PD}	1.8V	When the QSPI interface is operating in single-lane mode, this is the serial input from the slave. When operating in dual- or quad-lane mode, this is a bidirectional signal used as DQ[1]. **NOTE:** The QSPI interface only supports operating as a master.
IP_QSPI_MOSI	1	B_{PD}	1.8V	When the QSPI interface is operating in single-lane mode, this is the serial output to the slave. When operating in dual- or quad-lane mode, this is a bidirectional signal used as DQ[0]. **NOTE:** The QSPI interface only supports operating as a master.
IP_QSPI_SCK	1	O	1.8V	QSPI clock.
IP_QSPI_WP_L	1	B_{PD}	1.8V	When the QSPI interface is operating in single- or dual-lane mode, this is the QSPI write protect active low output signal. When operating in quad-lane mode, this is a bidirectional signal used as DQ[2].
Subtotal	6	—	—	—
SPI Signals				
IP_SPI_SCK	1	B_{PU}	1.8V	SPI serial clock.
IP_SPI_MISO	1	B_{PU}	1.8V	SPI serial input from the slave. **NOTE:** The SPI interface can operate in master or slave mode. The default is slave mode.
IP_SPI_MOSI	1	B_{PU}	1.8V	SPI serial output to the slave. **NOTE:** The SPI interface can operate in master or slave mode. The default is slave mode.
IP_SPI_SSN	1	B_{PU}	1.8V	SPI slave select (active low).
Subtotal	4	—	—	—
UART Signals				

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
IP_UART0_CTS_L, IP_UART2_CTS_L, IP_UART3_CTS_L	3	I_{PU}	1.8V	Active low, Clear to Send signal used by first, third, and fourth UART. **NOTE:** UART0-1 are used for peripheral devices. UART2-3 interfaces are used for MHOST0 and MHOST1, respectively.
IP_UART[3:0]_SIN	4	I_{PD}	1.8V	Serial input used by first UART Note: UART0-1 are used for peripheral devices. UART2-3 interfaces are used for MHOST0 and MHOST1, respectively.
IP_UART0_RTS_L, IP_UART2_RTS_L, IP_UART3_RTS_L	3	O	1.8V	Active low, Request to Send signal used by first, third, and fourth UART. **NOTE:** UART0-1 are used for peripheral devices. UART2-3 interfaces are used for MHOST0 and MHOST1, respectively.
IP_UART[3:0]_SOUT	4	O	1.8V	Serial output used by first UART. **NOTE:** UART0-1 are used for peripheral devices. UART2-3 interfaces are used for MHOST0 and MHOST1, respectively.
Subtotal	14	—	—	—
				NOTE: All UART pins and features are for dedicated IEEE 1588 application only. They do not support generic use.
MIIM Signals				
IP_MDC[11:0]	12	O	1.2V	Serial management clocks for external PHY management. These signals conform to the Clause 45 electrical specification and protocol. Each clock corresponds to the associated IP_MDIO[11:0] signal. Use an external pull-up resistor on each signal to the IP_VDDO_[2:1] supply. The internal MDIO to Blackhawk Core, MGMT, and PCIe connection are listed below. The external PHY mapping can be configured by SDK software.
IP_MDIO[11:0]	12	B_{OD}	1.2V	Serial management clocks for external PHY management. These signals conform to the Clause 45 electrical specification and protocol. An external pull-up resistor on each signal to the IP_VDDO_[2:1] supply is recommended.
Subtotal	24	—	—	—
BlackhawkCore Signals				
BC[19:0]_RDP/N[7:0]	320	I	0.75V	BlackhawkCores lane [7:0] receive differential pair.
BC[19:0]_TDP/N[7:0]	320	O	0.75V	BlackhawkCores lane [7:0] transmit differential pair.
NOTE: BC0, BC9, BC10, and BC19 are disabled on BCM56784. Leave those signals NC on BCM56784.				
Subtotal	640	—	—	—
MerlinCore Signals				
MGMT_RDP/N[3:0]	8	I	0.75V	MerlinCore lane [3:0] receive differential pair.
MGMT_TDP/N[3:0]	8	O	0.75V	MerlinCore lane [3:0] transmit differential pair.
Subtotal	16	—	—	—

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
Test/Reserved Signals				
BC0_TESTP/N BC4_TESTP/N BC5_TESTP/N BC9_TESTP/N BC10_TESTP/N BC14_TESTP/N BC15_TESTP/N BC19_TESTP/N	16	O	1.2V	Signal should be left unconnected; for factory use only.
BC_4_REFCLKP/ N_RESERVED BC_5_REFCLKP/ N_RESERVED BC_14_REFCLKP/ N_RESERVED BC_15_REFCLKP/ N_RESERVED	8	I	0.75V	Signal should be left unconnected; for factory use only.
BS_PLL[1:0]_TESTP/N	4	O	1.8V	Signal should be left unconnected; for factory use only.
BYP_OTP_AUTOLOAD_ RESERVED	1	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
CORE_MS_PLL_TESTP/N	2	O	1.8V	Signal should be left unconnected; for factory use only.
DFT_GATING_RESERVED	1	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
GLOBAL_DISABLE_L_ RESERVED	1	I_{PU}	1.8V	Signal should be left unconnected; for factory use only.
IDDQ_RESERVED	1	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
NC_IP_PLL_FREFP/N	2	I	1.8V	Signal should be left unconnected; for factory use only.
IP_PLL_TESTP/N	2	O	1.8V	Signal should be left unconnected; for factory use only.
MGMT_TESTP/N	2	O	0.75V	Signal should be left unconnected; for factory use only.
OTP_LVM_RESERVED	1	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
PCIE_TESTP/N	2	O	0.75V	Signal should be left unconnected; for factory use only.
PLL_BYP_RESERVED	1	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
PP_PLL_FREFP/ N_RESERVED	2	I	1.8V	Signal should be left unconnected; for factory use only.
PP_PLL_TESTP/N	2	O	1.8V	Signal should be left unconnected; for factory use only.
SWCLKTCK_RESERVED	1	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
SWD_RESERVED	1	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
TEMPDIODE0_FORCE_P/ N_RESERVED	2	O	1.8V	Signal should be left unconnected; for factory use only.
TEMPDIODE1_FORCE_P/ N_RESERVED	2	O	1.8V	Signal should be left unconnected; for factory use only.
TESTIO[55:0]	56	I_{PD}	1.8V	TESTIO pins. For factory use only.
CHIP_TEST_MODE[3:0]_ RESERVED	4	I_{PD}	1.8V	Signal should be left unconnected; for factory use only.
NC_ORIENTATION_CHECK	1	I	1.8V	Signal should be left unconnected; for factory use only.
TS_PLL_TESTP/N	2	O	1.8V	Signal should be left unconnected; for factory use only.

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
VDD18_RESERVED	1	PWR	1.8V	Connect VDD18_RESERVED using a 10-kΩ resistor (1% tolerance) in parallel with a 1-µF capacitor (10% tolerance) to ground.
NC[11:0]_PLLVDD[1:0]	24	I	0.75V	Signal should be left unconnected; for factory use only.
NC_VTMON10_AVDD1P8	1	I	1.8V	Signal should be left unconnected.
NC_AVS_VTMON_AVDD1P8	1	I	1.8V	Signal should be left unconnected.
Subtotal	144	—	—	—
OOBFC Signals				
TX_OOBFC_CLK	1	O	1.8V	Clock signals for the OOBFC interface.
TX_OOBFC_SYNC	1	O	1.8V	Sync signals for the OOBFC interface.
TX_OOBFC_DATA[1:0]	2	O	1.8V	Data signals for transmit OOBFC signals.
Subtotal	4	—	—	—
System Monitoring				
AVS_VTMON_ADC	1	I	various	Input to Analog-to-Digital Converter in Adaptive Voltage Scaling monitor block. This input can be left unconnected; for factory use only.
AVS_VTMON_VDAC	1	O	various	Output from Digital-to-Analog Converter in Adaptive Voltage Scaling monitor block. This output can be left unconnected; for factory use only.
MAX_TEMP_CLK	1	O	1.8V	TBD
MIN_TEMP_CLK	1	O	1.8V	TBD
TRVDD0P75_SENSE[3:0]	4	O	various	TRVDD supply sense output used as a feedback voltage to the voltage regulator module for transmit and receive analog supplies.
VDD_SENSE	1	O	various	Core voltage monitor. Used for remote sensing of VDD rail. This pin connects directly to die VDD rail. This pin should be connected to VRM positive sense pin. If unused, leave pin NC.
GND_SENSE	1	O	OV	Ground monitor. Used for remote sensing of GND rail. This pin connects directly to the die GND rail. Connect this pin to the VRM negative sense pin. If unused, leave pin NC.
VTMON[0:5]_ADC_VDAC, VTMON7_ADC_VDAC	7	B	various	Input/outputs to Analog-to-Digital and Digital-to-Analog Converters in Process/ Temperature/Voltage monitoring blocks. These I/Os can be left unconnected; for factory use only.
Subtotal	17	—	—	—
Digital Power Supplies				
VDDO18	17	PWR	1.8V	I/O power. Requires a clean power rail with minimal noise.
IP_VDDO1P2_1	4	PWR	1.2V	Voltage setting for MDIO interfaces. Connect IP_VDDO1P2_1 pins to 1.2V.
IP_VDDO1P8_0	8	PWR	1.8V	IProc 1.8V voltage.
VDD (Programmable)	241	PWR	0.72V – 0.9V	Core VDD, can operate at ROV or AVS output setting. Requires a clean programmable voltage rail with minimal noise.
Subtotal	270	—	—	—
Analog Power Supplies				
MGMT_PVDD0P75	2	PWR	0.75V	Filtered 0.75V voltage source for MerlinCore PLL.

Table 9: Signal Descriptions (Continued)

Names	Qty	I/O	Voltage	Description
MGMT_TRVDD0P75	4	PWR	0.75V	Filtered 0.75V voltage source for MerlinCore transmitter and receiver.
PCIE_PVDD0P75	2	PWR	0.75V	Filtered 0.75V source for PCIe PLL.
PCIE_TRVDD0P75	4	PWR	0.75V	Filtered 0.75V source for PCIe transmitter and receiver.
TRVDD0P75_[3:0]	237	PWR	0.75V	Filtered 0.75V voltage source for BlackhawkCore analog transmitter and receiver.
TVDD1P2_[3:0]	40	PWR	1.2V	Filtered 1.2V voltage source for BlackhawkCore analog four transmitter.
BS_PLL[1:0]_AVDD1P8	4	PWR	1.8V	Filtered BroadSync 1.8V voltage source.
CORE_PLL_AVDD1P8	1	PWR	1.8V	Filtered Core PLL 1.8V voltage source.
MS_PLL_AVDD1P8	1	PWR	1.8V	RESERVED. Connect to filtered 1.8V voltage source.
PP_PLL_AVDD1P8	2	PWR	1.8V	Filtered PP PLL 1.8V voltage source.
IP_PLL_AVDD1P8	2	PWR	1.8V	Filtered IP PLL 1.8V voltage source.
TS_PLL_AVDD1P8	2	PWR	1.8V	Filtered TimeSync PLL 1.8V voltage source.
BC[19:0]_PLLVDD[1:0]_0P75	40	PWR	0.75V	Filtered Blackhawk core PLL 0.75V voltage source. **NOTE:** Although Blackhawk cores 0, 9, 10, and 19 are disabled on the BCM56784, connect the corresponding PLLVDD[1:0] power pins to the filtered 0.75V voltage source.
Subtotal	341	—	—	—
Diagnostics/Monitoring Supplies				
VTMON[7:0]_AVDD1P8	8	PWR	1.8V	Filtered VT Monitor 1.8V voltage source.
Subtotal	8	—	—	—
Ground				
GND	1710	GND		Ground.
Subtotal	1710	—	—	—
TOTAL	3315	—	—	—

Chapter 5: Electrical Specifications

5.1 Operating Conditions

The following table describes the recommended operation conditions for the BCM56780.

Table 10: Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
0.72V to 0.9V ± 3%, AVS core voltage	—	–3%	AVS Core Voltage	+3%	V
0.75V ± 3%, analog voltage	—	0.727	0.75	0.772	V
1.20V ± 3%, (analog and I/O) voltage	—	1.164	1.20	1.236	V
1.80V ± 3%, (analog and I/O) voltage	—	1.746	1.80	1.854	V
Ambient temperature	T_A	0	—	70	°C
Junction temperature	T_J	0	—	105	°C

NOTES:

- VRM can be controlled through I^2C or AVS pins to provide the AVS core voltage.
- ±3% tolerance includes ±1% DC voltage accuracy and ±2% AC ripple content.
- The AVS functionality is TBD until silicon validation is complete. A core voltage of 0.8V allows the use of AVS. For implementation details, refer to the *BCM56780 Hardware Design Guidelines* (56780-DG1xx).

5.2 Power-Up and Power-Down Specifications

This device requires a power-up sequence and a power-down sequence. Violating the power sequencing requirement can cause latch-up damage. See Section 5.5.1, Power-Up, Power-Down, and Reset Specifications and Section 5.5.1.1, Power-Down Requirement, and the *BCM56780 Hardware Design Guidelines* (56780-DG1xx) for additional details.

5.3 Device Power Supply Requirement

Table 11: BCM56780 Per Rail Current for Power Supply Design

Supply	Supply Name	Voltage (V)	Maximum Power Supply Current (A)
AVS core voltage	VDD	0.72V to 0.9V	246.61 (Note b)
1.8 I/O	VDDO18, IP_VDDO1P8_0	1.8	1.44
1.2 I/O	IP_VDDO1P2_1	1.2	0.33
1.8 analog	*AVDD1P8	1.8	0.32
1.2 analog	TVDD1P2	1.2	2.60
0.75 analog	TRVDD0P75, *PVDD0P75	0.75	47.90

Table 12: BCM56784 Per Rail Current for Power Supply Design

Supply	Supply Name	Voltage (V)	Maximum Power Supply Current (A)
AVS core voltage	VDD	0.72V to 0.9V	236.47 (Note b)
1.8 I/O	VDDO18, IP_VDDO1P8_0	1.8	1.44
1.2 I/O	IP_VDDO1P2_1	1.2	0.33

Table 12: BCM56784 Per Rail Current for Power Supply Design (Continued)

Supply	Supply Name	Voltage (V)	Maximum Power Supply Current (A)
1.8 analog	*AVDD1P8	1.8	0.32
1.2 analog	TVDD1P2	1.2	2.08
0.75 analog	TRVDD0P75, *PVDD0P75	0.75	38.45

NOTE: a: The maximum per-rail current values in the preceding tables are used to design the system power supply. Each supply rail current may not track each other with process variations (that is, analog current goes up while digital current goes down). The maximum system power values in the following tables are used for thermal design calculation.
b: The maximum current of AVS core voltage is estimated at 0.76V.

Table 13: Maximum System Power

Device	System Thermal Power (W)
BCM56780	230
BCM56784	215

NOTE: These maximum power values include the use of the mandatory AVS feature.

Table 14: BCM56780Per-SerDes, Voltage Rail Maximum Power Numbers

SerDes	Voltage Rail	Maximum Power (W)
Blackhawk7	TVDD1P2	0.13
	TRVDD0P75	1.204
	PVDD075	0.202
Merlin7	TRVDD0P75	0.128
	PVDD0P75	
PCIe SerDes	PVDD0P75	0.136
	VDD0P75	

NOTE: It is a design requirement that all SerDes cores must be connected to their specified supply rails.

5.4 DC Characteristics

5.4.1 Standard 1.8V Interfaces

The specifications shown in the following table apply to all CMOS 1.8V general-purpose I/O signals along with synchronous Ethernet interface, UART, GPIO, JTAG, SPI, QSPI, BSC, and LED signals except for MIIM interface signals, which are 1.2V.

Table 15: Standard 1.8V Signals

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	0.0	—	1.98	V
Input low voltage	V_{IL}	—	—	0.35 × VDD1P8[a]	V
Input high voltage	V_{IH}	0.65 × VDD1P8[a]	—	—	V
Output low voltage	V_{OL}	—	—	0.45	V
Output low current	I_{OL}	8	—	—	mA
Output high voltage	V_{OH}	VDD1P8[a] – 0.45	—	—	V
Output high current	I_{OH}	8	—	—	mA
Pull-up or pull-down resistor	R_p	—	50	—	kΩ

a. See Table 27, Mapping of Device Power Signals to Supply Rails.

NOTE: The overshoot and undershoot limits are as follows:

- Overshoot: The maximum limit is 500 mV above supply for no more than 10% of the duty cycle.
- Undershoot: The maximum limit is 500 mV below ground for no more than 10% of the duty cycle.

5.4.2 Management Interface (MIIM)

Table 16: MIIM, Clause 45 Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	—	0	—	1.5	V
Input low voltage	V_{IL}	—	—	—	0.36	V
Input high voltage	V_{IH}	—	0.84	—	—	V
Output low voltage	V_{OL}	I_{OL} = 100 µA	—	—	0.2	V
Output low current	I_{OL}	V_{OL} = 0.2V	4.0	—	—	mA
Output high voltage	V_{OH}	I_{OH} = –100 µA	1.0	—	—	V
Output high current	I_{OH}	V_{OH} = 1.0V	—	—	–4.0	mA

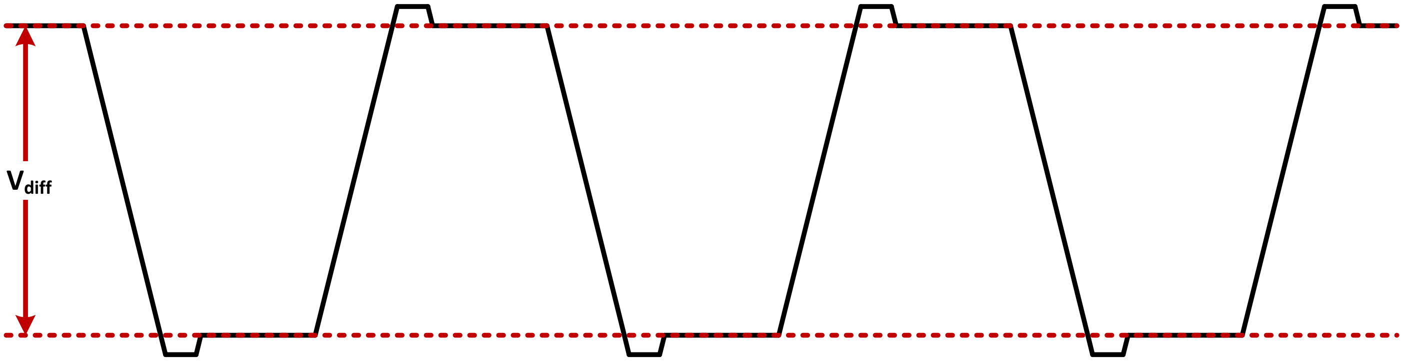
NOTE: The overshoot and undershoot limits are as follows:

- Overshoot: The maximum limit is 500 mV above supply for no more than 10% of the duty cycle.
- Undershoot: The maximum limit is 500 mV below ground for no more than 10% of the duty cycle.

5.4.3 Reference Clocks

The following figure is applicable to all reference clocks in this subsection.

Figure 10: Reference Clock Differential DC Parameters



5.4.3.1 Core PLL Reference Clock (CORE_PLL_FREF)

The Core PLL is used to clock all switching and iProc logic.

Table 17: Core PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-mode voltage	V_{cm}	—	650	—	mV_{se}
Differential swing	V_{diff}	500	—	2000	mV_{ppd}
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	—	100	—	Ω

a. External AC coupling is required. The recommended AC-coupling capacitor value is 10 nF.

5.4.3.2 Blackhawk7 SerDes Core IP Reference Clocks (BC#_PLL_REFLCK)

The Blackhawk7 SerDes Core PLL reference clocks are used to clock all The Blackhawk7 SerDes core used for Ethernet connectivity.

Table 18: The Blackhawk7 SerDes Core REFCLK Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-mode voltage	V_{cm}	—	375	—	mV_{se}
Differential swing	V_{diff}	800	1000	1400	mV_{ppd}
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	80	100	120	Ω

a. External AC coupling is required. The recommended AC-coupling capacitor value is 10 nF.

5.4.3.3 Merlin7 SerDes Core IP Reference Clock (MGMT_REFCLK)

The Merlin7 SerDes Core PPL reference clock is used to clock the Merlin7 SerDes used for Ethernet connectivity.

Table 19: Merlin7 SerDes Core REFCLK Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-mode voltage	V_{cm}	—	375	—	mV_{se}
Differential swing	V_{diff}	300	—	1200	mV_{ppd}
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	80	100	120	Ω

a. External AC coupling is required. The recommended AC-coupling capacitor value is 10 nF.

5.4.3.4 Time Sync PLL Reference Clock (TS_PLL_FREF)

The TimeSync PLL is used to clock the TimeSync and timestamp logic.

Table 20: TimeSync PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-mode voltage	V_{cm}	—	650	—	mV_{se}
Differential swing	V_{diff}	500	—	2000	mV_{ppd}
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	—	100	—	Ω

a. External AC coupling is required. The recommended AC-coupling capacitor value is 10 nF.

5.4.3.5 PCIe PLL Reference Clock (PCIE_REFCLK)

The PCIe PLL is used to clock the SerDes used for PCIe connectivity.

Table 21: PCIe PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-mode voltage	V_{cm}	—	375	—	mV_{se}
Single-ended swing	V_{ilse} / V_{ihse}	0	—	800	mV_{se}
Differential swing	V_{diff}	600	—	1200	mV_{ppd}
Internal AC coupling[a]	C_{ac}	—	6	—	pF
Internal differential termination	Rterm	—	—	—	Ω
NOTE: ■ External 100Ω termination resistor is required.					

a. External AC coupling is required. The recommended AC-coupling capacitor value is 10 nF.

5.4.3.6 BroadSync PLL Reference Clocks (BS_PLL0_FREF / BS_PLL1_FREF)

The BroadSync PLLs are used to clock the associated BroadSync block used to transmit or receive timing information from an external entity.

Table 22: BroadSync PLL Reference Clock DC Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit
Common-mode voltage	V_{cm}	—	650	—	mV_{se}
Differential swing	V_{diff}	500	—	2000	mV_{ppd}
Internal AC coupling[a]	C_{ac}	—	—	—	pF
Internal differential termination	R_{term}	—	100	—	Ω

a. External AC coupling is required. The recommended AC-coupling capacitor value is 10 nF.

5.4.4 Blackhawk7 (TSC-BH7) Interface

Table 23: Blackhawk7 SerDes DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver					
Input voltage (differential peak-to-peak), AC-coupled	V_{ID}	85	—	1600	mVp-p
Input impedance (differential), integrated on-chip	R_{IN}	80	95	120	Ω
Transmitter					
Output voltage (differential peak-to-peak), programmable	V_{ODpp}	0	—	1050	mVp-p
Output impedance (differential)	R_{OUT}	—	85	—	Ω

5.4.5 Merlin7 (TSC-M7) Interface

Table 24: Merlin7 SerDes DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver					
Input voltage (differential peak-to-peak), AC-coupled	V_{ID}	85	—	1200	mVp-p
Input impedance (differential), integrated on-chip	R_{IN}	80	100	120	Ω
Transmitter					
Output voltage (differential peak-to-peak), programmable	V_{ODpp}	800	900	1200	mVp-p
Output impedance (differential)	R_{OUT}	—	100	—	Ω

5.4.6 PCIe Interface

Table 25: PCIe SerDes DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver					
Input voltage (differential peak-to-peak), AC-coupled	V_{ID}	85	—	1200	mVp-p
Input impedance (differential), integrated on-chip	R_{IN}	80	100	120	Ω
Transmitter					
Output voltage (differential peak-to-peak), programmable	V_{ODpp}	800	900	1200	mVp-p
Output impedance (differential)	R_{OUT}	—	100	—	Ω

5.5 AC Characteristics

5.5.1 Power-Up, Power-Down, and Reset Specifications

The following figure and Table 26 provide the required power-up and reset sequence timing for reliable device operation.

Figure 11: Power-Up and Reset Timing Diagram

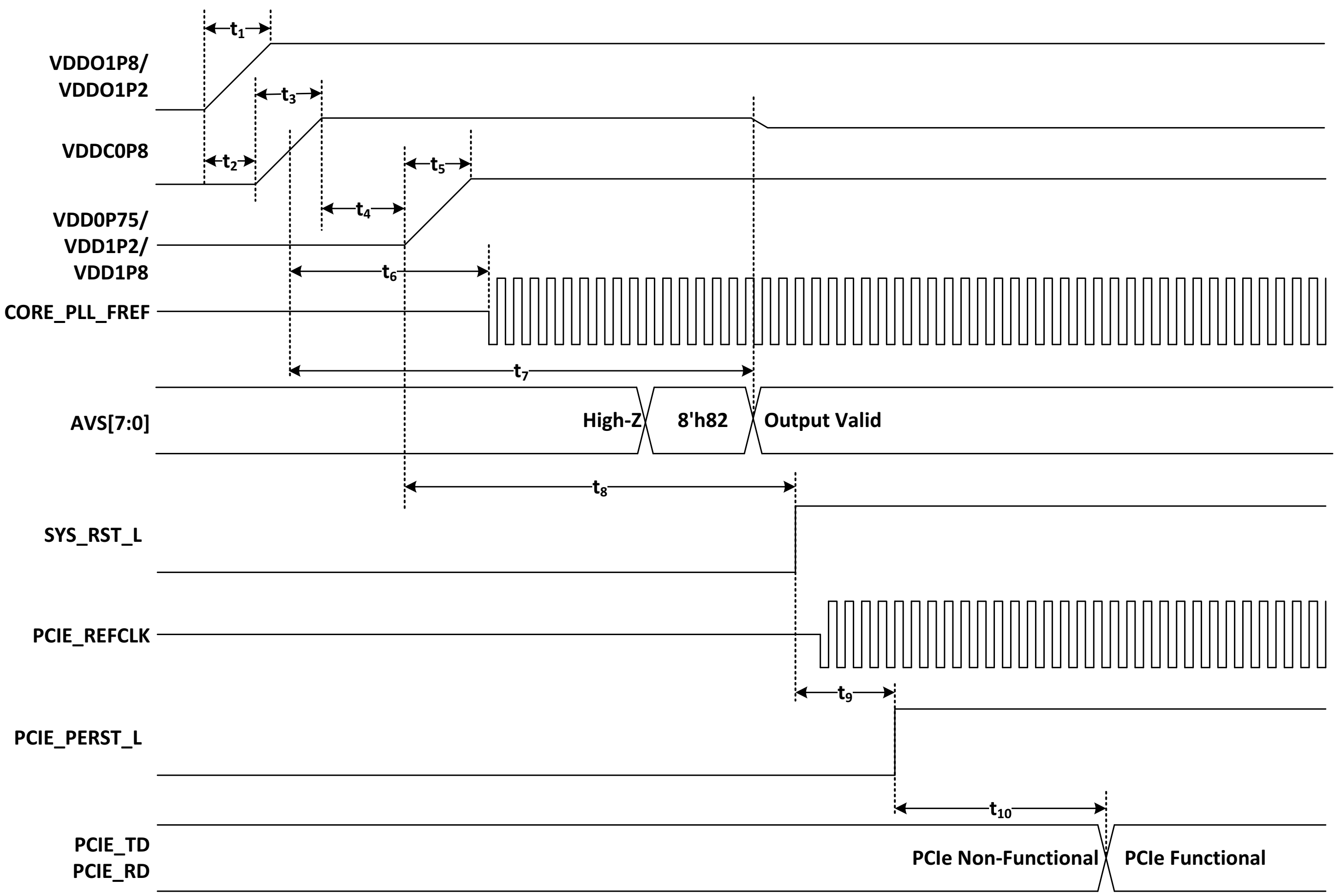


Table 26: Power-Up and Reset Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ramp time for 1.8V and 1.2V I/O supplies	t_1	0.09	—	5	ms
Delay from start of 1.8V ramp to start of VDDC0P8 supply ramp	t_2	0.0	—	—	ms
Ramp time for VDDC0P8 supply	t_3	0.05	—	10	ms
Delay from VDDC0P8 ramped up to start of 0.75V, 1.2V, and 1.8 AVDD supplies ramp	t_4	VDD reaches 0.72V	—	—	ms
Ramp time for 0.75V, 1.2V, and 1.8V supplies	t_5	0.1	—	10	ms
Time from first supply starting to ramp to last supply finish ramping	$t_2 + t_3 + t_4 + t_5$	—	—	10	ms
VDDC0P8 at 0.55V to CORE_PLL_FREF is stable	t_6	—	—	6.4	ms
VDDC0P8 at 0.55V to valid output at AVS[3:0]	t_7	14	—	90	ms
Start of ramp of 0.75V/1.2V/1.8V AVDD supplies to system reset signal deasserted	t_8	120	—	—	ms
PCIe reset signal deasserted	t_9	100	—	—	ms
PCIe interface is functional	t_{10}	—	—	20	ms

Table 27: Mapping of Device Power Signals to Supply Rails

Supply Name	Power Signal Names
VDDO1P8	VDDO18, IP_VDDO1P8_0
VDDO1P2	IP_VDDO1P2_1
VDDC0P8	VDD
VDD0P75	MGMT_PVDD0P75, MGMT_TRVDD0P75, PCIE_PVDD0P75, PCIE_TRVDD0P75, TRVDD0P75_[3:0], BC[19:0]_PLLVDD[1:0]_0P75
VDD1P2	TVDD1P2_[3:0]
VDD1P8	BS_PLL[1:0]_AVDD1P8, CORE_PLL_AVDD1P8, PP_PLL_AVDD1P8, IP_PLL_AVDD1P8, TS_PLL_AVDD1P8, MS_PLL_AVDD1P8

5.5.1.1 Power-Down Requirement

The VDDC0P8 must ramp down to < 0.1V, and maintain this level for at least 20 ms, before being powered back on.

5.5.2 Reference Clocks

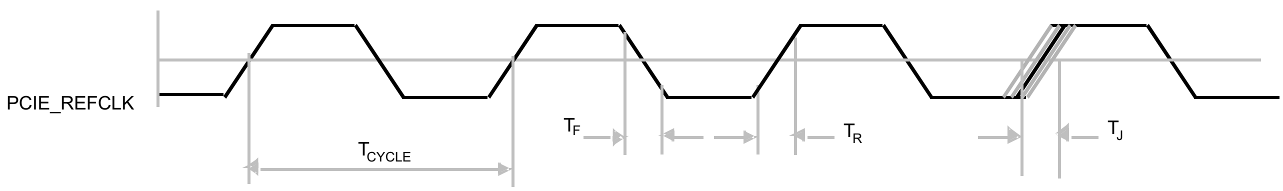
5.5.2.1 PCIE_REFCLK Timing

The following table shows the parameters for 100-MHz differential input and the following figure shows the input timing diagram.

Table 28: PCIE_REFCLK

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency (1/T_{CYCLE})	FREQ	—	100	—	MHz
Tolerance	TOL	–300	—	+300	ppm
Duty cycle	T_h/T_l	40	—	60	%
Rise/fall time (20% to 80%)	T_R/T_F	—	—	1.0	ns/V_{ppd}
Jitter RMS max (10 kHz to 1.5 MHz) for Gen3 8.0-Gb/s operation	T_J	—	—	1.0	ps
Jitter RMS max (10 kHz to 1.5 MHz) for Gen2 5.0-Gb/s operation	T_J	—	—	3.0	ps
Cycle-to-cycle jitter for Gen1 2.5-Gb/s operation	—	—	—	150	ps

Figure 12: PCIE_REFCLK Timing Diagram



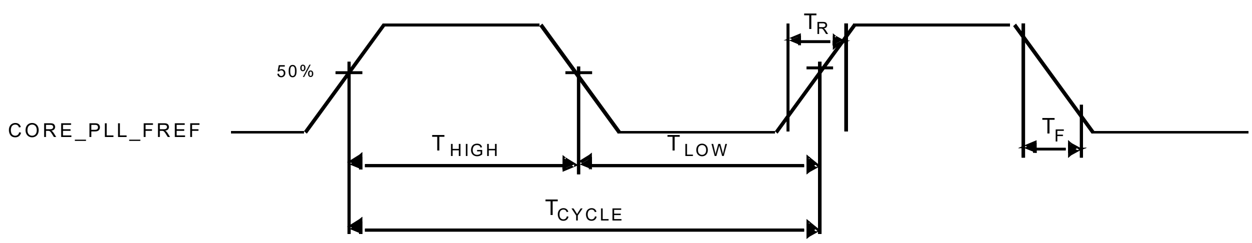
5.5.2.2 CORE_PLL_FREF Timing

The following table shows the parameters for 50-MHz differential input and the following figure shows the input timing diagram.

Table 29: CORE_PLL_FREF Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	C_{freq}	—	50	—	MHz
Frequency deviation	—	–50	—	+50	ppm
Duty cycle distortion	—	40	—	60	%
Rise/fall time (20% to 80%)	T_r/T_f	—	—	1	ns/V_{ppd}
RMS jitter (12 kHz to 20 MHz)	—	—	—	1	ps-rms

Figure 13: CORE_PLL_FREF Input Timing Diagram



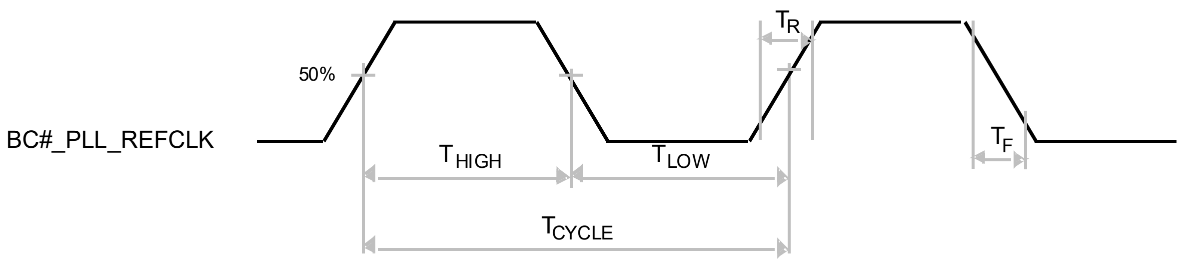
5.5.2.3 Blackhawk7 SerDes Core Reference Clock Timing (BC#_PLL_REFCLK)

The following table shows the parameters for 156.25-MHz differential input and the following figure shows the input timing diagram.

Table 30: BC#_PLL_REFCLK Clock Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	C_{freq}	—	156.25	—	MHz
Frequency deviation	—	–50	—	50	ppm
Duty cycle	T_h/T_l	40	50	60	%
Rise/fall time (20% to 80%)	T_r/T_f	—	—	0.5	ns/V_{ppd}
RMS jitter maximum (12 kHz to 20 MHz)	—	—	—	0.3	ps-rms

Figure 14: BC#_PLL_REFCLK Timing Diagram



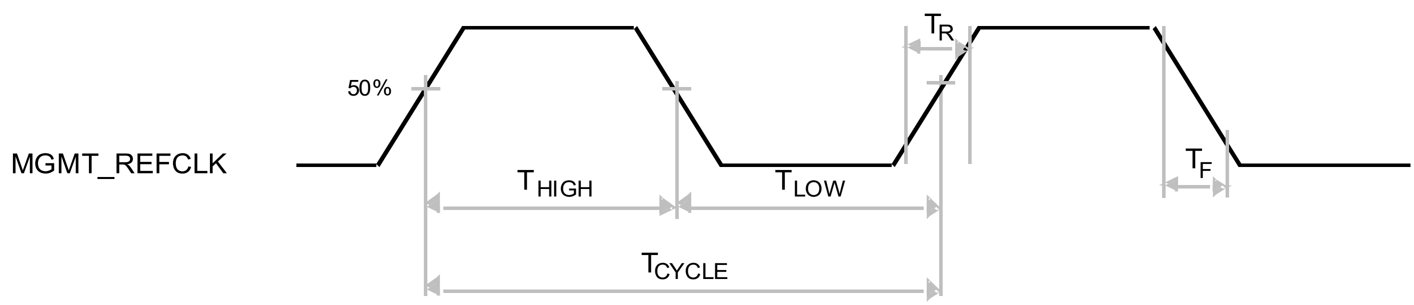
5.5.2.4 Merlin7 SerDes Core Reference Clock Timing (MGMT_REFCLK)

The following table shows the parameters for the 156.25-MHz differential input, and the following figure shows the input timing diagram.

Table 31: MGMT_REFCLK Clock Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	C_{freq}	—	156.25	—	MHz
Frequency deviation	—	–50	—	+50	ppm
Duty cycle	T_h/T_l	40	—	60	%
Rise/fall time (20% to 80%)	T_r/T_f	0.2	—	0.9	ns/V_{ppd}
RMS jitter maximum (12 kHz to 20 MHz)	—	—	—	0.3	ps-rms

Figure 15: MGMT_REFCLK Input Timing Diagram



5.5.2.5 Time Sync Reference Clock Timing (TS_PLL_FREF)

The TS_PLL_FREFP/N clock supports a 50-MHz differential source with characteristics shown in the following table.

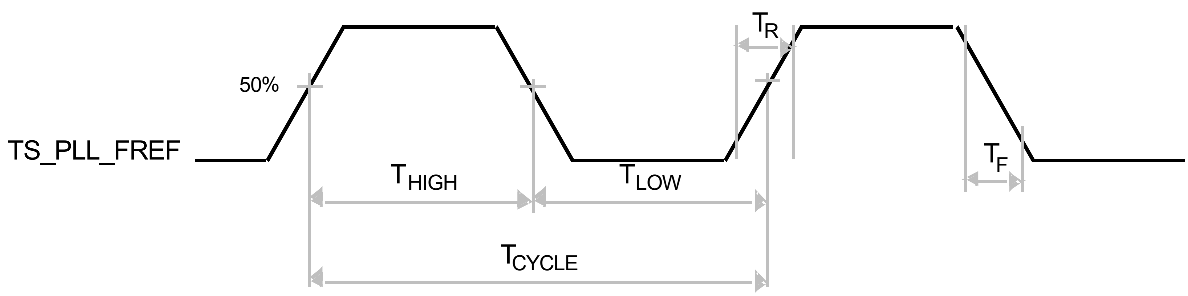
Table 32: TS_PLL_FREF Clock Input Timing Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency	C_{freq}	—	50	—	MHz
Frequency deviation	—	–50	—	+50	ppm
Duty cycle	T_h/T_l	40	—	60	%
Rise/fall time (20% to 80%)	T_r/T_f	—	—	1	ns/V_{ppd}
RMS jitter maximum (12 kHz to 20 MHz)	—	—	—	1	ps-rms
NOTE: The ±50 ppm accuracy is the minimum requirement for the operation of Transparent Clock (TC) functionality only. Input clock accuracy may be application dependent.					

NOTE: Do not use PLL-based oscillators or zero-delay buffers as a source for TS_PLL_FREF because this introduces excessive jitter that may result in unacceptable bit error rate performance.

The following figure shows the input timing diagram.

Figure 16: TS_PLL_FREF Input Timing Diagram



5.5.2.6 BroadSync PLL Reference Clocks Timing (BS_PLL0_FREF / BS_PLL1_FREF)

The BS_PLL0/1_FREFp/n supports differential source with characteristics shown in the following table.

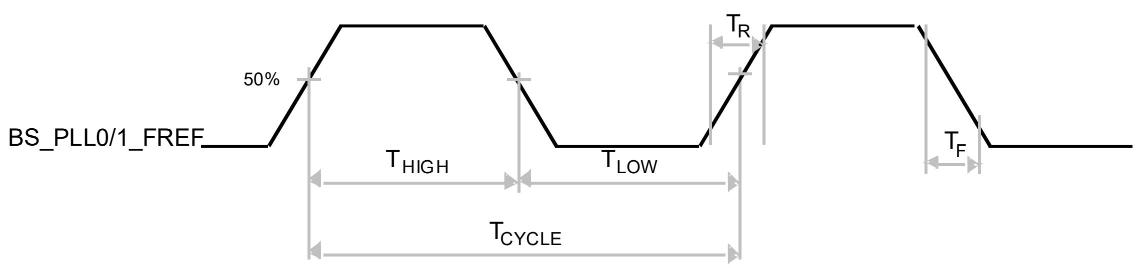
Table 33: BS_PLL0_FREF / BS_PLL1_FREF

Parameter	Symbol	Min.	Typ.	Max.	Unit
Frequency ($1/T_{CYCLE}$)[a]	—	—	12.8	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	20	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	25	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	32	—	MHz
Frequency ($1/T_{CYCLE}$)[a]	—	—	50	—	MHz
Tolerance	—	–50	—	50	PPM
Duty cycle	T_h/T_l	40	50	60	%
Rise/fall time (20% to 80%)	T_r/T^f	—	—	1	ns/V_{ppd}
RMS jitter (12 kHz to 20 MHz)	T_J	—	—	1	ps

a. The Broadcom SDK automatically programs the PLL appropriately for the provided reference clock frequency.

The following figure shows the input timing diagram.

Figure 17: BS_PLL0/1_FREF Input Timing Diagram



5.5.3 Blackhawk7 SerDes Core (TSC-BH7) Interface

The device serial interface confirm to IEEE 802.3bs and 802.3cd specifications:

- Octal SerDes block supporting eight serial links.
- Supports line rates from 10.3125 Gb/s to 53.125 Gb/s (PAM4 53.125 Gb/s or NRZ 26.5625 Gb/s).
- The receiver inputs include on-die AC caps with a low corner frequency, and in most cases, an external AC capacitor is not needed. The main limitation is that the absolute maximum RX input voltage must not exceed 1.6V, and so limits the maximum input Vcm to ~0.7V. The peak amplitude limit should not be exceeded over all PVT and any transient effects, such as reflections and power supply ramps.

The serial interface operating conditions are shown in the following table.

Table 34: Blackhawk7 Interface Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud, symbol rate	B_{PS}	10.3125	—	53.125	Gbaud
Unit interval	UI	18.82	—	96.96	ps

The serial interface receive characteristics are shown in the following table.

Table 35: Blackhawk7 Receiver Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Jitter tolerance	Δt_{RXtot}	Total, peak-to-peak	—	—	0.65	UI
	Δt_{RXdet}	Deterministic, peak-to-peak	—	—	0.37	UI

The serial interface transmit characteristics are shown in the following table.

Table 36: Serial Interface Transmitter Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Output voltage fall time	t_{fall}	80% to 20% (based on 10GBASE-KR waveform, eight ones, eight zeros)	—	TBD	—	ps
Output voltage rise time	t_{rise}	20% to 80% (based on 10GBASE-KR waveform, eight ones, eight zeros)	—	TBD	—	ps
Output differential skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge	—	—	2	ps
Transmit output jitter	Δt_{TXRND}	Random, wideband, RMS	—	0.008	0.010	UI
	Δt_{TXtot}	Total, peak-to-peak	—	0.15	0.28	UI
	Δt_{TXdet}	Deterministic, peak-to-peak	—	0.05	—	UI

5.5.4 Merlin7 SerDes Core (TSC-M7) Interface

The device serial interface supports the following features:

- Quad SerDes block supporting four serial links.
- Supports line rates of 1.25G up to 10.3125 Gbaud per serial link. Oversampling mode is used if speed is below 2.5G.
- Controlled peak-to-peak amplitude.

The serial interface operating conditions are shown in the following table.

Table 37: Merlin7 Interface Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud, symbol rate	B_{PS}	1.25	—	10.3125	Gbaud
Unit interval	UI	—	97	—	ps

The serial interface receive characteristics are shown in the following table.

Table 38: Serial Interface Receive Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Jitter tolerance	Δt_{RXtot}	Total, peak-to-peak	—	—	0.65	UI
	Δt_{RXdet}	Deterministic, peak-to-peak	—	—	0.42	UI

The serial interface transmit characteristics are shown in the following table.

Table 39: Serial Interface Transmit Characteristics

Parameter	Symbol	Description	Min.	Typ.	Max.	Unit
Output voltage fall time	t_{fall}	80% to 20% (based on 10GBASE-KR waveform, eight ones, eight zeros)	24	—	36	ps
Output voltage rise time	t_{rise}	20% to 80% (based on 10GBASE-KR waveform, eight ones, eight zeros)	24	—	36	ps
Output differential skew	t_{skewo}	50% rising/falling versus 50% falling/rising edge	—	—	5	ps
Transmit output jitter	Δt_{TXRND}	Random, wideband, RMS	—	0.008	0.130	UI
	Δt_{TXtot}	Total, peak-to-peak	—	—	0.18	UI
	Δt_{TXdet}	Deterministic, peak-to-peak	—	0.05	—	UI

5.5.5 PCIe Interface

5.5.5.1 PCIe Receiver

Figure 18: PCIe_RX Timing Diagram

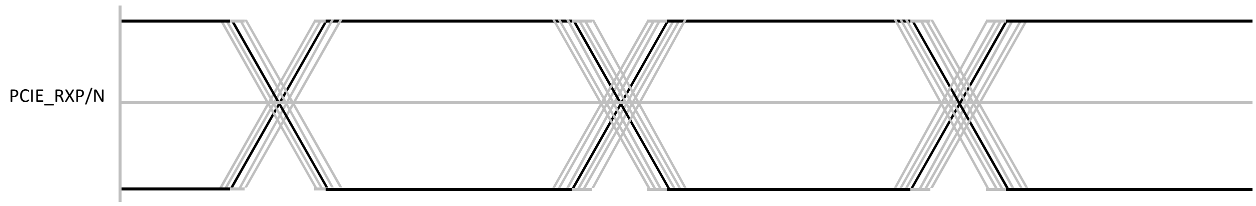


Table 40: PCIe_RX

Parameter	Symbol	Min.	Typ.	Max.	Unit
Baud rate	FREQ	—	2.5, 5.0, or 8.0	—	Gbaud
Minimum RX eye width	T_J	0.6	—	—	UI
NOTE: Includes on-chip AC-coupling capacitors.					

5.5.5.2 PCIe Transmitter

Figure 19: PCIe_TX Timing Diagram

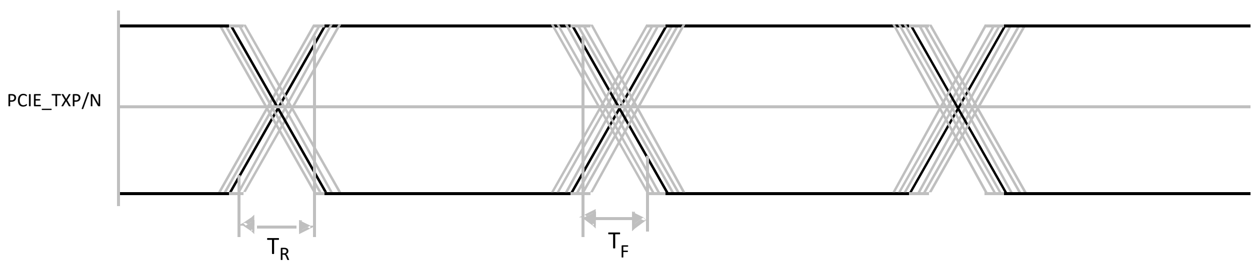


Table 41: PCIe_TX Output Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Baud rate	FREQ	—	—	2.5, 5.0, or 8.0	—	Gbaud
Output rise/fall time (20% to 80%)	T_R/T_F	—	30	—	90	ps
Output deemphasis[a]	V_{OEQ}	Gen1: 2.5 Gb/s Gen2: 5.0 Gb/s	–3.0 –5.5	–3.5 –6.0	–4.0 –6.5	dB
Minimum TX eye width	T_J	—	0.75	—	—	UI

a. Output deemphasis figures listed in this table are the default settings. TX deemphasis can be software configured in the range of 0 dB to 8 dB, overriding the defaults.

5.5.6 BroadSync Interface

The following figure and the following table show the slave mode input timing.

Figure 20: BroadSync Input Timing – Slave Mode

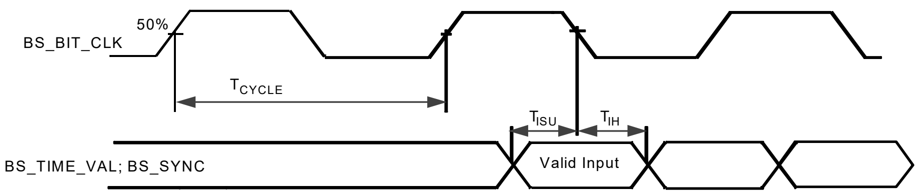


Table 42: BroadSync Input Timing – Slave Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	500	—	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	%
BS_TIME_VAL; BS_SYNC input setup time	t_{ISU}	20	—	—	ns
BS_TIME_VAL; BS_SYNC input hold time	t_{IH}	0	—	—	ns

The following figure and the following table show the master mode input timing.

Figure 21: BroadSync Output Timing – Master Mode

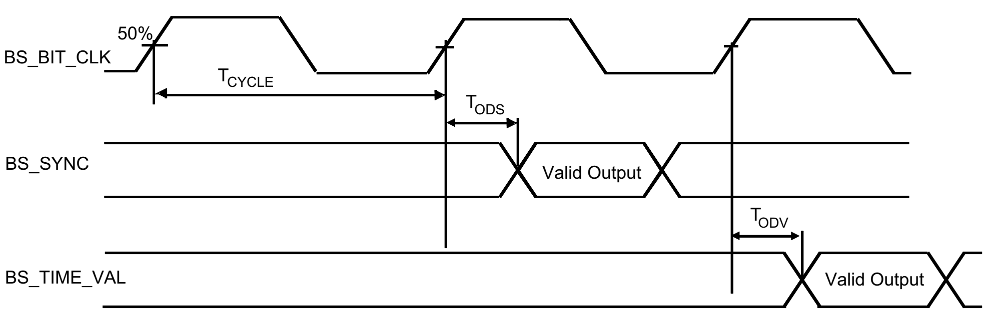


Table 43: BroadSync Output Timing – Master Mode

Parameters	Symbol	Min.	Typ.	Max.	Unit
BS_BIT_CLK cycle time	t_{CYC}	500	—	—	ns
BS_BIT_CLK duty cycle	t_{HIGH}	40	—	60	%
BS_SYNC output delay	t_{ODS}	0	—	25	ns
BS_TIME_VAL output delay	t_{ODV}	0	—	25	ns

5.5.7 Broadcom Serial Controller Interface

Two of the Broadcom serial controller (BSC) interfaces can operate in master-only mode, while the remaining BSC interface can operate in slave-only mode.

Figure 22: BSC Timing Diagram

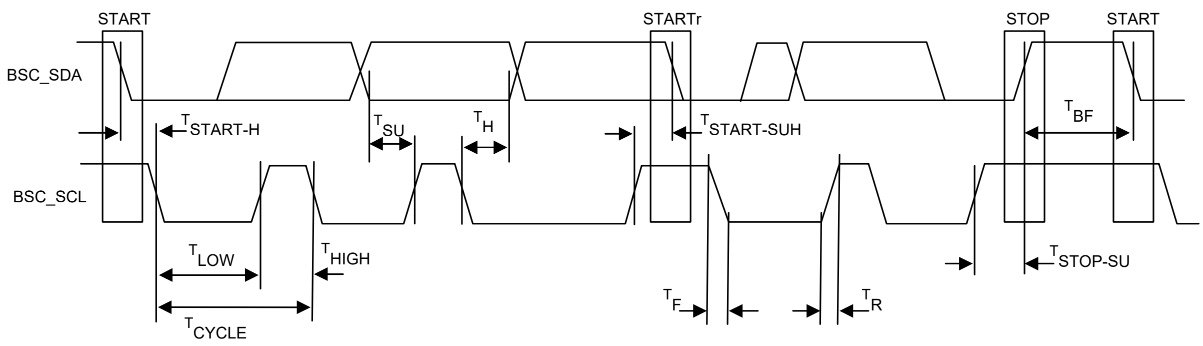


Table 44: BSC Master/Slave Fast-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	400	kHz
BSC_SCL cycle time	T_{CYCLE}	2.5	—	—	µs
BSC_SCL low time	T_{LOW}	1.3	—	—	µs
BSC_SCL high time	T_{HIGH}	0.6	—	—	µs
Data hold time	T_H	0	—	—	µs
Data setup time	T_{SU}	100	—	—	ns
Rise time, clock, and data[a]	T_R	—	—	300	ns
Fall time, clock, and data (GBD)	T_F	—	—	300	ns
Hold time, start or repeated start	$T_{START–H}$	0.6	—	—	µs
Setup time, repeated start	$T_{START–SU}$	0.6	—	—	µs
Setup time, stop	$T_{STOP–SU}$	0.6	—	—	µs
Bus free time (between stop and start)	T_{BF}	1.3	—	—	µs

a. BSC_SCL and BSC_SDA are open-drain outputs. The rise time is dependent on the strength of the external pull-up resistor, which must be chosen to meet the rise time requirement.

Table 45: BSC Master/Slave Standard-Mode Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
BSC_SCL clock frequency	f_{CLK}	—	—	100	kHz
BSC_SCL cycle time	T_{CYCLE}	10	—	—	µs
BSC_SCL low time	T_{LOW}	4.7	—	—	µs
BSC_SCL high time	T_{HIGH}	4.0	—	—	µs
Data hold time	T_H	0.0	—	—	µs
Data setup time	T_{SU}	250	—	—	ns
Rise time, clock, and data[a] (see note)	T_R	—	—	1000	ns
Fall time, clock, and data (GBD)	T_F	—	—	300	ns
Hold time, start, or repeated start	$T_{START–H}$	4.0	—	—	µs
Setup time, repeated start	$T_{START–SU}$	4.7	—	—	µs
Setup time, stop	$T_{STOP–SU}$	4.0	—	—	µs
Bus free time (between stop and start)	T_{BF}	4.7	—	—	µs

a. BSC_SCL and BSC_SDA are open-drain outputs. The rise time is dependent on the strength of the external pull-up resistor, which must be chosen to meet the rise time requirement.

The device drives the BSC_SCL clock with a programmable speed of 100 kHz or 400 kHz based on the mode bit called MODE_400. The device drives BSC_SDA during a write operation and samples BSC_SDA during a read operation.

5.5.8 LED Interface

LED[1:0]_CLK and LED[1:0]_DATA are outputs. LED[1:0]_CLK output clock period is programmable based on firmware but defaults to 200 ns (5.0 MHz).

Figure 23: LED Timing Diagram

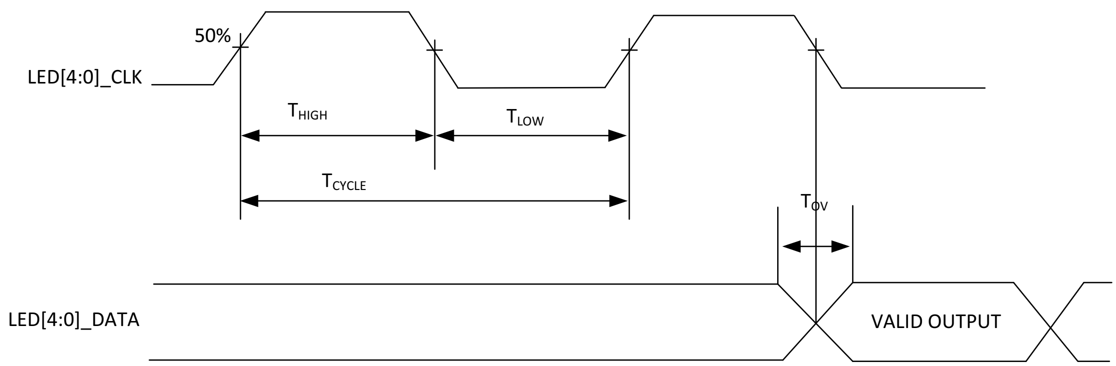


Table 46: LED Timing[a]

Parameter	Symbol	Min.	Typ.	Max.	Unit
LED[4:0]_CLK clock frequency	f_{CLK}	—	5	5	MHz
LED[4:0]_CLK cycle time	T_{CYCLE}	200	200	—	ns
LED[4:0]_CLK high time	T_{HIGH}	70	100	130	ns
LED[4:0]_CLK low time	T_{LOW}	70	100	130	ns
LED[4:0]_DATA output valid time	T_{OV}	–15	—	15	ns

a. Timing figures are specified at the 50% crossing thresholds.

5.5.9 Management Interface (MIIM)

5.5.9.1 MDIO AC Characteristics

Figure 24: MIIM Interface Timing Diagram

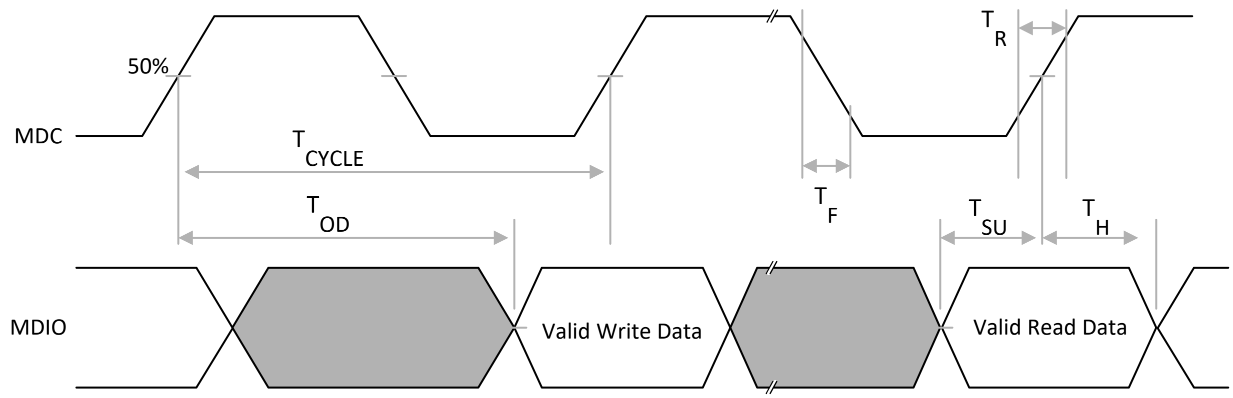


Table 47: MDC/MDIO Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
MDC clock frequency	f_{CLK}	—	2.5	12.5	MHz
MDC cycle time	T_{CYCLE}	80	400	—–	ns
MDC duty cycle	—	40	—	60	%
MDIO setup time	T_{SU}	20	—	—	ns
MDIO hold time	T_H	0	—	—	ns
MDIO output delay	T_{OD}	10	—	30	ns

NOTE:
- Output load conditions = 25 pF.
- External device to conform to IEEE specifications.
- MDIO output delay is programmable.

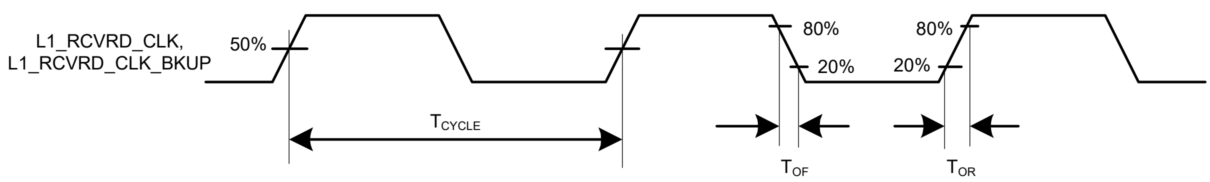
5.5.10 Synchronous Ethernet Interface

5.5.10.1 L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Table 48: L1_RCVRD_CLK and L1_RCVRD_CLK_BKUP Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP cycle time	T_{CYCLE}	6.4	—	40	ns
L1_RCVRD_CLK, L1_RCVRD_CLK_BKUP duty cycle	T_{HIGH}	45	—	55	%

Figure 25: Synchronous Ethernet Output Timing Diagram



5.5.11 JTAG Interface

Figure 26: JTAG Timing Diagram

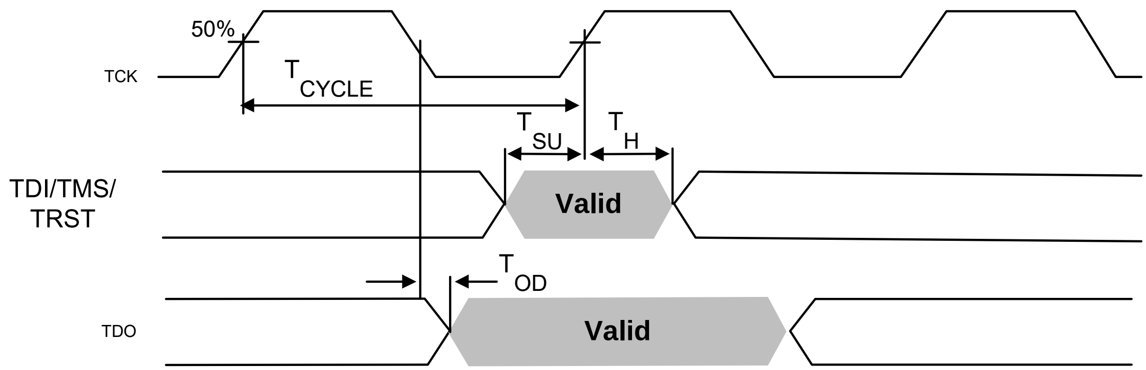


Table 49: JTAG AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
JTCK clock frequency	f_{CLK}	—	—	12.5	MHz
JTCK duty cycle	—	45	—	55	%
JTCK cycle time	t_{CYCLE}	80.0	—	—	ns
JTCK falling edge to output valid Applicable to JTDO	t_{OD}	0	—	25	ns
Data input setup time before JTCK Applicable to JTDI and JTMS	t_{SU_JT}	13	—	—	ns
Data hold time after JTCK rise Applicable to JTDI and JTMS	t_{H_JT}	5	—	—	ns
Input setup time before JTCK rising edge Applicable to JTRST_N	t_{SU_JTRS}	15	—	—	ns
Input hold time after JTCK rising edge Applicable to JTRST_N	t_{H_JTRS}	5	—	—	ns

NOTE: Unless otherwise noted, the specifications are valid across the following operating conditions:

- The threshold value is at 50% of the applicable I/O rail voltage.
- The default loading on an output is 5 pF.

5.5.12 OOBFC Interface

Figure 27: OOBFC Interface Output Timing Diagram

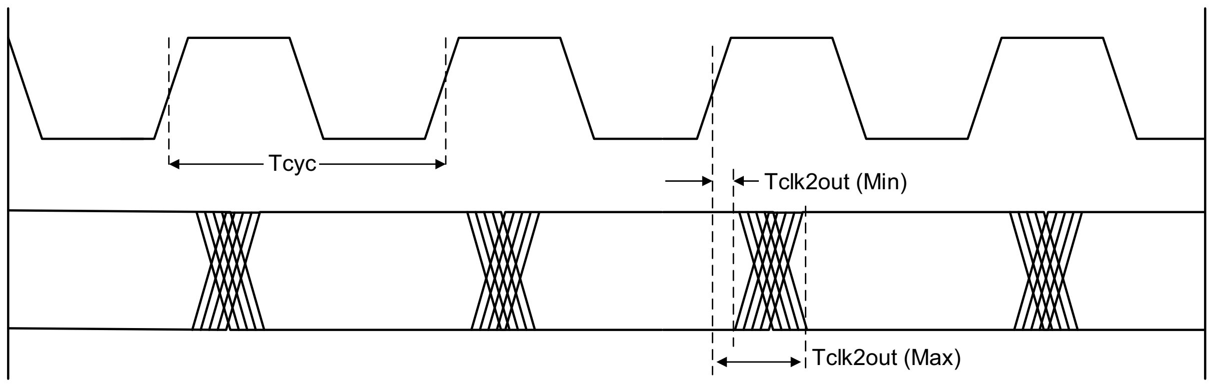


Table 50: OOBFC Output Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
OOBFC_TX_CLK cycle time	t_{CYC}	—	8	—	ns
OOBFC_TX_CLK duty cycle	t_{DUTY}	40	—	60	%
OOBFC_TX_SYNC output delay	$t_{CLK2OUT}$	0.8	—	4.5	ns
OOBFC_TX_DATA output delay	$t_{CLK2OUT}$	0.8	—	4.5	ns

5.5.13 QSPI Interface

Figure 28: QSPI Timing (Read/Write Mode Using MSPI Controller)

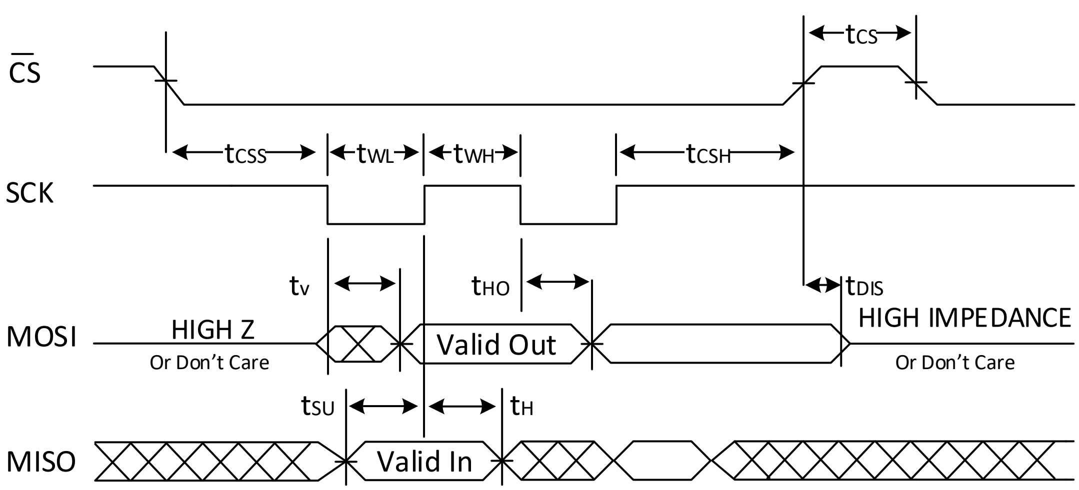


Table 51: QSPI Timing (Read/Write Mode Using MSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	15.625	MHz
SCK clock low period	t_{WL}	0.5 / Fsck – 0.5	—	—	ns
SCK clock high period	t_{WH}	0.5 / Fsck – 0.7	—	—	ns
CS lead time	t_{CSS}	0.5 / Fsck – 4	—	—	ns
CS trail time	t_{CSH}	9.6	—	—	ns
CS high time	t_{CS}	81	—	—	ns
MOSI output valid	t_V	—	—	16	ns
MOSI output hold	t_{HO}	4	—	—	ns
MISO input setup	t_{SU}	9	—	—	ns
MISO input hold	t_H	4	—	—	ns
MOSI output disable[a]	t_{DIS}	—	—	—	ns

a. The IP_QSPI_MOSI signal is always driven.

Figure 29: QSPI Timing (Read/Write Mode Using BSPI Controller)

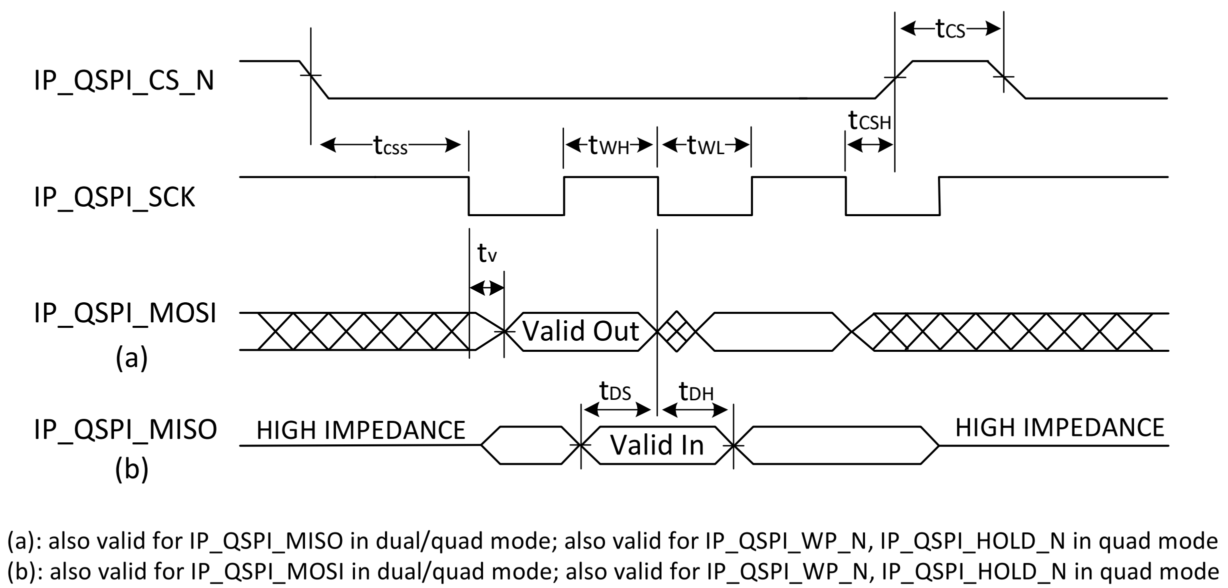


Table 52: QSPI Timing (Boot Read Mode Using BSPI Controller)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	62.5	MHz
SCK clock low period	t_{WL}	0.5 / Fsck – 0.5	—	—	ns
SCK clock high period	t_{WH}	0.5 / Fsck – 0.5	—	—	ns
CS lead time	t_{CSS}	1 / Fsck – 2.9	—	—	ns

Table 52: QSPI Timing (Boot Read Mode Using BSPI Controller) (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CS trail time	t_{CSH}	–1.6	—	—	ns
MOSI output valid	t_V	–1.6	—	3	ns
MISO input setup	t_{SU}	4	—	—	ns
MISO input hold	t_H	1.3	—	—	ns

5.5.14 SPI Interface

Figure 30: SPI Timing (SPI Master – Mode 0)

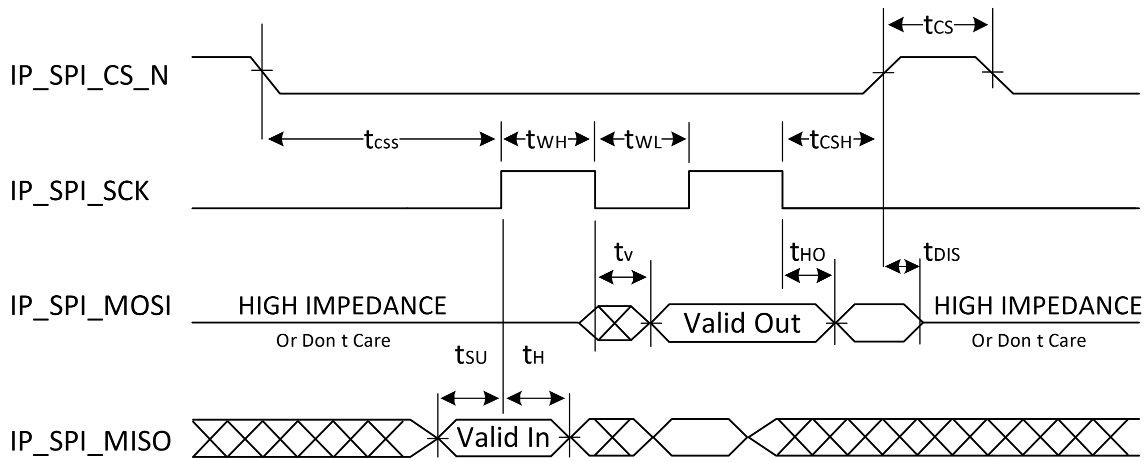


Figure 31: SPI Timing (SPI Master – Mode 3)

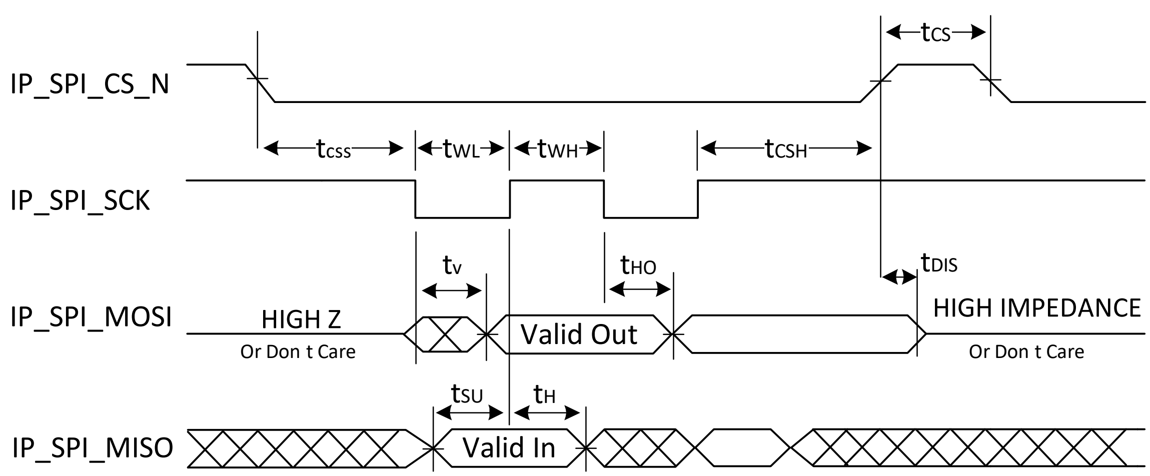


Table 53: SPI Timing (Master Mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCK frequency	F_{SCK}	—	—	31.25	MHz
SCK clock low period	t_{WL}	0.5 / Fsck – 1	—	—	ns
SCK clock high period	t_{WH}	0.5 / Fsck – 1	—	—	ns
CS lead time	t_{CSS}	0.5 / Fsck – 4	—	—	ns
CS trail time	t_{CSH}	0.5 / Fsck – 4	—	—	ns
CS high time (SPH = 0)	t_{CS}	0.5 / Fsck	—	—	ns
CS high time (SPH = 1)	t_{CS}	0	—	—	ns
MOSI output valid	t_{V}	—	—	4	ns
MOSI output hold	t_{HO}	–4	—	—	ns
MISO input setup	t_{SU}	9	—	—	ns
MISO input hold	t_{H}	0	—	—	ns
MOSI output disable	t_{DIS}	—	—	4	ns

Chapter 6: Standard Electrical Characteristics

6.1 PAM4 Electrical Characteristics

The device is designed in compliance to CEI-56G-VSR, CEI-56G-LR, IEEE 802.3bs CDAUI-8 C2C/C2M, and IEEE 802.3cd standards.

6.2 40G XLAUI Electrical Characteristics

6.2.1 Transmitter

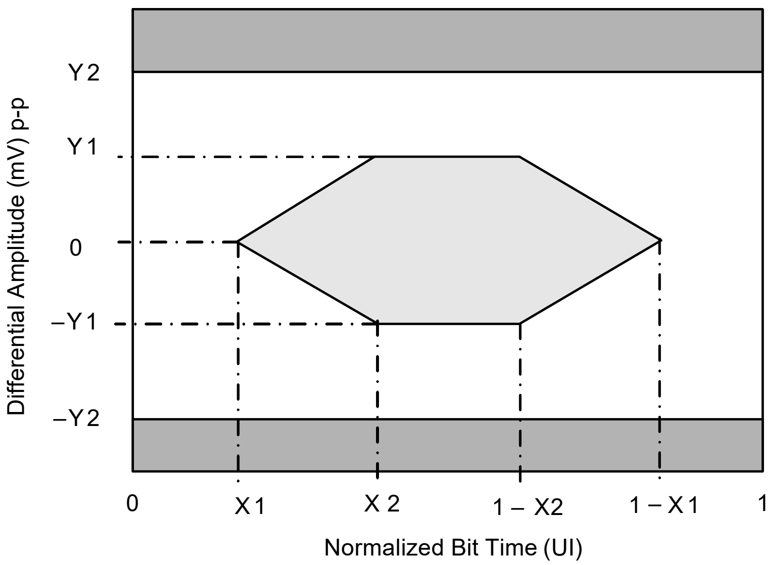
Table 54: XLAUI TX

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output speed per lane	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Differential output voltage (peak-to-peak)	VOD	—	—	760	mV_{ppd}
Transmit eye mask (Figure 32)	X1	—	—	0.16	UI
Transmit eye mask (Figure 32)	X2	—	—	0.38	UI
Transmit eye mask (Figure 32)	Y1	200	—	—	mV
Transmit eye mask (Figure 32)	Y2	—	—	380	mV
Differential output return loss (min.)	Equation[a]	—	—	—	dB
Common-mode output return loss (min.)	Equation[b]	—	—	—	dB
Output rise time (20% to 80%)	Tr	24	—	—	pS
Output fall time (20% to 80%)	Tf	24	—	—	pS
Output jitter at $1e^{-12}$ BER Deterministic Total	 sDJ sTJ	 — —	 — —	 0.17 0.32	 UI UI

a. Return loss ≤ 12 dB for 10 MHz ≤ *f* < 2.125 GHz.
Return loss ≤ [6.5 – 13.33 log (*f* / 5.5)] dB for 2.125 GHz ≤ *f* ≤ 11.1 GHz

b. Return loss ≤ 9 dB for 10 MHz ≤ *f* < 2.125 GHz.
Return loss ≤ [3.5 – 13.33 log (f / 5.5)] dB for 2.125 GHz ≤ *f* ≤ 7.1 GHz
Return loss ≤ 2 dB for 7.1 GHz < f < 11.1 GHz.

Figure 32: XLAUI Transmit Eye Mask



6.2.2 Receiver

Table 55: XLAUI RX

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver coupling	AC	0.05	—	0.1	µF
Receive eye mask (Figure 33)	X1	—	—	0.31	UI
Receive eye mask (Figure 33)	X2	—	—	0.5	UI
Receive eye mask (Figure 33)	Y1	42.5	—	—	mV
Receive eye mask (Figure 33)	Y2	—	—	425	mV
Differential input return loss	Equation[a]	—	—	—	dB
Common-mode input return loss	Equation[b]	—	—	—	dB
Receiving speed per lane	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Sinusoidal jitter tolerance	Figure 34	—	—	—	bps
Bit error rate based channel characteristics per Clause 83A in IEEE 802.3ba.	—	—	—	1e-12	bps

a. Return loss ≤ 12 dB for 10 MHz ≤ *f* < 2.125 GHz
Return loss ≤ [6.5 – 13.33 log (*f* / 5.5)] dB for 2.125 GHz ≤ *f* ≤ 11.1 GHz

b. Return loss ≤ 15 dB for 10 MHz ≤ *f* < 11.1 GHz

Figure 33: XLAUI Receive Eye Mask

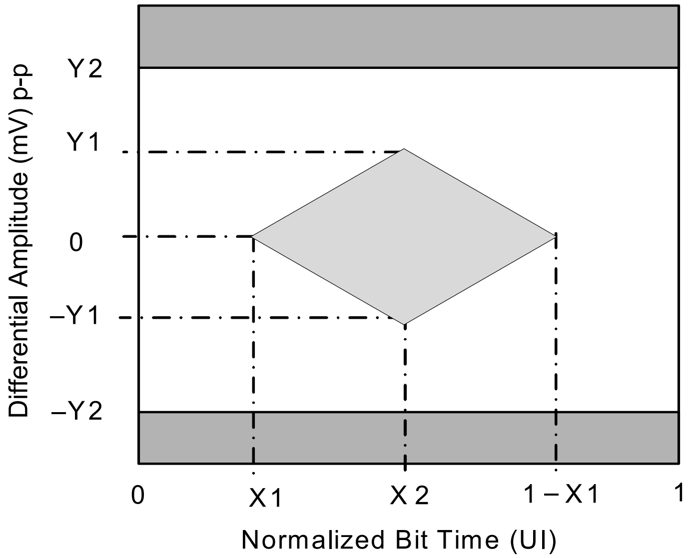
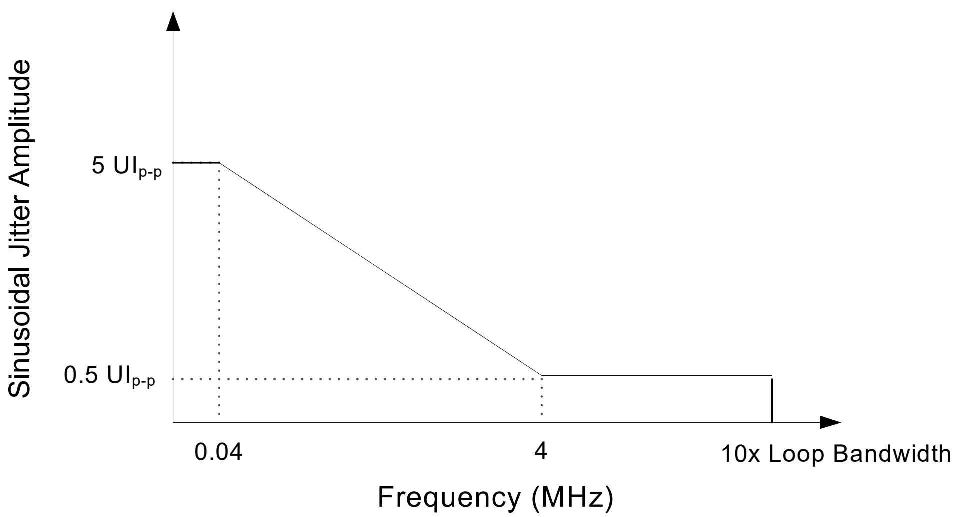


Figure 34: Single-Tone Sinusoidal Jitter Mask



6.3 10GBASE-KR Electrical Characteristics

6.3.1 Transmitter

Table 56: 10GBASE-KR TX

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output speed	—	–100 ppm	+10.3125 ppm	+100 ppm	Gbaud
Differential output voltage (peak-to-peak) based on 101010 pattern	VOD	—	—	1200	mV_{ppd}
Output voltage (peak-to-peak) when TX is disabled	VOD	—	—	30	mV_{ppd}
Common-mode voltage	VCM	0	—	1.9V	V
Differential output return loss (min.)	Equation[a]	—	—	—	dB
Common-mode output return loss (min.)	Equation[b]	—	—	—	dB
Output rise time (20% to 80%)	Tr	24	—	47	pS
Output fall time (20% to 80%)	Tf	24	—	47	pS
Output jitter at 1e-12 BER					
■ Random	sRJ	—	—	0.15	UI
■ Deterministic	sDJ	—	—	0.15	UI
■ Duty cycle distortion	sDCD	—	—	0.035	UI
■ Total	sTJ	—	—	0.28	UI

a. Return loss ≤ 9 dB for 50 MHz ≤ f ≤ 2500 MHz
Return loss ≤ [9 – 12 log (f / 2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz

b. Return loss ≤ 6 dB for 50 MHz ≤ f < 2500 MHz
Return loss ≤ [6 – 12 log (f / 2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz

6.3.2 Receiver

Table 57: 10GBASE-KR RX

Parameter	Symbol	Min.	Typ.	Max.	Unit
Receiver coupling	AC	0.05	—	0.1	µF
Differential input voltage (peak-to-peak)	VID	—	—	1200	mVp-p
Differential input return loss (min.)	Equation[a]	—	—	—	dB
Receiving speed	—	–100 ppm	10.3125 ppm	+100 ppm	Gbaud

a. Return loss ≤ 9 dB for 50 MHz ≤ f ≤ 2500 MHz
Return loss ≤ [9 – 12 log (f / 2500 MHz)] dB for 2500 MHz ≤ f ≤ 7500 MHz

Chapter 7: Thermal Specifications

7.1 Thermal Requirements

The tables in this section provide device thermal specifications for the different packages. The maximum θ_{JA} is a function of the maximum allowed ambient air temperature of the system and is given for ambient air temperatures of 50°C and 70°C.

The device requires a steady-state maximum junction temperature at 105°C. It allows an excursion of junction temperature up to 115°C with a maximum total accumulated excursion time of 15 days per year and up to four consecutive days. During the excursion period, the device continues to operate, but its performance may degrade.

Table 58: BCM56780 Package Thermal Specifications for TA = 70°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power dissipation	P	—	—	230	W
Maximum junction temperature	T	—	—	105	°C
Maximum ambient temperature	A	—	—	70	°C
Maximum calculated θ_{JA}: (T – A) / P	O	—	—	0.152	°C/W

Table 59: BCM56784 Package Thermal Specifications for TA = 70°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power dissipation	P	—	—	215	W
Maximum junction temperature	T	—	—	105	°C
Maximum ambient temperature	A	—	—	70	°C
Maximum calculated θ_{JA}: (T – A) / P	O	—	—	0.163	°C/W

7.2 Heat Sink

7.2.1 Heat Sink Selection

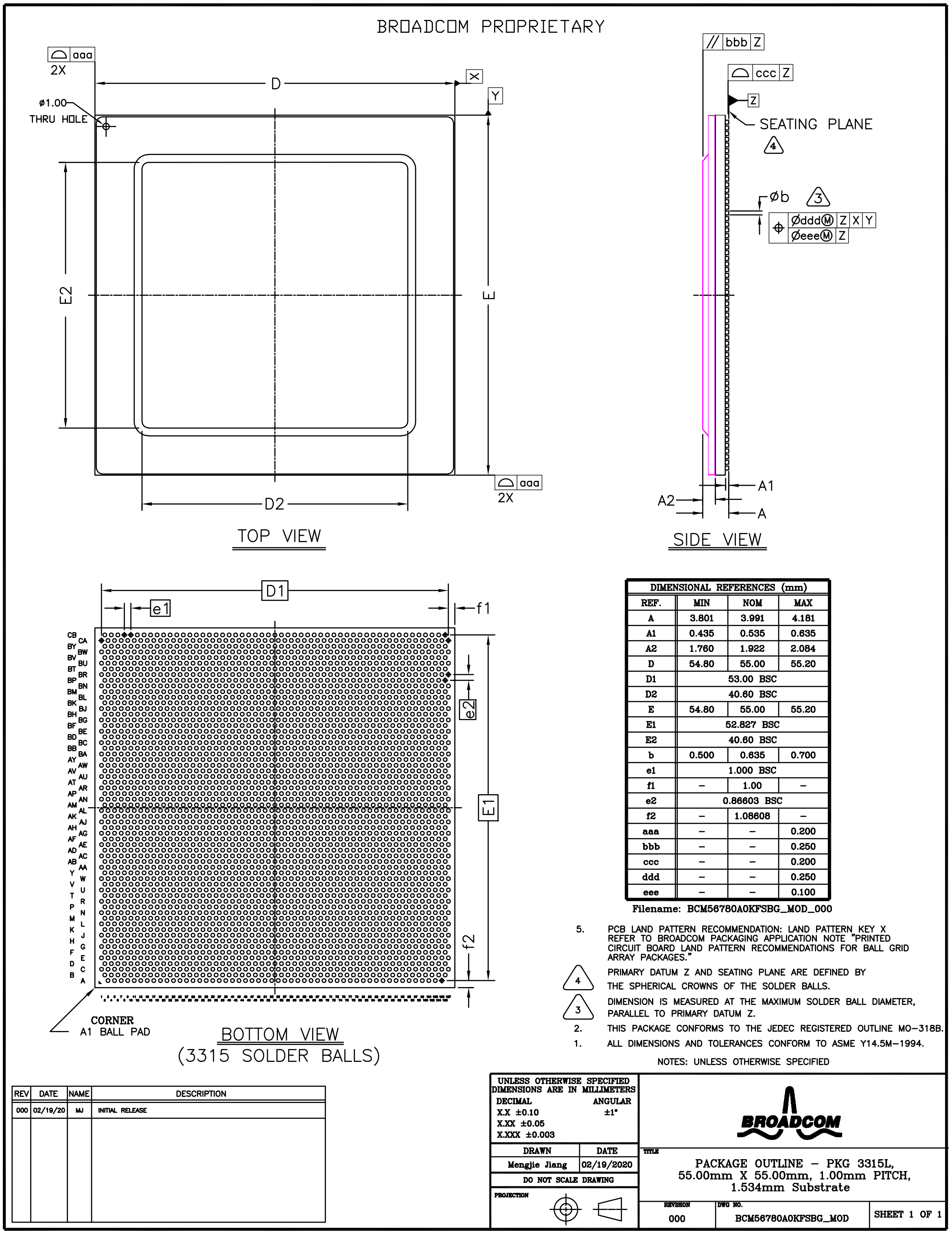
The device is required to be used with a heat sink. The end-use thermal environment combined with the operating mode of the device dictate the required thermal characteristics (size, thermal resistance, and so forth) of the heat sink.

7.2.2 Heat Sink Attachment

For heat sink attachment details, refer to the *BCM56780 Hardware Design Guidelines* (56780-DG1xx).

Chapter 8: Mechanical Information

Figure 35: 3315-Ball FCBGA (55 mm × 55 mm)



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	3.801	3.991	4.181
A1	0.435	0.535	0.635
A2	1.760	1.922	2.084
D	54.80	55.00	55.20
D1		53.00 BSC	
D2		40.60 BSC	
E	54.80	55.00	55.20
E1		52.827 BSC	
E2		40.60 BSC	
b	0.500	0.635	0.700
e1		1.000 BSC	
f1	–	1.00	–
e2		0.86603 BSC	
f2	–	1.08608	–
aaa	–	–	0.200
bbb	–	–	0.250
ccc	–	–	0.200
ddd	–	–	0.250
eee	–	–	0.100

Chapter 9: Ordering Information

The following table lists the product part numbers available for order, their descriptions, and selected specifications.

Table 60: Device Ordering Information

Part Number	Description	I/O Bandwidth	Package	Temperature
BCM56780A0KFSBG	160 × 50G SerDes	8.0 Tb/s	3315-ball, 55 mm × 55 mm, RoHS-compliant	0°C to 70°C
BCM56784A0KFSBG	96 × 50G + 32 × 25G SerDes	5.6 Tb/s	3315-ball, 55 mm × 55 mm, RoHS-compliant	0°C to 70°C

9.1 PB-Free Packaging

Broadcom offers Pb-free package. Pb-free parts have a letter G added to the top line of the part marking. Refer to *Reflow Process Guidelines for Surface Mount Assemblies* (Packaging-AN1xx) for details. Broadcom Pb-free parts comply with RoHS and Waste Electrical and Electronic Equipment (WEEE) directives. Broadcom Pb-free parts are fully RoHS 6/6 compatible and require no exemption to comply with European limitations on hazardous substances. The following table shows the solder ball composition and maximum reflow temperature Pb-free parts.

Table 61: Solder Ball Composition and Recommended and Maximum Reflow Temperature

Part Number	Solder Ball Composition	Recommended Reflow Peak Temperature	Maximum Allowed Reflow Peak Temperature
Pb-free RoHS-compliant package	95.5% Sn, 3% Ag, 0.5% Cu	232°C to 237°C	245°C

Refer to the *SMT Guidelines* for more information. Refer to *Reflow Process Guidelines for Surface Mount Assemblies* (Packaging-AN1xx).

References

The references in this section may be used with this document.

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document Name
BCM56780 Hardware Design Guidelines
BCM56780 Theory of Operation
Datacenter NPL Application (DNA) Feature List
Reflow Process Guidelines for Surface Mount Assemblies Application Note
BCM56883 to BCM56780 Migration Guide
BCM56780 A0 Family Ballout Rev X.X
BCM56784 A0 Family Ballout Rev X.X

Glossary

The following is a list of acronyms and other terms used in Broadcom documents.

Table 62: Acronyms and Abbreviations

Term	Description
ACL	Access control list
API	Application Programming Interface
AVS	Adaptive voltage scaling
BSC	Broadcom Serial Controller
BSPI	Boot SPI (serial peripheral interface)
CMIC	CPU management interface controller
CMICx	CPU management interface controller
CoS	Class-of-Service
DCI	Data center interconnect
DLB	Dynamic load balancing
DMA	Direct memory access
DP	Datapath pipeline
ECN	Explicit congestion notification
FEC	Forward error correction
GPIO	General-purpose I/O
LED	Light emitting diode
MIIB	Management information base
MIIM	MII management
MMU	Memory management unit
MSDC	Massively scalable data center
MSPI	Master SPI (serial peripheral interface)
NPL	Network programming language
OC	Ordinary clock
OOBFC	Out-of-band flow control
PAM4	Pulse amplitude modulation
PCIe	Peripheral component interconnect express
PFC	Priority flow control
PFM	Port filter mode
PHY	Physical layer interface
PTP	Precision time protocol
QoS	Quality-of-Service
QSPI	Quad serial peripheral interface
RAF	Read-ahead FIFO
RMON MIIB	Remote monitoring management information base
RR	Round-robin
RTS	Real-time subsystem
SDK	Software development kit
SDKLT	Software development kit – logical table

Table 62: Acronyms and Abbreviations (Continued)

Term	Description
SerDes	Serializer/Deserializer
SMON MIIB	Switched network monitoring management information base
SNMP	Simple network management protocol
SP	Strict priority
srTCM	Single-rate three color marking
TC	Transparent clock
TDM	Time division multiplexing
ToR	Top-of-Rack
trTCM	Two-rate three color marking
TSC	Time division multiplexing SerDes Controller
WDRR	Weighted deficit round-robin
WRED	Weighted random early detection
WRR	Weighted round-robin