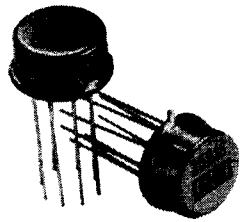
BURR-BROWN®

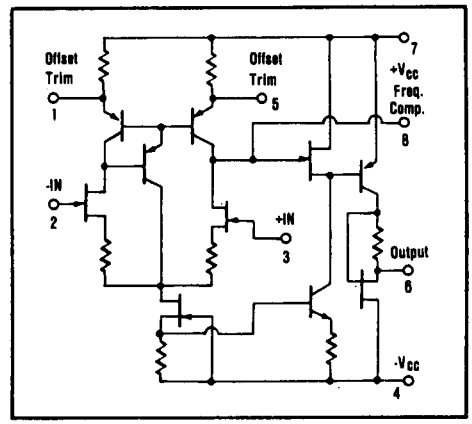


3551 SERIES

Wideband and Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- **REDUCES WIDEBAND ERRORS**
  - **50MHz Gain-bandwidth product (ACL ≥10)**
  - **250V/μs slew rate (Cf = 0)**
- **VERSATILE**
  - **Single compensation capacitor allows optimum response**
  - **True differential input**
- **PRESERVES DC ACCURACY**
  - **Bias current, 100pA, max**
  - **Laser-trimmed offset voltage**



DESCRIPTION

The 3551 is designed to offer the user versatility in wideband steady state and fast transient applications. The use of a single external compensation capacitor allows the user to optimize frequency response for maximum bandwidth for a variety of closed loop gains and capacitive loads. The amplifier is stable at closed loop gains of greater than 10V/V, with no external compensation and may be stabilized at all gains with the single 10pF compensation capacitor.

In addition to the excellent dynamic response characteristics, the 3551 also has good DC properties. The use of a monolithic FET input stage gives the 3551 very low input bias and offset currents. This is in contrast to the high input currents usually associated with fast amplifiers having bipolar input stages. Also, the input offset voltage and offset voltage drift are low as a result of Burr-Brown's laser-trimming techniques.

Unlike many wideband and fast settling amplifiers, the 3551 has a true differential input. This means it can provide its excellent wideband response in the inverting, noninverting, current-to-voltage and difference configurations.

The 3551 is an excellent choice for applications such as fast D/A and A/D converters, high speed comparators and fast sampling circuits, to name just a few.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-301C

SPECIFICATIONS

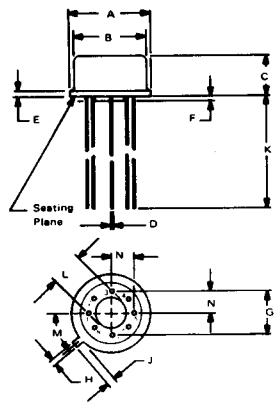
ELECTRICAL

Specifications typical at 25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3551J	3551S
OPEN LOOP GAIN, DC		
No Load 1kΩ, Load min	100dB 88dB	
RATED OUTPUT		
Voltage, min Current, min Open Loop Output Resistance	±10V ±10mA 100Ω at 1MHz	
DYNAMIC RESPONSE		
Gain-Bandwidth Product Gain = 1000 Gain = 10 Slew Rate (Cf = 0)	 50MHz 50MHz 250V/μsec	
INPUT OFFSET VOLTAGE		
Initial Offset, 25°C, max vs. Temp[1] vs. Supply Voltage vs. Time	±1mV ±50μV/°C ±500μV/V ±100μV/mo	
INPUT BIAS CURRENT		
Initial Bias, 25°C, max vs. Temperature vs. Supply Voltage	-400pA (after full warm-up) doubles every 10°C ±1pA/V	
INPUT DIFFERENCE CURRENT		
Initial Difference, 25°C	±40pA	
INPUT IMPEDANCE		
Differential Common-mode	$10^{11}\Omega$ || 3pF $10^{11}\Omega$ || 3pF	
INPUT NOISE		
Voltage, 0.01Hz to 10Hz, p-p Voltage, 10Hz to 10kHz, rms Current, 0.01Hz to 10Hz, p-p Current, 10Hz to 10kHz, rms	20μV 4μV 0.2pA 1.5pA	
INPUT VOLTAGE RANGE		
Common-mode Voltage Common-mode Rejection Max. Safe Input Voltage	±(|Vcc|-5)V 70dB at +5V, -10V ±Supply	
POWER SUPPLY		
Rated Voltage Voltage Range, derated Current, quiescent[1]	±15VDC ±5VDC to ±20VDC 11mA (15mA max)	
TEMPERATURE RANGE		
Specification Operating Storage	0°C to +70°C -55°C to +125°C -65°C to +150°C	-55°C to +125°C -55°C to +125°C

NOTE:
1. The use of a finned heat sink is recommended.

MECHANICAL TO-99



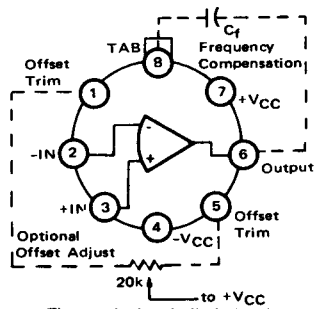
NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

Pin numbers shown for reference only
Numbers may not be marked on package

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

CONNECTION DIAGRAM

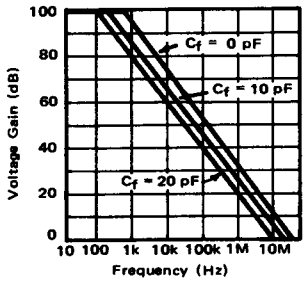


The case is electrically isolated.

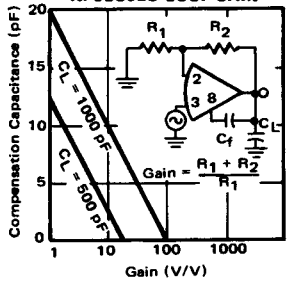
TYPICAL PERFORMANCE CURVES

T_A = 25°C V_s = ±15 VDC unless otherwise indicated.

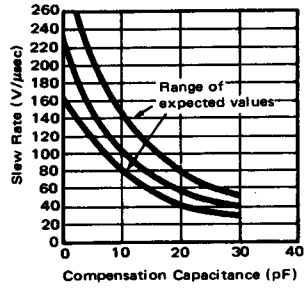
OPEN LOOP RESPONSE



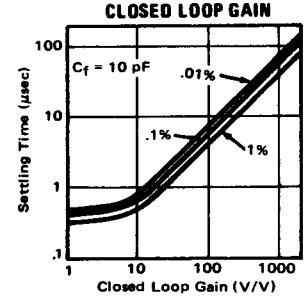
RECOMMENDED VALUES OF FREQUENCY COMPENSATION CAPACITANCE vs. CLOSED LOOP GAIN



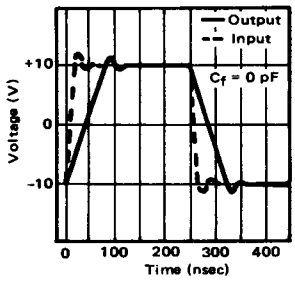
SLEW RATE vs. COMPENSATION CAPACITANCE



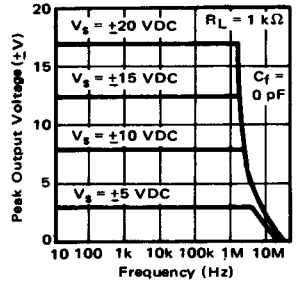
SETTLING TIME vs. CLOSED LOOP GAIN



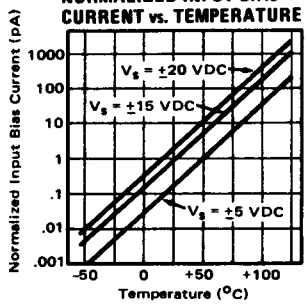
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



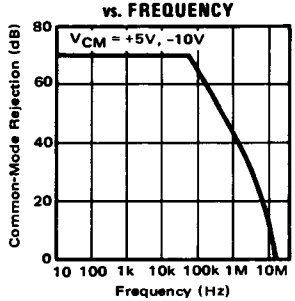
OUTPUT VOLTAGE vs. FREQUENCY



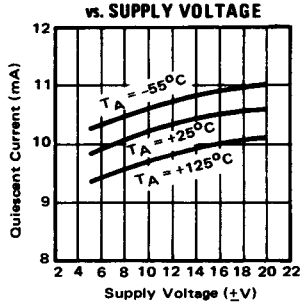
NORMALIZED INPUT BIAS CURRENT vs. TEMPERATURE



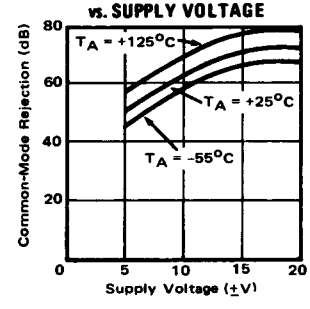
COMMON-MODE REJECTION vs. FREQUENCY



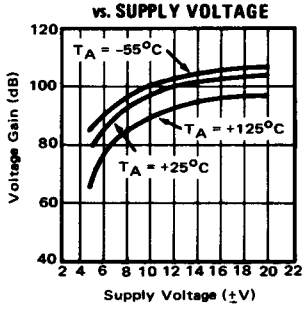
QUIESCENT CURRENT vs. SUPPLY VOLTAGE



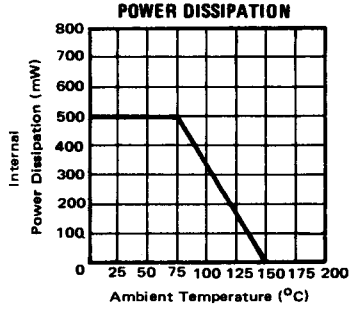
COMMON-MODE REJECTION vs. SUPPLY VOLTAGE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3551, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the output to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedances. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

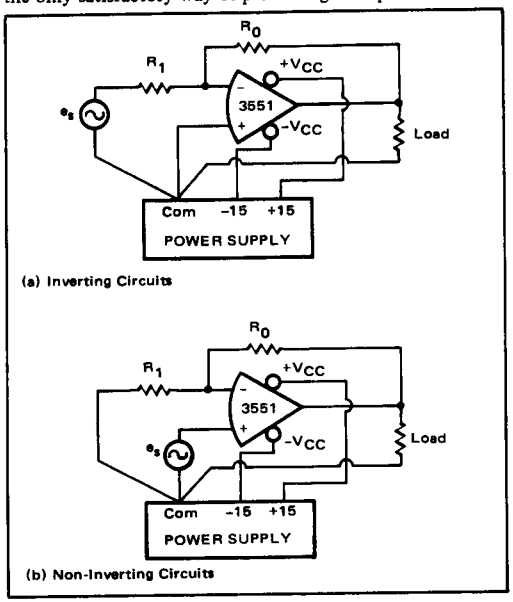


FIGURE 1. Proper Grounding Methods.

Provision for phase compensation should always be made on the PC board even if initial calculations and breadboarding may indicate that none is needed.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10 μf tantalum capacitor in parallel with a 0.001 μf ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3551 is specified for best operation on power supply voltage of ±15 VDC, it will operate with minor performance changes over a power supply voltage range of ±5 VDC to ±20 VDC. Many of the performance curves show performance of the 3551 when operated from supplies other than ±15 VDC.

INPUT/OUTPUT PROTECTION

All of the amplifiers listed in the specification table are designed to withstand input voltages as high as the supply voltage, without damage to the amplifier. Thus, inputs may be subjected to either supply voltage, in any combination, without damage.

Output stages are internally current limited and will withstand short-circuit-to-ground conditions. However, application of nonzero potential to the output pin may cause permanent damage and should be prevented by the proper precautions.

SETTLING TIME

Settling time of an amplifier is defined as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition.

Because settling time is affected by bandwidth which in turn is dependent upon closed loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling time vs. gain curves illustrate this effect for the 3551 at several levels of settling accuracy.