

**2N7002**

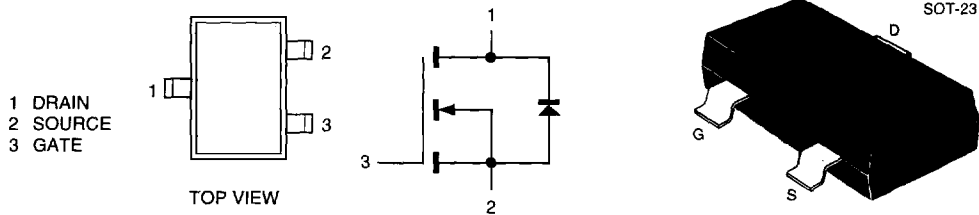
**DESCRIPTION**

Calogic's 2N7002 device type is a vertical DMOS FET transistor housed in a surface mount SOT-23 for micro-assembly applications. The device is an excellent choice for switching applications where breakdown ( $B_v$ ) and low on-resistance are important.

**ORDERING INFORMATION**

Part	Package	Temperature Range
2N7002	Plastic SOT-23 Package	-55°C to +150°C
X2N7002	Sorted Chips in Carriers	-55°C to +150°C

**PIN CONFIGURATION**



CD5

**PRODUCT SUMMARY**

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ ( $\Omega$ )	$I_D$ (A)
60	7.5	0.115

PRODUCT MARKING	
2N7002	V02

**ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

SYMBOL	PARAMETERS	LIMITS	UNITS	TEST CONDITIONS
$V_{DS}$	Drain-Source Voltage	60	V	
$V_{GS}$	Gate-Source Voltage	$\pm 40$		
$I_D$	Continuous Drain Current	0.115	A	$T_A = 25^\circ\text{C}$
		0.073		$T_A = 100^\circ\text{C}$
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	0.8		
$P_D$	Power Dissipation	200	mW	$T_A = 25^\circ\text{C}$
		80		$T_A = 100^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$	
$T_{stg}$	Storage Temperature Range	-55 to 150		
$T_L$	Lead Temperature (1/16" from case for 10 sec.)	300		

**THERMAL RESISTANCE RATINGS**

SYMBOL	THERMAL RESISTANCE	LIMITS	UNITS
$R_{\theta JA}$	Junction-to-Ambient	625	K/W

NOTE: 1. Pulse width limited by maximum junction temperature.

**SPECIFICATIONS<sup>1</sup>**

SYMBOL	PARAMETER	MIN	TYP <sup>2</sup>	MAX	UNIT	TEST CONDITIONS
<b>STATIC</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	60	70		V	$I_D = 10\mu\text{A}$ , $V_{GS} = 0\text{V}$
$V_{GS(th)}$	Gate-Threshold Voltage	1	1.9	2.5		$V_{DS} = V_{GS}$ , $I_D = 0.25\text{mA}$
$I_{GSS}$	Gate-Body Leakage			$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{OSS}$	Zero Gate Voltage Drain Current			1	$\mu\text{A}$	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$
$I_{D(ON)}$	On-State Drain Current <sup>3</sup>	500	1000		mA	$V_{DS} = \geq 2V_{DS(ON)}$ , $V_{GS} = 10\text{V}$
$r_{DS(ON)}$	Drain-Source On-Resistance <sup>3</sup>		5	7.5	$\Omega$	$V_{GS} = 5\text{V}$ , $I_D = 50\text{mA}$
			9	13.5		$T_C = 125^\circ\text{C}$
			2.5	7.5		$V_{GS} = 10\text{V}$ , $I_D = 0.5\text{A}$
			4.4	13.5		$T_C = 125^\circ\text{C}$
$V_{DS(ON)}$	Drain-Source On-Voltage <sup>3</sup>		0.25	0.375	V	$V_{GS} = 5\text{V}$ , $I_D = 50\text{mA}$
			1.25	3.75		$V_{GS} = 10\text{V}$ , $I_D = 0.5\text{A}$
			2.2	6.75		$T_C = 125^\circ\text{C}^4$
$g_{FS}$	Forward Transconductance <sup>3</sup>	80	170		mS	$V_{DS} = 10\text{V}$ , $I_D = 0.2\text{A}$
$g_{OS}$	Common Source Output Conductance <sup>3, 4</sup>		500		$\mu\text{S}$	$V_{DS} = 5\text{V}$ , $I_D = 50\text{mA}$
<b>DYNAMIC</b>						
$C_{iss}$	Input Capacitance		16	50	pF	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$
$C_{oss}$	Output Capacitance <sup>4</sup>		11	25		
$C_{rss}$	Reverse Transfer Capacitance		2	5		
<b>SWITCHING</b>						
$t_{ON}$	Turn-On Time		7	20	nS	$V_{DD} = 30\text{V}$ , $R_L = 150\Omega$ , $I_D = 0.2\text{A}$ $V_{GEN} = 10\text{V}$ , $R_G = 25\Omega$ (Switching time is essentially independent of operating temperature)
$t_{OFF}$	Turn-Off Time		7	20		

- NOTES: 1.  $T_A = 25^\circ\text{C}$  unless otherwise specified.  
 2. For design aid only, not subject to production testing.  
 3. Pulse test;  $PW = \leq 80\mu\text{S}$ , duty cycle  $\leq 1\%$ .  
 4. This parameter not registered with JEDEC.