# 4-Level Gray Scale 64×16 LCD Controller for I/O MCU

## PATENTED
## PAT No. : TW 099352

### Technical Document

- Tools Information
- FAQs
- Application Note

### Features

- Operating voltage: 2.7V~5.2V
- Built-in 32kHz RC oscillator
- External 32.768kHz crystal oscillator or 32kHz frequency source input
- Standby current: < 1μA at 3V, < 2μA at 5V
- Internal resistor type: 1/5 bias or 1/4 bias, 1/16 duty
- Two selectable LCD frame frequencies: 89Hz or 170Hz
- Max. 64×16 patterns, 64 segments and 16 commons
- Built-in bit-map display RAM: 2048 bits (=64×16×2 bits)
- Built-in internal resistor type bias generator
- Six-wire interface (four data wires)
- Eight kinds of time base/WDT selection
- Time base or WDT overflow output
- R/W address auto increment
- Built-in buzzer driver (2kHz/4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- Provides VLCD pin to adjust LCD operating voltage
- Provides three kinds of bias current programming
- Control of TN-type, STN-type LCDs and ECB-type LCDs
- Four-level gray scale output for TN-type, STN-type LCDs panel
- Four-color output for ECB-type LCDs panel
- HT1647: 100-pin LQFP package and in chip form
  HT1647G: Gold bumped chip

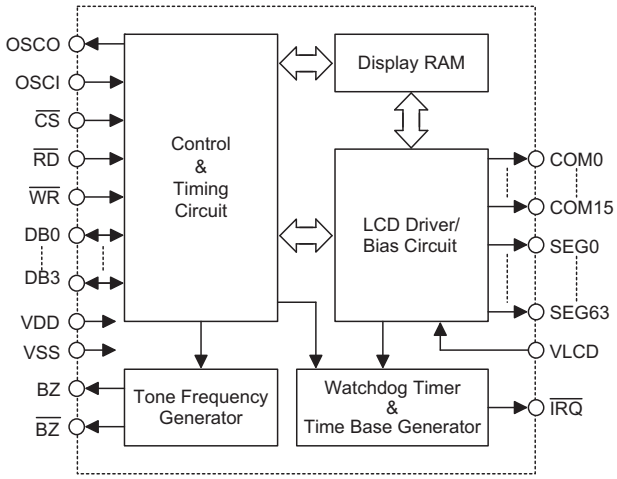
### Applications

- Leisure products
- Games
- Personal digital assistant
- Cellular phone
- Global positioning system
- Consumer electronics

### General Description

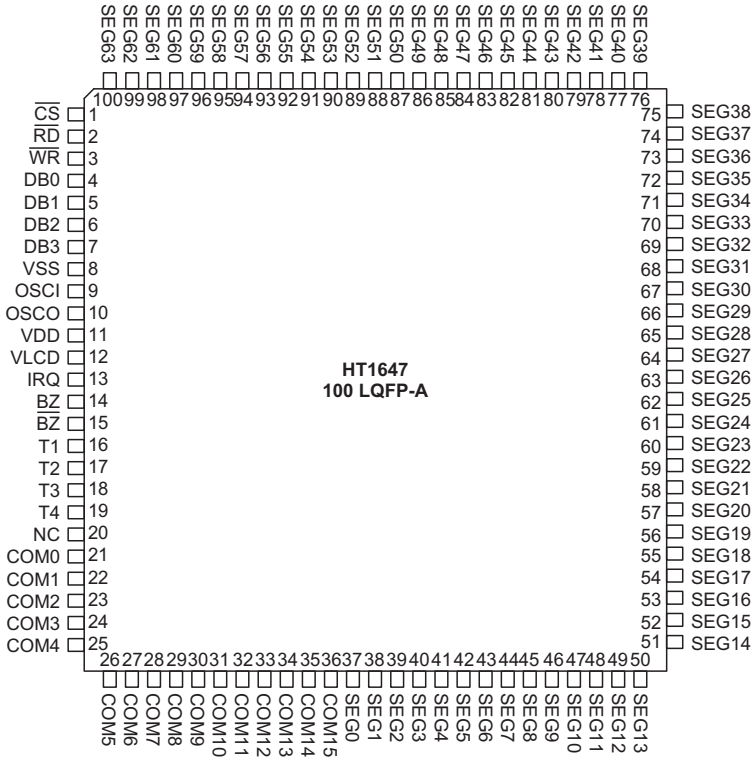
The HT1647 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 1024 patterns (64 segments and 16 commons). It also supports four data bits interface, buzzer sound, Watchdog Timer or time base timer functions. The HT1647 is a memory mapping and multi-function LCD controller. Since the HT1647 can control ECB-type (Electrically Controlled Birefringence) LCDs in addition to current TN-type (Twisted Nematic) or STN-type (Super Twisted Nematic) LCDs, it can support 4-color display as well as 4-level gray scale display. It displays 4-level gray scale output when the HT1647 drives a TN-type, STN-type LCDs. It displays four color output when the HT1647 drives an ECB-type. HT1647 uses PWM (Pulse Width Modulation) technique. The software configuration feature of the HT1647 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only six lines ($\overline{CS}$, $\overline{WR}$, DB0~DB3) are required for the interface between the host controller and the HT1647.

## Block Diagram

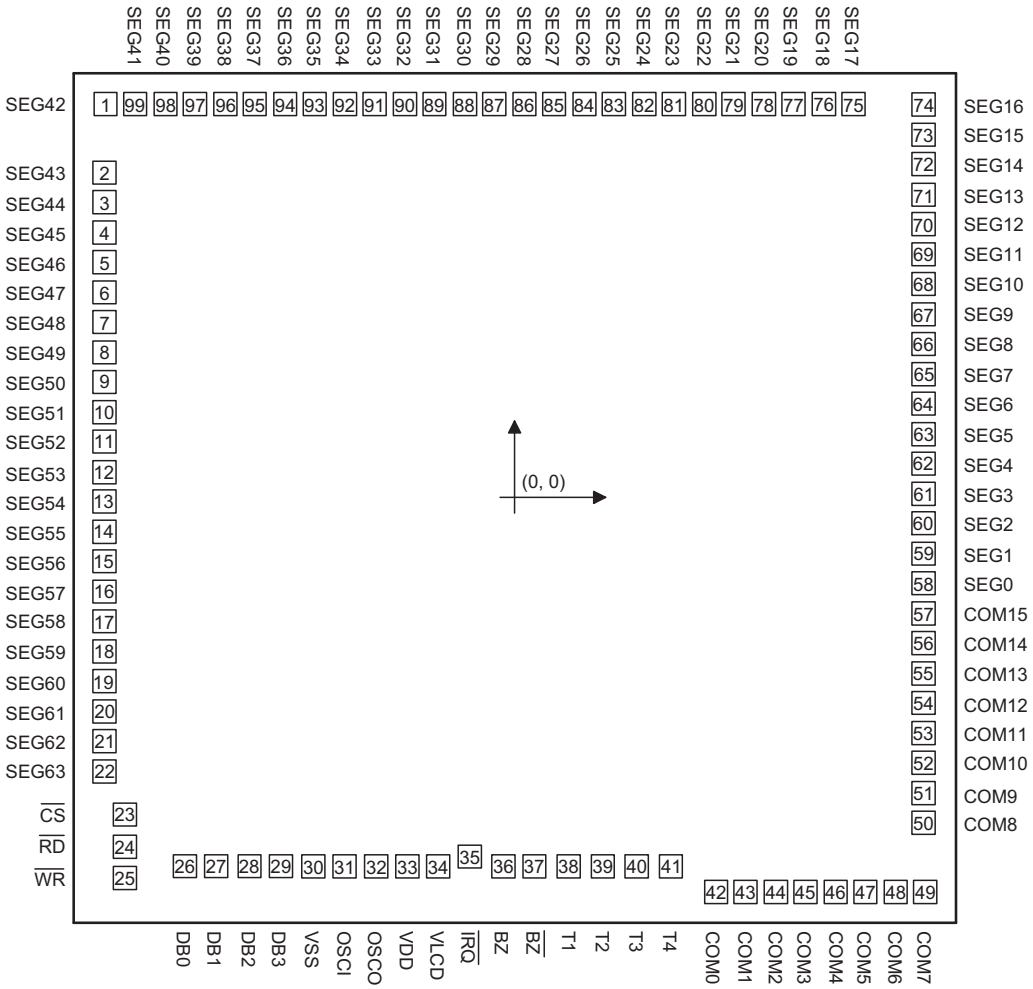



Note: CS: Chip selection
BZ, BZ: Tone outputs
WR, RD: WRITE clock, READ clock
DB0~DB3: Data bus
COM0~COM15, SEG0~SEG63: LCD outputs
IRQ: Time base or WDT overflow output

## Pin Assignment



## Pad Assignment




Chip size: 3865 × 3770 (μm)$^2$

Bump height: 18μm ± 3μm

Min. Bump spacing: 30μm

Bump size: 98 × 98μm$^2$

* The IC substrate should be connected to VSS in the PCB layout artwork.

## Pad Coordinates

Unit: μm

| Pad No. | X | Y | Pad No. | X | Y | Pad No. | X | Y |
|---|---|---|---|---|---|---|---|---|
| 1 | −1774.50 | 1708.30 | 34 | −331.40 | −1600.00 | 67 | 1775.70 | 795.30 |
| 2 | −1779.30 | 1409.80 | 35 | −194.50 | −1558.30 | 68 | 1775.70 | 927.10 |
| 3 | −1779.30 | 1281.80 | 36 | −48.00 | −1600.00 | 69 | 1775.70 | 1055.10 |
| 4 | −1779.30 | 1150.00 | 37 | 87.40 | −1600.00 | 70 | 1775.70 | 1186.90 |
| 5 | −1779.30 | 1022.00 | 38 | 235.20 | −1600.00 | 71 | 1775.70 | 1314.90 |
| 6 | −1779.30 | 890.20 | 39 | 383.40 | −1600.00 | 72 | 1775.70 | 1446.70 |
| 7 | −1779.30 | 762.20 | 40 | 530.40 | −1600.00 | 73 | 1775.70 | 1574.70 |
| 8 | −1779.30 | 630.40 | 41 | 678.60 | −1600.00 | 74 | 1775.70 | 1706.50 |
| 9 | −1779.30 | 502.40 | 42 | 875.00 | −1712.30 | 75 | 1471.10 | 1708.30 |
| 10 | −1779.30 | 370.60 | 43 | 1003.00 | −1712.30 | 76 | 1343.10 | 1708.30 |
| 11 | −1779.30 | 242.60 | 44 | 1134.80 | −1712.30 | 77 | 1211.30 | 1708.30 |

| Pad No. | X | Y | Pad No. | X | Y | Pad No. | X | Y |
|---|---|---|---|---|---|---|---|---|
| 12 | –1779.30 | 110.80 | 45 | 1262.80 | –1712.30 | 78 | 1083.30 | 1708.30 |
| 13 | –1779.30 | –17.20 | 46 | 1394.60 | –1712.30 | 79 | 951.50 | 1708.30 |
| 14 | –1779.30 | –149.00 | 47 | 1522.60 | –1712.30 | 80 | 823.50 | 1708.30 |
| 15 | –1779.30 | –277.00 | 48 | 1654.40 | –1712.30 | 81 | 691.70 | 1708.30 |
| 16 | –1779.30 | –408.80 | 49 | 1782.40 | –1712.30 | 82 | 563.70 | 1708.30 |
| 17 | –1779.30 | –536.80 | 50 | 1775.70 | –1411.10 | 83 | 431.90 | 1708.30 |
| 18 | –1779.30 | –668.60 | 51 | 1775.70 | –1283.10 | 84 | 303.90 | 1708.30 |
| 19 | –1779.30 | –796.60 | 52 | 1775.70 | –1151.30 | 85 | 172.10 | 1708.30 |
| 20 | –1779.30 | –928.80 | 53 | 1775.70 | –1023.30 | 86 | 44.10 | 1708.30 |
| 21 | –1779.30 | –1056.80 | 54 | 1775.70 | –891.50 | 87 | –87.70 | 1708.30 |
| 22 | –1779.30 | –1189.00 | 55 | 1775.70 | –763.50 | 88 | –215.70 | 1708.30 |
| 23 | –1690.00 | –1375.40 | 56 | 1775.70 | –631.70 | 89 | –347.50 | 1708.30 |
| 24 | –1690.00 | –1515.40 | 57 | 1775.70 | –503.70 | 90 | –475.50 | 1708.30 |
| 25 | –1690.00 | –1651.00 | 58 | 1775.70 | –371.90 | 91 | –607.30 | 1708.30 |
| 26 | –1430.20 | –1599.90 | 59 | 1775.70 | –243.90 | 92 | –735.30 | 1708.30 |
| 27 | –1294.80 | –1599.90 | 60 | 1775.70 | –112.10 | 93 | –867.10 | 1708.30 |
| 28 | –1149.50 | –1599.90 | 61 | 1775.70 | 15.90 | 94 | –995.10 | 1708.30 |
| 29 | –1013.90 | –1599.90 | 62 | 1775.70 | 147.70 | 95 | –1126.90 | 1708.30 |
| 30 | –872.80 | –1600.00 | 63 | 1775.70 | 275.70 | 96 | –1254.90 | 1708.30 |
| 31 | –738.30 | –1600.00 | 64 | 1775.70 | 407.50 | 97 | –1386.70 | 1708.30 |
| 32 | –600.10 | –1600.00 | 65 | 1775.70 | 535.50 | 98 | –1514.70 | 1708.30 |
| 33 | –465.60 | –1600.00 | 66 | 1775.70 | 667.30 | 99 | –1646.50 | 1708.30 |

## Pad Description

| Pad No. | Pad Name | I/O | Description |
|---|---|---|---|
| 23 | $\overline{CS}$ | I | Chip selection input with pull-high resistor. When the $\overline{CS}$ is logic high, the data and command read from or write to the HT1647 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at a logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1647 are all enabled. |
| 24 | $\overline{RD}$ | I | READ clock input with pull-high resistor. Data in the RAM of the HT1647 are clocked out on the rising edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next falling edge to latch the clocked out data. |
| 25 | $\overline{WR}$ | I | WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1647 on the rising edge of the $\overline{WR}$ signal. |
| 26~29 | DB0~DB3 | I/O | Parallel data input/output with a pull-high resistor |
| 30 | VSS | — | Negative power supply for logic circuit, ground |
| 31 | OSCI | I | The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected, the OSCI and OSCO pads can be left open. |
| 32 | OSCO | O | |
| 33 | VDD | — | Positive power supply for logic circuit |
| 34 | VLCD | I | Power supply for LCD driver circuit |
| 35 | $\overline{IRQ}$ | O | Time base or Watchdog Timer overflow flag, NMOS open drain output. |
| 36, 37 | BZ, $\overline{BZ}$ | O | 2kHz or 4kHz frequency output pair (tristate output buffer) |
| 38~41 | T1~T4 | I | Not connected |
| 42~57 | COM0~COM15 | O | LCD common outputs |
| 58~99, 1~22 | SEG0~SEG63 | O | LCD segment outputs |

## Absolute Maximum Ratings

Supply Voltage ..... $V_{SS}$–0.3V to $V_{SS}$+5.5V

Input Voltage ..... $V_{SS}$–0.3V to $V_{DD}$+0.3V

Storage Temperature ..... –50°C to 125°C

Operating Temperature ..... –25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## D.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $V_{DD}$ | Operating Voltage | — | — | 2.7 | — | 5.2 | V |
| $I_{DD1}$ | Operating Current | 3V | No load/LCD ON On-chip RC oscillator | — | 150 | 250 | μA |
| | | 5V | | — | 250 | 370 | μA |
| $I_{DD2}$ | Operating Current | 3V | No load/LCD ON Crystal oscillator | — | 135 | 200 | μA |
| | | 5V | | — | 200 | 300 | μA |
| $I_{DD11}$ | Operating Current | 3V | No load/LCD OFF On-chip RC oscillator | — | 15 | 30 | μA |
| | | 5V | | — | 50 | 70 | μA |
| $I_{DD22}$ | Operating Current | 3V | No load/LCD OFF Crystal oscillator | — | 2 | 10 | μA |
| | | 5V | | — | 3 | 10 | μA |
| $I_{STB}$ | Standby Current | 3V | No load, Power down mode | — | — | 1 | μA |
| | | 5V | | — | — | 2 | μA |
| $V_{IL}$ | Input Low Voltage | 3V | DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$ | 0 | — | 0.6 | V |
| | | 5V | | 0 | — | 1.0 | V |
| $V_{IH}$ | Input High Voltage | 3V | DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$ | 2.4 | — | 3 | V |
| | | 5V | | 4.0 | — | 5 | V |
| $I_{OL1}$ | BZ, $\overline{BZ}$, $\overline{IRQ}$ Sink Current | 3V | $V_{OL}$=0.3V | 1.2 | 2.5 | — | mA |
| | | 5V | $V_{OL}$=0.5V | 3 | 6 | — | mA |
| $I_{OH1}$ | BZ, $\overline{BZ}$ Source Current | 3V | $V_{OH}$=2.7V | –0.9 | –1.8 | — | mA |
| | | 5V | $V_{OH}$=4.5V | –2 | –4 | — | mA |
| $I_{OL2}$ | DB0~DB3 Sink Current | 3V | $V_{OL}$=0.3V | 1.2 | 2.5 | — | mA |
| | | 5V | $V_{OL}$=0.5V | 3 | 6 | — | mA |
| $I_{OH2}$ | DB0~DB3 Source Current | 3V | $V_{OH}$=2.7V | –0.9 | –1.8 | — | mA |
| | | 5V | $V_{OH}$=4.5V | –2 | –4 | — | mA |
| $I_{OL3}$ | LCD Common Sink Current | 3V | $V_{OL}$=0.3V | 80 | 160 | — | μA |
| | | 5V | $V_{OL}$=0.5V | 180 | 360 | — | μA |
| $I_{OH3}$ | LCD Common Source Current | 3V | $V_{OH}$=2.7V | –40 | –80 | — | μA |
| | | 5V | $V_{OH}$=4.5V | –90 | –180 | — | μA |
| $I_{OL4}$ | LCD Segment Sink Current | 3V | $V_{OL}$=0.3V | 50 | 100 | — | μA |
| | | 5V | $V_{OL}$=0.5V | 120 | 240 | — | μA |
| $I_{OH4}$ | LCD Segment Source Current | 3V | $V_{OH}$=2.7V | –30 | –60 | — | μA |
| | | 5V | $V_{OH}$=4.5V | –70 | –140 | — | μA |
| $R_{PH}$ | Pull-high Resistor | 3V | DB0~DB3, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$ | 150 | 250 | 410 | kΩ |
| | | 5V | | 60 | 125 | 210 | kΩ |

## A.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_{DD}$ | Conditions | | | | |
| $f_{SYS1}$ | System Clock | 3V | On-chip RC oscillator | 22 | 32 | 40 | kHz |
| | | 5V | | 24 | 32 | 40 | kHz |
| $f_{SYS2}$ | System Clock | 3V | Crystal oscillator | — | 32.768 | — | kHz |
| | | 5V | | — | 32.768 | — | kHz |
| $f_{SYS3}$ | System Clock | 3V | External clock source | — | 32 | — | kHz |
| | | 5V | | — | 32 | — | kHz |
| $f_{LCD1}$ | LCD Frame Frequency | 3V | On-chip RC oscillator | 61/117 | 89/170 | 111/213 | Hz |
| | | 5V | | 61/117 | 89/170 | 111/213 | Hz |
| $f_{LCD2}$ | LCD Frame Frequency | 3V | Crystal oscillator | — | 64 | — | Hz |
| | | 5V | | — | 64 | — | Hz |
| $f_{LCD3}$ | LCD Frame Frequency | 3V | External clock source | — | 64 | — | Hz |
| | | 5V | | — | 64 | — | Hz |
| $t_{COM}$ | LCD Common Period | — | n: Number of COM | — | $n/f_{LCD}$ | — | sec |
| $f_{CLK1}$ | 4-Bit Data Clock ($\overline{WR}$ Pin) | 3V | Duty cycle 50% | — | — | 150 | kHz |
| | | 5V | | — | — | 300 | kHz |
| $f_{CLK2}$ | 4-Bit Data Clock ($\overline{RD}$ Pin) | 3V | Duty cycle 50% | — | — | 75 | kHz |
| | | 5V | | — | — | 150 | kHz |
| $t_{CS}$ | 4-Bit Interface Reset Pulse Width (Figure 3) | — | $\overline{CS}$ | — | 250 | — | ns |
| $t_{CLK}$ | $\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1) | 3V | Write mode | 3.34 | — | — | μs |
| | | | Read mode | 6.67 | | | |
| | | 5V | Write mode | 1.67 | — | — | μs |
| | | | Read mode | 3.34 | | | |
| $t_r$, $t_f$ | Rise/Fall Time Serial Data Clock Width (Figure 1) | 3V | — | — | 120 | — | ns |
| | | 5V | | | | | |
| $t_{su}$ | Setup Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2) | 3V | — | — | 120 | — | ns |
| | | 5V | | | | | |
| $t_h$ | Hold Time for DB to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2) | 3V | — | — | 120 | — | ns |
| | | 5V | | | | | |
| $t_{su1}$ | Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3) | 3V | — | — | 100 | — | ns |
| | | 5V | | | | | |
| $t_{h1}$ | Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3) | 3V | — | — | 100 | — | ns |
| | | 5V | | | | | |

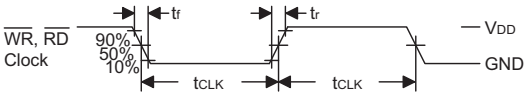



Figure 1

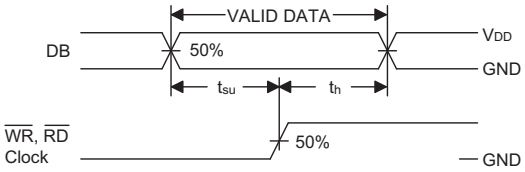



Figure 2

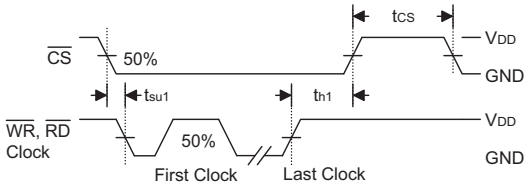



Figure 3

## Functional Description

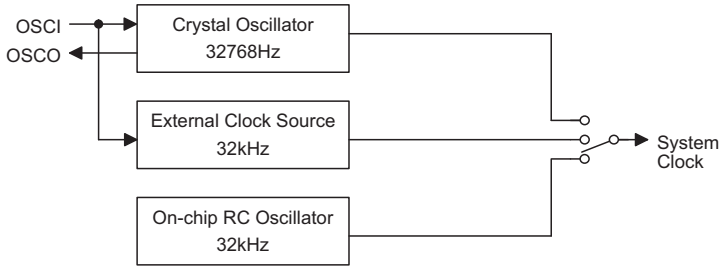
### System Oscillator

The HT1647 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The clock source may be from an on-chip RC oscillator (32kHz), a crystal oscillator (32.768kHz), or an external 32kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT loses its function as well.

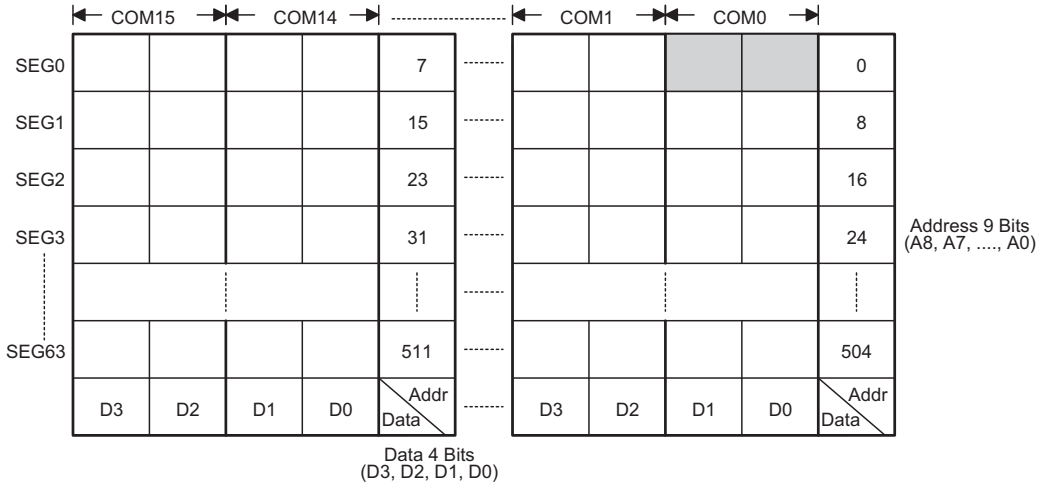
The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, thus serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 32kHz clock source operation. At the initial system power on, the HT1647 is at the SYS DIS state.

### Display Memory – RAM Structure

The static display RAM is organized into 512×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.




System Oscillator Configuration




: Two bits of RAM map to LCD's one pixel and decide 4-level gray scale or 4-color display concurrently.

**Display Memory – RAM Structure**

### Gray Scale Level Decision

HT1647 uses PWM technique to provide 4-level gray scale display. Two bits of RAM data code ((D3, D2) or (D1, D0)) decide one pixel level of LCDs, level 1~level divided by 4. Every level must be defined as one kind of gray scale by PWM data (namely B4~B0) previously.

| RAM Data Code (D3, D2) or (D1, D0) | Choice Gray Scale Level |
|---|---|
| (1, 1) | Level 1 |
| (1, 0) | Level 2 |
| (0, 1) | Level 3 |
| (0, 0) | Level 4 |

**RAM Data Defined Gray Scale Level**

### Frame Frequency

HT1647 provides two kinds of frame frequency option by command code; 89Hz and 170Hz respectively. FRAME 89Hz provides 89Hz frame frequency and active segment signal width can be divided into 24 sections concurrently. FRAME 170Hz provides 170Hz frame frequency and active segment signal width can be divided into 13 sections concurrently. The 24 sections display a particularly gray scale more than the 13 sections by PWM data. The default is FRAME 89Hz.

### Gray Scale Display

If the user choose 89Hz frame frequency, a max. of 24 sections can be programmed to suit a satisfactory gray scale in every level. Similarly, if the user choose 170Hz frame frequency, a max. of 13 sections can be programmed to suit a satisfactory gray scale in every level. HT1647 provides 5-bit PWM data to control the length of the section. In other words, a max. Of 24 gray scales are generated by 5-bit binary PWM data. At FRAME 89Hz mode, the HT1647 only provides a max. of 24 adjustable gray scales although 32 is the expressed max. value by 5 bits binary code. When 5 bits binary code value is more than 23, the PWM control circuit uniformly regards 23. To increase PWM data indicates to increase the length of the active segment signal. The varied length of the active segment signal displays varied gray scale in TN-type, STN-type LCDs (refer to table 1). Similarly, it displays varied color in ECB-type LCDs. The color display is derived from ECB-type LCD specification. At FRAME 170Hz mode, the HT1647 only provides a max. of 13 adjustable gray scales although 32 is the expressed max. value by 5 bits binary code. When the 5 bits binary code value is more than 12, the PWM control circuit uniformly regards 12. The user must appoint four kinds of PWM data to four kinds of different gray scale level by commanding PWM data (refer to table 2).

| Name | Command Code | Function |
|---|---|---|
| FRAME 170Hz | X**100**-0001-1000-XXXX | Select 170Hz frame frequency and active segment signal width can be divided into 13 sections |
| FRAME 89Hz | X**100**-0001-1101-XXXX | Select 89Hz frame frequency and active segment signal width can be divided into 24 sections |

**Frame Frequency Selection Command Code**

**Relationship Table between PWM Data and Gray Scale**

| Value | 5 bits PWM data | | | | | PWM (ON width) | Gray Scale |
|---|---|---|---|---|---|---|---|
| | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 (0/23) | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1/23 | |
| 2 | 0 | 0 | 0 | 1 | 0 | 2/23 | |
| 3 | 0 | 0 | 0 | 1 | 1 | 3/23 | |
| 4 | 0 | 0 | 1 | 0 | 0 | 4/23 | |
| 5 | 0 | 0 | 1 | 0 | 1 | 5/23 | |
| 6 | 0 | 0 | 1 | 1 | 0 | 6/23 | |
| 7 | 0 | 0 | 1 | 1 | 1 | 7/23 | |
| 8 | 0 | 1 | 0 | 0 | 0 | 8/23 | |
| 9 | 0 | 1 | 0 | 0 | 1 | 9/23 | |
| 10 | 0 | 1 | 0 | 1 | 0 | 10/23 | |
| 11 | 0 | 1 | 0 | 1 | 1 | 11/23 | |
| 12 | 0 | 1 | 1 | 0 | 0 | 12/23 | |
| 13 | 0 | 1 | 1 | 0 | 1 | 13/23 | |
| 14 | 0 | 1 | 1 | 1 | 0 | 14/23 | |
| 15 | 0 | 1 | 1 | 1 | 1 | 15/23 | |
| 16 | 1 | 0 | 0 | 0 | 0 | 16/23 | |
| 17 | 1 | 0 | 0 | 0 | 1 | 17/23 | |
| 18 | 1 | 0 | 0 | 1 | 0 | 18/23 | |
| 19 | 1 | 0 | 0 | 1 | 1 | 19/23 | |
| 20 | 1 | 0 | 1 | 0 | 0 | 20/23 | |
| 21 | 1 | 0 | 1 | 0 | 1 | 21/23 | |
| 22 | 1 | 0 | 1 | 1 | 0 | 22/23 | |
| 23 | 1 | 0 | 1 | 1 | 1 | 1 (23/23) | |
| 24 | 1 | 1 | 0 | 0 | 0 | 1 (24/23) | |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| 31 | 1 | 1 | 1 | 1 | 1 | 1 (31/23) | |

**Table 1: FRAME 89Hz Mode**

| Value | 5 bits PWM data | | | | | PWM (ON width) | Gray Scale |
|---|---|---|---|---|---|---|---|
| | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 (0/12) | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1/12 | |
| 2 | 0 | 0 | 0 | 1 | 0 | 2/12 | |
| 3 | 0 | 0 | 0 | 1 | 1 | 3/12 | |
| 4 | 0 | 0 | 1 | 0 | 0 | 4/12 | |
| 5 | 0 | 0 | 1 | 0 | 1 | 5/12 | |
| 6 | 0 | 0 | 1 | 1 | 0 | 6/12 | |
| 7 | 0 | 0 | 1 | 1 | 1 | 7/12 | |
| 8 | 0 | 1 | 0 | 0 | 0 | 8/12 | |
| 9 | 0 | 1 | 0 | 0 | 1 | 9/12 | |
| 10 | 0 | 1 | 0 | 1 | 0 | 10/12 | |
| 11 | 0 | 1 | 0 | 1 | 1 | 11/12 | |
| 12 | 0 | 1 | 1 | 0 | 0 | 1 (12/12) | |
| 13 | 0 | 1 | 1 | 0 | 1 | 1 (13/12) | |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| 31 | 1 | 1 | 1 | 1 | 1 | 1 (31/12) | |

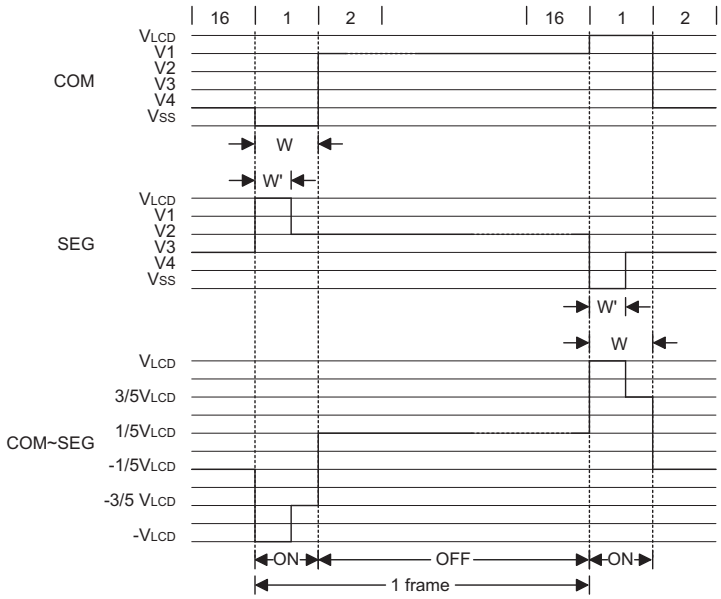
**Table 2: FRAME 170Hz Mode**

Note: The varied PWM data displays various gray scale in TN-type, STN-type LCDs.

The color display derives from ECB-type LCD's specification.

| Name | Command Code | Function |
|---|---|---|
| GRS LEVEL 1 | X**100**-001 B4-B3 B2 B1 B0-XXXX | Set PWM data in gray scale level 1 |
| GRS LEVEL 2 | X**100**-010 B4-B3 B2 B1 B0-XXXX | Set PWM data in gray scale level 2 |
| GRS LEVEL 3 | X**100**-011 B4-B3 B2 B1 B0-XXXX | Set PWM data in gray scale level 3 |
| GRS LEVEL 4 | X**100**-100 B4-B3 B2 B1 B0-XXXX | Set PWM data in gray scale level 4 |

**Four Kinds of Gray Scale Level Command Code**




Note: "W"' Real active segment signal width (adjustable width by PWM data)
"W" Max. active segment signal width
PWM (ON width): W'/W, 0≤W'/W≤1 (refer to table 1 & tabel 2)

**Example of Waveform (B Type) in 1/5 Bias, 1/16 Duty Cycle Drive**

### Time Base and Watchdog Timer – WDT

The time base generator and WDT share the same counter which is divided by 256. The $\overline{IRQ}$ clock can be programmed as 1Hz, 2Hz, ...., 128Hz output. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will remain at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.

If an external clock is selected as the system frequency source, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

### Buzzer Tone Output

A simple tone generator is implemented in the HT1647. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

By executing the TONE 4K and TONE 2K commands there are two tone frequency outputs selectable that can turn on the tone output. The TONE 4K and TONE 2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned off by invoking the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

### Command Format

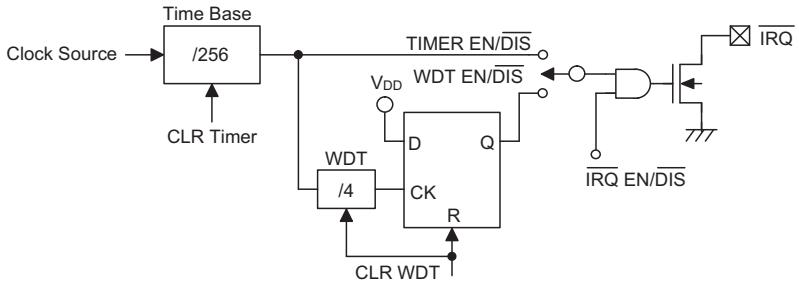
The HT1647 can be configured by software setting. There are two mode commands to configure the HT1647 resource and to transfer the LCD display data.

The configuration mode of the HT1647 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a bias current selection command, a gray scale level selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode ID and the command mode ID:

| Operation | Mode | ID |
|---|---|---|
| READ | Data | 110 |
| WRITE | Data | 101 |
| READ-MODIFY-WRITE | Data | 101 |
| COMMAND | Command | 100 |

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will also be reset. The $\overline{CS}$ pin returns to "0", so a new operation mode ID should be issued first.




**Time Base and WDT Configurations**

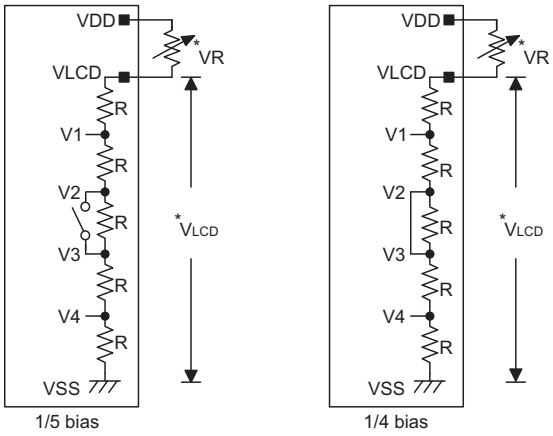
| Name | Command Code | Function |
|---|---|---|
| TONE OFF | **X100**-0000-1000-XXXX | Turn-off tone output |
| TONE 4K | **X100**-0001-0000-XXXX | Turn-on tone output, tone frequency is 4kHz |
| TONE 2K | **X100**-0001-0001-XXXX | Turn-on tone output, tone frequency is 2kHz |

**Buzzer Tone Output Command Code**

### Bias Generator

The HT1647 bias voltage belongs to internal resistor type. It provides two kinds of bias option named 1/5 bias and 1/4 bias respectively. It is recommended to select 1/5 bias to fit TN-type, STN-type LCDs and select 1/4 bias to fit ECB-type LCDs. It also provides three kinds of bias current option by programming to suitably drive an LCD panel. The three kinds of bias current are large, middle, and small, respectively. Usually, large panel LCD can be excellently displayed by large bias current. Relatively, it consumes large current when LCD ON command is used. Small bias current provides low power consumption during On condition when the LCD is normally displayed. The following are the reference value table.

| $V_{LCD}$ | Bias | Large Bias Current | Middle Bias Current | Small Bias Current |
|---|---|---|---|---|
| 4V | 1/5 | 300μA | 100μA | 40μA |
| 4V | 1/4 | 375μA | 125μA | 50μA |




* The voltage applied to VLCD pin must be equal to or lower than VDD.
* Adjust VR to fit LCD display, at $V_{DD}$=5V, $V_{LCD}$=4V, VR=15kΩ±20%.

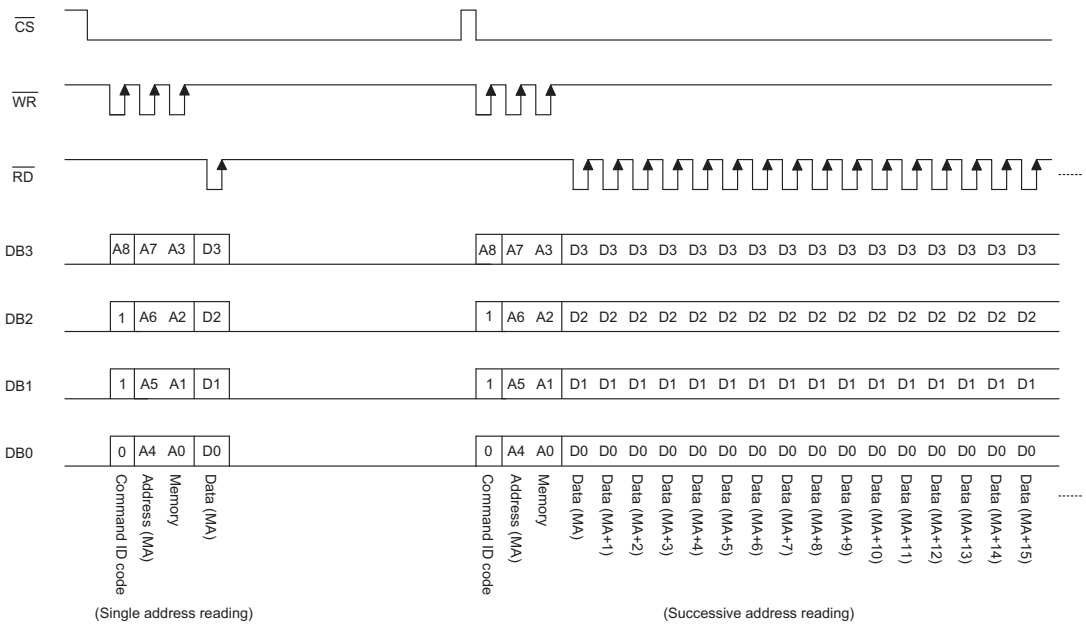
**Internal Resistor Type Bias Generator Configurations**

### Interfacing

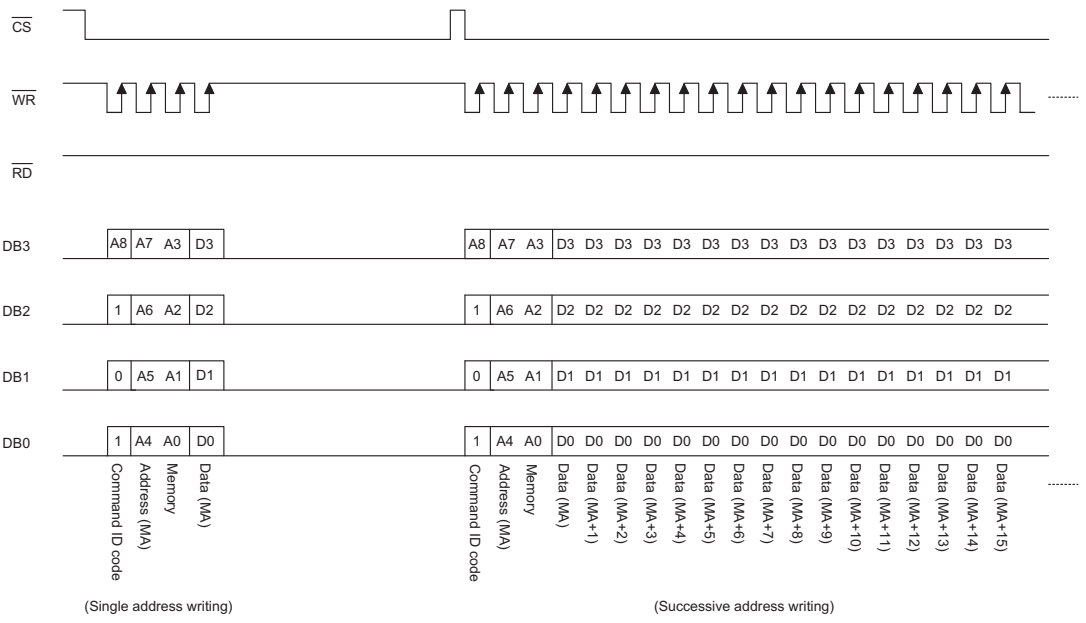
Only six lines are required to interface with the HT1647. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1647. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the HT1647 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1647. The DB0~DB3 are the 4-bit parallel data input/output lines. Data to be read or written or commands to be written have to pass through the DB0~DB3 lines. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DB0~DB3 lines. It is recommended that the host controller read correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DB0~DB3 lines are all clocked into the HT1647 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the HT1647. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by connecting with the $\overline{IRQ}$ pin of the HT1647.

## Timing Diagrams

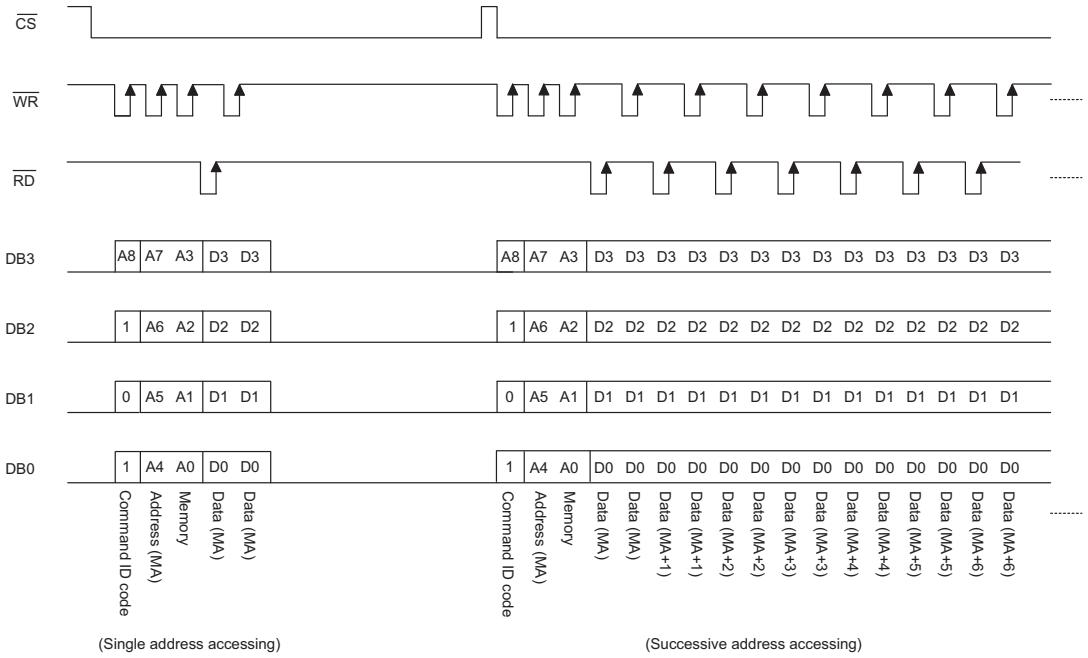
### READ mode (command ID code : 1 1 0)




### WRITE mode (command ID code : 1 0 1)

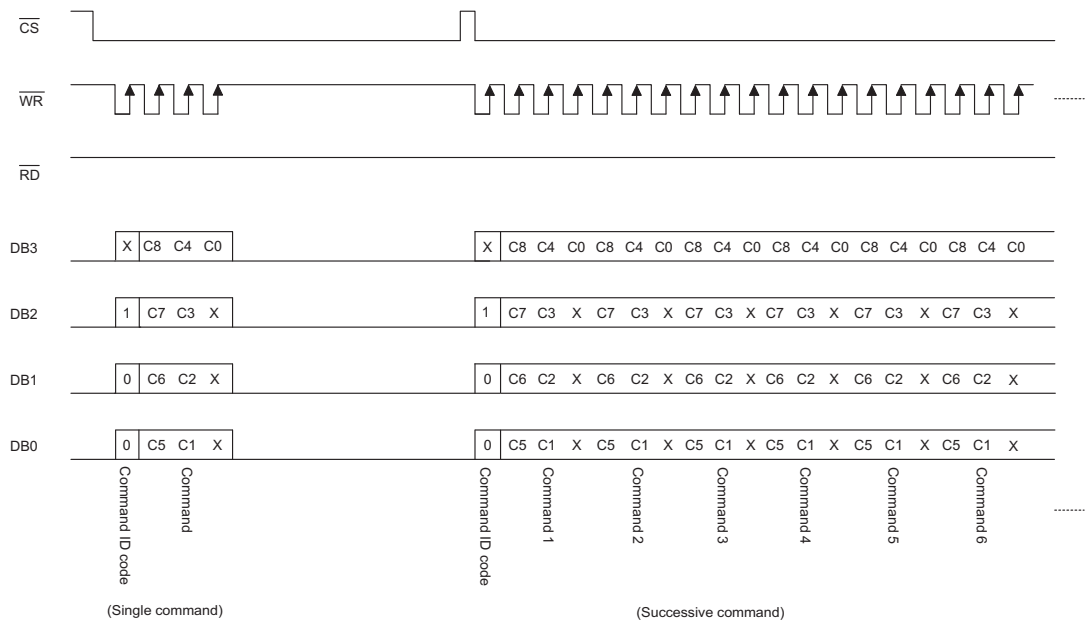


**READ-MODIFY-WRITE mode (command ID code : 1 0 1)**




(Single address accessing) (Successive address accessing)

**Command mode (command ID code : 1 0 0)**

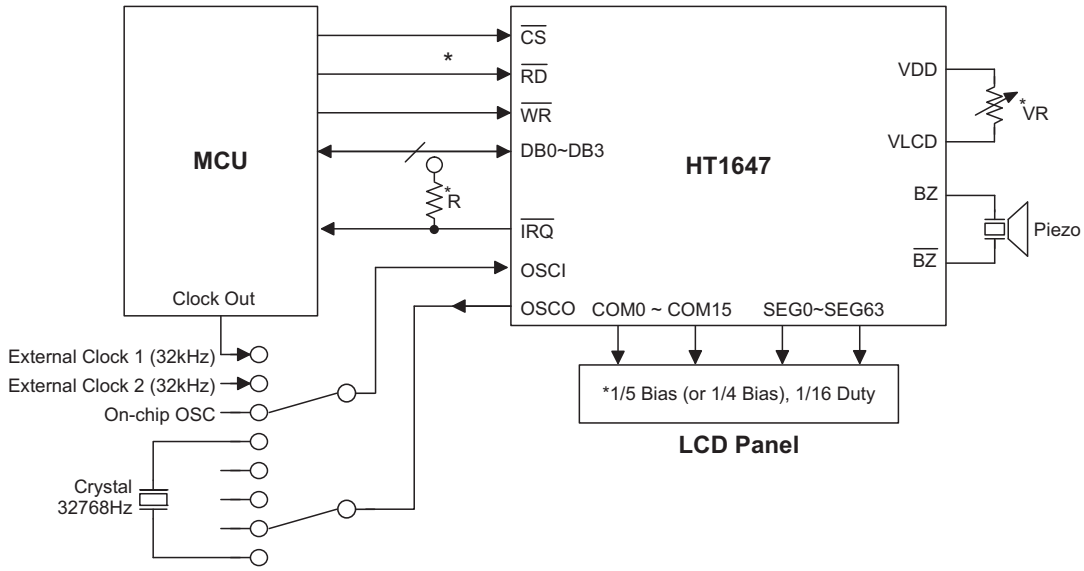



(Single command) (Successive command)

Note: "X" stands for don't care

## Application Circuits

**Host Controller with an HT1647 Display System**




*Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the MCU.

The voltage applied to $V_{LCD}$ pin must be equal to or lower than $V_{DD}$.

Adjust VR to fit user's LCD panel display voltage ($V_{LCD}$).

It is recommended to select 1/5 bias to fit TN-type, STN-type LCDs and select 1/4 bias to fit ECB-type LCDs.

Adjust R (external pull high resistance) to fit user's time base clock.

## Instruction Set Summary

| Name | Command Code | D/C | Function | Def. |
|---|---|---|---|---|
| READ | A8**110**-A7A6A5A4A3A2A1A0D3D2D1D0 | D | Read data from the RAM | |
| WRITE | A8**101**-A7A6A5A4A3A2A1A0D3D2D1D0 | D | Write data to the RAM | |
| READ-MODIFY-WRITE | A8**101**-A7A6A5A4A3A2A1A0D3D2D1D0 | D | Read and Write data to the RAM | |
| SYS DIS | X**100**-0000-0000-XXXX | C | Turn Off both system oscillator and LCD bias generator | Yes |
| SYS EN | X**100**-0000-0001-XXXX | C | Turn On system oscillator | |
| LCD OFF | X**100**-0000-0010-XXXX | C | Turn Off LCD display | Yes |
| LCD ON | X**100**-0000-0011-XXXX | C | Turn On LCD display | |
| TIMER DIS | X**100**-0000-0100-XXXX | C | Disable time base output | Yes |
| WDT DIS | X**100**-0000-0101-XXXX | C | Disable WDT time-out flag output | Yes |
| TIMER EN | X**100**-0000-0110-XXXX | C | Enable time base output | |
| WDT EN | X**100**-0000-0111-XXXX | C | Enable WDT time-out flag output | |
| TONE OFF | X**100**-0000-1000-XXXX | C | Turn Off tone outputs | Yes |
| CLR TIMER | X**100**-0000-1101-XXXX | C | Clear the contents of the time base generator | |
| CLR WDT | X**100**-0000-1111-XXXX | C | Clear the contents of the WDT stage | |
| TONE 4K | X**100**-0001-0000-XXXX | C | Turn on tone output, tone frequency output: 4kHz | |
| TONE 2K | X**100**-0001-0001-XXXX | C | Turn on tone output, tone frequency output: 2kHz | |

| Name | Command Code | D/C | Function | Def. |
|---|---|---|---|---|
| IRQ DIS | X**100**-0001-0010-XXXX | C | Disable $\overline{IRQ}$ output | Yes |
| IRQ EN | X**100**-0001-0011-XXXX | C | Enable $\overline{IRQ}$ output | |
| RC 32K | X**100**-0001-0100-XXXX | C | System clock source, on-chip RC oscillator | Yes |
| EXT (XTAL) | X**100**-0001-0101-XXXX | C | System clock source, external 32kHz clock source or crystal oscillator 32.768kHz | |
| LARGE BIAS | X**100**-0001-0110-XXXX | C | Large bias current option | Yes |
| MIDDLE BIAS | X**100**-0001-0111-XXXX | C | Middle bias current option | |
| SMALL BIAS | X**100**-0001-1000-XXXX | C | Small bias current option | |
| BIAS 1/5 | X**100**-0001-1001-XXXX | C | LCD 1/5 bias option | Yes |
| BIAS 1/4 | X**100**-0001-1010-XXXX | C | LCD 1/4 bias option | |
| FRAME 170Hz | X**100**-0001-1100-XXXX | C | Selects 170Hz frame frequency and active segment signal width can be divided into 13 sections | |
| FRAME 89Hz | X**100**-0001-1101-XXXX | C | Selects 89Hz frame frequency and active segment signal width can be divided into 24 sections | Yes |
| GRS LEVEL1 | X**100**-001 B4-B3 B2 B1 B0-XXXX | C | Sets PWM data in gray scale level 1 | |
| GRS LEVEL2 | X**100**-010 B4-B3 B2 B1 B0-XXXX | C | Sets PWM data in gray scale level 2 | |
| GRS LEVEL3 | X**100**-011 B4-B3 B2 B1 B0-XXXX | C | Sets PWM data in gray scale level 3 | |
| GRS LEVEL4 | X**100**-100 B4-B3 B2 B1 B0-XXXX | C | Sets PWM data in gray scale level 4 | |
| F1 | X**100**-1010-0000-XXXX | C | Time base clock output: 1Hz<br>The WDT time-out flag after: 4s | |
| F2 | X**100**-1010-0001-XXXX | C | Time base clock output: 2Hz<br>The WDT time-out flag after: 2s | |
| F4 | X**100**-1010-0010-XXXX | C | Time base clock output: 4Hz<br>The WDT time-out flag after: 1s | |
| F8 | X**100**-1010-0011-XXXX | C | Time base clock output: 8Hz<br>The WDT time-out flag after: 1/2s | |
| F16 | X**100**-1010-0100-XXXX | C | Time base clock output: 16Hz<br>The WDT time-out flag after: 1/4s | |
| F32 | X**100**-1010-0101-XXXX | C | Time base clock output: 32Hz<br>The WDT time-out flag after: 1/8s | |
| F64 | X**100**-1010-0110-XXXX | C | Time base clock output: 64Hz<br>The WDT time-out flag after: 1/16s | |
| F128 | X**100**-1010-0111-XXXX | C | Time base clock output: 128Hz<br>The WDT time-out flag after: 1/32s | Yes |
| TEST | X**100**-1111-1111-XXXX | C | Test mode, user don't use. | |
| NORMAL | X**100**-1111-1110-XXXX | C | Normal mode | Yes |

Note: "X" stands for don't care

A8~A0: RAM address

D3~D0: RAM data

B4~B0: PWM data

D/C: Data/Command mode

Def.: Power-on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The tone frequency source and the time base/WDT clock frequency source can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1647 after power-on reset, otherwise, power on reset may fail, which in turn leads to the malfunctioning of the HT1647.

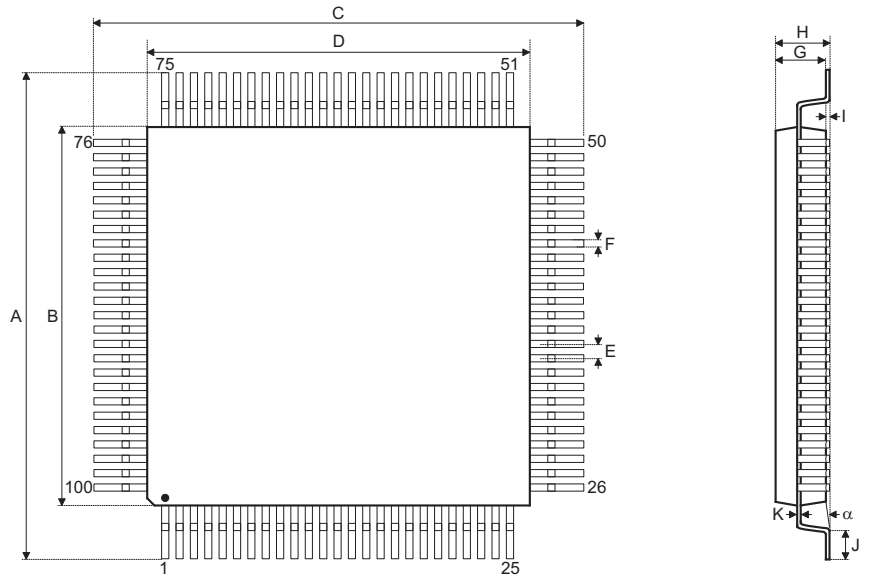
## Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

**100-pin LQFP (14mm×14mm) Outline Dimensions**




| Symbol | Dimensions in inch | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 0.630 BSC | — |
| B | — | 0.551 BSC | — |
| C | — | 0.630 BSC | — |
| D | — | 0.551 BSC | — |
| E | — | 0.020 BSC | — |
| F | 0.007 | 0.009 | 0.011 |
| G | 0.053 | 0.055 | 0.057 |
| H | — | — | 0.063 |
| I | 0.002 | — | 0.006 |
| J | 0.018 | 0.024 | 0.030 |
| K | 0.004 | — | 0.008 |
| α | 0° | — | 7° |

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | 16 BSC | — |
| B | — | 14 BSC | — |
| C | — | 16 BSC | — |
| D | — | 14 BSC | — |
| E | — | 0.50 BSC | — |
| F | 0.17 | 0.22 | 0.27 |
| G | 1.35 | 1.40 | 1.45 |
| H | — | — | 1.60 |
| I | 0.05 | — | 0.15 |
| J | 0.45 | 0.60 | 0.75 |
| K | 0.09 | — | 0.20 |
| α | 0° | — | 7° |