Dual N-Channel OptiMOS™ MOSFET

Features

· Dual N-channel OptiMOS™ MOSFET

· Enhancement mode

· Logic level (4.5V rated)

· Avalanche rated

· 100% Lead-free; RoHS compliant

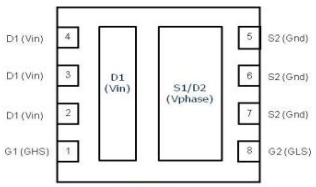
· Halogen-free according to IEC61249-2-21

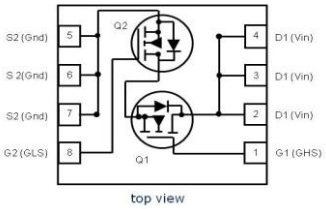
RoHS Halogen-Free

Product Summary

		Q1	Q2	
V_{DS}		30	30	V
$R_{DS(on),max}$	V_{GS}=10 V	9.5	7.2	mΩ
	V_{GS}=4.5 V	13	10	
I_D		25	30	A

PG-WISON-8





Type	Package	Marking	Lead Free
BSZ0907ND	PG-WISON-8	0907ND	Yes

Maximum ratings, at T_j=25 °C, unless otherwise specified [1)]

Parameter	Symbol	Conditions	Value		Unit
			Q1	Q2	
Continuous drain current	I_D	T_C=70 °C	25	30	A
		T_A=25 °C[2)]	11.1	13.8	
		T_A=70 °C[2)]	8.9	11.1	
		T_A=25 °C[3)]	6.7	8.5	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C	40		
Avalanche energy, single pulse	E_{AS}	I_D=9 A, R_{GS}=25 Ω	20		mJ
Gate source voltage	V_{GS}		±20		V
Power dissipation	P_{tot}	T_A=25 °C[2)]	1.9	2.3	W
		T_A=25 °C[3)]	0.70	0.86	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

[1)] Remark: only one of both transistors active

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Thermal characteristics							
Thermal resistance, junction - case	Q1	R_{thJC}		-	-	4	K/W
	Q2			-	-	3.8	
Thermal resistance, junction - ambient[1)]	Q1	R_{thJA}	6 cm^2 cooling area[2)]	-	-	65	
	Q2			-	-	55	
	Q1		minimal footprint, steady state[3)]	-	-	180	
	Q2			-	-	145	
Electrical characteristics, at T_j=25 °C, unless otherwise specified							
Static characteristics							
Drain-source breakdown voltage	Q1	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	-	-	30	V
	Q2						
Gate threshold voltage	Q1	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	1.6	2	
	Q2						
Zero gate voltage drain current	Q1	I_{DSS}	V_{DS}=30 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
	Q2						
	Q1		V_{DS}=30 V, V_{GS}=0 V, T_j=150 °C	-	-	100	
	Q2						
Gate-source leakage current	Q1	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
	Q2						
Drain-source on-state resistance	Q1	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=9 A	-	10.4	13	mΩ
	Q2			-	8.3	10	
	Q1		V_{GS}=10 V, I_D=9 A	-	7.6	9.5	
	Q2			-	6	7.2	
Gate resistance	Q1	R_G		1.8	3.5	7.0	Ω
	Q2			0.6	1.2	2.4	
Transconductance	Q1	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=9 A	16	33	-	S
	Q2			18	37	-	

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

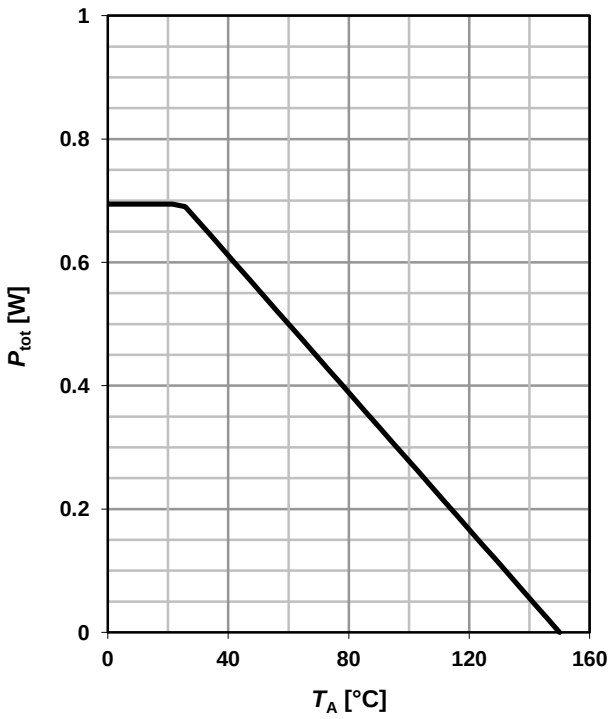
[3)] device mounted on a minimum pad (one layer, 70 µm thick)

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Dynamic characteristics							
Input capacitance	Q1	C_{iss}	V_{GS}=0 V, V_{DS}= 15 V, f=1 MHz	-	550	730	pF
	Q2			-	680	900	
Output capacitance	Q1	C_{oss}		-	220	293	
	Q2			-	270	359	
Reverse transfer capacitance	Q1	C_{rss}		-	34	-	
	Q2			-	40	-	
Turn-on delay time	Q1	$t_{d(on)}$	V_{DD}=15 V, V_{GS}=10 V, R_G=6 Ω, I_D=9 A	-	6.2	-	ns
	Q2			-	6	-	
Rise time	Q1	t_r		-	3.2	-	
	Q2			-	3.4	-	
Turn-off delay time	Q1	$t_{d(off)}$		-	18.5	-	
	Q2			-	17.2	-	
Fall time	Q1	t_f		-	2.8	-	
	Q2			-	2.4	-	
Gate Charge Characteristics							
Gate to source charge	Q1	Q_{gs}	V_{DD}=15 V, I_D=9 A, V_{GS}=0 to 4.5 V	-	1.4	1.9	nC
Gate to drain charge		Q_{gd}		-	1.4	1.8	
Switching charge		Q_g		-	4.3	6.4	
Gate plateau voltage		$V_{plateau}$		-	2.6	-	
Gate to source charge	Q2	Q_{gs}		-	1.7	2.3	
Gate to drain charge		Q_{gd}		-	1.7	2.2	
Switching charge		Q_g		-	5.3	7.9	
Gate plateau voltage		$V_{plateau}$		-	2.5	-	

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Reverse Diode							
Diode continuous forward current	Q1	I_S	T_C=25 °C	-	-	25	A
	Q2					27	
Diode pulse current	Q1	$I_{S,pulse}$		-	-	40	
	Q2					40	
Diode forward voltage	Q1	V_{SD}	V_{GS}=0 V, I_F=9 A, T_j=25 °C	-	0.86	1.2	V
	Q2			-	0.84	1.2	
Reverse recovery charge	Q1	Q_{rr}	V_R=15 V, I_F=I_S, di_F/dt=100 A/µs	-	5	-	nC
	Q2			-	5	-	

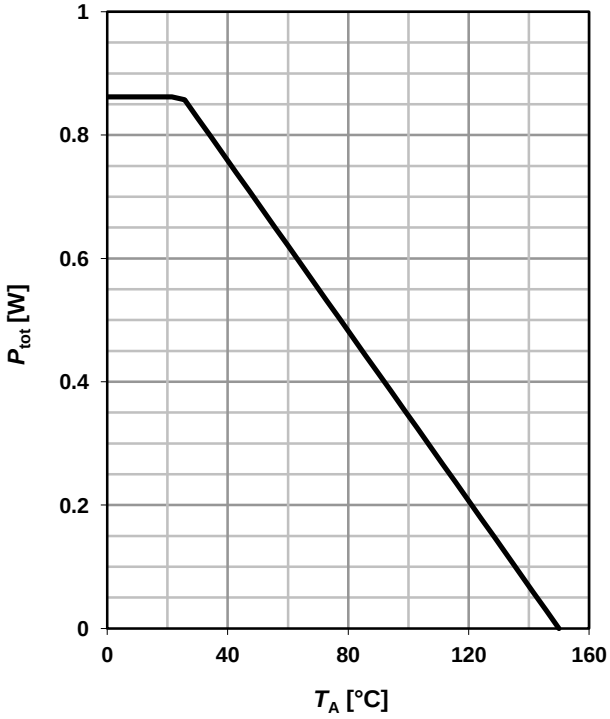
1 Power dissipation (Q1)

$P_{tot}=f(T_A)^{3)}$



2 Power dissipation (Q2)

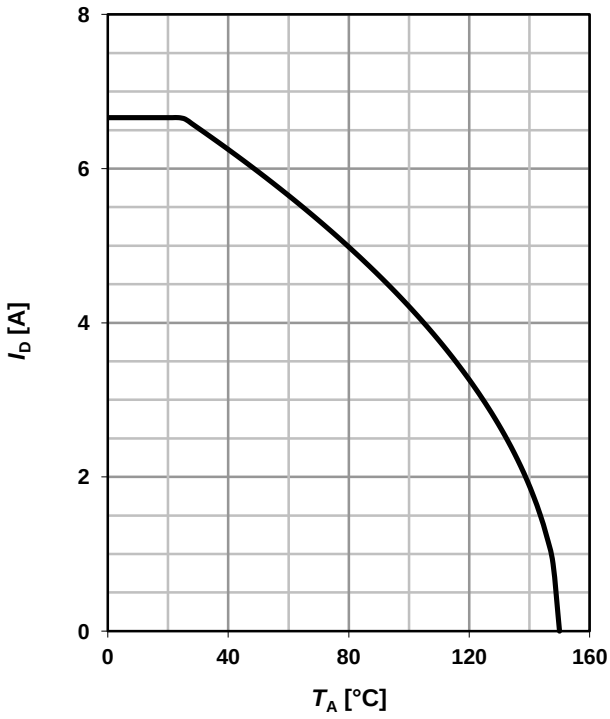
$P_{tot}=f(T_A)^{3)}$



3 Drain current (Q1)

$I_D=f(T_A)^{3)}$

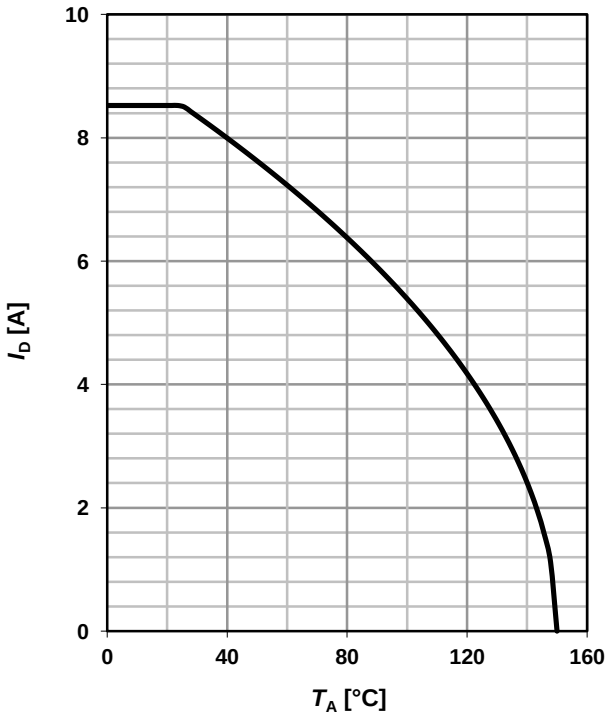
parameter: $V_{GS}\geq 10$ V



4 Drain current (Q2)

$I_D=f(T_A)^{3)}$

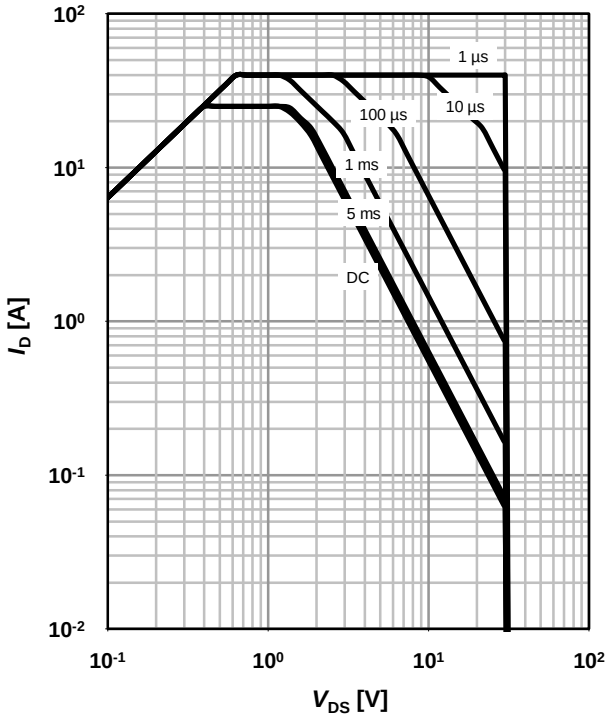
parameter: $V_{GS}\geq 10$ V



5 Safe operating area (Q1)

I_D=f(V_{DS}); T_C=25 °C; D=0

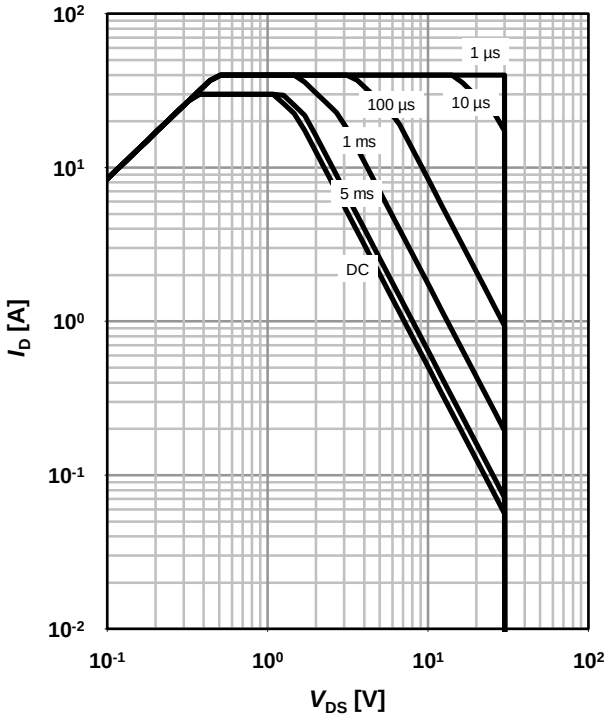
parameter: t_p



6 Safe operating area (Q2)

I_D=f(V_{DS}); T_C=25 °C; D=0

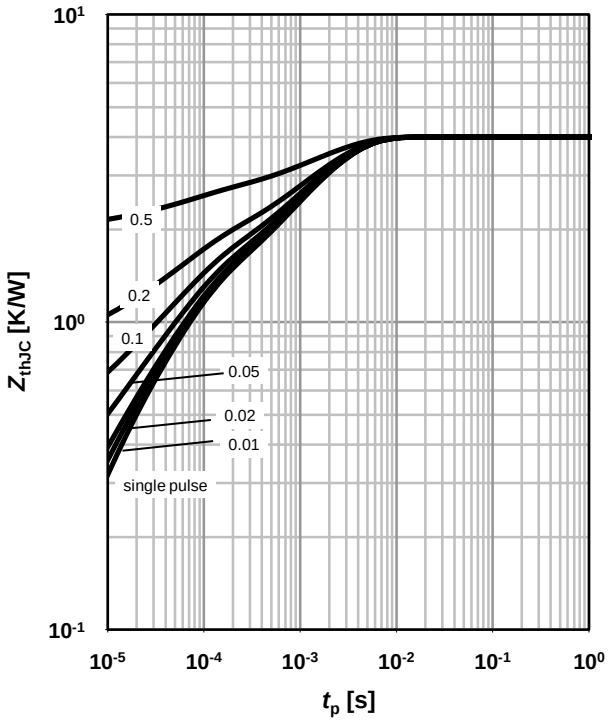
parameter: t_p



7 Max. transient thermal impedance (Q1)

Z_{thJC}=f(t_p)

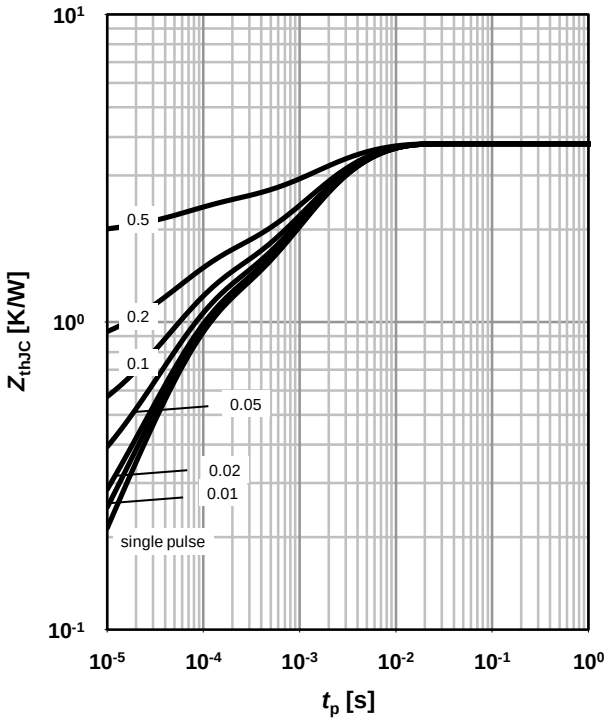
parameter: $D=t_p/T$



8 Max. transient thermal impedance (Q2)

Z_{thJC}=f(t_p)

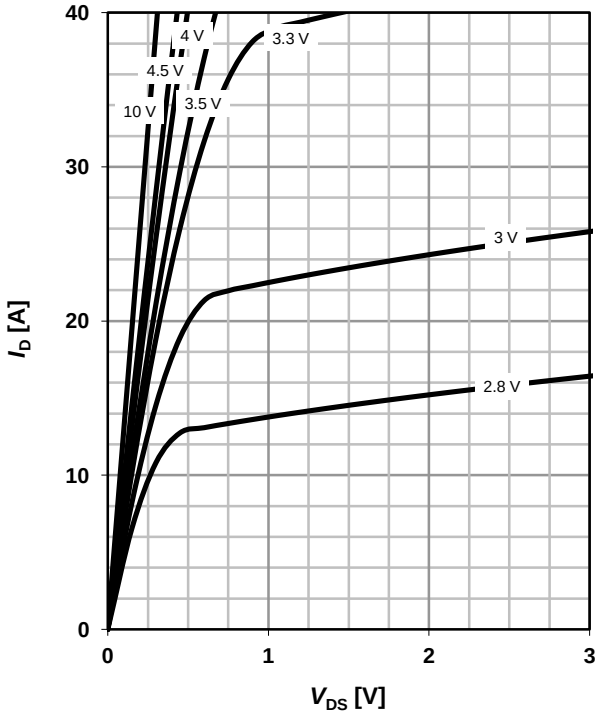
parameter: $D=t_p/T$



9 Typ. output characteristics (Q1)

I_D=f(V_{DS}); T_j=25 °C

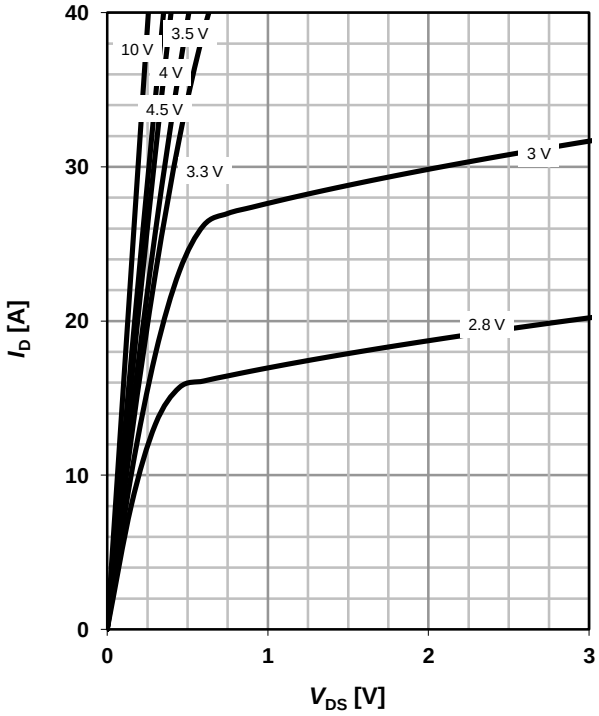
parameter: V_{GS}



10 Typ. output characteristics (Q2)

I_D=f(V_{DS}); T_j=25 °C

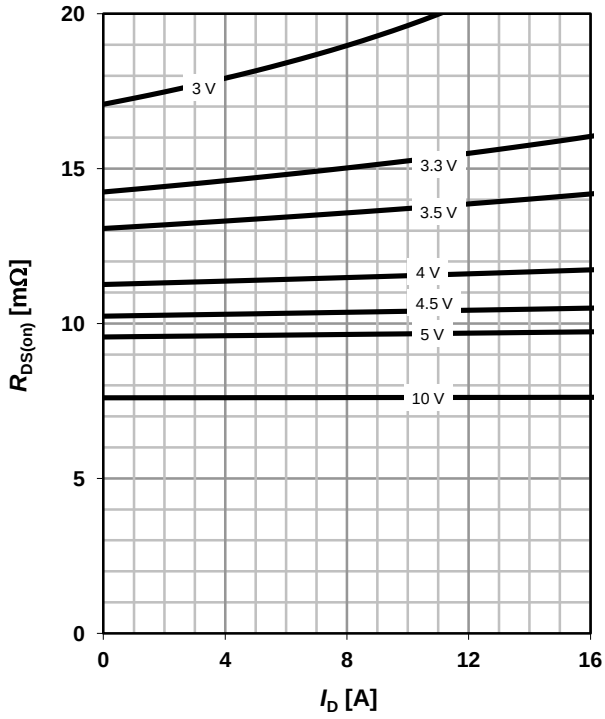
parameter: V_{GS}



11 Typ. drain-source on resistance (Q1)

$R_{DS(on)}$=f(I_D); T_j=25 °C

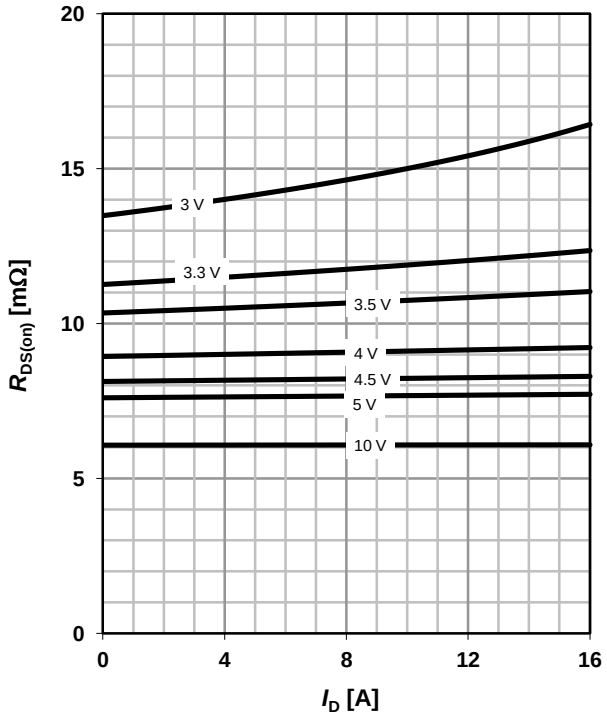
parameter: V_{GS}



12 Typ. drain-source on resistance (Q2)

$R_{DS(on)}$=f(I_D); T_j=25 °C

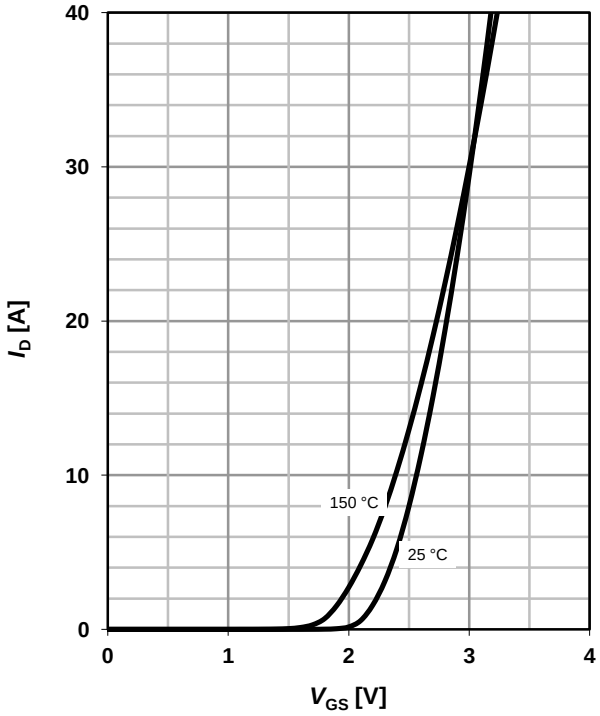
parameter: V_{GS}



13 Typ. transfer characteristics (Q1)

$I_D=f(V_{GS})$; $|V_{DS}|>2 | I_D| R_{DS(on)max}$

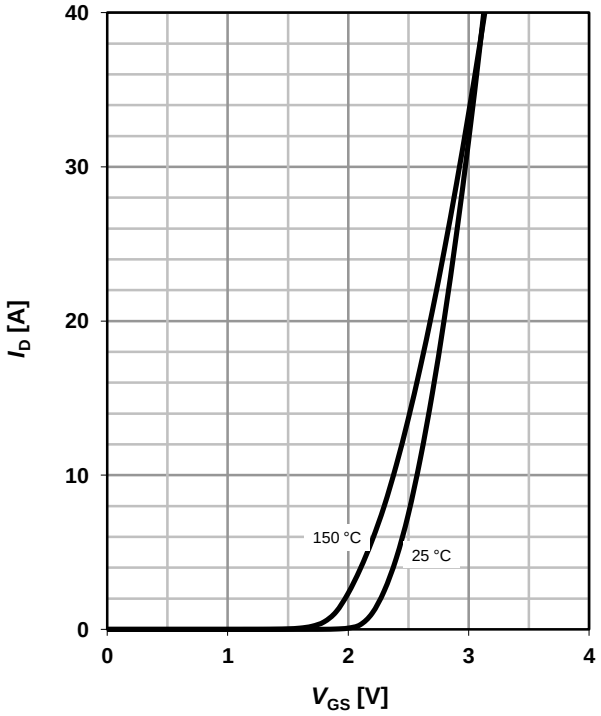
parameter: T_j



14 Typ. transfer characteristics (Q2)

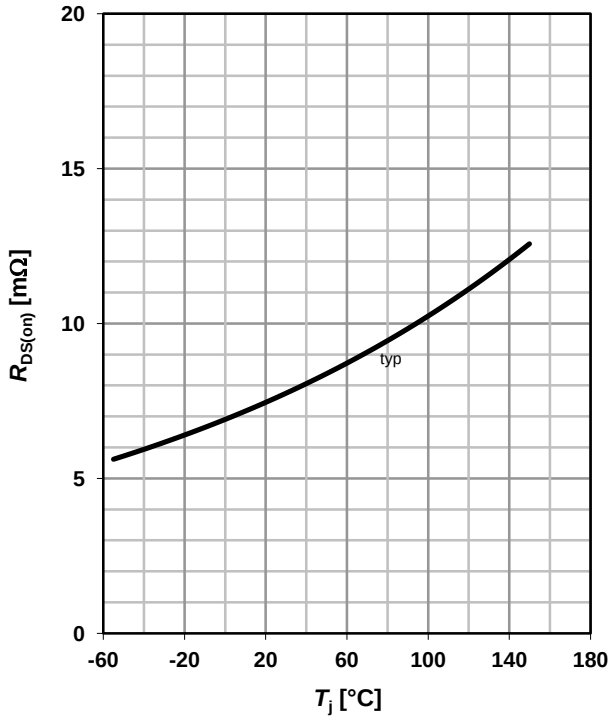
$I_D=f(V_{GS})$; $|V_{DS}|>2 | I_D | R_{DS(on)max}$

parameter: T_j



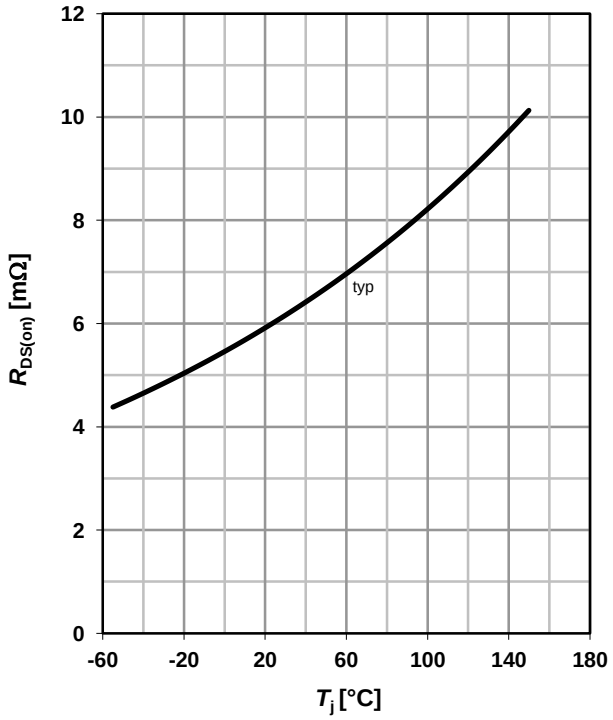
15 Drain-source on-state resistance (Q1)

$R_{DS(on)}=f(T_j)$; I_D=9 A; V_{GS}=10 V



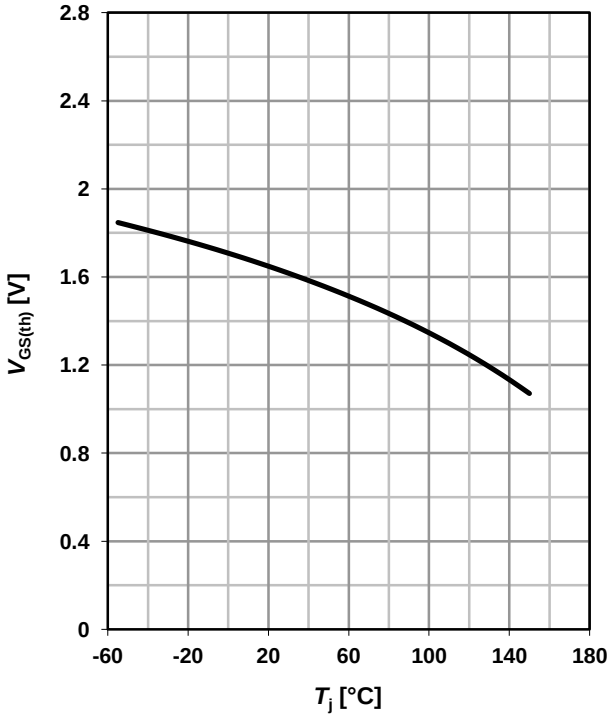
16 Drain-source on-state resistance (Q2)

$R_{DS(on)}=f(T_j)$; I_D=9 A; V_{GS}=10 V



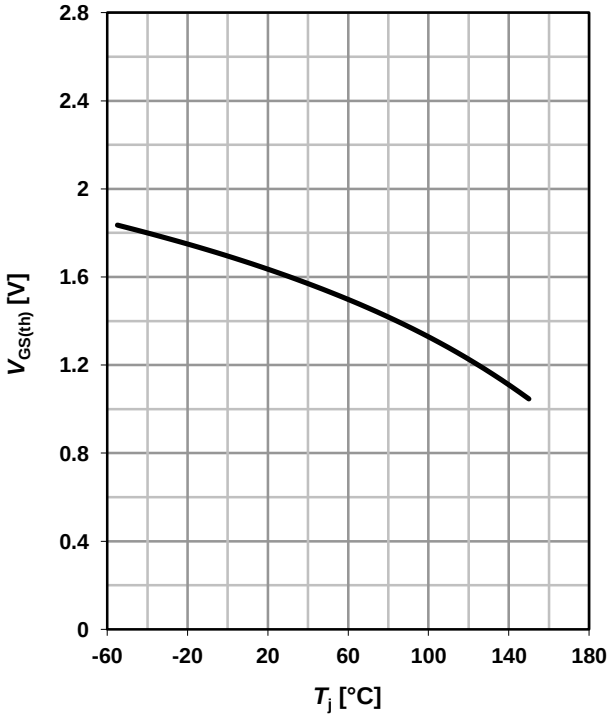
17 Typ. gate threshold voltage (Q1)

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=250$ µA



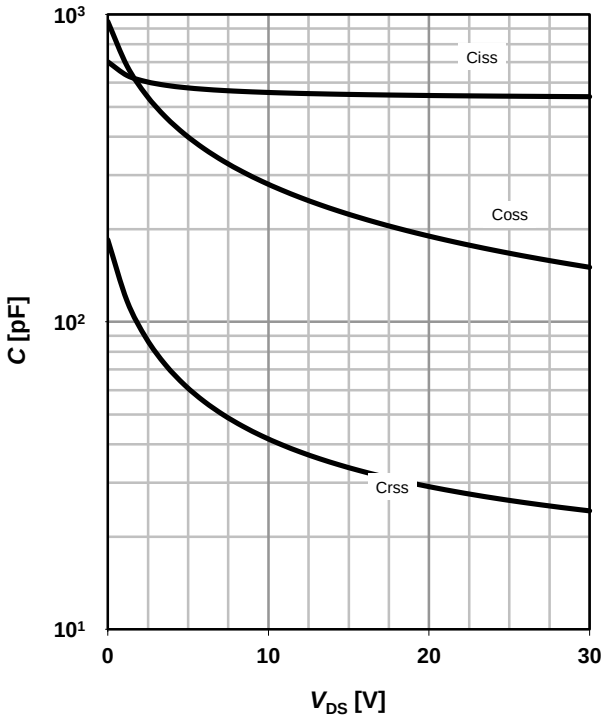
18 Typ. gate threshold voltage (Q2)

$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; $I_D=250$ µA



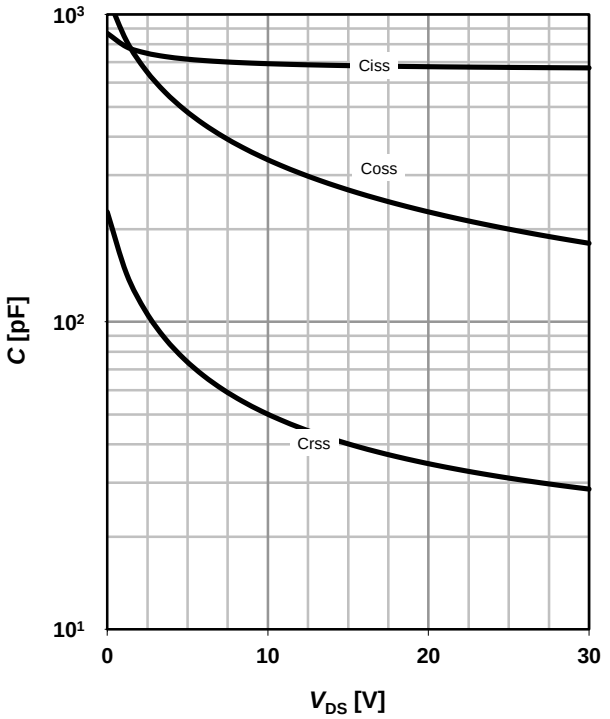
19 Typ. capacitances (Q1)

$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



20 Typ. capacitances (Q2)

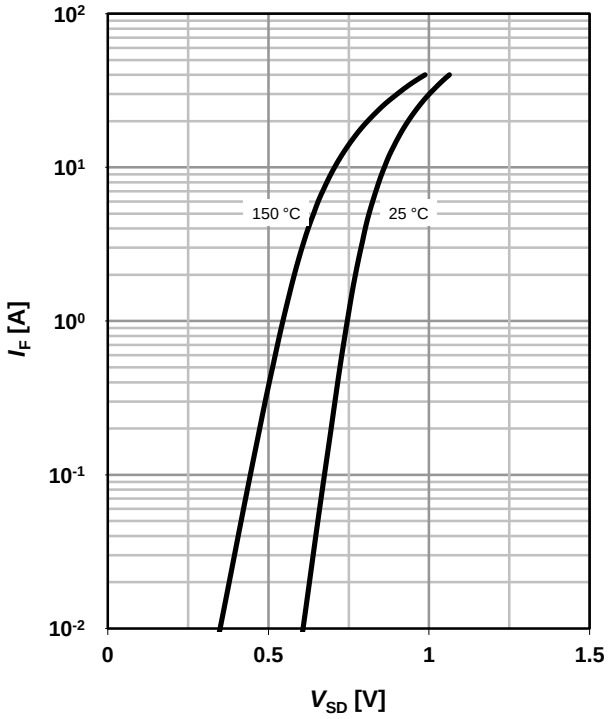
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



21 Forward characteristics of reverse diode (Q1)

$I_F=f(V_{SD})$

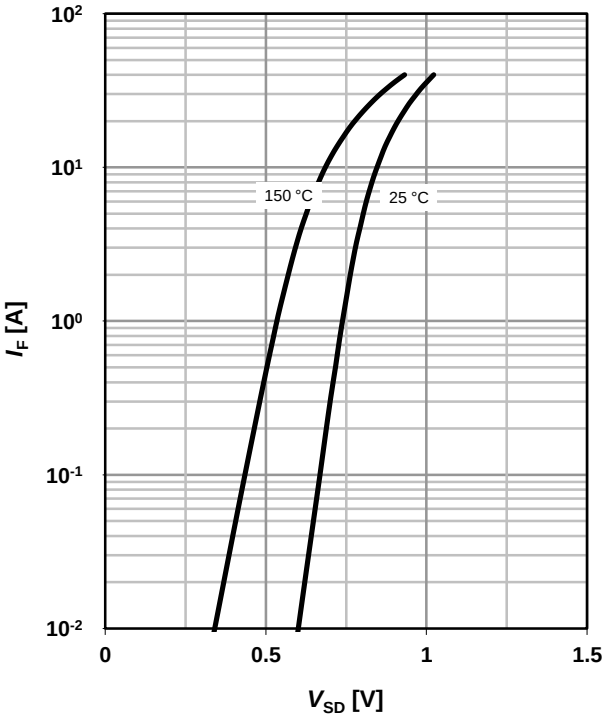
parameter: T_j



22 Forward characteristics of reverse diode (Q2)

$I_F=f(V_{SD})$

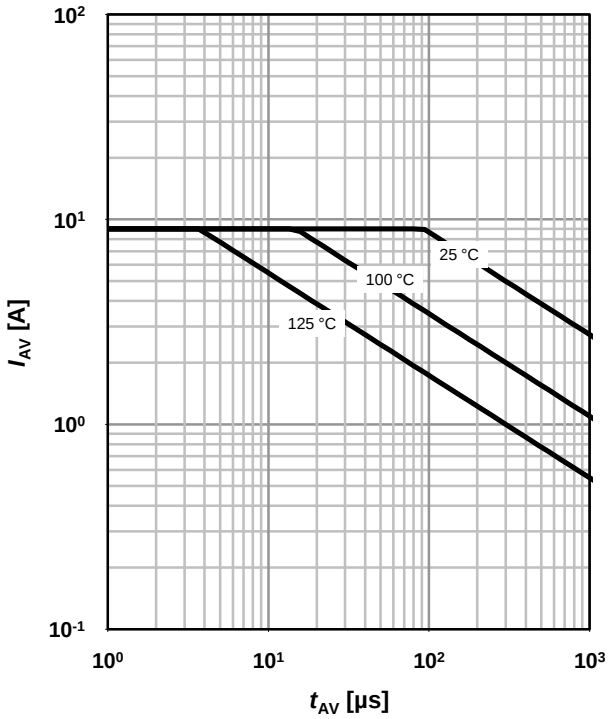
parameter: T_j



23 Avalanche characteristics (Q1)

$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$

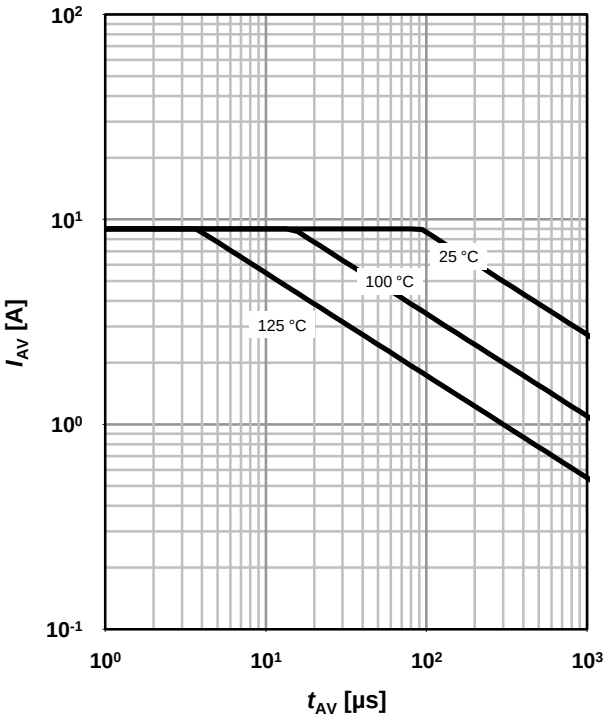
parameter: $T_{j(start)}$



24 Avalanche characteristics (Q2)

$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$

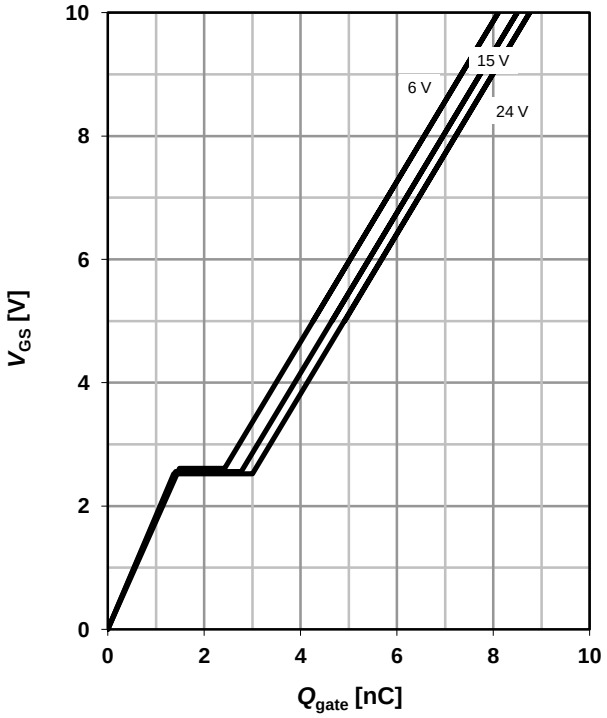
parameter: $T_{j(start)}$



25 Typ. gate charge (Q1)

V_{GS}=f(Q_{gate}); I_D=9 A pulsed

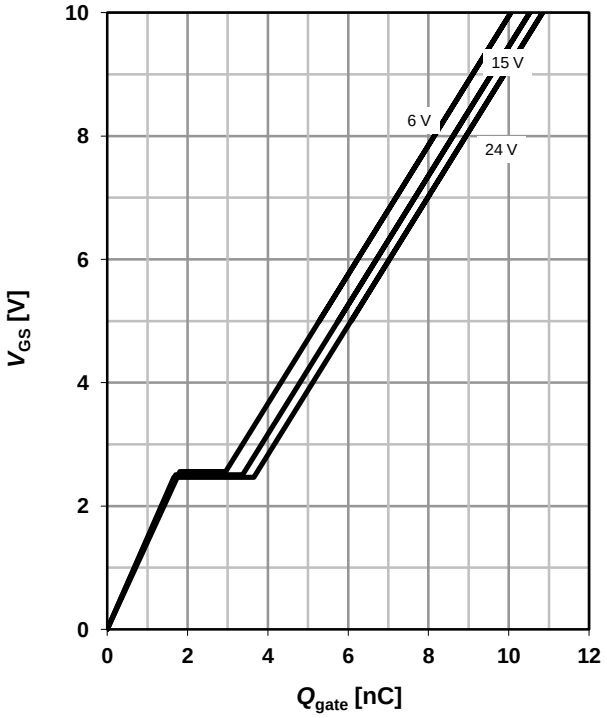
parameter: V_{DD}



26 Typ. gate charge (Q2)

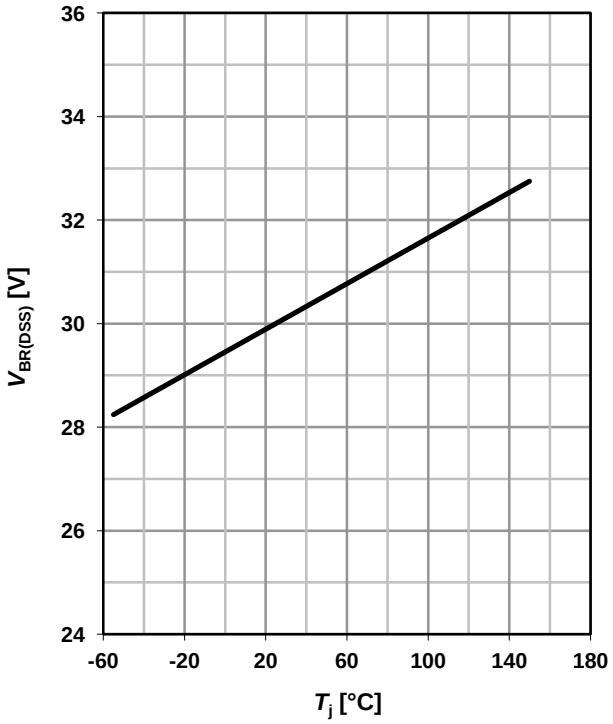
V_{GS}=f(Q_{gate}); I_D=9 A pulsed

parameter: V_{DD}



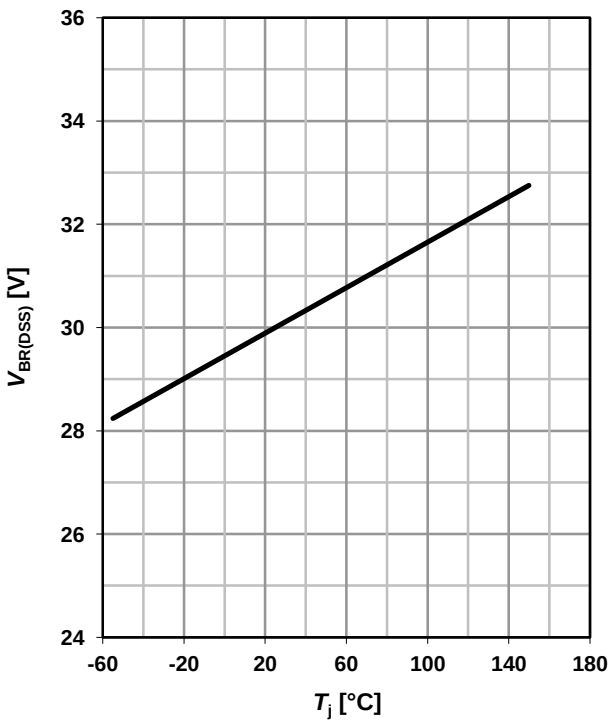
27 Drain-source breakdown voltage (Q1)

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



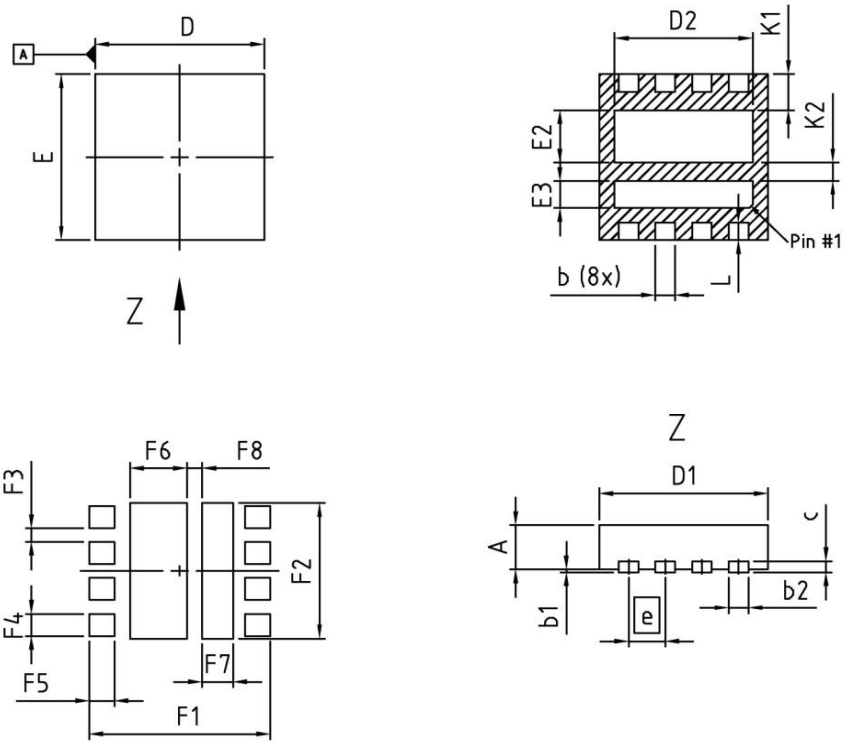
28 Drain-source breakdown voltage (Q2)

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



PG-WISON-8

WISON-8



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
b	0.25	0.45	0.010	0.018
b1	0.00	0.05	0.000	0.002
b2	0.25	0.45	0.010	0.018
c	0.10	0.30	0.004	0.012
D=D1	2.90	3.10	0.114	0.122
D2	2.35	2.55	0.093	0.100
E=E1	2.90	3.10	0.114	0.122
E2	0.85	1.05	0.033	0.041
E3	0.39	0.59	0.015	0.023
K1	0.55	0.75	0.022	0.030
K2	0.23	0.43	0.009	0.017
e	0.65 (BSC)		0.026 (BSC)	
N	8		8	
L	0.22	0.42	0.009	0.017
F1	3.21		0.126	
F2	2.45		0.096	
F3	0.25		0.010	
F4	0.40		0.016	
F5	0.45		0.018	
F6	1.01		0.040	
F7	0.55		0.022	
F8	0.27		0.011	

DOCUMENT NO.
Z8B00158767

SCALE
0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
15-09-2010

REVISION
01

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.