MC74HC237

1-of-8 Decoder/Demultiplexer with Address Latch

High–Performance Silicon–Gate CMOS

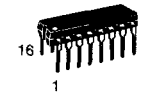
The MC74HC237 is identical in pinout to the LS137, but has noninverting outputs. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC237 decodes a three–bit Address to one–of–eight active–high outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active–low and one active–high, are provided to facilitate the demultiplexing, cascading, and chip–selecting functions.

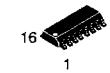
The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC237 is the noninverting version of the HC137.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity: 156 FETs or 39 Equivalent Gates



N SUFFIX
PLASTIC PACKAGE
CASE 648–08

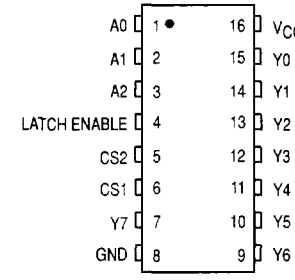


D SUFFIX
SOIC PACKAGE
CASE 751B–05

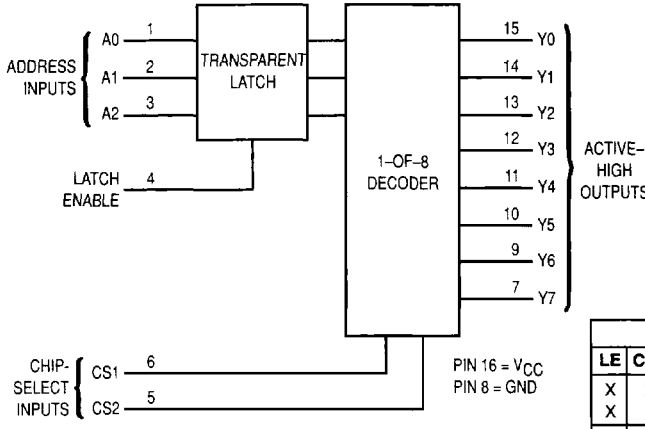
ORDERING INFORMATION

MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

PIN ASSIGNMENT



LOGIC DIAGRAM



FUNCTION TABLE

Inputs						Outputs							
LE	CS1	CS2	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X					*			

* = Depends upon the Address previously applied while LE was at a low level.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 1.5 to V_{CC} + 1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air Plastic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 2)	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1 2	
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\|$ ≤ 5.2 mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 4.0 mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\|$ ≤ 5.2 mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2.

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6)	2.0 4.5 6.0	235 47 40	295 59 50	355 71 60	ns
t_{PHL}		2.0 4.5 6.0	185 37 31	230 46 39	280 56 48	
t_{PLH}	Maximum Propagation Delay, CS2 to Output Y (Figures 2 and 6)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
t_{PHL}		2.0 4.5 6.0	145 29 25	180 36 31	220 44 38	
t_{PLH}	Maximum Propagation Delay, CS1 to Output Y (Figures 3 and 6)	2.0 4.5 6.0	200 40 34	250 50 43	300 60 51	ns
t_{PHL}		2.0 4.5 6.0	160 32 27	200 40 34	240 48 41	
t_{PLH}	Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t_{PHL}		2.0 4.5 6.0	190 38 32	240 48 41	285 57 48	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Package)*	100	pF

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Input A to Latch Enable (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Latch Enable to Input A (Figure 5)	2.0 4.5 6.0	50 10 9	65 13 11	75 15 13	ns
t_w	Minimum Pulse Width, Latch Enable (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 2)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2.

PIN DESCRIPTIONS

ADDRESS INPUTS

A0, A1, A2 (Pins 1, 2, 3)

Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

CONTROL INPUTS

CS1, CS2 (Pins 6, 5)

Chip select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the data inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a low level.

Latch Enable (Pin 4)

Latch Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the Address (CS1 = H and CS2 = L).

OUTPUTS

Y0–Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)

Active–high outputs. One of these eight outputs is selected when the chip is enabled (CS1 = H and CS2 = L) and the Address inputs correspond to that particular output. The selected output is at a high level while all others remain at a low level.

SWITCHING WAVEFORMS

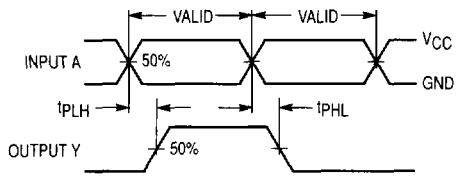


Figure 1.

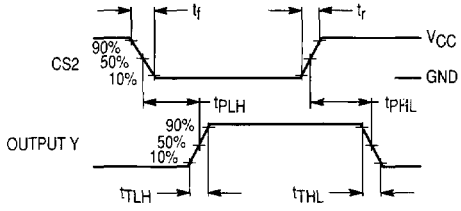


Figure 2.

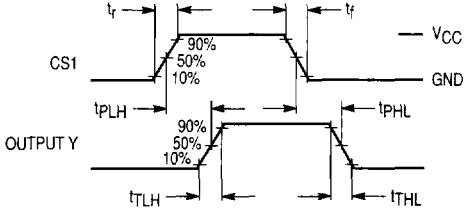


Figure 3.

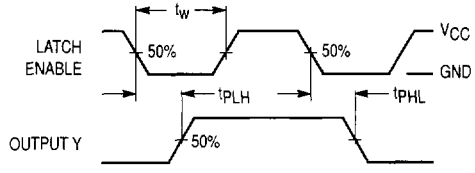


Figure 4.

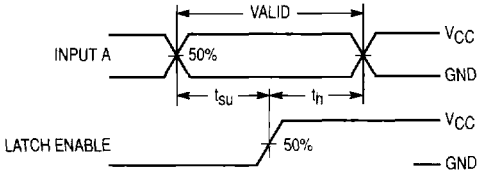
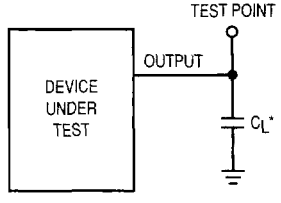


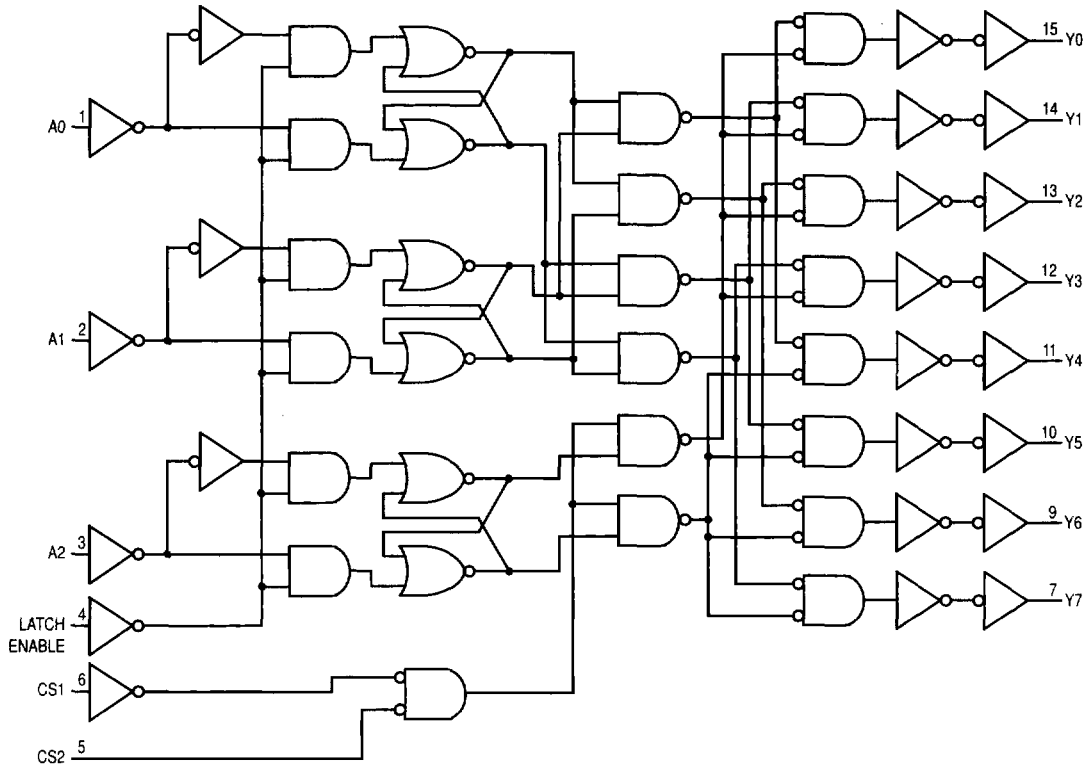
Figure 5.



* Includes all probe and jig capacitance

Figure 6. Test Circuit

EXPANDED LOGIC DIAGRAM



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