RClamp3331ZA
Ultra Small RailClamp®
1-Line, 3.3V ESD Protection

PROTECTION PRODUCTS

Description

RailClamp® TVS diodes are ultra low capacitance devices designed to protect sensitive electronics from damage or latch-up due to ESD, EFT, and EOS. They are designed for use on high speed ports in applications such as cell phones, notebook computers, and other portable electronics. These devices offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

RClamp®3331ZA features extremely good ESD protection characteristics including a low typical dynamic resistance of 0.20 Ohms, low peak ESD clamping voltage, and high ESD withstand voltage (±18kV contact per IEC 61000-4-2). Low typical capacitance (0.35pF at V_R=0V) allows the RClamp3331ZA to be used in applications operating in excess of 5GHz without appreciable signal attenuation. Each device will protect one high speed data line operating at 3.3 Volts.

RClamp3331ZA is in a 2-pin SLP0603P2X3F package measuring 0.6 x 0.3 mm with a nominal height of 0.25mm. Leads are finished with lead-free NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical. The combination of low peak ESD clamping, low dynamic resistance, and low capacitance makes this device suitable for applications such as USB 3.0, MIPI and V-By-One interfaces in portable devices.

Features

- High ESD withstand Voltage: ±20kV (air), ±18kV (contact) per IEC 61000-4-2
- Able to withstand over 1000 ESD strikes per IEC 61000-4-2 Level 4
- Ultra-small 0201 package
- Protects one high speed data line
- Working voltage: ± 3.3V
- Low capacitance: 0.35 pF (Typical)
- Extremely low dynamic resistance: 0.20 ohms (Typical)
- Low ESD clamping voltage
- Solid-state silicon-avalanche technology

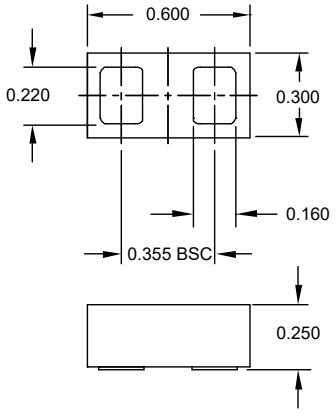
Mechanical Characteristics

- SLP0603P2X3F package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Nominal Dimensions: 0.6 x 0.3 x 0.25 mm
- Lead Finish: NiAu
- Marking: Marking code
- Packaging: Tape and Reel

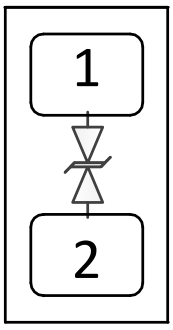
Applications

- USB2.0 / USB 3.0
- MIPI/MDDI
- V-By-One
- eDP
- MHL
- LVDS

Package Dimension



Schematic & Pin Configuration



SLP0603P2X3F (Bottom View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	30	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	4	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±20 ±18	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1 to 2 or 2 to 1				3.3	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 10 µA		5.5	8	10.5	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3V, Pin 1 to 2 or 2 to 1			<1	50	nA
Clamping Voltage	V_C	tp = 8/20µs, Pin 1 to 2 or 2 to 1	I_{PP} = 1A		3.8	5.5	V
		tp = 8/20µs, Pin 1 to 2 or 2 to 1	I_{PP} = 4A		5.5	7.5	
ESD Clamping Voltage[2]	V_C	tp = 0.2/100ns	I= 4A		4.5		
		tp = 0.2/100ns	I=16A		7		
Dynamic Resistance[2,3]	R_{DYN}	tp = 0.2/100ns			0.20		Ω
Junction Capacitance	C_J	V_R = 0V, f = 1MHz			0.35	0.45	pF

Notes

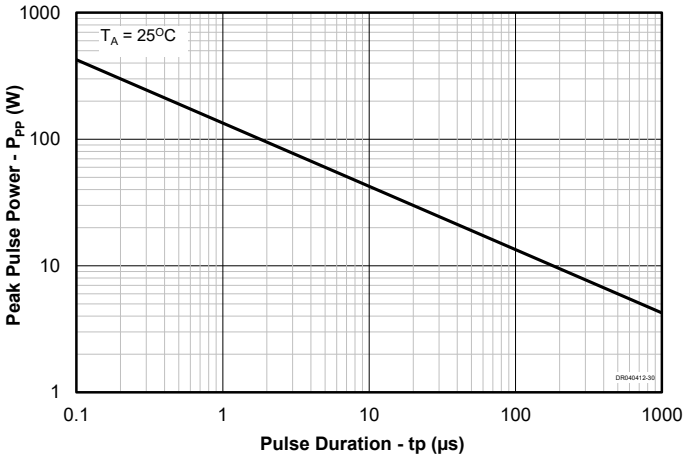
1) ESD gun return path connected to ESD ground plane.

2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.

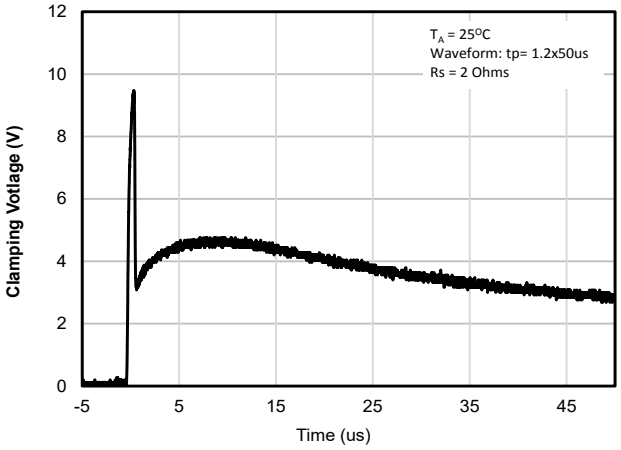
3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

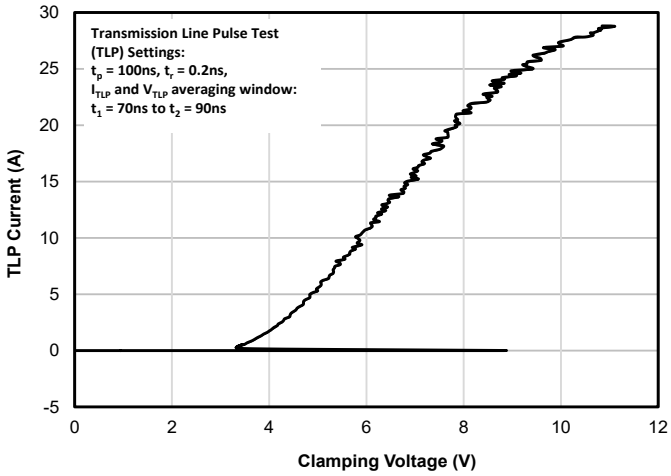
Non-Repetitive Peak Pulse Power vs. Pulse time



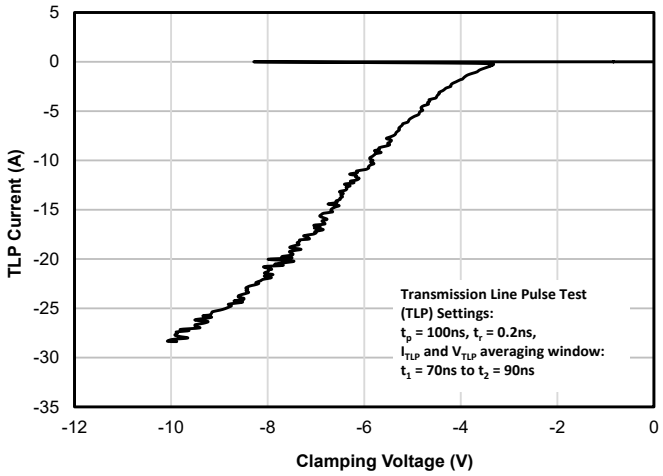
Clamping Voltage (tp = 1.2/50 µs)



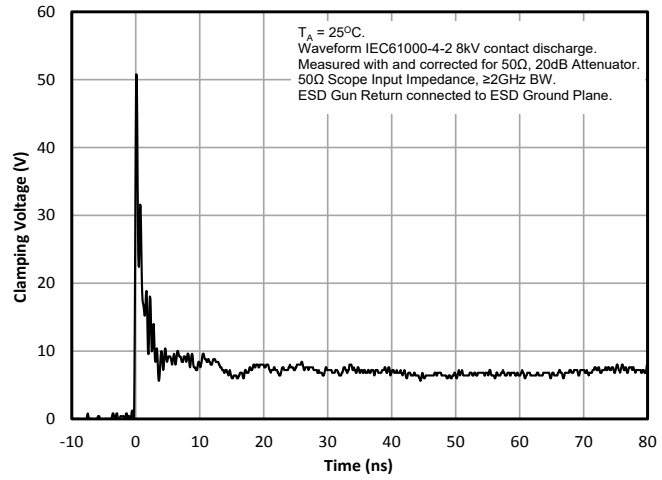
TLP Characteristic (Positive Pulse)



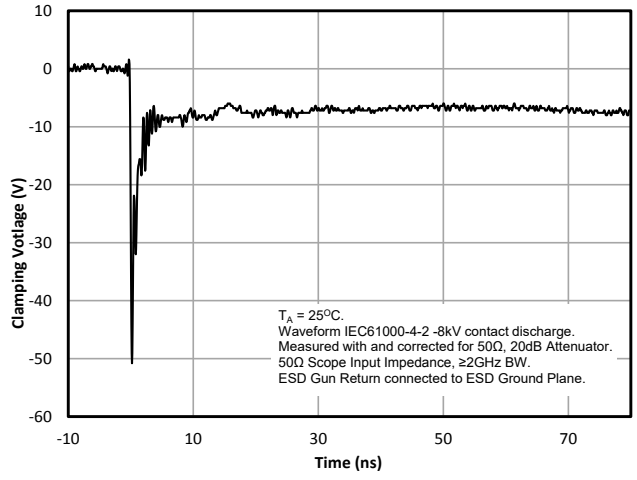
TLP Characteristic (Negative Pulse)



ESD Clamping (+8kV Contact per IEC 61000-4-2)

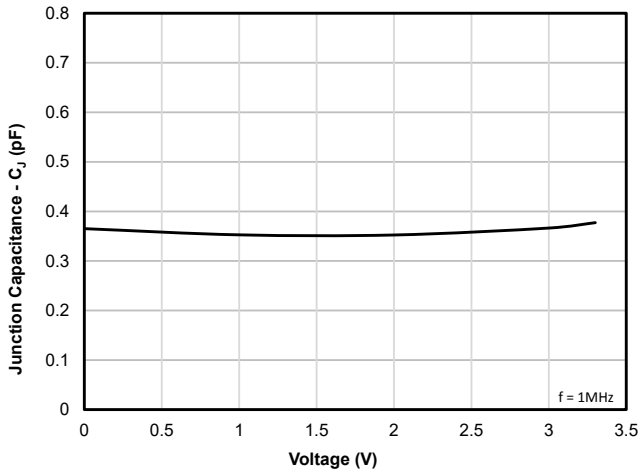


ESD Clamping (-8kV Contact per IEC 61000-4-2)

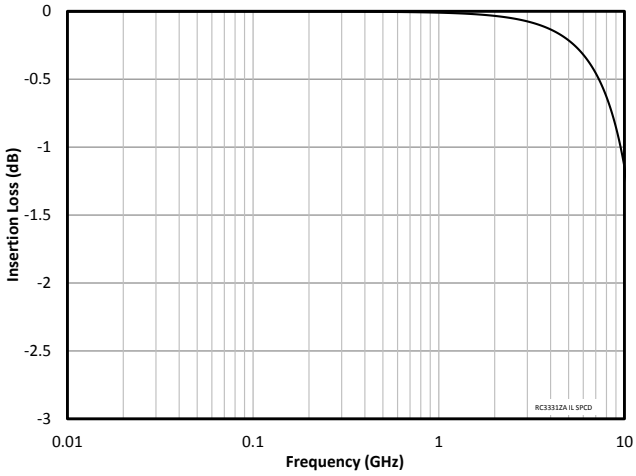


Typical Characteristics (Continued)

Junction Capacitance vs. Reverse Voltage



Insertion Loss - S21



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

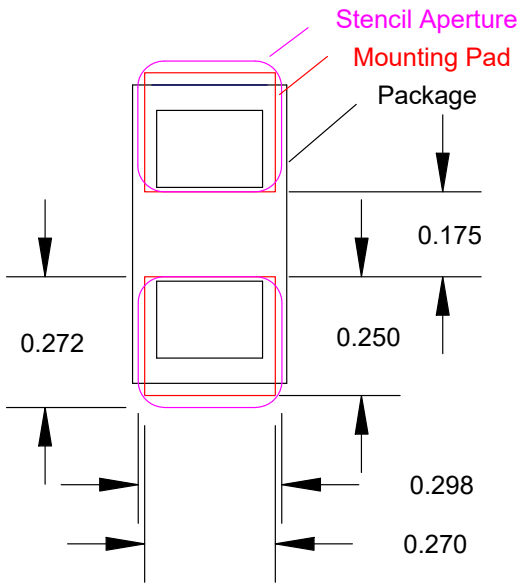
Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. An area ratio of 0.70 – 0.75 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

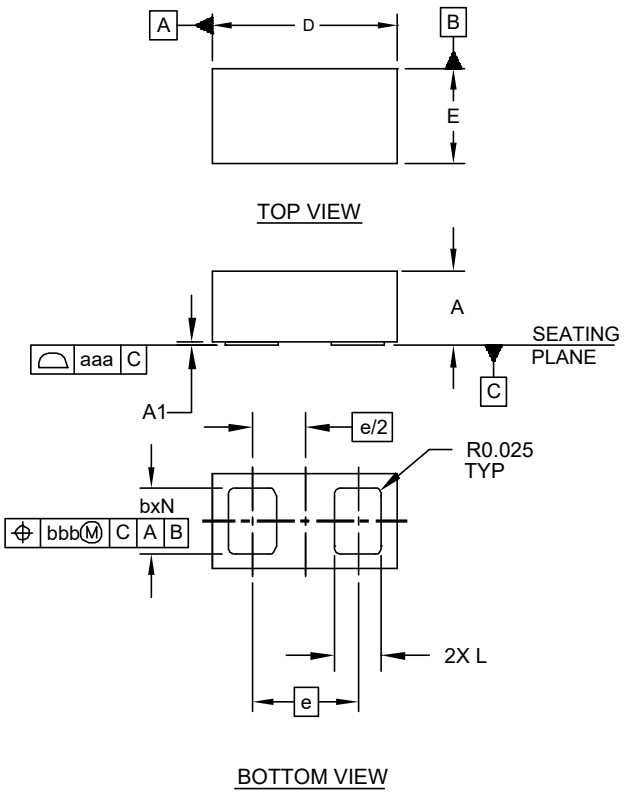
Semtech recommends a stencil thickness of 0.100mm for this device. The stencil should be laser cut with electropolished finish. The stencil should have a positive taper of approximately 5 degrees. Electro polishing and tapering the walls results in reduced surface friction and better paste release. For small pitch components, Semtech recommends a square aperture with rounded corners for consistent solder release. Due to the small aperture size, a solder paste with Type 4 or smaller particles are recommended.

Recommended Mounting Pattern



Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu

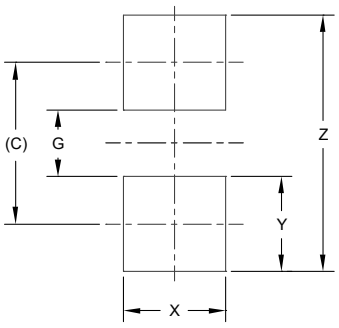
Outline Drawing - SLP0603P2X3F



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.235	0.250	0.265
A1	0.000	0.010	0.050
b	0.200	0.220	0.240
D	0.580	0.600	0.620
E	0.280	0.300	0.320
e	0.355 BSC		
L	0.140	0.160	0.180
N	2		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

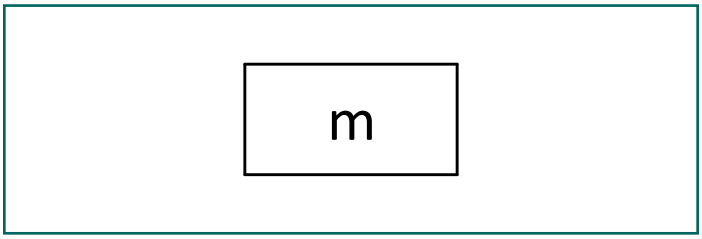
Land Pattern - SLP0603P2X3F



DIMENSIONS	
DIM	MILLIMETERS
(C)	(0.425)
G	0.175
X	0.270
Y	0.250
Z	0.675

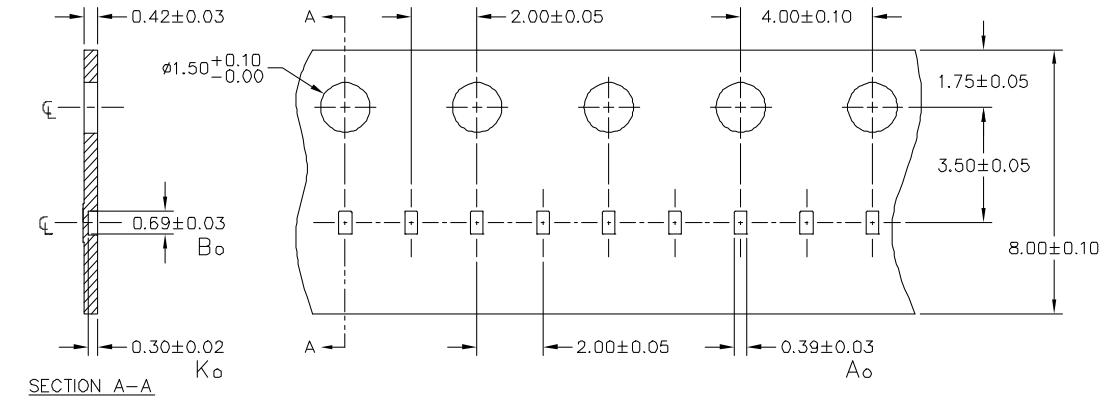
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

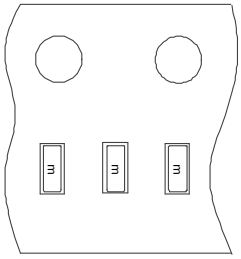


Note: Device is electrically symmetrical.

Tape and Reel Specification



NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Device Orientation in Tape

Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp3331ZATFT	15,000	7″

Contact Information

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