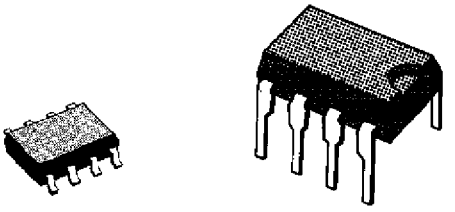
SGS-THOMSON MICROELECTRONICS

LCP1511
LCP1512

PROGRAMMABLE TRANSIENT VOLTAGE SUPPRESSOR FOR SLIC PROTECTION

FEATURES

- DUAL PROGRAMMABLE TRANSIENT SUPPRESSOR.
- WIDE NEGATIVE FIRING VOLTAGE RANGE: V_{MGL} = -80 V max
- HOLDING CURRENT = 150 mA.
- LOW GATE TRIGGERING CURRENT: I_{GT} = 15 mA max.
- PEAK PULSE CURRENT : I_{PP} = 30 A , 10/1000 µs
- AVAILABLE IN SO 8 AND DIP 8.



SO 8
(Plastic)

DIL 8
(Plastic)

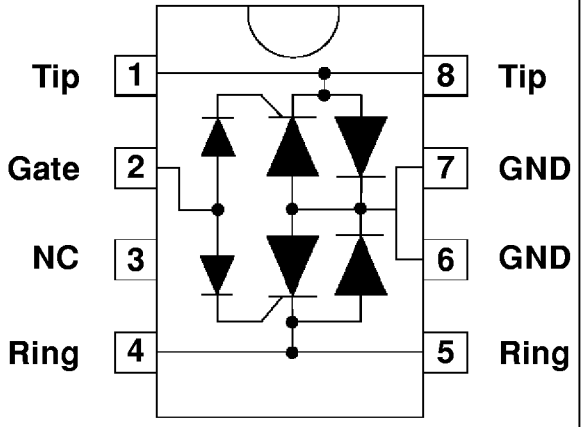
DESCRIPTION

This device has been especially designed to protect subscriber line card interfaces (SLIC) against transient overvoltages.

Positive overloads are clipped with two diodes. When negative surges are suppressed by two protection thyristors, the breakdown voltage of which is referenced to the -Vbat.

This component presents a very low gate triggering current (I_{GT}) in order to reduce the current comsumption on PC board during the firing phase .
A particular attention has been given to the internal wire bonding . A "4-points configuration" ensures a reliable protection, eliminating the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt) especially for very fast transients.

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

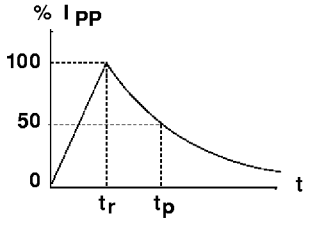
CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (-40°C ≤ Tamb ≤ +85°C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current see note 1.	10/1000 µs 5/320 µs 2/10 µs	30 40 90	A
I_{TSM}	Non repetitive surge peak on-state current f = 50 Hz	tp = 10 ms tp = 1 s	5 3.5	A
I_{GSM}	Maximum gate current (hall sine wave 10 ms)		2	A
V_{MLG} V_{MGL}	Maximum Voltage LINE/GND Maximum Voltage GATE/LINE		- 100 - 80	V
T_{stg} T_j	Storage and operating junction temperature range		- 55 to + 150 150	°C °C

Note 1: Pulse waveform

10/1000 µs	tr = 10 µs	tp = 1000 µs
5/320 µs	tr = 5 µs	tp = 320 µs
2/10 µs	tr = 2 µs,	tp = 10 µs

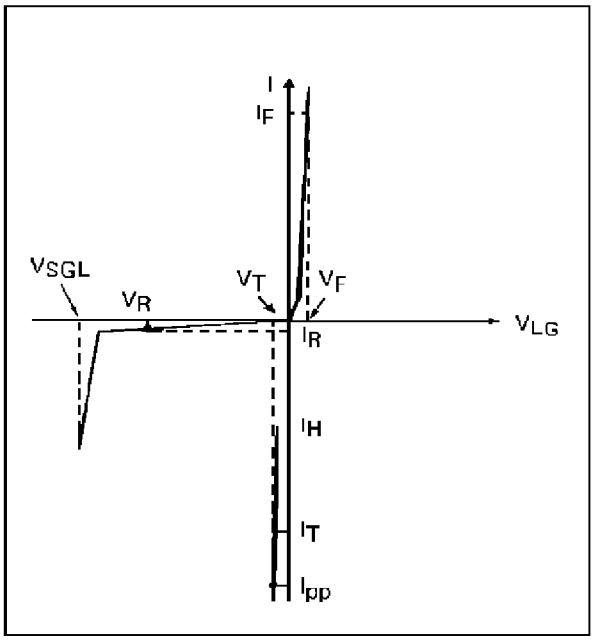


THERMAL RESISTANCES

Symbol	Parameter		Value	Unit
R_{th} (j-a)	Junction-to-ambient	DIL 8 SO 8	125 171	°C/W °C/W

ELECTRICAL CHARACTERISTICS

Symbol	Parameter
I_{GT}	Gate Trigger Current
I_H	Holding Current
I_R	Reverse Leakage Current LINE/GND
I_{RG}	Reverse Leakage Current GATE/LINE
V_R	Reverse Voltage LINE/GND
V_F	Forward Voltage LINE/GND
V_{GT}	Gate Trigger Voltage
V_{FP}	Peak Forward Voltage LINE/GND
V_{SGL}	Dynamic Switching Voltage GND/LINE
V_{gate}	GATE/GND Voltage
V_{LG}	LINE/GND Voltage
dv/dt	Critical Rate of rise of off State Voltage
V_T	On State Voltage
C_{off}	Off State Capacitance LINE/GND



PARAMETERS RELATED TO THE DIODE LINE/GND

Symbol	Test Conditions	Max.	Unit
V_F	Square pulse, tp = 500 µs, I_F = 5 A	3	V
V_{FP}	Ipp = 30 A, 10/1000 µs.	15	V

PARAMETERS RELATED TO PROTECTION THYRISTOR

Symbol	Tests Conditions		Min.	Max.	Unit
I_{GT}	$V_{GND/LINE}$ = -48 V		0.2	15	mA
I_H	V_{GATE}= -48 V	Note 2.	150		mA
V_{GT}	at I_{GT}			2.5	V
I_{RG}	Tc = 25°C Tc = 70°C	V_{RG} = -75 V V_{RG} = -75 V		5 50	µA µA
V_{SGL}	V_{GATE}= -48 V	Note 2.		- 63	V
V_T	Square pulse, Tp = 500 µs, I_T = 0.5 A Square pulse, Tp = 500 µs, I_T = 3 A			3 4	V V

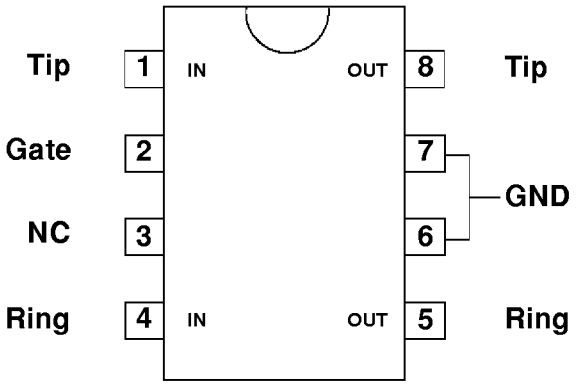
PARAMETERS RELATIVE TO DIODE AND PROTECTION THYRISTOR

Symbol	Tests Conditions			Min.	Max.	Unit
I_R	Tc = 25°C Tc = 70°C	-1 < V_{GL} < -Vbat -1 < V_{GL} < -Vbat	V_R = - 85 V V_R = - 85 V		5 50	µA µA
C_{off}	V_R = - 3 V V_R = - 48 V		F < 1MHz F < 1MHz		100 50	pF pF

All Parameters Tested at 25 °C except when indicated.

Note 2 : See test circuit for I_H and V_{SGL}.

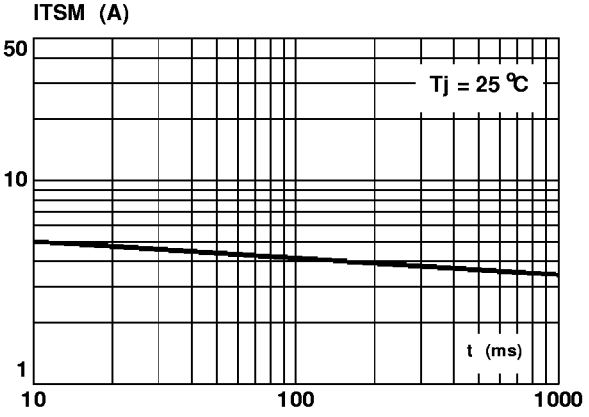
APPLICATION NOTE



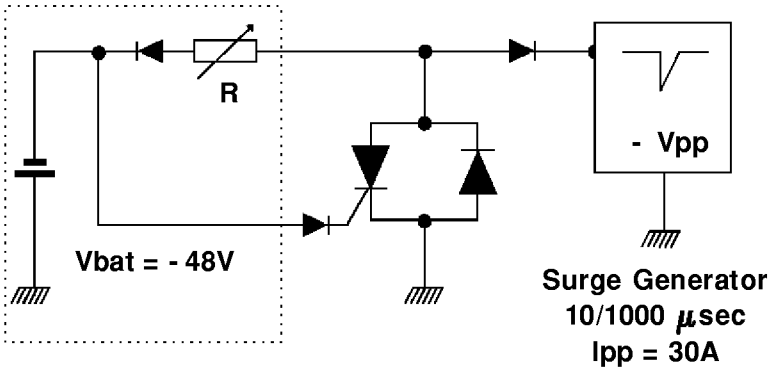
4- points structure lay-out.

In order to take advantage of the "4-points structure" of the LCPxxxx, the tip and Ring lines have to cross through the device. In this case, the device will eliminate the overvoltages generated by the parasitic inductances of the wiring (Ldi/dt), especially for very fast Transients.

Figure 1 : Non repetitive surge peak on-state current. (with sinusoidal pulse : F =50Hz)



TEST CIRCUIT FOR I_H AND V_{SGL} PARAMETERS



This is a GO-NOGO Test which allows to confirm the holding current (I_H) level, and to measure the dynamic switching voltage (V_{SGL}).

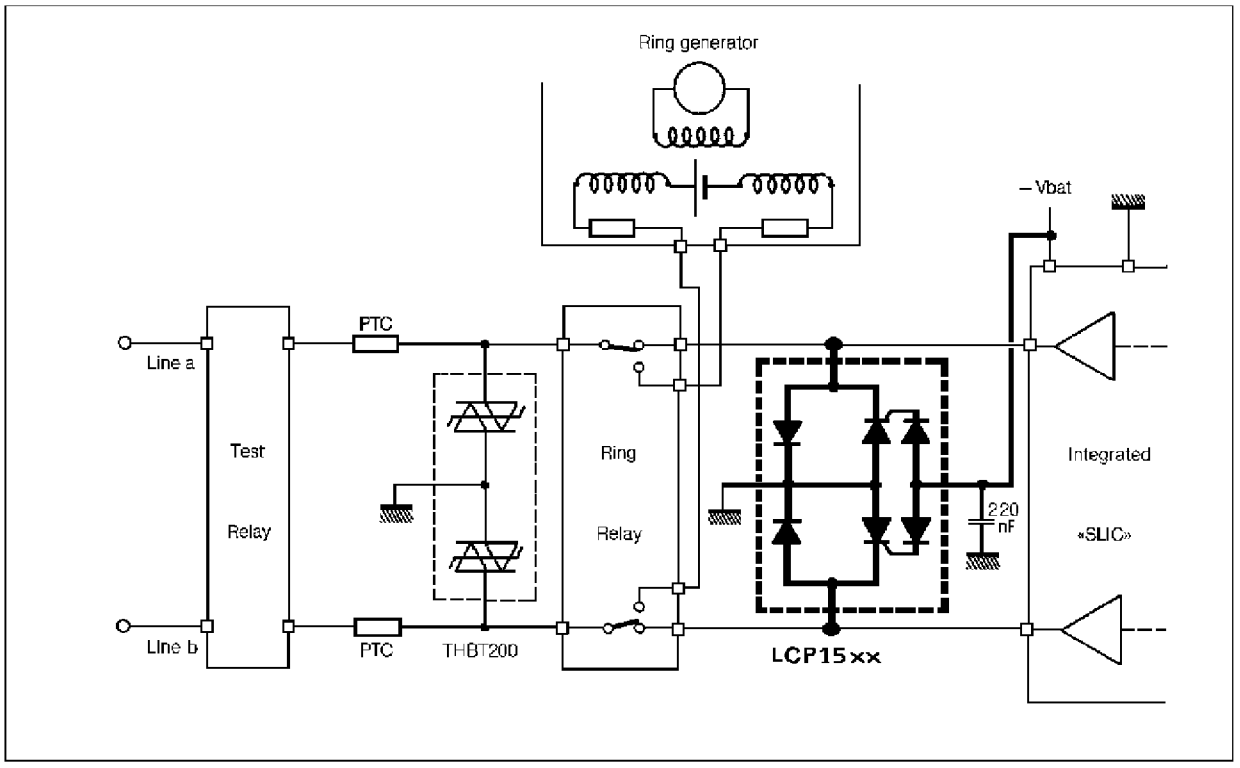
TEST PROCEDURE :

1) Adjust the current level at the I_H value by short circuiting the AK of the D.U.T.
2) Fire the D.U.T with a surge Current : Ipp = 30A , 10/1000 µs.
3) The D.U.T will come back to the OFF-State within a duration of 50 ms max.

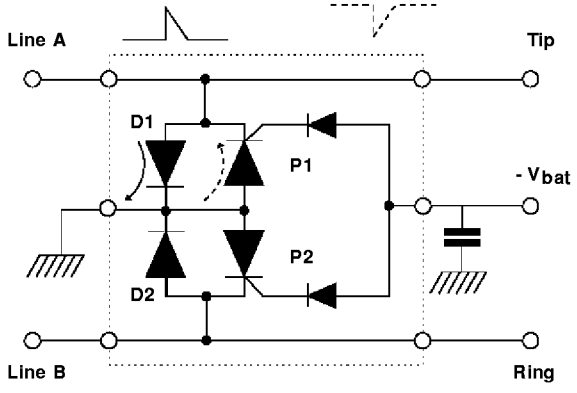
- The V_{SGL} is measured just before firing.

APPLICATION CIRCUIT

Typical slic protection concept



FUNCTIONAL DESCRIPTION



LINE A PROTECTION:

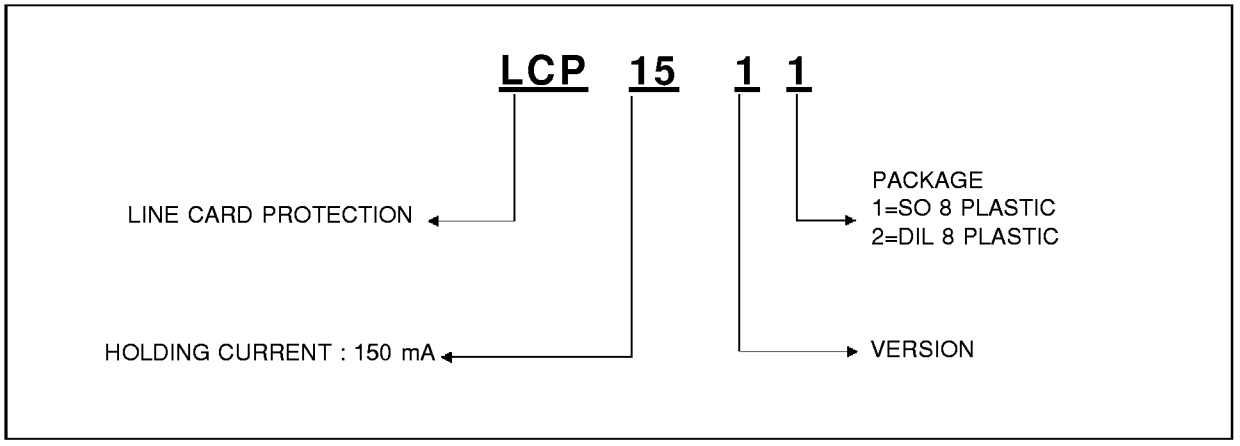
- For positive surges versus GND, the diode D1 will conduct.
- For negative surges versus GND, the protection device P1 will trigger at a voltage fixed by the -VBAT reference.

LINE B PROTECTION:

- For surges on Line B, the operating mode is the same , D2 or P2 is activated.

- A capacitor (C = 220nF) can be added close to the gate of the LCP15xx, in order to speed up the triggering.

ORDER CODE



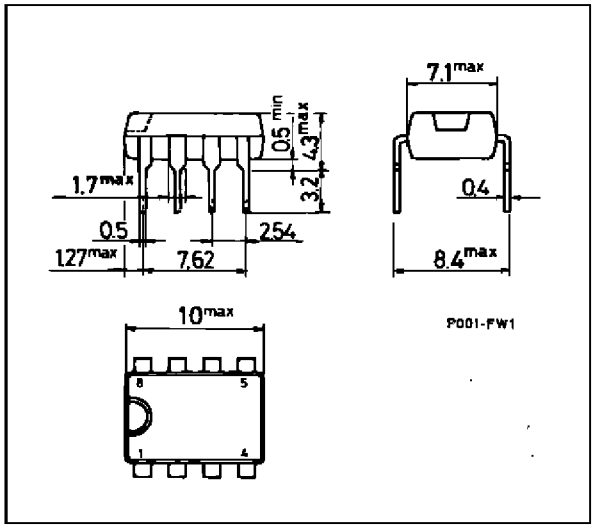
MARKING

Package	Type	Marking
SO8	LCP1511	CP1511
DIL8	LCP1512	CP1512

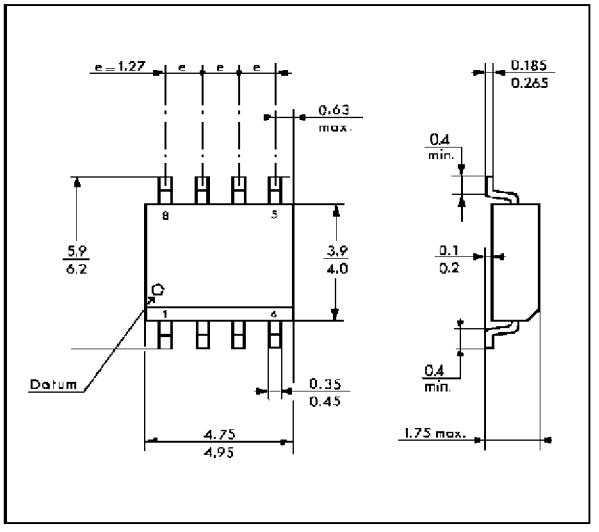
Packaging : Products supplied in antistatic tubes.

PACKAGE MECHANICAL DATA (in millimeters)

DIL 8 Plastic

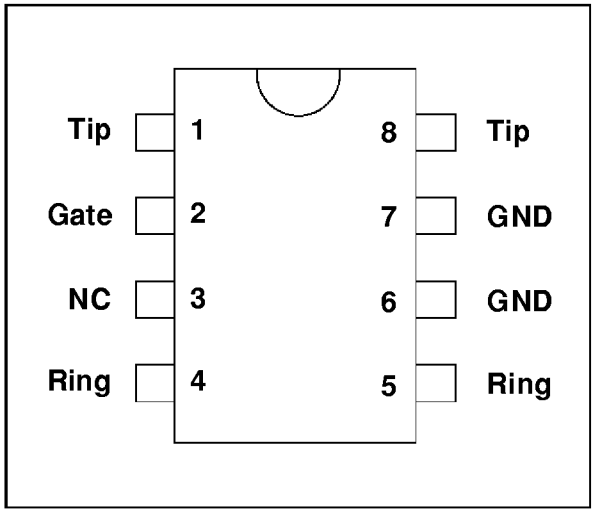


SO 8 Plastic



CONNECTION DIAGRAMS

DIL 8 Plastic



SO 8 Plastic