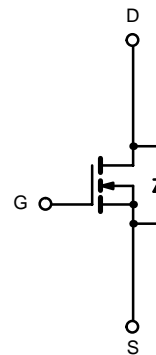
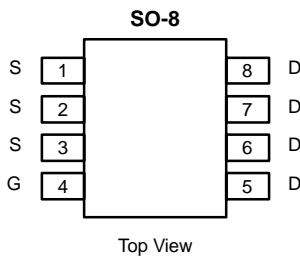




N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.024 @ $V_{GS} = 10$ V	7.5
	0.03 @ $V_{GS} = 6.0$ V	6.5



Ordering Information: Si4450DY
Si4450DY-T1 (with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	7.5	A
	$T_A = 70^\circ\text{C}$		5.5	
Pulsed Drain Current		I_{DM}	50	
Continuous Source Current (Diode Conduction) ^a		I_S	2.1	
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	50	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

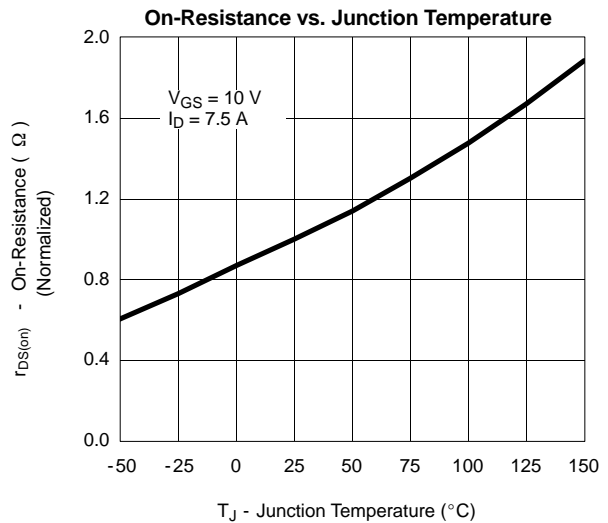
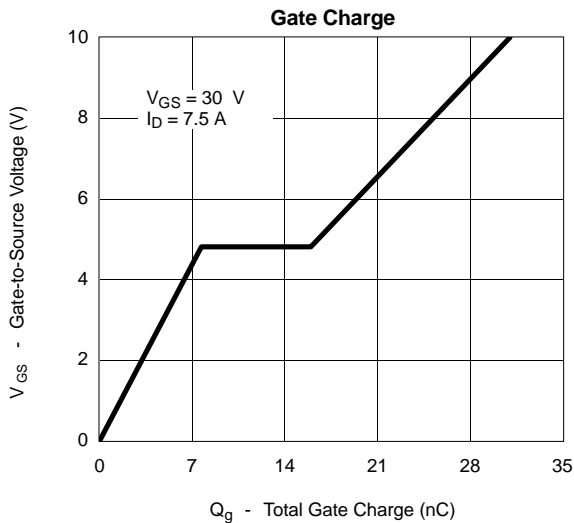
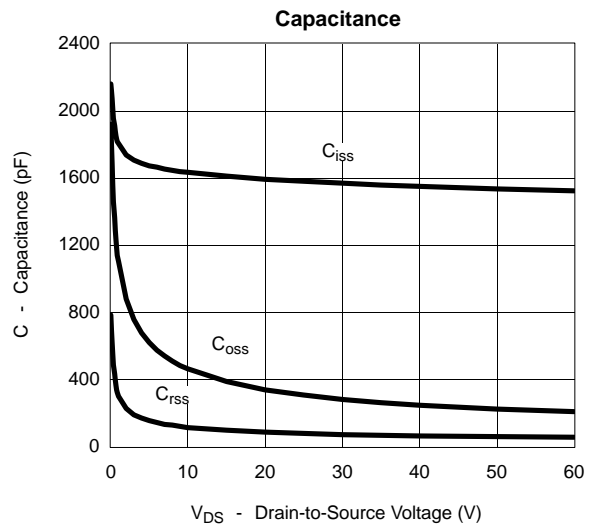
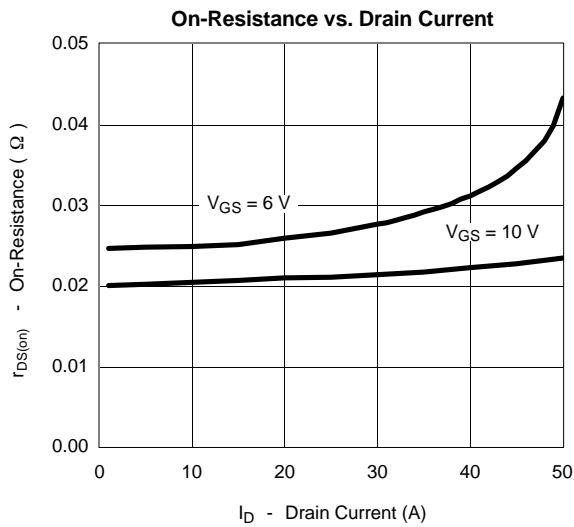
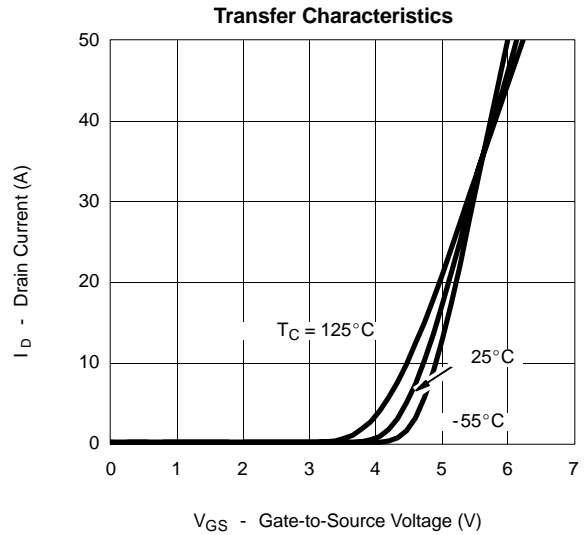
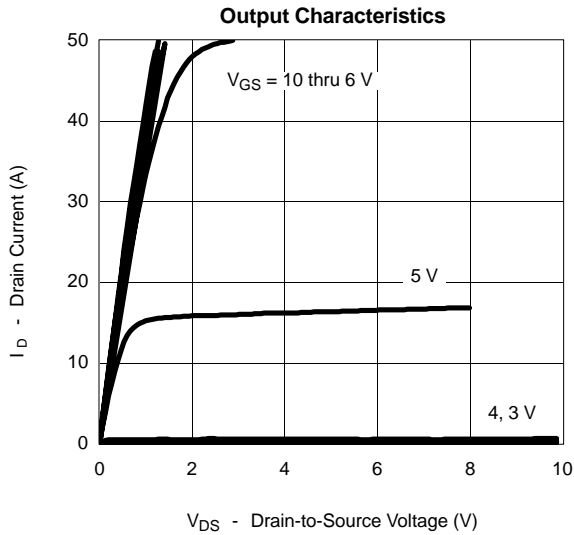
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			20	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.5 A		0.020	0.024	Ω
		V _{GS} = 6.0 V, I _D = 6.5 A		0.025	0.03	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 7.5 A		18.5		S
Diode Forward Voltage ^b	V _{SD}	I _S = 2.1 A, V _{GS} = 0 V		0.75	1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 7.5 A		31	50	nC
Gate-Source Charge	Q _{gs}			7.7		
Gate-Drain Charge	Q _{gd}			8.3		
Gate Resistance	R _g		1		5.8	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		16	30	ns
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			41	80	
Fall Time	t _f			21	40	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.1 A, di/dt = 100 A/μs		46	80	

Notes

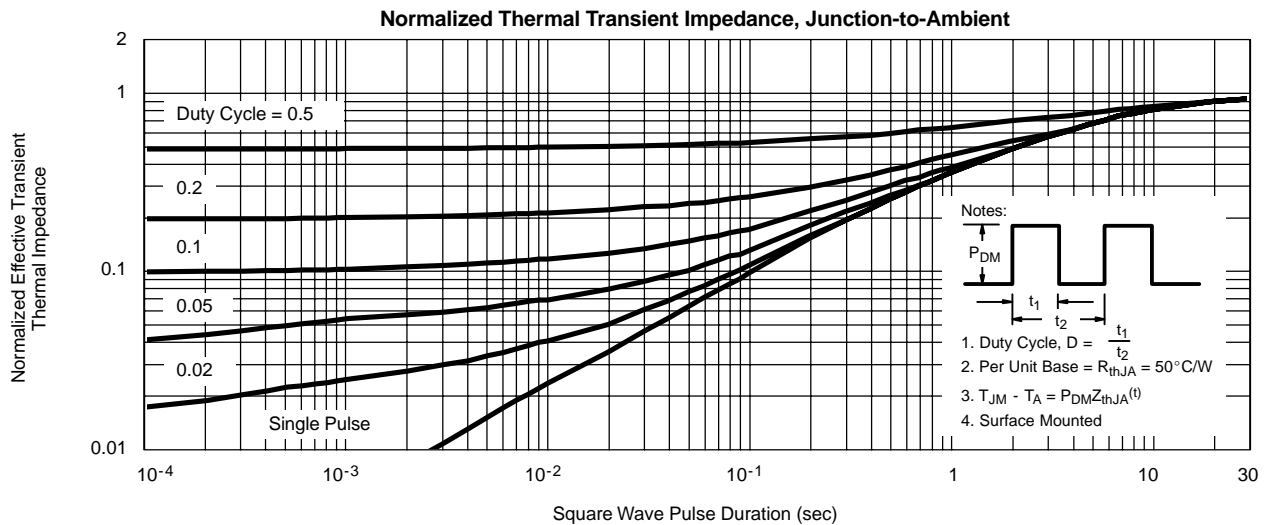
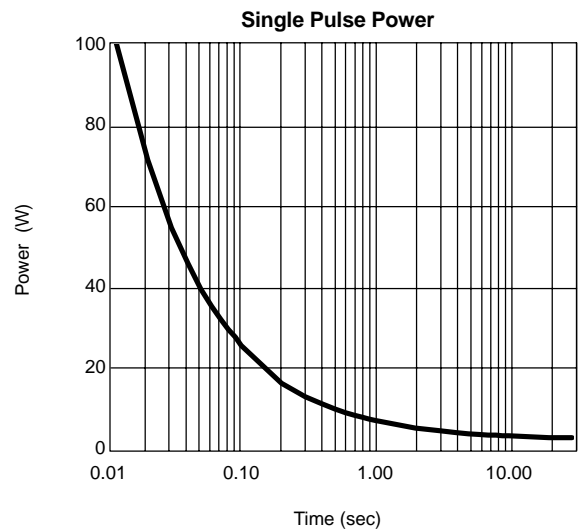
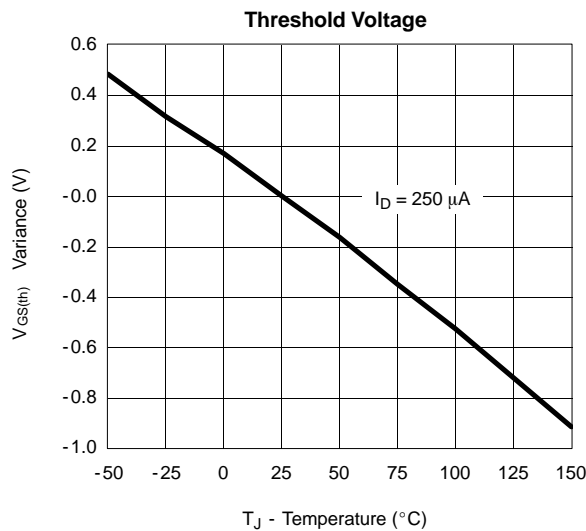
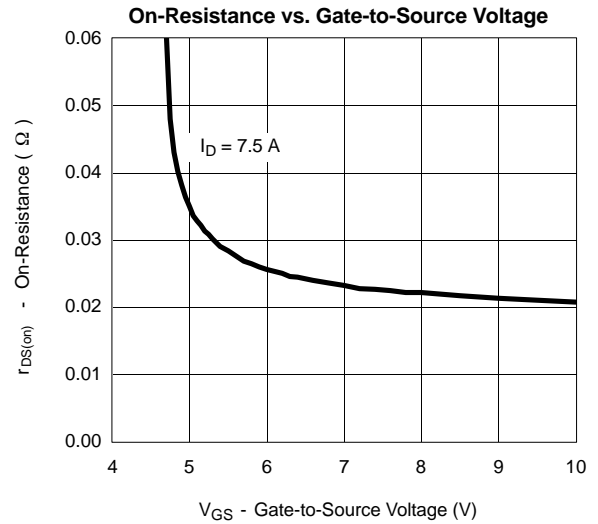
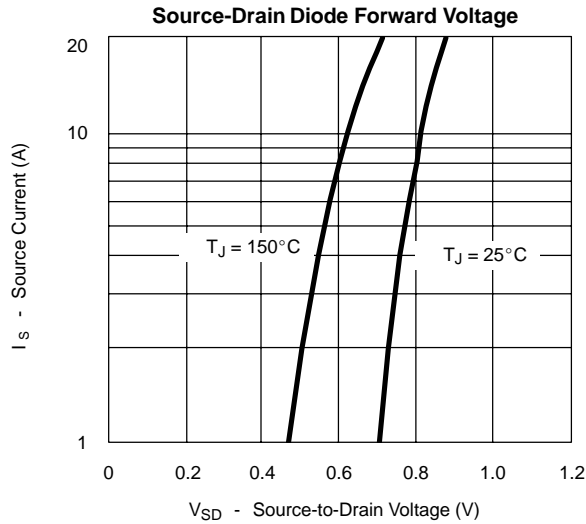
- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





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