

## FINAL DATA SHEET

# SKY5®-3728-11: 5G NR UHB Diversity Receive Module

## Applications

- 5G NR sub-6GHz smartphones and tablets
- 5G NR sub-6GHz data cards

## Features

- Low insertion loss
- High-performance variable gain LNAs
- Integrated SRS support through TRX port
- Integrated MIPI v2.1+ interface
- Integrated package shielding
- Small ( $2.8 \times 2.6 \times 0.7$  mm [max]) 21-lead MCM package (MSL3, 260 °C per JEDEC J-STD-020)



Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

## Description

The SKY53728-11 is a highly integrated LNA filter module that enables users to support new 5G New Radio (NR) bands in the 3.3 to 4.2 GHz and 4.4 to 5.0 GHz frequency ranges. It utilizes the latest advanced SOI process technologies to achieve leading high-bandwidth, low noise figure (NF) LNA performance in a small package footprint. It also integrates all the required filtering to attenuate unwanted out-of-band blockers in adjacent and far-out frequency bands while maintaining very low insertion loss (IL) performance in the pass-band frequencies.

The SKY53728-11 is packaged in a small  $2.8 \times 2.6 \times 0.7$  mm (max), 21-lead surface-mount package. No external DC blocking capacitors are required on the RF paths as long as no DC voltage is applied. The part can operate over the temperature range of -30 °C to +85 °C.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

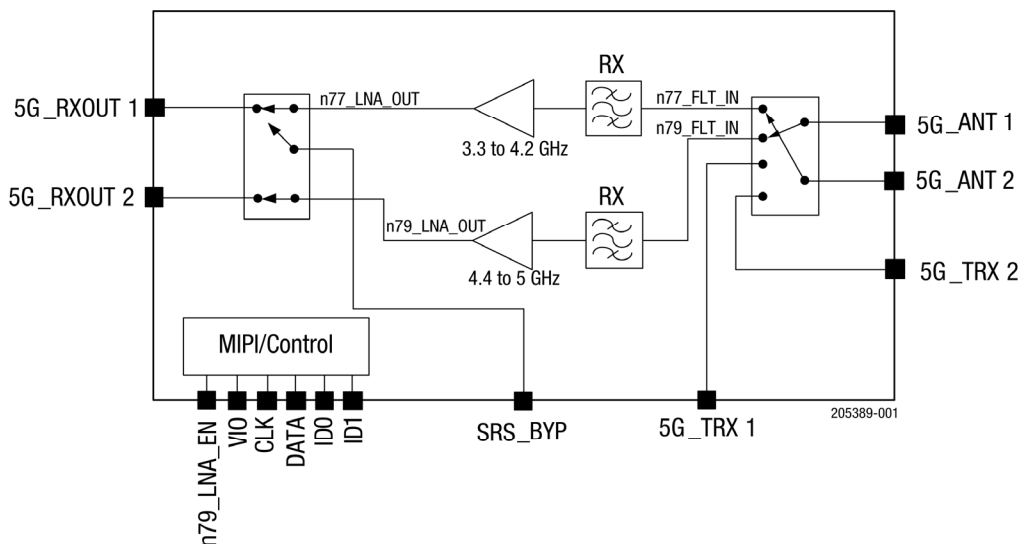
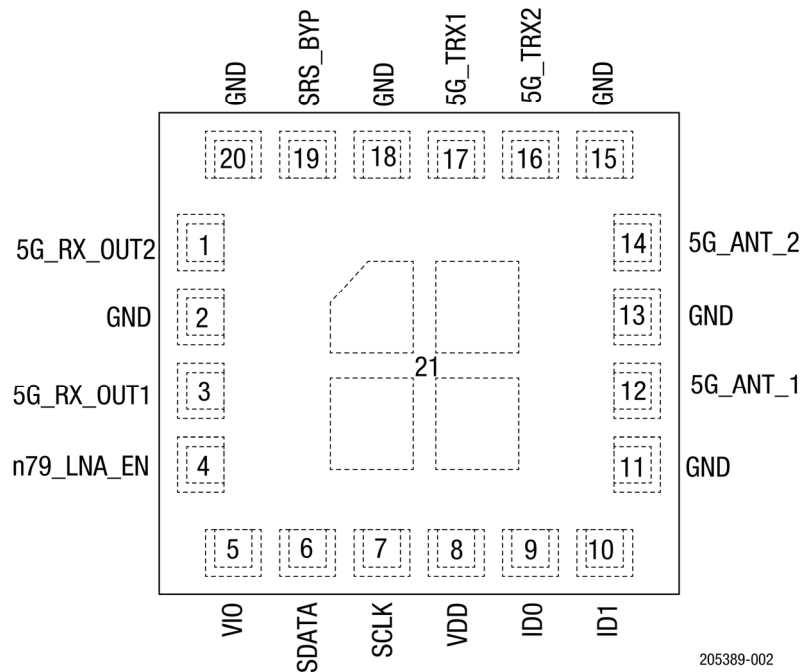


**Figure 1. SKY53728-11 Block Diagram**



205389-002

**Figure 2. SKY53728-11 Pinout  
(Top View)**

**Table 1. SKY53728-11 Signal Descriptions**

| Pin | Name                    | Description       | Pin | Name    | Description |
|-----|-------------------------|-------------------|-----|---------|-------------|
| 1   | 5G_RX_OUT2              | DRx output 2      | 12  | 5G_ANT1 | ANT1 input  |
| 2   | GND                     | Ground            | 13  | GND     | Ground      |
| 3   | 5G_RX_OUT1              | DRx output 1      | 14  | 5G_ANT2 | ANT2 input  |
| 4   | n79_LNA_EN <sup>1</sup> | n79 LNA control   | 15  | GND     | Ground      |
| 5   | VIO                     | VIO voltage       | 16  | 5G_TRX2 | TRX2 input  |
| 6   | SDATA                   | Data input/output | 17  | 5G_TRX1 | TRX1 input  |
| 7   | SCLK                    | Clock input       | 18  | GND     | Ground      |
| 8   | VDD                     | Supply voltage    | 19  | SRS_BYP | SRS bypass  |
| 9   | ID0 <sup>2</sup>        | ID select, bit 0  | 20  | GND     | Ground      |
| 10  | ID1 <sup>2</sup>        | ID select, bit 1  | 21  | GND     | Ground      |
| 11  | GND                     | Ground            |     |         |             |

<sup>1</sup> If this pin is high (VIO), n79 LNA is disabled and overrides MIPI. If it is low (GND) or N/C, n79 LNA is controlled through MIPI.

<sup>2</sup> USID decoding information:

| ID1 | ID0 | USID |
|-----|-----|------|
| 0   | 0   | 0111 |
| 0   | 1   | 1000 |
| 1   | 0   | 1001 |
| 1   | 1   | 1010 |

## Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY53728-11 are provided in Table 2. Electrical specifications are provided in Table 3.

The RFFE register map information is shown in Table 4. RF performance specifications for individual band frequencies are shown in Tables 5 and 6.

**Table 2. SKY53728-11 Absolute Maximum Ratings<sup>1</sup>**  
(TOP = +25 °C, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)

| Parameter                                                                                                                                                                      | Symbol             | Conditions                   | Min  | Typ | Max            | Units             |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------------------|------|-----|----------------|-------------------|
| Maximum input power:<br>All gain modes ANT - All in-band LNA_OUT (CW, 5000 hrs)<br>All gain modes ANT - All out-of-band LNA_OUT (CW, 5000 hrs)<br>All TRX - ANT (CW, 5000 hrs) | PIN <sub>MAX</sub> |                              |      |     | 12<br>15<br>36 | dBm<br>dBm<br>dBm |
| Storage temperature                                                                                                                                                            | T <sub>STG</sub>   |                              | -30  |     | 150            | °C                |
| Operating case temperature                                                                                                                                                     | T <sub>CASE</sub>  |                              | -30  |     | 100            | °C                |
| Supply voltage                                                                                                                                                                 | V <sub>DD</sub>    | DC voltage to GND, VDD pin   | -0.5 |     | 2.5            | V                 |
| MIPI VIO voltage                                                                                                                                                               | VIO                | DC voltage to GND, RFFE pins | -0.5 |     | 2.5            | V                 |
| Electrostatic discharge:<br>Charged Device Model (CDM)<br>Human Body Model (HBM)                                                                                               | ESD                |                              |      |     | ≥1000<br>≥1000 | V<br>V            |

<sup>1</sup> Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

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**ESD HANDLING:** Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.

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**Table 3. SKY53728-11 General Electrical Specifications****(V<sub>DD</sub> = 1.2 V, V<sub>IO</sub> = 1.8 V, T<sub>OP</sub> = +25 °C, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)**

| Specification                                  | Test Conditions                                    | Min  | Typ | Max   | Units |
|------------------------------------------------|----------------------------------------------------|------|-----|-------|-------|
| Normal operating case temperature              | Normal                                             |      | 25  |       | °C    |
| Extreme operating case temperature             | Extreme                                            | -30  |     | 85    | °C    |
| 1.2 V normal supply voltage (VDD)              | Normal                                             | 1.15 | 1.2 | 1.25  | V     |
| 1.8 V normal supply voltage (VDD)              | Normal                                             | 1.7  | 1.8 | 1.9   | V     |
| Extreme supply voltage (VDD)                   | Extreme                                            | 1.15 | 1.8 | 1.9   | V     |
| Normal supply voltage (VIO)                    | Normal                                             | 1.7  | 1.8 | 1.95  | V     |
| Extreme supply voltage (VIO)                   | Extreme                                            | 1.7  | 1.8 | 1.95  | V     |
| Insertion loss, TRX - ANT                      | 3300 MHz to 5000 MHz                               |      | 1.3 | 2.1   | dB    |
| Insertion loss for B41, TRX – ANT <sup>1</sup> | 2496 MHz to 2690 MHz                               |      | 2   | 3.0   | dB    |
| Insertion loss, 5G_RX_OUT1 - SRS_BYP           | 2496 MHz to 2690 MHz, 3300 MHz to 5000 MHz         |      | 0.8 | 1.7   | dB    |
| 2nd harmonic <sup>2</sup>                      | P <sub>IN</sub> = 26 dBm, CW                       |      | -70 | -40   | dBm   |
| 3rd harmonic <sup>2</sup>                      | P <sub>IN</sub> = 26 dBm, CW                       |      | -70 | -40   | dBm   |
| NR RF input power <sup>2</sup>                 | DFT-S-OFDM QPSK inner full RB, SCS = 30 kHz (MPRO) |      |     | +29.5 | dBm   |
| LTE RF input power <sup>2</sup>                | QPSK 10 MHz 12 RB (MPRO)                           |      |     | +29.5 | dBm   |

<sup>1</sup> With external matching: 1.1 dB.<sup>2</sup> TRX - ANT, 5G\_RX\_OUT1 - SRS\_BYP.

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name      | Data Bits | Bit Name              | Default        | Description           | Value     | State                 | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W      | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|--------------------|-----------|-----------------------|----------------|-----------------------|-----------|-----------------------|-----------------------------------------------|-----------------|----------------|----------------------|----------|---------------|---------------|
| UDR            | 0                       | 0x00                    | n77/n78 LNA Enable | 7:2       | Reserved              | 000000         | Reserved              |           |                       | No                                            | No              | NA             | Yes                  | R/W      | No            | Static        |
|                |                         |                         |                    | 1         | n77/n78 Band Select   | 0              | n77/n78 Band Select   | 0         | 0 n77                 |                                               |                 |                |                      | R/W      |               |               |
|                |                         |                         |                    |           |                       |                |                       | 1         | 1 n78                 |                                               |                 |                |                      |          |               |               |
|                |                         |                         |                    | 0         | n77/n78 LNA Enable    | 0              | n77/n78 LNA Enable    | 0         | 0 LNA Disable         |                                               |                 |                |                      | R/W      |               |               |
|                |                         |                         |                    |           |                       |                |                       | 1         | 1 LNA Enable          |                                               |                 |                |                      |          |               |               |
|                |                         |                         |                    | 1         | 0x01                  | n79 LNA Enable | 7:1                   | Reserved  | 0000000               |                                               |                 |                |                      | Reserved |               |               |
|                | 0                       | n79 LNA Enable          | 0                  |           |                       |                | n79 LNA Enable        | 0         | 0 n79 LNA Disable     | R/W                                           |                 |                |                      |          |               |               |
|                |                         |                         |                    |           |                       |                |                       | 1         | 1 n79 LNA Enable      |                                               |                 |                |                      |          |               |               |
|                | 2                       | 0x02                    | RX_OUT1            | 7:3       | Reserved              | 00000          | Reserved              |           |                       | No                                            | Standard        | Trigger 1      | Yes                  | R/W      | Yes           | Static        |
|                |                         |                         |                    | 2:0       | Selects Output of RX1 | 000            | Selects output of RX1 | 000       | 000 Isolation         |                                               |                 |                |                      | R/W      |               |               |
|                |                         |                         |                    |           |                       |                |                       | 001       | 001 n77/n78 LNA       |                                               |                 |                |                      |          |               |               |
|                |                         |                         |                    |           |                       |                |                       | 010       | 010 n79 LNA           |                                               |                 |                |                      |          |               |               |
|                |                         |                         |                    |           |                       |                |                       | 011       | 011 SRSBYP to RX_OUT1 |                                               |                 |                |                      |          |               |               |
|                |                         |                         |                    |           |                       |                |                       | 100 - 111 | 100 - 111 Reserved    |                                               |                 |                |                      |          |               |               |
|                |                         |                         |                    |           |                       |                |                       |           |                       |                                               |                 |                |                      |          |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| UDR            |                         |                         |               |           |                      |         |                       |           |                    |                                               |                 |                |                      |     |               |               |  |
|----------------|-------------------------|-------------------------|---------------|-----------|----------------------|---------|-----------------------|-----------|--------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|--|
| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name             | Default | Description           | Value     | State              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |  |
|                | 3                       | 0x03                    | RX_OUT2       | 7:3       | Reserved             | 00000   | Reserved              |           |                    | No                                            | Standard        | Trigger 1      | Yes                  | R/W | Yes           | Static        |  |
|                |                         |                         |               | 2:0       | Select Output of RX2 | 000     | Selects output of RX2 | 000       | 000 Isolation      |                                               |                 |                |                      | R/W |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 001       | 001 n77/n78 LNA    |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 010       | 010 n79 LNA        |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 011 - 111 | 011 - 111 Reserved |                                               |                 |                |                      |     |               |               |  |
|                | 4                       | 0x04                    | ANT_1_CONTROL | 7:3       | Reserved             | 00000   | Reserved              |           |                    | No                                            | Standard        | Trigger 2      | Yes                  | R/W | Yes           | Static        |  |
|                |                         |                         |               | 2:0       | ANT1 SELECT          | 000     | ANT1 SELECT           | 000       | 000:TERM           |                                               |                 |                |                      | R/W |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 001       | 001:n77/n78 LNA    |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 010       | 010:n79 LNA        |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 011       | 011:TRX1           |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 100       | 100:TRX2           |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 101 - 111 | 101 - 111 High Iso |                                               |                 |                |                      |     |               |               |  |
|                | 5                       | 0x05                    | ANT_2_CONTROL | 7:3       | Reserved             | 00000   | Reserved              |           |                    | No                                            | Standard        | Trigger 2      | Yes                  | R/W | Yes           | Static        |  |
|                |                         |                         |               | 2:0       | ANT2 SELECT          | 000     | ANT2 SELECT           | 000       | 000:TERM           |                                               |                 |                |                      | R/W |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 001       | 001:n77/n78 LNA    |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 010       | 010:n79 LNA        |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 011       | 011:TRX1           |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 100       | 100:TRX2           |                                               |                 |                |                      |     |               |               |  |
|                |                         |                         |               |           |                      |         |                       | 101 - 111 | 101 - 111 High Iso |                                               |                 |                |                      |     |               |               |  |

Table 4. SKY53728-11 5G DRx Controller Register Map

| Register Class | Register Address (Dec.)  | Register Address (Hex.) | Register Name         | Data Bits | Bit Name                   | Default | Description                                                                             | Value | State                                            | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|--------------------------|-------------------------|-----------------------|-----------|----------------------------|---------|-----------------------------------------------------------------------------------------|-------|--------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| UDR            | 6                        | 0x06                    | n77/n78 LNA Gain/Bias | 7         | Reserved                   | 0       | Reserved                                                                                |       |                                                  | No                                            | Extended        | UDR_SET_A      | Yes                  | R/W | Yes           | Dynamic       |
|                |                          |                         |                       | 6         | n77/n78 LNA Enable         | 0       | n77/n78 LNA Enable                                                                      | 0     | 0: n77/n78 LNA Disable                           |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 1     | 1: n77/n78 LNA Enable                            |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       | 5:3       | n77/n78 Gain (Mode1/Mode0) | 000     | n77/n78 Gain (Mode1/Mode0)<br>Gain setting options selected in bit [0] of Register 0x08 | 000   | 000 G7 (Max Gain/Max Gain)                       |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 001   | 001 G6 (Max Gain -2 dB/ Max Gain -3 dB)          |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 010   | 010 G5 (Max Gain -8 dB/ Max Gain -6 dB)          |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 011   | 011 G4 (Max Gain -14 dB/ Max Gain -9 dB)         |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 100   | 100 G3 (Max Gain -20 dB/ Max Gain -12 dB)        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 101   | 101 G2 (Max Gain -26 dB/ Max Gain -15 dB)        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 110   | 110 G1 (Max Gain -32 dB/ Max Gain -24 dB active) |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 111   | 111 G0 (NA/Max Gain -24 dB passive)              |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       | 2:0       | n77/n78 Bias               | 000     | n77/n78 Bias                                                                            | 000   | 000 bias0 (lowest bias)                          |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 001   | 001 bias1                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 010   | 010 bias2                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 011   | 011 bias3                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 100   | 100 bias4                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 101   | 101 bias5                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                       |           |                            |         |                                                                                         | 110   | 110 bias6                                        |                                               |                 |                |                      |     |               |               |
| 111            | 111 bias7 (highest bias) |                         |                       |           |                            |         |                                                                                         |       |                                                  |                                               |                 |                |                      |     |               |               |

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| Register Class | Register Address (Dec.)  | Register Address (Hex.) | Register Name     | Data Bits | Bit Name               | Default | Description                                                                         | Value | State                                            | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|--------------------------|-------------------------|-------------------|-----------|------------------------|---------|-------------------------------------------------------------------------------------|-------|--------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| UDR            | 7                        | 0x07                    | n79 LNA Gain/Bias | 7         | Reserved               | 0       | Reserved                                                                            |       |                                                  | No                                            | Extended        | UDR_SET_B      | Yes                  | R/W | Yes           | Dynamic       |
|                |                          |                         |                   | 6         | n79 LNA Enable         | 0       | n79 LNA Enable                                                                      | 0     | 0: n79 LNA Disable                               |                                               |                 |                |                      | R/W |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 1     | 1: n79 LNA Enable                                |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   | 5:3       | n79 Gain (Mode1/Mode0) | 000     | n79 Gain (Mode1/Mode0)<br>Gain setting options selected in bit [0] of Register 0x08 | 000   | 000 G7 (Max Gain/Max Gain)                       |                                               |                 |                |                      | R/W |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 001   | 001 G6 (Max Gain -2 dB/ Max Gain -3 dB)          |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 010   | 010 G5 (Max Gain -8 dB/ Max Gain -6 dB)          |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 011   | 011 G4 (Max Gain -14 dB/ Max Gain -9 dB)         |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 100   | 100 G3 (Max Gain -20 dB/ Max Gain -12 dB)        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 101   | 101 G2 (Max Gain -26 dB/ Max Gain -15 dB)        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 110   | 110 G1 (Max Gain -32 dB/ Max Gain -24 dB active) |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 111   | 111 G0 (NA/Max Gain -24 dB passive)              |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   | 2:0       | n79 Bias               | 000     | n79 Bias                                                                            | 000   | 000 bias0 (lowest bias)                          |                                               |                 |                |                      | R/W |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 001   | 001 bias1                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 010   | 010 bias2                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 011   | 011 bias3                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 100   | 100 bias4                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 101   | 101 bias5                                        |                                               |                 |                |                      |     |               |               |
|                |                          |                         |                   |           |                        |         |                                                                                     | 110   | 110 bias6                                        |                                               |                 |                |                      |     |               |               |
| 111            | 111 bias7 (highest bias) |                         |                   |           |                        |         |                                                                                     |       |                                                  |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name       | Data Bits | Bit Name          | Default  | Description                  | Value | State                                         | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------------|-----------|-------------------|----------|------------------------------|-------|-----------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| UDR            | 8                       | 0x08                    | Gain Mode           | 7:1       | Reserved          | 00000000 | Reserved                     |       |                                               | No                                            | No              | NA             | Yes                  | R/W | No            | Static        |
|                |                         |                         |                     | 0         | Gain Mode Select  | 0        | Gain Mode Select             |       | 0 = Mode0 gain table;<br>1 = Mode1 gain table |                                               |                 |                |                      | R/W |               |               |
|                | 9                       | 0x09                    | UDR_SET_B/A Control | 7:4       | UDR_SET_B Trigger | 0000     | Configurable Trigger Control |       | cTrig B Define                                | No                                            | No              | NA             | Yes                  | R/W | No            | Static        |
|                |                         |                         |                     | 3:0       | UDR_SET_A Trigger | 0000     | Configurable Trigger Control |       | cTrig A Define                                |                                               |                 |                |                      | R/W |               |               |

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| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name                      | Default | Description                                                                                                                                                                             | Value | State                                | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|-------------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 28                      | 0x1C                    | PM_TRIG       | 7         | PWR_MODE[1], Operation Mode   | 1       | Defines Normal Operation and Secondary Operation Modes. When the slave is in Secondary Operation Mode, charge pumps shall be disabled and the slave shall be listening to the RFFE bus. | 0     | Normal Operation Mode (ACTIVE)       | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |                               |         |                                                                                                                                                                                         | 1     | Secondary Operation Mode (LOW POWER) |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               | 6         | PWR_MODE[0], State Bit Vector | 0       | Single bit Powered Reset. Writing a 1 resets all slave registers to their default settings including the Operation Mode bit in PWR_MODE[1]. Always reads back 0.                        | 0     | No action (ACTIVE)                   |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                               |         |                                                                                                                                                                                         | 1     | Powered Reset                        |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name       | Default | Description    | Value | State                                                                                                       | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|----------------|---------|----------------|-------|-------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 28                      | 0x1C                    | PM_TRIG       | 5         | TRIGGER_MASK_2 | 0       | Trigger Mask 2 | 0     | Data writes to registers tied to TRIGGER_2 is held in shadow registers until the TRIGGER_2 bit is set to 1. | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |                |         |                | 1     | Data writes to registers tied to TRIGGER_2 go directly to the active registers.                             |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               | 4         | TRIGGER_MASK_1 | 0       | Trigger Mask 1 | 0     | Data writes to registers tied to TRIGGER_1 is held in shadow registers until the TRIGGER_1 bit is set to 1. |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |         |                | 1     | Data writes to registers tied to TRIGGER_1 go directly to the active registers.                             |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               | 3         | TRIGGER_MASK_0 | 0       | Trigger Mask 0 | 0     | Data writes to registers tied to TRIGGER_0 is held in shadow registers until the TRIGGER_0 bit is set to 1. |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |         |                | 1     | Data writes to registers tied to TRIGGER_0 go directly to the active registers.                             |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name  | Default | Description                                                                                                                                                                                                                | Value | State                                                                                          | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|-----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 28                      | 0x1C                    | PM_TRIG       | 2         | TRIGGER_2 | 0       | Trigger 2. This bit has no effect if TRIGGER_MASK_2 is 1. When the part is in LOW POWER and a trigger request is sent in the same command sequence that still keeps the part in LOW POWER, the trigger request is ignored. | 0     | No action. Data is held in shadow registers.                                                   | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |           |         | This applies to Triggers only, not to Trigger Masks. When the part is in ACTIVE and sent to LOW POWER, or when the part is in LOW POWER and sent to ACTIVE, trigger requests in the same command sequence are NOT ignored. | 1     | Data is transferred from shadow registers to active registers for registers tied to TRIGGER_2. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name  | Default | Description                                                                                                                                                                                                                | Value | State                                                                                          | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|-----------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 28                      | 0x1C                    | PM_TRIG       | 1         | TRIGGER_1 | 0       | Trigger 1. This bit has no effect if TRIGGER_MASK_1 is 1. When the part is in LOW POWER and a trigger request is sent in the same command sequence that still keeps the part in LOW POWER, the trigger request is ignored. | 0     | No action. Data is held in shadow registers.                                                   | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |           |         | This applies to Triggers only, not to Trigger Masks. When the part is in ACTIVE and sent to LOW POWER, or when the part is in LOW POWER and sent to ACTIVE, trigger requests in the same command sequence are NOT ignored. | 1     | Data is transferred from shadow registers to active registers for registers tied to TRIGGER_1. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name        | Default   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Value | State                                                                                          | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|-----------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 28                      | 0x1C                    | PM_TRIG       | 0         | TRIGGER_0       | 0         | <p>Trigger 0. This bit has no effect if TRIGGER_MASK_0 is 1. When the part is in LOW POWER and a trigger request is sent in the same command sequence that still keeps the part in LOW POWER, the trigger request is ignored.</p> <p>This applies to Triggers only, not to Trigger Masks. When the part is in ACTIVE and sent to LOW POWER, or when the part is in LOW POWER and sent to ACTIVE, trigger requests in the same command sequence are NOT ignored.</p> | 0     | No action. Data is held in shadow registers.                                                   | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |                 |           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1     | Data is transferred from shadow registers to active registers for registers tied to TRIGGER_0. |                                               |                 |                |                      |     |               |               |
|                | 29                      | 0x1D                    | PRODUCT_ID    | 7:0       | PRODUCT_ID[7:0] | 1010 0110 | This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.                                                                                                                                                                                                                                                                                  | 0xA6  |                                                                                                | No                                            | No              | No             | No                   | R   | No            | NA            |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name   | Data Bits | Bit Name              | Default      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           | Value | State | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W  | Change Detect | Register Type |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
|----------------|-------------------------|-------------------------|-----------------|-----------|-----------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-----------------------------------------------|-----------------|----------------|----------------------|------|---------------|---------------|---|---|------|---|---|------|---|---|------|---|---|------|-----|--|-----|
| RFFE Reserved  | 30                      | 0x1E                    | MANUFACTURER_ID | 7:0       | MANUFACTURER_ID[7:0]  | 1010<br>0101 | Manufacturer ID. This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. See <a href="http://mid.mipi.org">http://mid.mipi.org</a> .                                                                                                                                                                                      | 0xA5  |       | No                                            | No              | No             | No                   | R    | No            | NA            |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
|                | 31                      | 0x1F                    | MAIN_USID       | 7:4       | MANUFACTURER_ID[11:8] | 0001         | Manufacturer ID. These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. See <a href="http://mid.mipi.org">http://mid.mipi.org</a> .                                                                                                                                                                                           | 0x1   |       | No                                            | No              | No             | No                   | R    | No            | NA            |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
|                |                         |                         |                 | 3:0       | USID[3:0]             | 0111         | These bits store the USID of the device. Performing a write to this register using the described programming sequences will re-program the USID. The default value shall not be fused.<br><br>USID DECODING:<br><table><tr><th>ID1</th><th>ID0</th><th>USID</th></tr><tr><td>0</td><td>0</td><td>0111</td></tr><tr><td>0</td><td>1</td><td>1000</td></tr><tr><td>1</td><td>0</td><td>1001</td></tr><tr><td>1</td><td>1</td><td>1010</td></tr></table> | ID1   | ID0   |                                               |                 |                |                      | USID |               |               | 0 | 0 | 0111 | 0 | 1 | 1000 | 1 | 0 | 1001 | 1 | 1 | 1010 | 0x7 |  | R/W |
|                |                         |                         |                 | ID1       | ID0                   | USID         |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |       |                                               |                 |                |                      |      |               |               |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
| 0              | 0                       | 0111                    |                 |           |                       |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |       |                                               |                 |                |                      |      |               |               |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
| 0              | 1                       | 1000                    |                 |           |                       |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |       |                                               |                 |                |                      |      |               |               |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
| 1              | 0                       | 1001                    |                 |           |                       |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |       |                                               |                 |                |                      |      |               |               |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
| 1              | 1                       | 1010                    |                 |           |                       |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |       |                                               |                 |                |                      |      |               |               |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |
|                |                         |                         |                 |           |                       |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |       |                                               |                 |                |                      |      |               |               |   |   |      |   |   |      |   |   |      |   |   |      |     |  |     |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name  | Data Bits | Bit Name            | Default      | Description                                                                                                                                                                                                                  | Value | State | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|----------------|-----------|---------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 32                      | 0x20                    | EXT_PRODUCT_ID | 7:0       | EXT_PRODUCT_ID[7:0] | 0000<br>0110 | Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value. | 0x06  |       | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                | 33                      | 0x21                    | REV_ID         | 7:0       | REV_ID              | 0000<br>0000 |                                                                                                                                                                                                                              | 0x00  |       | No                                            | No              | No             | No                   | R   | No            | NA            |
|                | 34                      | 0x22                    | GROUP_SID      | 7:4       | GSID0[3:0]          | 0000         | Primary Group Slave ID.                                                                                                                                                                                                      |       |       | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |                | 3:0       | GSID1[3:0]          | 0000         | Secondary Group Slave ID.                                                                                                                                                                                                    |       |       |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name                 | Default  | Description                                                                                                                                               | Value | State            | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|--------------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-------|------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 35                      | 0x23                    | UDR_RST       | 7         | UDR_RST                  | 0        | Reset all configurable non-RFFE Reserved registers to default values. The UDR_RST bit shall revert to default value of 0 after software reset is enabled. | 0     | Normal Operation | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |                          |          |                                                                                                                                                           | 1     | Software Reset   |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               | 6:0       | RESERVED                 | 000 0000 | Reserved for future use. Set to all 0.                                                                                                                    |       |                  |                                               |                 |                |                      |     |               |               |
|                | 36                      | 0x24                    | ERR_SUM       | 7         | RESERVED                 | 0        | Reserved for future error codes. The ERR_SUM register reports error codes until read. The ERR_SUM register shall reset after it is read.                  |       |                  | No                                            | No              | No             | No                   | R   | No            | NA            |
|                |                         |                         |               | 6         | COMMAND_FRAME_PARITY_ERR | 0        | Command Sequence received with parity error – discard command. The ERR_SUM register shall reset after it is read.                                         |       |                  |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name                 | Default | Description                                                                             | Value | State | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|--------------------------|---------|-----------------------------------------------------------------------------------------|-------|-------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 36                      | 0x24                    | ERR_SUM       | 5         | COMMAND_LENGTH_ERR       | 0       | Command length error. The ERR_SUM register shall reset after it is read.                |       |       | No                                            | No              | No             | No                   | R   | No            | NA            |
|                |                         |                         |               | 4         | ADDRESS_FRAME_PARITY_ERR | 0       | Address frame with parity error. The ERR_SUM register shall reset after it is read.     |       |       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               | 3         | DATA_FRAME_PARITY_ERR    | 0       | Data frame with parity error. The ERR_SUM register shall reset after it is read.        |       |       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               | 2         | READ_UNUSED_REG          | 0       | Read command to an invalid address. The ERR_SUM register shall reset after it is read.  |       |       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               | 1         | WRITE_UNUSED_REG         | 0       | Write command to an invalid address. The ERR_SUM register shall reset after it is read. |       |       |                                               |                 |                |                      |     |               |               |

Table 4. SKY53728-11 5G DRx Controller Register Map

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name       | Default   | Description                                                                                      | Value | State                                                        | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|----------------|-----------|--------------------------------------------------------------------------------------------------|-------|--------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 36                      | 0x24                    | ERR_SUM       | 0         | BID_GID_ERR    | 0         | Read command with a BROADCAST_ID or GROUP_ID. The ERR_SUM register shall reset after it is read. |       |                                                              |                                               |                 |                |                      |     |               |               |
|                | 43                      | 0x2B                    | BUS_LD        | 7:4       | RESERVED       | 0000      | Reserved for future use. Set to all 0.                                                           |       |                                                              | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               | 3:0       | BUS_LD[3:0]    | 0100      | RFFE drive strength select. Programs the drive strength of the SDATA driver in readback modes.   | 0x0   | 10 pF                                                        |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x1   | 20 pF                                                        |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x2   | 30 pF                                                        |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x3   | 40 pF                                                        |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x4   | 50 pF                                                        |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x5   | 60 pF                                                        |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x6   | 80 pF                                                        |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x7   | 100 pF                                                       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x8   | 120 pF                                                       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0x9   | 140 pF                                                       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0xA   | 160 pF                                                       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0xB   | 180 pF                                                       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0xC   | 200 pF                                                       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0xD   | 250 pF                                                       |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0xE   | Reserved for future drive strength based on 300 pF bus load. |                                               |                 |                |                      |     |               |               |
|                |                         |                         |               |           |                |           |                                                                                                  | 0xF   | Reserved for future drive strength based on 350 pF bus load. |                                               |                 |                |                      |     |               |               |
|                | 44                      | 0x2C                    | TEST_PATT     | 7:0       | TEST_PATT[7:0] | 1101 0010 | A read to this register address will trigger the slave to transmit a fixed test pattern of 0xD2. |       |                                                              | No                                            | No              | No             | No                   | R   | No            | NA            |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name    | Data Bits | Bit Name            | Default | Description         | Value | State                                                                                                                                                                                                                                                        | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|------------------|-----------|---------------------|---------|---------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 45                      | 0x2D                    | EXT_TRIGGER_MASK | 7         | EXT_TRIGGER_MASK_10 | 0       | Ext Trigger Mask 10 | 0     | Extended Trigger Mask 10 is de-asserted (via a logic '0'), then Extended Trigger 10 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 10 is asserted. | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |                  |           |                     |         |                     | 1     | Extended Trigger 10 is disabled, or masked - in that case data written to a register associated with Extended Trigger 10 goes directly to the destination register                                                                                           |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  | 6         | EXT_TRIGGER_MASK_9  | 0       | Ext Trigger Mask 9  | 0     | Extended Trigger Mask 9 is de-asserted (via a logic '0'), then Extended Trigger 9 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 9 is asserted.    |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  |           |                     |         |                     | 1     | Extended Trigger 9 is disabled, or masked - in that case data written to a register associated with Extended Trigger 9 goes directly to the destination register                                                                                             |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name    | Data Bits | Bit Name           | Default | Description        | Value | State                                                                                                                                                                                                                                                     | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|------------------|-----------|--------------------|---------|--------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 45                      | 0x2D                    | EXT_TRIGGER_MASK | 5         | EXT_TRIGGER_MASK_8 | 0       | Ext Trigger Mask 8 | 0     | Extended Trigger Mask 8 is de-asserted (via a logic '0'), then Extended Trigger 8 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 8 is asserted. | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |                  |           |                    |         |                    | 1     | Extended Trigger 8 is disabled, or masked - in that case data written to a register associated with Extended Trigger 8 goes directly to the destination register                                                                                          |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  | 4         | EXT_TRIGGER_MASK_7 | 0       | Ext Trigger Mask 7 | 0     | Extended Trigger Mask 7 is de-asserted (via a logic '0'), then Extended Trigger 7 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 7 is asserted. |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  |           |                    |         |                    | 1     | Extended Trigger 7 is disabled, or masked - in that case data written to a register associated with Extended Trigger 7 goes directly to the destination register                                                                                          |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name    | Data Bits | Bit Name           | Default | Description        | Value | State                                                                                                                                                                                                                                                     | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|------------------|-----------|--------------------|---------|--------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 45                      | 0x2D                    | EXT_TRIGGER_MASK | 3         | EXT_TRIGGER_MASK_6 | 0       | Ext Trigger Mask 6 | 0     | Extended Trigger Mask 6 is de-asserted (via a logic '0'), then Extended Trigger 6 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 6 is asserted. | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |                  |           |                    |         |                    | 1     | Extended Trigger 6 is disabled, or masked - in that case data written to a register associated with Extended Trigger 6 goes directly to the destination register                                                                                          |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  | 2         | EXT_TRIGGER_MASK_5 | 0       | Ext Trigger Mask 5 | 0     | Extended Trigger Mask 5 is de-asserted (via a logic '0'), then Extended Trigger 5 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 5 is asserted. |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  |           |                    |         |                    | 1     | Extended Trigger 5 is disabled, or masked - in that case data written to a register associated with Extended Trigger 5 goes directly to the destination register                                                                                          |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name    | Data Bits | Bit Name           | Default | Description        | Value | State                                                                                                                                                                                                                                                     | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|------------------|-----------|--------------------|---------|--------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 45                      | 0x2D                    | EXT_TRIGGER_MASK | 1         | EXT_TRIGGER_MASK_4 | 0       | Ext Trigger Mask 4 | 0     | Extended Trigger Mask 4 is de-asserted (via a logic '0'), then Extended Trigger 4 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 4 is asserted. | No                                            | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |                  |           |                    |         |                    | 1     | Extended Trigger 4 is disabled, or masked - in that case data written to a register associated with Extended Trigger 4 goes directly to the destination register                                                                                          |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  | 0         | EXT_TRIGGER_MASK_3 | 0       | Ext Trigger Mask 3 | 0     | Extended Trigger Mask 3 is de-asserted (via a logic '0'), then Extended Trigger 3 is enabled, or unmasked, and incoming data is written to the shadow register only, and the destination register remains unchanged until Extended Trigger 3 is asserted. |                                               |                 |                |                      |     |               |               |
|                |                         |                         |                  |           |                    |         |                    | 1     | Extended Trigger 3 is disabled, or masked - in that case data written to a register associated with Extended Trigger 3 goes directly to the destination register                                                                                          |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name       | Default | Description    | Value | State                                                                                                                                                                                                                                                                                                                                                                                                                  | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|----------------|---------|----------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER   | 7         | EXT_TRIGGER_10 | 0       | Ext Trigger 10 | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                      | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |                |         |                | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 10 and loads the destination registers associated with Extended Trigger 10 with the data in the parallel shadow register, provided that Extended Trigger Mask 10 is de-asserted (logic '0'), i.e. that Extended Trigger 10 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name      | Default | Description   | Value | State                                                                                                                                                                                                                                                                                                                                                                                                              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|---------------|---------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER   | 6         | EXT_TRIGGER_9 | 0       | Ext Trigger 9 | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                  | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |               |         |               | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 9 and loads the destination registers associated with Extended Trigger 9 with the data in the parallel shadow register, provided that Extended Trigger Mask 9 is de-asserted (logic '0'), i.e. that Extended Trigger 9 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name      | Default | Description   | Value | State                                                                                                                                                                                                                                                                                                                                                                                                              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|---------------|---------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER   | 5         | EXT_TRIGGER_8 | 0       | Ext Trigger 8 | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                  | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |               |         |               | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 8 and loads the destination registers associated with Extended Trigger 8 with the data in the parallel shadow register, provided that Extended Trigger Mask 8 is de-asserted (logic '0'), i.e. that Extended Trigger 8 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name      | Default | Description   | Value | State                                                                                                                                                                                                                                                                                                                                                                                                              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|---------------|---------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER   | 4         | EXT_TRIGGER_7 | 0       | Ext Trigger 7 | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                  | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |               |         |               | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 7 and loads the destination registers associated with Extended Trigger 7 with the data in the parallel shadow register, provided that Extended Trigger Mask 7 is de-asserted (logic '0'), i.e. that Extended Trigger 7 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name      | Default | Description   | Value | State                                                                                                                                                                                                                                                                                                                                                                                                              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|---------------|---------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER   | 3         | EXT_TRIGGER_6 | 0       | Ext Trigger 6 | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                  | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |               |         |               | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 6 and loads the destination registers associated with Extended Trigger 6 with the data in the parallel shadow register, provided that Extended Trigger Mask 6 is de-asserted (logic '0'), i.e. that Extended Trigger 6 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name      | Default | Description   | Value | State                                                                                                                                                                                                                                                                                                                                                                                                              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|---------------|---------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER   | 2         | EXT_TRIGGER_5 | 0       | Ext Trigger 5 | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                  | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |               |         |               | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 5 and loads the destination registers associated with Extended Trigger 5 with the data in the parallel shadow register, provided that Extended Trigger Mask 5 is de-asserted (logic '0'), i.e. that Extended Trigger 5 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name | Data Bits | Bit Name      | Default | Description   | Value | State                                                                                                                                                                                                                                                                                                                                                                                                              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|---------------|-----------|---------------|---------|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER   | 1         | EXT_TRIGGER_4 | 0       | Ext Trigger 4 | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                  | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |               |           |               |         |               | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 4 and loads the destination registers associated with Extended Trigger 4 with the data in the parallel shadow register, provided that Extended Trigger Mask 4 is de-asserted (logic '0'), i.e. that Extended Trigger 4 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name  | Data Bits           | Bit Name            | Default                                                                                                                                                            | Description                                                                                                                                                        | Value | State                                                                                                                                                                                                                                                                                                                                                                                                              | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|----------------|---------------------|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 46                      | 0x2E                    | EXT_TRIGGER    | 0                   | EXT_TRIGGER_3       | 0                                                                                                                                                                  | Ext Trigger 3                                                                                                                                                      | 0     | No effect on the destination register contents, data is held in shadow registers.                                                                                                                                                                                                                                                                                                                                  | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                |                         |                         |                |                     |                     |                                                                                                                                                                    |                                                                                                                                                                    | 1     | Setting this bit to a logic '1' level 'fires' Extended Trigger 3 and loads the destination registers associated with Extended Trigger 3 with the data in the parallel shadow register, provided that Extended Trigger Mask 3 is de-asserted (logic '0'), i.e. that Extended Trigger 3 is enabled, or unmasked.<br><br>When the part is in LOW POWER and the trigger is fired the trigger is ignored and not fired. |                                               |                 |                |                      |     |               |               |
|                | 56                      | 0x38                    | EXT_TRIG_CNT_3 | 7:0                 | EXT_TRIG_CNT_3[8:1] | 0000<br>0000                                                                                                                                                       | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |       |                                                                                                                                                                                                                                                                                                                                                                                                                    | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
| 57             | 0x39                    | EXT_TRIG_CNT_4          | 7:0            | EXT_TRIG_CNT_4[8:1] | 0000<br>0000        | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |                                                                                                                                                                    |       |                                                                                                                                                                                                                                                                                                                                                                                                                    | Yes                                           | No              | No             | No                   | R/W | No            | NA            |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name  | Data Bits | Bit Name            | Default      | Description                                                                                                                                                        | Value | State | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|----------------|-----------|---------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 58                      | 0x3A                    | EXT_TRIG_CNT_5 | 7:0       | EXT_TRIG_CNT_5[8:1] | 0000<br>0000 | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |       |       | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                | 59                      | 0x3B                    | EXT_TRIG_CNT_6 | 7:0       | EXT_TRIG_CNT_6[8:1] | 0000<br>0000 | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |       |       | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                | 60                      | 0x3C                    | EXT_TRIG_CNT_7 | 7:0       | EXT_TRIG_CNT_7[8:1] | 0000<br>0000 | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |       |       | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                | 61                      | 0x3D                    | EXT_TRIG_CNT_8 | 7:0       | EXT_TRIG_CNT_8[8:1] | 0000<br>0000 | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |       |       | Yes                                           | No              | No             | No                   | R/W | No            | NA            |

**Table 4. SKY53728-11 5G DRx Controller Register Map**

| Register Class | Register Address (Dec.) | Register Address (Hex.) | Register Name   | Data Bits | Bit Name             | Default      | Description                                                                                                                                                        | Value | State | Broadcast Slave ID and Group Slave ID Support | Trigger Support | Active Trigger | Masked Write Support | R/W | Change Detect | Register Type |
|----------------|-------------------------|-------------------------|-----------------|-----------|----------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-----------------------------------------------|-----------------|----------------|----------------------|-----|---------------|---------------|
| RFFE Reserved  | 62                      | 0x3E                    | EXT_TRIG_CNT_9  | 7:0       | EXT_TRIG_CNT_9[8:1]  | 0000<br>0000 | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |       |       | Yes                                           | No              | No             | No                   | R/W | No            | NA            |
|                | 63                      | 0x3F                    | EXT_TRIG_CNT_10 | 7:0       | EXT_TRIG_CNT_10[8:1] | 0000<br>0000 | Counter register's most significant 8 bits for a 9 bit counter, the least significant bit of the counter shall be set to 0b0 whenever this register is written to. |       |       | Yes                                           | No              | No             | No                   | R/W | No            | NA            |

**Table 5. SKY53728-11 n77, n78, B42, B43, B48 RF Performance (1 of 2)**

(V<sub>DD</sub> = 1.2 V, V<sub>IO</sub> = 1.8 V, T<sub>OP</sub> = +25 °C, f = 3750 MHz, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)

| Parameter           |     | Symbol         | Conditions                                                                        | Mode 0 |       |      | Mode 1 |       |       | Units |
|---------------------|-----|----------------|-----------------------------------------------------------------------------------|--------|-------|------|--------|-------|-------|-------|
|                     |     |                |                                                                                   | Min    | Typ   | Max  | Min    | Typ   | Max   |       |
| Operating Frequency | n77 | f <sub>o</sub> |                                                                                   | 3300   |       | 4200 | 3300   |       | 4200  | MHz   |
|                     | n78 |                |                                                                                   | 3300   |       | 3800 | 3300   |       | 3800  | MHz   |
|                     | B42 |                |                                                                                   | 3400   |       | 3600 | 3400   |       | 3600  | MHz   |
|                     | B43 |                |                                                                                   | 3600   |       | 3800 | 3600   |       | 3800  | MHz   |
|                     | B48 |                |                                                                                   | 3550   |       | 3700 | 3550   |       | 3700  | MHz   |
| LNA Current         | G7  | IDD            | NTC                                                                               |        | 8.4   | 13.0 |        | 6.5   | 9.0   | mA    |
|                     | G6  |                |                                                                                   |        | 6.8   | 10.0 |        | 4.2   | 6.0   |       |
|                     | G5  |                |                                                                                   |        | 7.7   | 12.0 |        | 8.1   | 11.5  |       |
|                     | G4  |                |                                                                                   |        | 2.9   | 5.0  |        | 3.5   | 5.0   |       |
|                     | G3  |                |                                                                                   |        | 3.8   | 5.5  |        | 1.5   | 2.4   |       |
|                     | G2  |                |                                                                                   |        | 4.2   | 6.0  |        | 1.7   | 3.0   |       |
|                     | G1  |                |                                                                                   |        | 2.8   | 4.5  |        | 1.7   | 4.0   |       |
| In-Band Gain        | G7  | G <sub>n</sub> | NTC                                                                               | 14.5   | 16.7  | 20.5 | 15.5   | 16.5  | 19.5  | dB    |
|                     | G6  |                |                                                                                   | 12.5   | 14.2  | 17.5 | 13.0   | 14.9  | 17.5  |       |
|                     | G5  |                |                                                                                   | 9.5    | 11.0  | 14.5 | 7.0    | 8.3   | 11.0  |       |
|                     | G4  |                |                                                                                   | 6.0    | 7.6   | 11.0 | 1.5    | 1.6   | 5.5   |       |
|                     | G3  |                |                                                                                   | 3.0    | 4.7   | 8.0  | -6.5   | -4.1  | -0.5  |       |
|                     | G2  |                |                                                                                   | 0.0    | 1.9   | 5.0  | -12.0  | -9.9  | -6.5  |       |
|                     | G1  |                |                                                                                   | -9.0   | -6.8  | -4.0 | -17.0  | -15.2 | -11.5 |       |
| Noise Figure        | G7  | NF             | NTC                                                                               |        | 2.8   | 3.5  |        | 2.8   | 3.5   | dB    |
|                     | G6  |                |                                                                                   |        | 2.9   | 3.5  |        | 2.9   | 3.5   |       |
|                     | G5  |                |                                                                                   |        | 3.0   | 3.9  |        | 3.1   | 4.0   |       |
|                     | G4  |                |                                                                                   |        | 4.0   | 5.4  |        | 4.6   | 6.0   |       |
|                     | G3  |                |                                                                                   |        | 4.4   | 5.8  |        | 12.6  | 14.5  |       |
|                     | G2  |                |                                                                                   |        | 4.9   | 6.3  |        | 13.9  | 17.0  |       |
|                     | G1  |                |                                                                                   |        | 8.0   | 11.3 |        | 15.7  | 19.0  |       |
| In-Band Input P1dB  | G7  | P1dB           | NTC                                                                               | -20.8  | -20.2 |      | -20.5  | -19.3 |       | dBm   |
|                     | G6  |                |                                                                                   | -20.1  | -19.4 |      | -18.0  | -17.1 |       |       |
|                     | G5  |                |                                                                                   | -20.2  | -19.6 |      | -20.5  | -19.4 |       |       |
|                     | G4  |                |                                                                                   | -13.0  | -12.0 |      | -13.0  | -12.4 |       |       |
|                     | G3  |                |                                                                                   | -13.0  | -11.9 |      | -5.0   | -2.9  |       |       |
|                     | G2  |                |                                                                                   | -13.0  | -12.0 |      | -4.0   | -0.7  |       |       |
|                     | G1  |                |                                                                                   | -4.5   | -1.9  |      | -2.5   | 0.2   |       |       |
| In-Band IIP3        | G7  | IIP3           | NTC, f <sub>CW2</sub> = f <sub>CW1</sub> ±1MHz, Measured at 20 dB lower than P1dB | -8.9   | -7.5  |      | -9.2   | -7.4  |       | dBm   |
|                     | G6  |                |                                                                                   | -9.0   | -7.6  |      | -8.5   | -6.7  |       |       |
|                     | G5  |                |                                                                                   | -9.3   | -7.9  |      | -9.6   | -8.2  |       |       |
|                     | G4  |                |                                                                                   | -4.3   | -2.3  |      | -4.7   | -2.7  |       |       |
|                     | G3  |                |                                                                                   | -4.9   | -3.0  |      | 1.7    | 3.8   |       |       |
|                     | G2  |                |                                                                                   | -4.8   | -2.9  |      | 2.4    | 4.5   |       |       |
|                     | G1  |                |                                                                                   | 2.9    | 4.5   |      | 2.9    | 5.0   |       |       |

**Table 5. SKY53728-11 n77, n78, B42, B43, B48 RF Performance (2 of 2)****(V<sub>DD</sub> = 1.2 V, V<sub>IO</sub> = 1.8 V, T<sub>OP</sub> = +25 °C, f = 3750 MHz, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)**

| Parameter           | Symbol           | Conditions                                   | Mode 0 |      |     | Mode 1 |      |     | Units |
|---------------------|------------------|----------------------------------------------|--------|------|-----|--------|------|-----|-------|
|                     |                  |                                              | Min    | Typ  | Max | Min    | Typ  | Max |       |
| Input return loss   | RL_I_G7          | NTC                                          | 3.9    | 11.9 |     | 5.0    | 11.3 |     | dB    |
| Output return loss  | RL_O_G7          | NTC                                          | 15.0   | 16.1 |     | 10.0   | 15.5 |     | dB    |
| Reverse isolation   | ISO_R_G7         | NTC                                          | 31.0   | 33.8 |     | 31.0   | 33.7 |     | dB    |
| Stability           | S                | NTC                                          | 1.0    | 2.0  |     | 1.0    | 2.0  |     | K     |
| Gain switching time | t <sub>sw</sub>  | NTC, ±0.5 dB of final value                  |        |      | 1   |        |      | 1   | us    |
| Turn-on time        | t <sub>ON</sub>  | Gain settled to within 0.5 dB of final value |        |      | 1   |        |      | 1   | us    |
| Turn-off time       | t <sub>OFF</sub> | Gain ≤ -30 dB of previous settled value      |        |      | 1   |        |      | 1   | us    |

**Table 6. SKY53728-11 n79 RF Performance (1 of 2)**

(VDD = 1.2 V, VIO = 1.8 V, TOP = +25 °C, f = 4700 MHz, Characteristic Impedance [Z0] = 50 Ω, Unless Otherwise Noted)

| Parameter           |     | Symbol | Conditions                                               | Mode 0 |       |      | Mode 1 |       |       | Units |
|---------------------|-----|--------|----------------------------------------------------------|--------|-------|------|--------|-------|-------|-------|
|                     |     |        |                                                          | Min    | Typ   | Max  | Min    | Typ   | Max   |       |
| Operating Frequency | n79 | fo     |                                                          | 4400   |       | 5000 | 4400   |       | 5000  | MHz   |
| LNA Current         | G7  | IDD    | NTC                                                      |        | 9.5   | 16.5 |        | 10.8  | 19.0  | mA    |
|                     | G6  |        |                                                          |        | 8.8   | 14.5 |        | 8.7   | 12.5  |       |
|                     | G5  |        |                                                          |        | 8.8   | 14.5 |        | 10.8  | 18.0  |       |
|                     | G4  |        |                                                          |        | 3.5   | 5.0  |        | 4.1   | 5.5   |       |
|                     | G3  |        |                                                          |        | 4.4   | 6.5  |        | 2.1   | 4.0   |       |
|                     | G2  |        |                                                          |        | 4.4   | 6.5  |        | 1.8   | 4.0   |       |
|                     | G1  |        |                                                          |        | 2.8   | 4.0  |        | 1.5   | 4.0   |       |
| In-Band Gain        | G7  | Gn     | NTC                                                      | 15.0   | 17.5  | 20.5 | 15.0   | 17.9  | 20.0  | dB    |
|                     | G6  |        |                                                          | 11.5   | 14.6  | 18.0 | 13.5   | 15.6  | 19.0  |       |
|                     | G5  |        |                                                          | 9.0    | 11.6  | 14.5 | 7.5    | 9.8   | 13.0  |       |
|                     | G4  |        |                                                          | 6.0    | 8.7   | 11.0 | 2.0    | 4.2   | 7.0   |       |
|                     | G3  |        |                                                          | 3.0    | 4.9   | 8.0  | -4.5   | -3.5  | 1.0   |       |
|                     | G2  |        |                                                          | 0.0    | 2.0   | 6.0  | -11.0  | -9.8  | -5.5  |       |
|                     | G1  |        |                                                          | -10.0  | -7.8  | -4.0 | -17.0  | -16.3 | -11.5 |       |
| Noise Figure        | G7  | NF     | NTC                                                      |        | 2.4   | 3.0  |        | 2.4   | 3.0   | dB    |
|                     | G6  |        |                                                          |        | 2.5   | 3.1  |        | 2.4   | 3.0   |       |
|                     | G5  |        |                                                          |        | 2.6   | 4.0  |        | 2.6   | 4.0   |       |
|                     | G4  |        |                                                          |        | 3.5   | 4.8  |        | 3.7   | 5.0   |       |
|                     | G3  |        |                                                          |        | 3.6   | 5.0  |        | 12.2  | 14.5  |       |
|                     | G2  |        |                                                          |        | 4.1   | 5.4  |        | 13.1  | 16.0  |       |
|                     | G1  |        |                                                          |        | 7.8   | 11.4 |        | 15.4  | 19.0  |       |
| In-Band Input P1dB  | G7  | P1dB   | NTC                                                      | -19.0  | -18.0 |      | -19.0  | -17.6 |       | dBm   |
|                     | G6  |        |                                                          | -18.0  | -17.1 |      | -19.0  | -17.3 |       |       |
|                     | G5  |        |                                                          | -18.0  | -16.6 |      | -18.0  | -16.2 |       |       |
|                     | G4  |        |                                                          | -13.0  | -12.1 |      | -12.0  | -10.6 |       |       |
|                     | G3  |        |                                                          | -13.0  | -11.2 |      | -4.5   | -3.4  |       |       |
|                     | G2  |        |                                                          | -13.0  | -11.0 |      | -3.5   | -1.4  |       |       |
|                     | G1  |        |                                                          | -4.0   | -2.1  |      | -1.0   | 3.6   |       |       |
| In-Band IIP3        | G7  | IIP3   | NTC, fCW2 = fCW1±1MHz, Measured at 20 dB lower than P1dB | -8.0   | -5.5  |      | -10.0  | -5.8  |       | dBm   |
|                     | G6  |        |                                                          | -8.0   | -5.5  |      | -10.0  | -5.8  |       |       |
|                     | G5  |        |                                                          | -7.8   | -5.2  |      | -10.0  | -6.0  |       |       |
|                     | G4  |        |                                                          | -2.7   | -1.2  |      | -4.0   | -0.9  |       |       |
|                     | G3  |        |                                                          | -2.1   | -0.6  |      | 2.7    | 5.0   |       |       |
|                     | G2  |        |                                                          | -2.2   | -0.7  |      | 3.9    | 6.2   |       |       |
|                     | G1  |        |                                                          | 4.2    | 6.0   |      | 4.9    | 7.3   |       |       |

**Table 6. SKY53728-11 n79 RF Performance (2 of 2)****(V<sub>DD</sub> = 1.2 V, V<sub>IO</sub> = 1.8 V, T<sub>OP</sub> = +25 °C, f = 4700 MHz, Characteristic Impedance [Z<sub>0</sub>] = 50 Ω, Unless Otherwise Noted)**

| Parameter           | Symbol           | Conditions                                   | Mode 0 |      |     | Mode 1 |      |     | Units |
|---------------------|------------------|----------------------------------------------|--------|------|-----|--------|------|-----|-------|
|                     |                  |                                              | Min    | Typ  | Max | Min    | Typ  | Max |       |
| Input return loss   | RL_I_G7          | NTC                                          | 9.0    | 12.5 |     | 10.0   | 16.3 |     | dB    |
| Output return loss  | RL_O_G7          | NTC                                          | 11.0   | 19.6 |     | 12.0   | 22.5 |     | dB    |
| Reverse isolation   | ISO_R_G7         | NTC                                          | 28.0   | 34.8 |     | 28.0   | 33.5 |     | dB    |
| Stability           | S                | NTC                                          | 1.0    | 2.0  |     | 1.0    | 2.0  |     | K     |
| Gain switching time | t <sub>sw</sub>  | NTC, ±0.5 dB of final value                  |        |      | 1   |        |      | 1   | us    |
| Turn-on time        | t <sub>ON</sub>  | Gain settled to within 0.5 dB of final value |        |      | 1   |        |      | 1   | us    |
| Turn-off time       | t <sub>OFF</sub> | Gain ≤ -30 dB of previous settled value      |        |      | 1   |        |      | 1   | us    |

## Package Dimensions

The typical part marking for the SKY53728-11 is shown in Figure 3. The PCB layout footprint is shown in Figure 4. Package dimensions are shown in Figure 5. Tape and reel dimensions are shown in Figure 6.

## Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY53728-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design & SMT Assembly/Rework Guidelines for MCM - L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

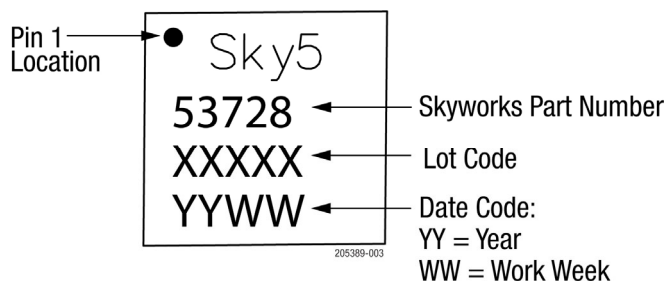
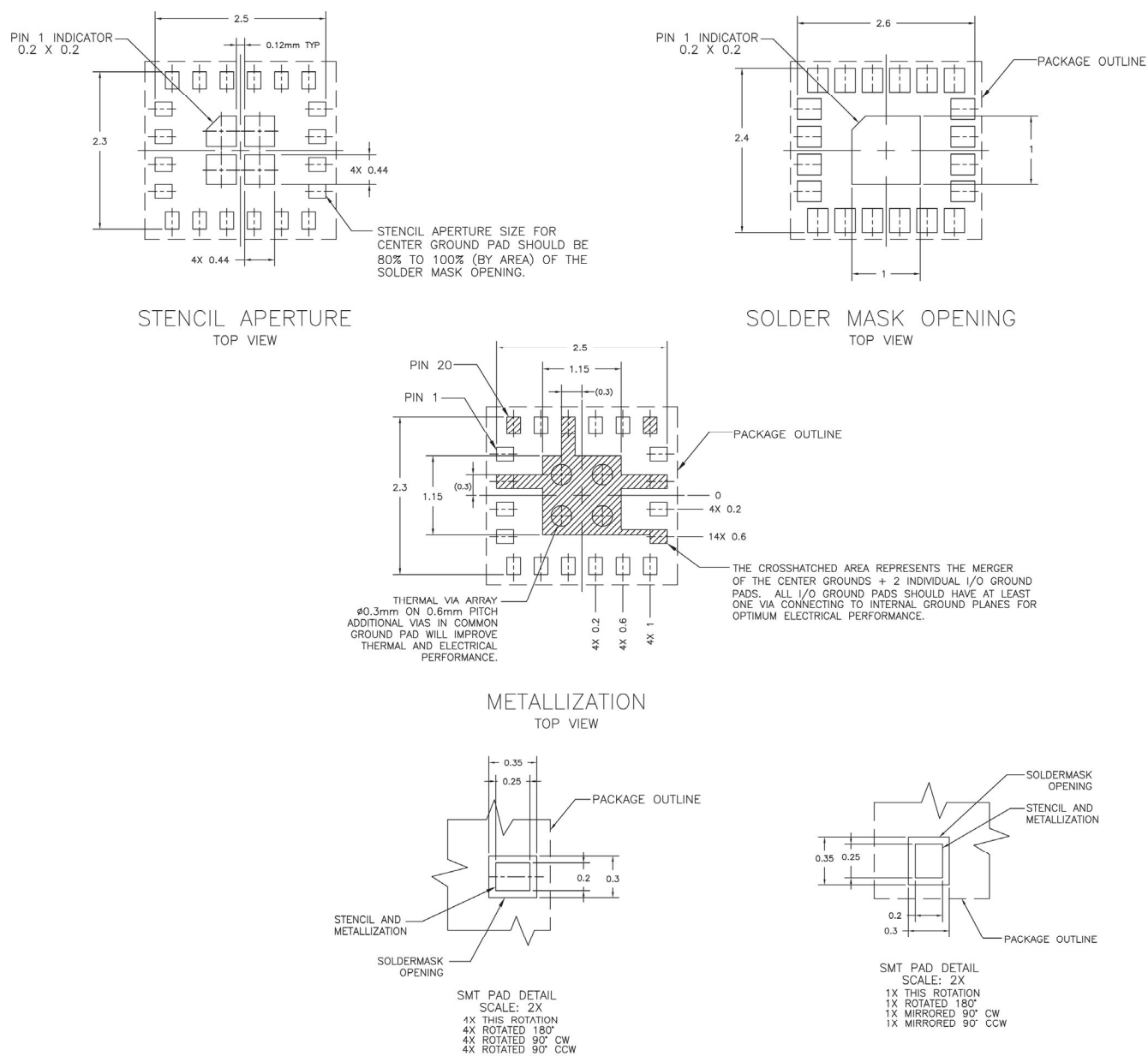


**Figure 3. SKY53728-11 Typical Part Marking**



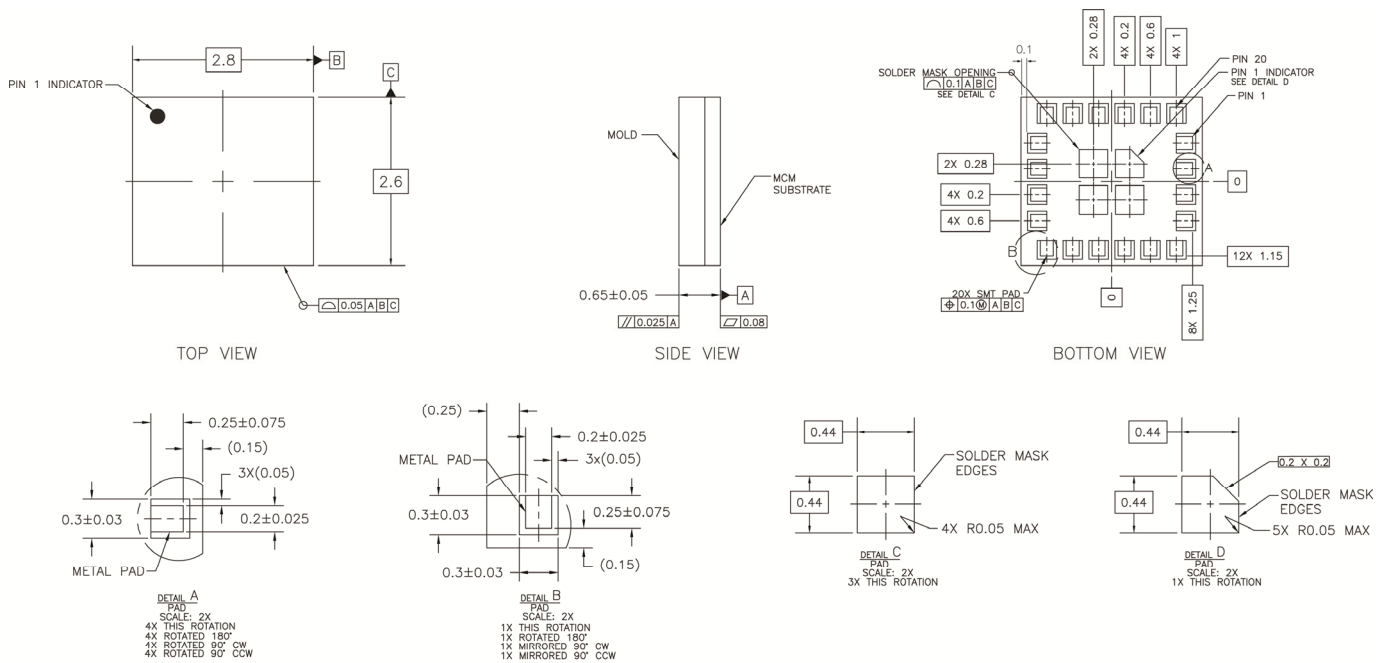
## NOTES:

1. DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. THERMAL VIAS SHOULD BE RESIN FILLED AND CAPPED IN ACCORDANCE WITH IPC-4761 TYPE VII VIAS. 30-35UM CU THICKNESS IS RECOMMENDED.

205389-004

**Figure 4. SKY53728-11 PCB Layout Footprint**

# FINAL DATA SHEET • SKY5<sup>®</sup>-3728-11: 5G NR UHB Diversity Receive Module

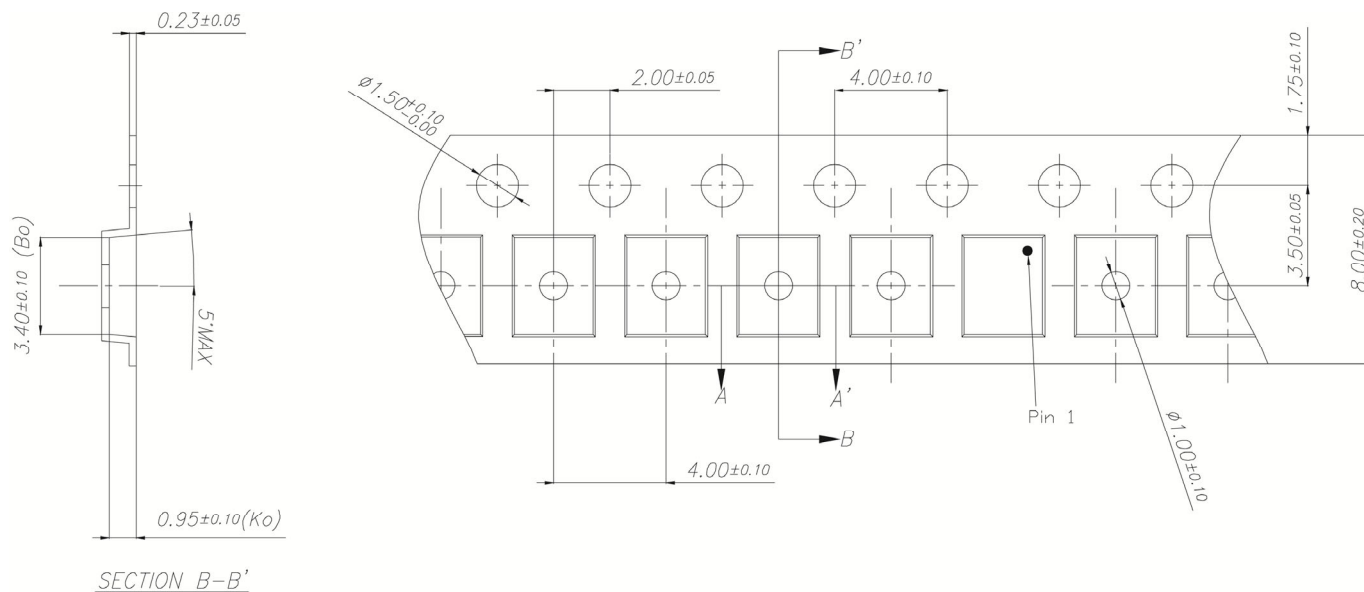


NOTES: UNLESS OTHERWISE SPECIFIED.

1. DIMENSIONING AND TOLERANCING IN ACCORDANCE WITH ASME Y14.5M-1994.
2. SEE APPLICABLE BONDING DIAGRAM AND DEVICE ASSEMBLY DRAWING FOR DIE AND COMPONENT PLACEMENT.
3. PAD DEFINITIONS PER DETAILS ON DRAWING.
4. PCB TYPE 6L NS SSV 60 G5 240.
5. THIS PACKAGE USES CONFORMAL SHIELDING.
6. THIS PACKAGE IS COMPATIBLE WITH TRANSFER AND COMPRESSION MOLD.

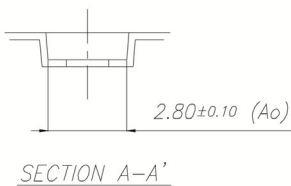
205389-005

**Figure 5. SKY53728-11 Package Dimensions**



NOTES:

1. CARRIER TAPE MUST MEET ALL REQUIREMENTS OF SKYWORKS GP01-D232 PROCUREMENT SPEC FOR TAPE and REEL SHIPPING.
2. CARRIER TAPE SHALL BE BLACK CONDUCTIVE POLYCARBONATE
3. COVER TAPE SHALL BE TRANSPARENT CONDUCTIVE MATERIAL
4. ESD-SURFACE RESISTIVITY SHALL MEET GP01-D232
5. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE :  $\pm 0.20\text{mm}$
6. A<sub>0</sub> & B<sub>0</sub> MEASURED ON PLANE 0.30mm ABOVE THE BOTTOM OF THE POCKET.
7. ALL DIMENSIONS ARE IN MILLIMETERS.



205389-006

### Figure 6. SKY53728-11 Tape and Reel Dimensions

## Ordering Information

| Part Number | Product Description                | Evaluation Board Part Number |
|-------------|------------------------------------|------------------------------|
| SKY53728-11 | 5G NR UHB Diversity Receive Module | SKY53728-11EK1               |

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