SONY

LCD Driver

CXA7009R

Description

The CXA7009R is a driver IC developed for use with Sony micro-display LCD panels. It supports 12-bit digital input, and the input data is demultiplexed into 12 parallel and output. The CXA7009R can directly drive an LCD panel, and also incorporates the VCOM setting circuit and precharge pulse waveform generation circuit needed for LCD panels.
The CXA7009R can replace the CXA7007R. In addition, the following functions have been added compared to the CXA7007R, so be sure to confirm operation before use.
(Applications: LCD projectors and other video equipment)

Features Added to the CXA7009R

◆ Slave address designation
Up to eight CXA7007R could be controlled simultaneously, but an extra device address pin has been added to the CXA7009, making it possible to control up to 15 CXA7009R simultaneously.
In addition, the same data can be written to all CXA7009R connected on the same I^2C bus by using 8Ehex as the slave address.
See “4. Slave Address Designation” (page 15) for details.

◆ I^2C bus read function
The CXA7007R supported only I^2C bus write mode and did not support read mode, but the CXA7009R also supports I^2C bus read mode in addition to I^2C bus write mode. (See page 16).

◆ Precharge pulse waveform
The CXA7007R could set three precharge operation modes by setting the two register bits SIDON (1 bit) and ALON (1 bit). However, the CXA7009R can set two additional modes for a total of five precharge operation modes by setting the three register bits SIDON (1 bit) and ALON (2 bits).
See “3. SID Signal Generation Block” (page 26) for details.

Features

◆ Supports 12-bit input
◆ Low output deviation
◆ Various adjustment functions using an I^2C bus interface
◆ Supports signals up to double-speed XGA when using one CXA7009R, and signals up to double-speed SXGA+ when using two CXA7009Rs
◆ VCOM voltage generation circuit
◆ Precharge pulse waveform generation circuit

Package

80-pin LQFP (Plastic)

Absolute Maximum Ratings

(V_{SS} = 0V)

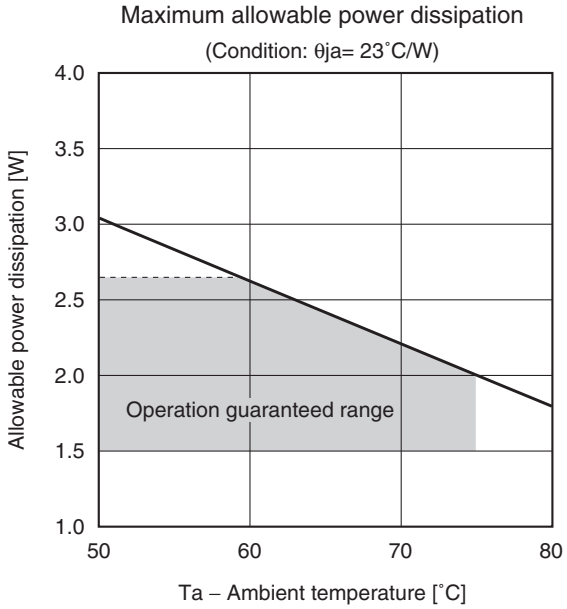
◆ Supply voltage	V_{CC}, PV_{CC}	16	V
	V_{DD}	4	V
◆ Operating temperature	Topr	–20 to +75	˚C
◆ Storage temperature	Tstg	–65 to +150	˚C
◆ Junction temperature	Tj	+125	˚C

Recommended Operating Conditions

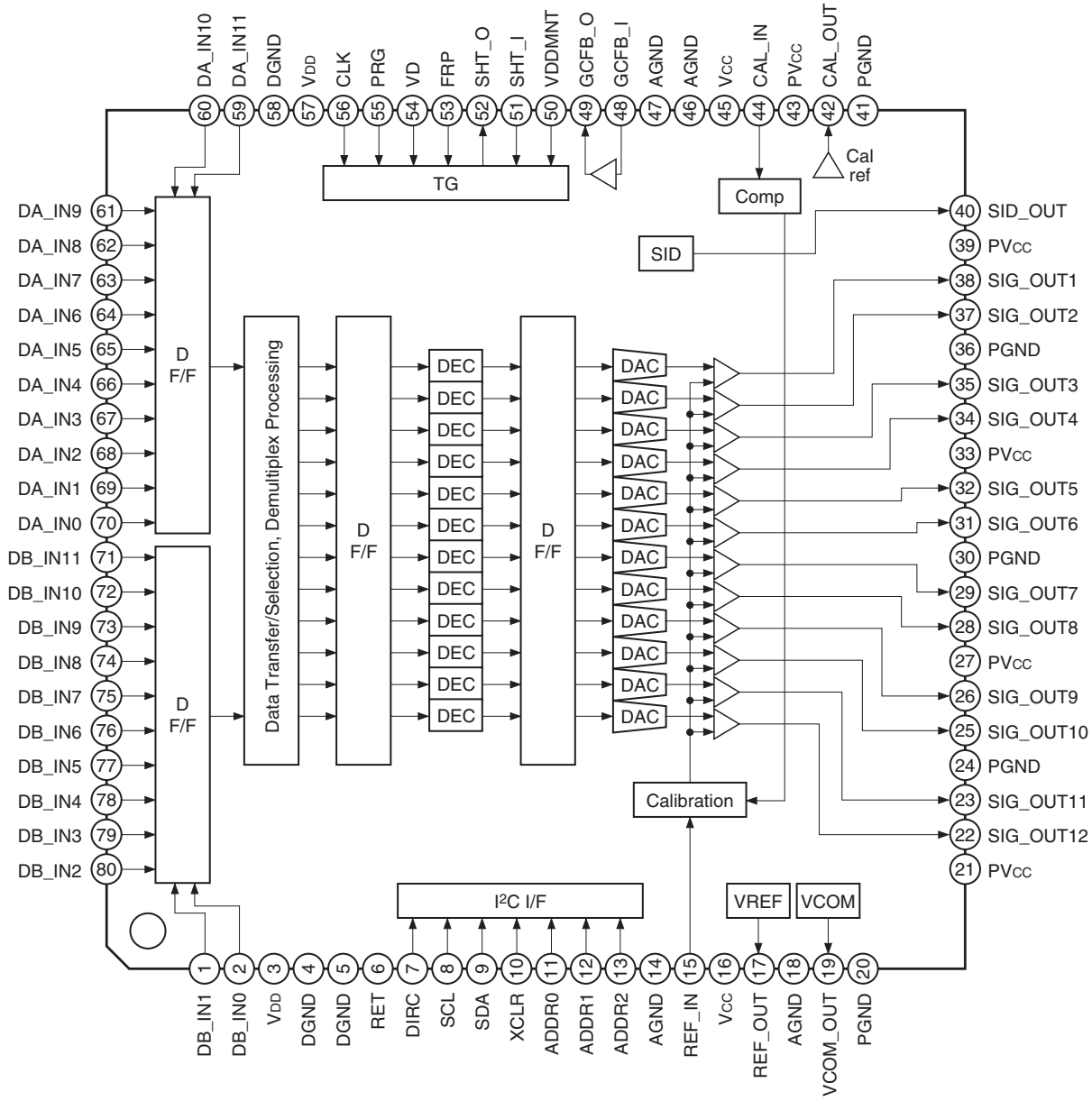
(V_{SS} = 0V)

◆ Supply voltage	V_{CC}, PV_{CC}	15.0 to 15.5	V
	V_{DD}	3.0 to 3.6	V
◆ Operating temperature	Topr	–20 to +75	˚C
◆ Allowable power dissipation	P_D	2100	mW
	θja	23	˚C/W
	θjc	2	˚C/W

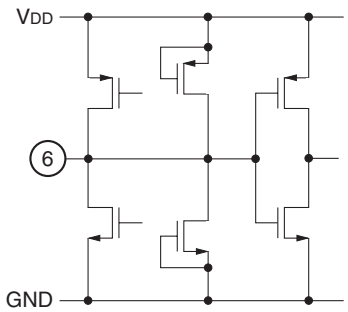
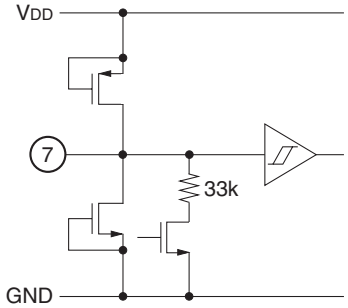
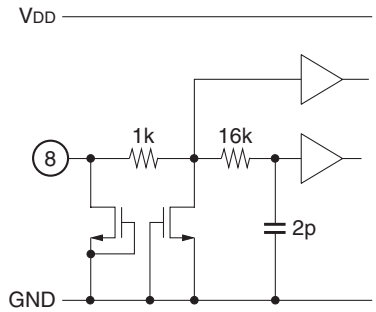
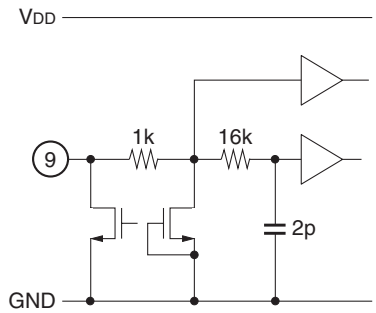
(Board conditions: four-layer board, internal layer GND)

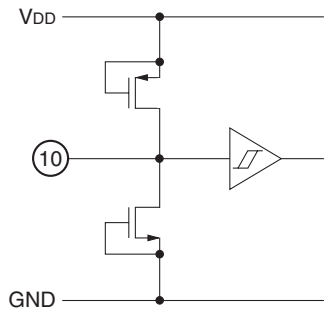
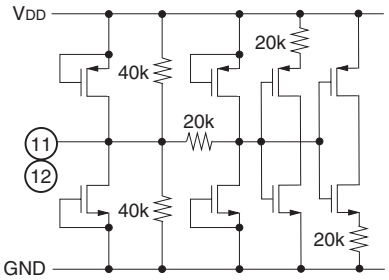
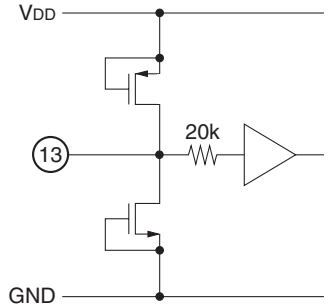
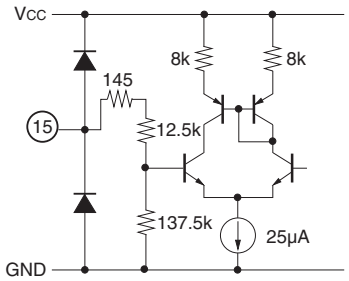
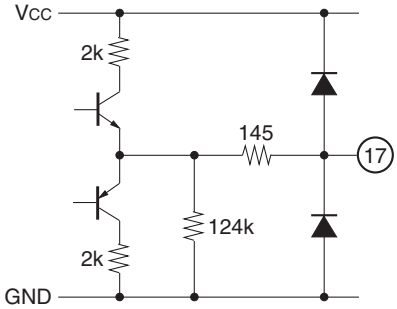


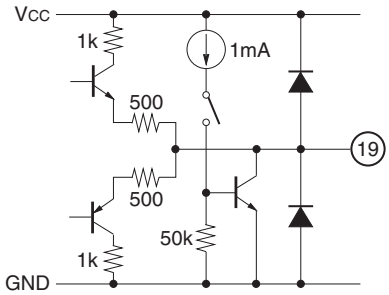
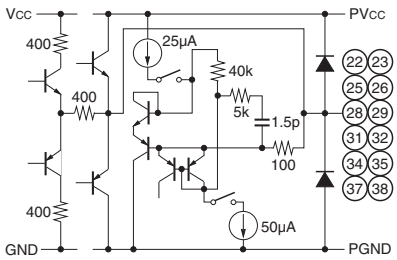
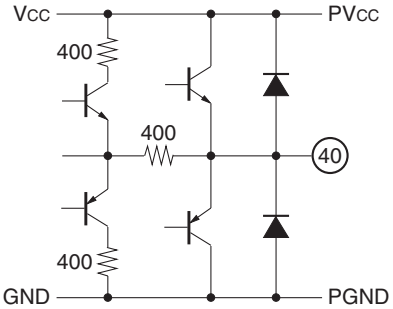
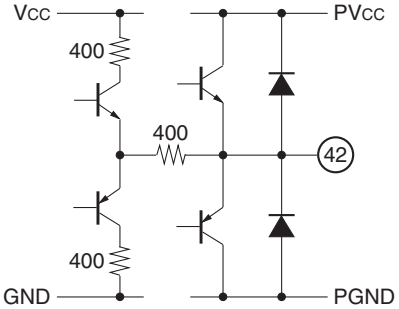
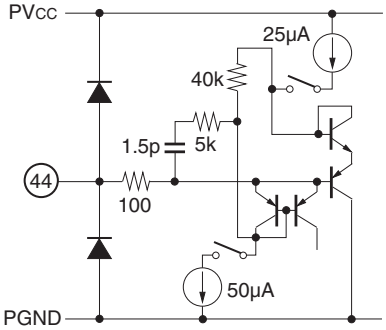
Block Diagram

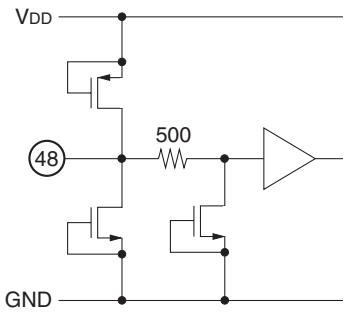
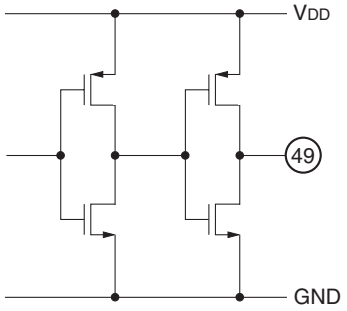
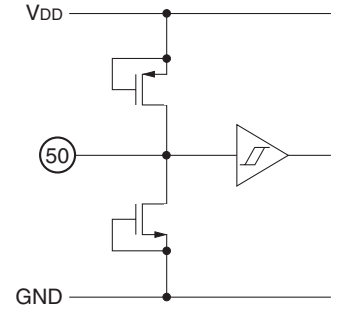
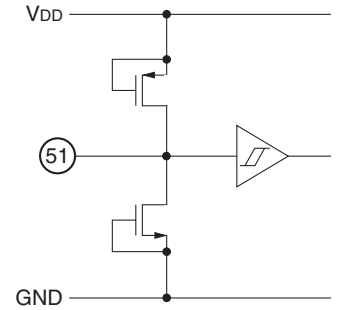


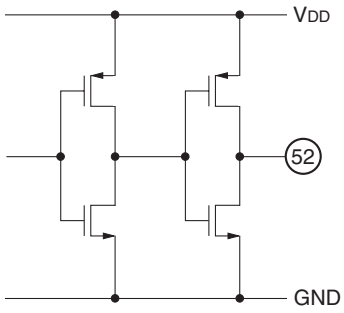
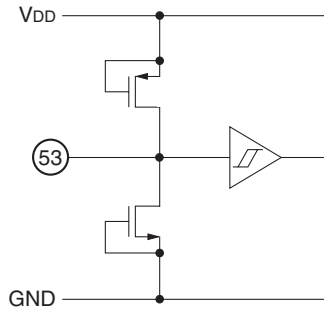
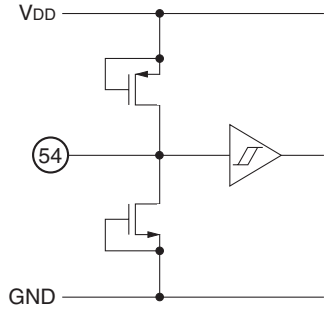
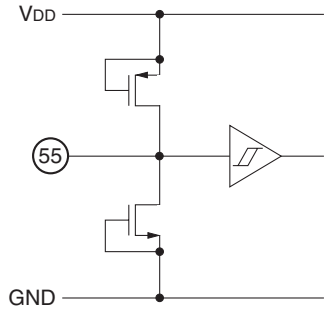
Pin Description

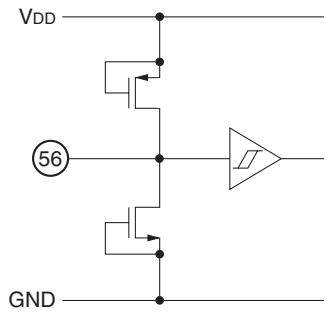
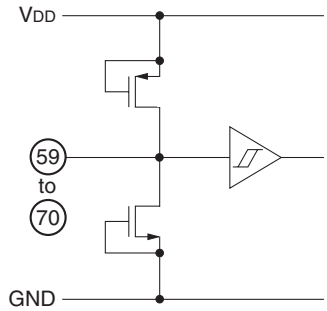
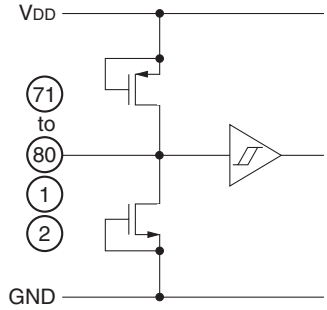
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
6	RET	I/O	Input High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3 Output CMOS output		Calibration retiming pulse I/O. When using multiple CXA7009Rs, connect RET between the ICs.
7	DIRC	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		Scan direction setting. The scan direction is set in combination with the I²C setting DIRCR.
8	SCL	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		I²C bus clock input. Supports a clock from 1kHz to 400kHz.
9	SDA	I/O	Input High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3 Output Nch open drain output		I²C bus data I/O

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
10	XCLR	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		XCLR. Initializes the internal flip-flop and other blocks.
11 12	ADDR0 ADDR1	I	High: ≥ V_{DD} – 0.8V V_{DD}/2 – 0.15V ≤ CENTER CENTER ≤ V_{DD}/2 + 0.15V Low: ≤ 0.6V		I²C bus IC address setting. When setting with an external pull-down or pull-up resistor, use 7kΩ or less. The Center setting can be left open.
13	ADDR2	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		I²C bus IC address setting. The addresses 70h, 72h, 74h, 76h, 78h, 7Ah, 7Ch, 7Eh, 80h, 82h, 84h, 86h, 88h, 8Ah and 8Ch can be set by changing the setting of the ADDR0, ADDR1 and ADDR2 pins.
15	REF_IN	I	6.0V		Reference voltage input. Connect to the REF_OUT pin (Pin 17) through a 1kΩ resistor. When using multiple CXA7009Rs, connect the output of one IC to the REF_IN of each IC. Connect a 1µF bypass capacitor.
17	REF_OUT	O	6.0V		Reference voltage output. Connect to the REF_IN pin (Pin 15) through a 1kΩ resistor.

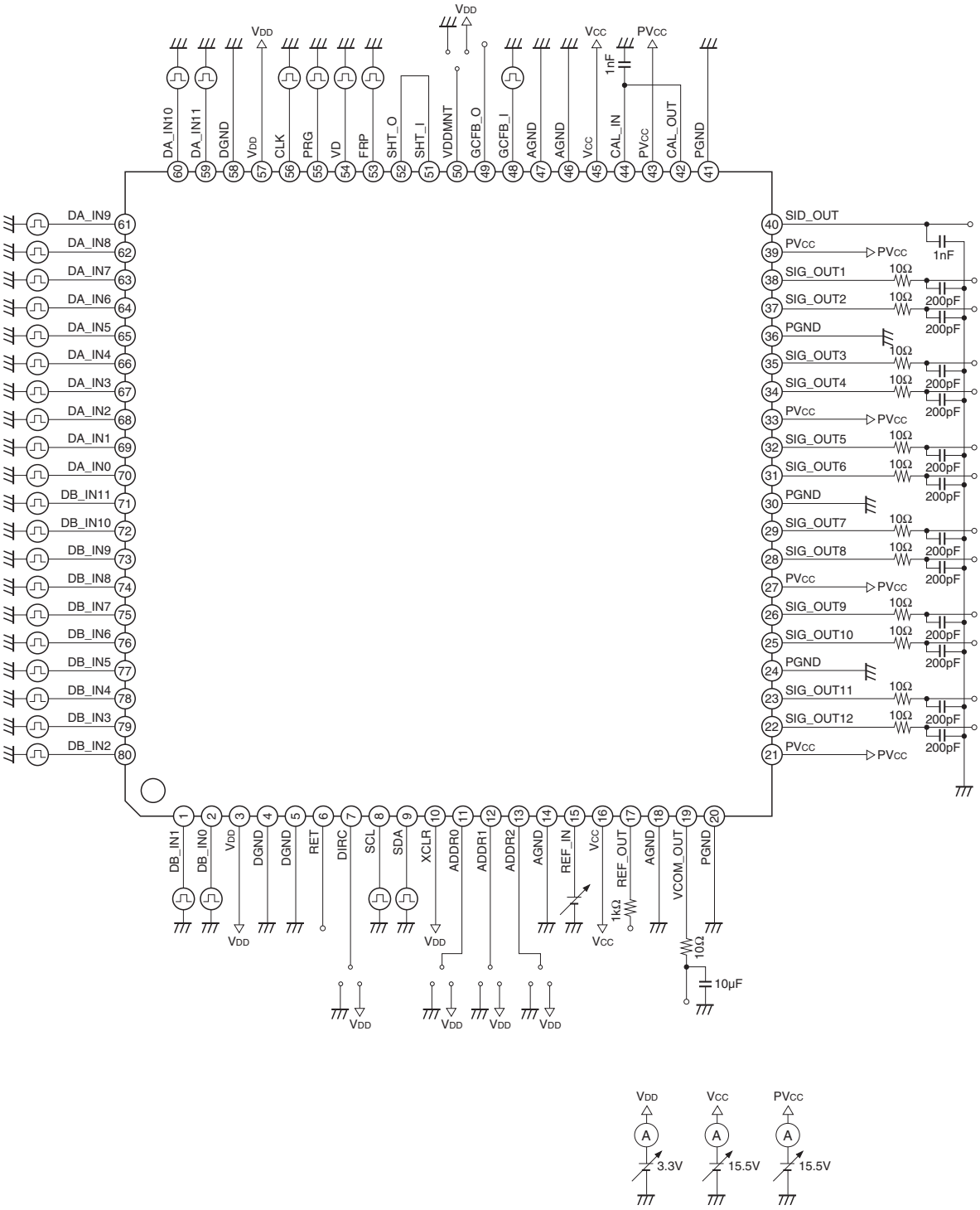
Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
19	VCOM_OUT	O	5.5 to 7.5V		Common voltage output of LCD panel. Adjustment is possible by the I²C setting. Connect to the panel through Rs = 10Ω. Connect the panel side to GND through 10μF. Make these connections even when not connecting this pin to the panel.
22, 23, 25, 26, 28, 29, 31, 32, 34, 35, 37, 38	SIG_OUT1 to SIG_OUT12	O	1.5 to 13.5V		Demultiplexed output of AC inverse driven video signals. These pins can be directly connected to the LCD panel.
40	SID_OUT	O	1.5 to 13.5V		LCD panel precharge signal waveform output. Adjustment is possible by the I²C setting.
42	CAL_OUT	O	1.5 to 13.5V		Reference signal output for offset calibration. Connect to the CAL_IN pin (Pin 44). When using multiple CXA7009Rs, connect the output of one IC to the CAL_IN of each IC.
44	CAL_IN	I	1.5 to 13.5V		Reference signal input for offset calibration. Connect a bypass capacitor near to the input pin. Even when using multiple CXA7009Rs, set so that the load as viewed from CAL_OUT is 1000pF or less.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
48	GCFB_I	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		Buffer input. The signal input from GCFB_I is buffered and output from GCFB_O (Pin 49).
49	GCFB_O	O	CMOS output		Buffer output. The signal input from GCFB_I (Pin 48) is buffered and output from GCFB_O.
50	VDDMNT	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		Momentary cut-off monitor. When this pin is High, normal operation is performed. When Low, SIG_OUT does not perform inversion operation and is fixed to the non-inverted side, and the VCOM output falls to 200mV or less.
51	SHT_I	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		Timing signal input for demultiplexed simultaneous output. When using multiple CXA7009Rs, connect the SHT_O (Pin 52) of the reference IC to the SHT_I of each IC using the shortest equivalent length wiring possible.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
52	SHT_O	O	CMOS output		Timing signal output for demultiplexed simultaneous output. When using multiple CXA7009Rs, connect the output of one IC to the SHT_I (Pin 51) of each IC.
53	FRP	I	High: ≥ VDD × 0.7 Low: ≤ VDD × 0.3		LCD panel AC drive inversion timing input. The polarity is inverted in combination with the FRINV setting. FRP EX-OR FRINV = High : Inverted FRP EX-OR FRINV = Low : Non-inverted
54	VD	I	High: ≥ VDD × 0.7 Low: ≤ VDD × 0.3		Offset calibration timing start signal input. Input a positive polarity timing pulse during the V blanking period.
55	PRG	I	High: ≥ VDD × 0.7 Low: ≤ VDD × 0.3		Timing pulse input for switching the Pin 40 output level (SID_OUT). In addition, it also functions as the circuit sync signal input and the V blanking calibration start timing, so always input signal to this pin.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
56	CLK	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		Master clock input. Supports a clock up to 85MHz. The polarity is determined by the I²C setting CKPOL. The clock is reverse polarity when CKPOL is High, and forward polarity when Low.
59 to 70	DA_IN0 to DA_IN11	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		Digital data A port input. DA_IN11 (MSB) DA_IN0 (LSB) Only this port is used during single data input.
71 to 80, 1, 2	DB_IN0 to DB_IN11	I	High: ≥ V_{DD} × 0.7 Low: ≤ V_{DD} × 0.3		Digital data B port input. DB_IN11 (MSB) DB_IN0 (LSB)
3, 57	V_{DD}		3.3V		3.3V power supply
16, 45	V_{CC}		15.5V		15V power supply
21, 27, 33, 39, 43	PV_{CC}		15.5V		Power V_{CC}
4, 5, 58	DGND		DGND		GND
14, 18, 46, 47	AGND		AGND		GND
20, 24, 30, 36, 41	PGND		PGND		Power GND

Electrical Characteristics Measurement Circuit

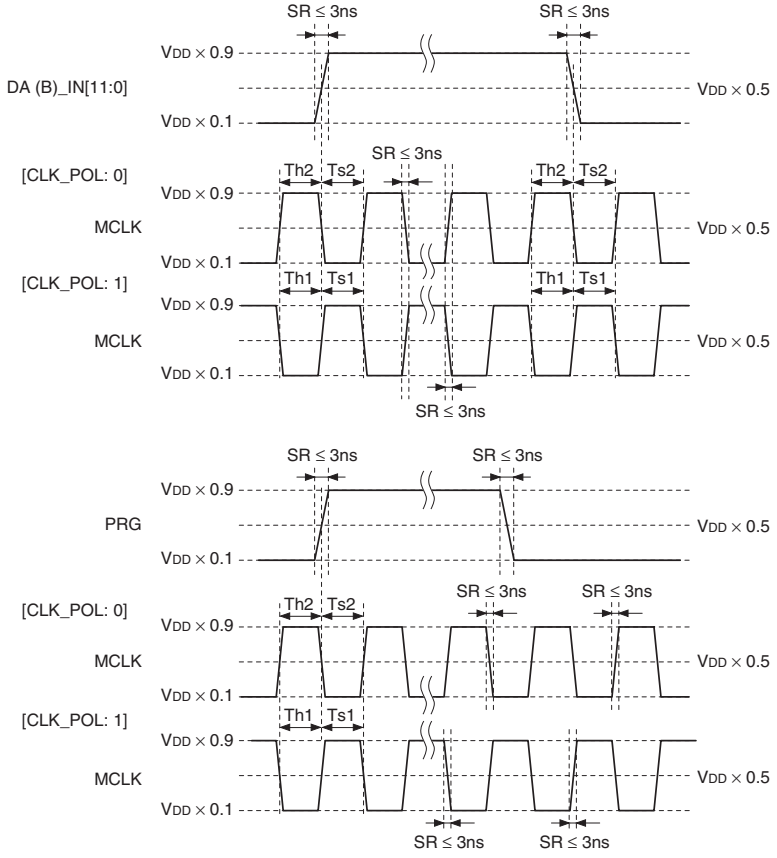


Electrical Characteristics

(Ta = 25℃, V_{CC}, PV_{CC} = 15.25V, V_{DD} = 3.3V)

No.	Item	Symbol	Measurement description	Min.	Typ.	Max.	Unit
1	Digital input resolution	n		—	12	—	bit
2	Digital input setup time 1	Ts1	CKPOL: 1, PRG and DA (B)_IN[11:0] minimum setup time for CLK input	3	—	—	ns
3	Digital input setup time 2	Ts2	CKPOL: 0, PRG and DA (B)_IN[11:0] minimum setup time for CLK input	3	—	—	ns
4	Digital input hold time 1	Th1	CKPOL: 1, PRG and DA (B)_IN[11:0] minimum hold time for CLK input	3	—	—	ns
5	Digital input hold time 2	Th2	CKPOL: 0, PRG and DA (B)_IN[11:0] minimum hold time for CLK input	3	—	—	ns
6	MCLK input frequency range	f_{MCLK}	Maximum frequency at which the internal timing generator and D/A converter operate normally	—	—	85	MHz
7	SIG_OUT amplitude adjustment range	$V_{SIGOUTp-p}$	Measure the SIG_OUT voltage difference between DA (B)_IN[11:0]: 000h and FFFh when Gain control = 00h and FFh.	2.2	—	5.5	Vp-p
8	SIG_OUT slew rate	SR_{OUT}	Load capacitance C = 100pF, measure the slew rate at 10 to 90% of SIG_OUT1 to SIG_OUT12 rise and fall when DA (B)_IN[11:0] is varied from 000h to FFFh or from FFFh to 000h when Gain control = FFh, SIG center = 20h and Brightness control = 00h.	300	430	—	V/μs
9	SIG_OUT minimum output voltage	V_{MIN}	Minimum voltage that SIG_OUT1 to SIG_OUT12 can output	1.5	—	—	V
10	SIG_OUT maximum output voltage	V_{MAX}	Maximum voltage that SIG_OUT1 to SIG_OUT12 can output	—	—	13.5	V
11	Output deviation between channels 1	D_{OUT1}	Value obtained by subtracting the minimum value from the maximum value of SIG_OUT1 to SIG_OUT12 when Gain control = 70h, SIG center = 04h, Brightness control = 00h, CALL[11:0] = 800h and DA (B)_IN[11:0] = 800h	—	—	4	mVp-p
12	Output deviation between channels 2	D_{OUT2}	Value obtained by subtracting the minimum value from the maximum value of SIG_OUT1 to SIG_OUT12 when Gain control = 70h, SIG center = 04h, Brightness control = 00h, CALL[11:0] = 800h and DA (B)_IN[11:0] = 000h or FFFh	—	—	10	mVp-p
13	Output deviation between ICs 1	D_{IC1}	Value obtained by subtracting the minimum value from the maximum value of SIG_OUT1 to SIG_OUT12 when Gain control = 70h, SIG center = 04h, Brightness control = 00h, CALL[11:0] = 800h and DA (B)_IN[11:0] = 800h (with two CXA7009Rs)	—	—	4	mVp-p

No.	Item	Symbol	Measurement description	Min.	Typ.	Max.	Unit
14	Output deviation between ICs 2	D_{IC2}	Value obtained by subtracting the minimum value from the maximum value of SIG_OUT1 to SIG_OUT12 when Gain control = 70h, SIG center = 04h, Brightness control = 00h, CALL[11:0] = 800h and DA (B)_IN[11:0] = 000h or FFFh (with two CXA7009Rs)	—	—	10	mVp-p
15	SID output gain 1	A_{SID1}	Adjustable range by SID control A	0.1	—	5.5	V
16	SID output gain 2	A_{SID2}	Adjustable range by SID control B	0.1	—	5.5	V
17	Signal center adjustable range	V_{SIGC}	SIG_C output voltage when SIG center is varied	6.5	—	8.5	V
18	SIG_OUT offset adjustable range	$V_{SIGOFST}$	Adjustable range by Brightness control	0.2	—	1.0	V
19	VCOM adjustable range	V_{COM}	VCOM_OUT adjustment range for the signal center voltage when VCOM control is varied	–2.0	—	0.1	V
20	V_{DD} current consumption	I_{VDD}	V_{DD} current consumption when CLK = 85MHz	13	23	35	mA
21	V_{CC} current consumption	I_{VCC}	CLK = 85MHz, inversion signal every DA (B)_IN = 000h, FRP =6CLK, I_{VCC} + I_{PVCC} current consumption when SIG_OUT load capacitance = 200pF	74	86	98	mA
22	MAIN DAC differential linearity error	DLE	MAIN DAC differential linearity error	—	1	—	LSB

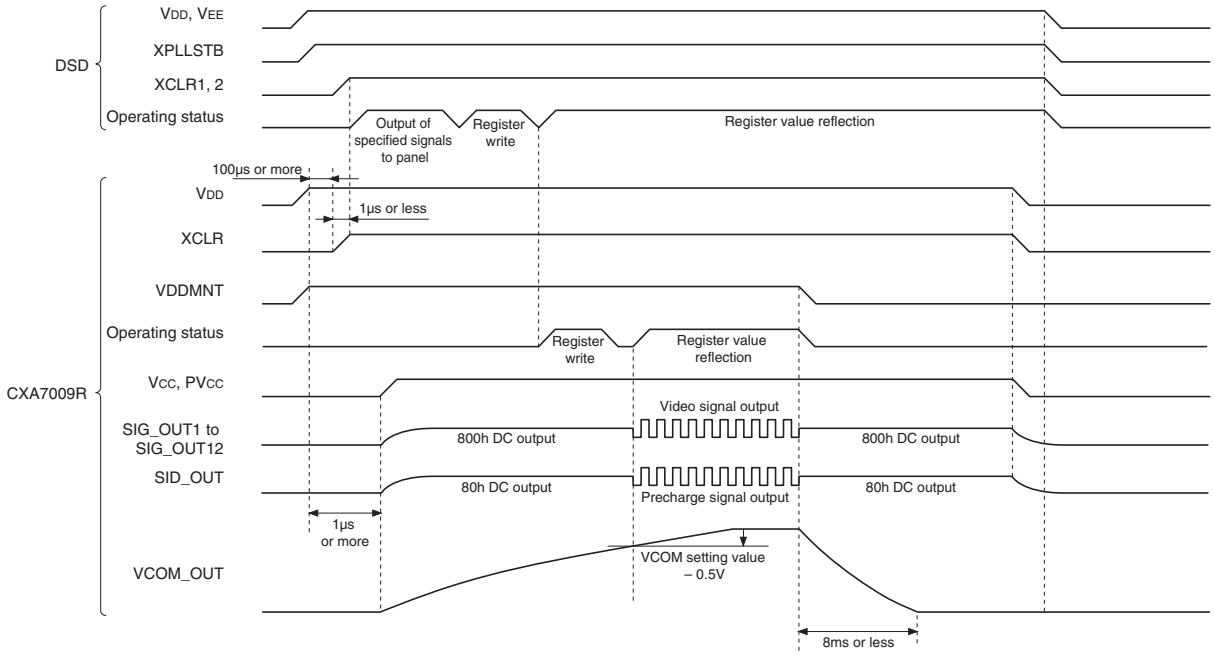


Definition of Digital Input Setup and Hold Time

Power-on Sequence

The CXA7009R requires multiple power supply inputs, and the power supply input order is prescribed as follows. In addition, the CXA7009R has a function that automatically detects the VCOM_OUT output rise during power-on, and locks the signal to the non-inverted side to prevent excessive voltage from being applied to the LCD panel when VCOM_OUT has not risen.

- ◆ V_{DD} (3.3V block) power ON (VDDMNT set High)
- ◆ V_{CC} and PV_{CC} (15.5V block) power ON
  → Inversion operation starts when the VCOM_OUT voltage rises to the setting value – 0.5V and the register setting OUTENB is set High.
  Until the inversion operation starts, SIG_OUT1 to SIG_OUT12 is fixed to the 800hex level of the non-inverted side, and SID_OUT is fixed to the 80hex level of the non-inverted side.
- ◆ XCLR canceled
- ◆ Timing pulse input



When the VDDMNT pin (Pin 50) is Low level, the 800hex level of the non-inverted side is output on SIG_OUT and the 80hex level of the non-inverted side is output on SID_OUT regardless of the FRP polarity, and the VCOM_OUT voltage is pulled down to 200mV or less.

I²C Bus Interface

The CXA7009R makes the various register settings using an I²C bus interface. The bus protocol conforms to I²C specifications, but the following restrictions apply.

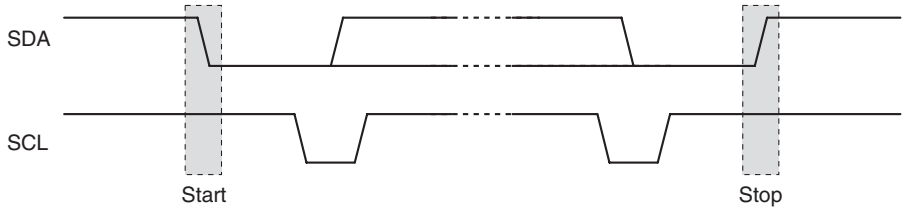
- ◆ Only I²C bus slave operation is performed.
- ◆ Standard mode and first mode are supported, but Hs mode is not supported.
- ◆ No response is sent back to the slave address general call address and start byte.
- ◆ C bus compatibility is not supported.
- ◆ No response is sent back to 10-bit slave addresses.
- ◆ I²C control is not reflected during the XCLR pin Low period.
- ◆ Communication should start 1μs or more after the XCLR pin goes High.

1. Start Condition

The Start mode is established and write is enabled when the SDA input changes from High to Low during the SCL input High period.

2. Stop Condition

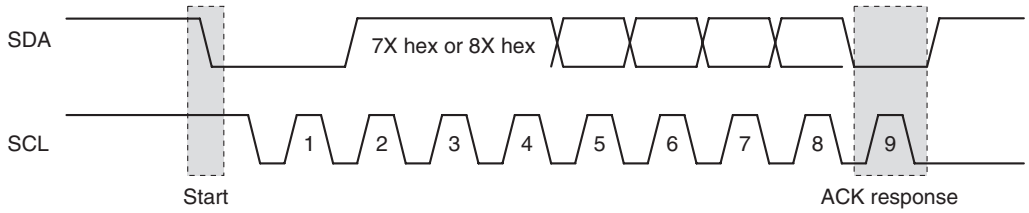
The Stop mode is established when the SDA input changes from Low to High during the SCL input High period. Write end can be indicated by setting the Stop mode.



Start Condition and Stop Condition

3. ACK Response

This status indicates whether data transmission was performed properly. The transmit side releases the bus at the 9th SCL clock, and the receive side drives Low to perform a transfer ACK response.



I²C Bus ACK Response

4. Slave Address Designation

A 7-bit slave address and a 1-bit write code (fixed Low) are transmitted following the Start condition.
The seven addresses 80hex, 82hex, 84hex, 86hex, 88hex, 8Ahex and 8Chex have been added to the CXA7009R in addition to the eight addresses 70hex, 72hex, 74hex, 76hex, 78hex, 7Ahex, 7Chex and 7Ehex that could be set by the CXA7007R. This means that a total of 15 addresses are reserved as slave addresses for this IC, and can be selected by the external pin setting.
Write operation to this IC is possible only when this input slave address and the device address set by the ADDR0, ADDR1 and ADDR2 pins match. When the device address does not match, an ACK response is not generated and subsequent operation is not performed.

A common address setting function has been added to the CXA7009R. When 8Ehex is designated as the slave address, data can be written to all connected CXA7009R regardless of the device address designated by the external pins.

Device Address

External pins			Device address	Slave address					Common address
ADDR2	ADDR1	ADDR0		ADH[3:0]	AD2	AD1	AD0		
L	L	L	0	LHHH	L	L	L	70hex	
L	L	C	1	LHHH	L	L	H	72hex	
L	L	H	2	LHHH	L	H	L	74hex	
L	C	L	3	LHHH	L	H	H	76hex	
L	C	H	4	LHHH	H	L	L	78hex	
L	H	L	5	LHHH	H	L	H	7Ahex	
L	H	C	6	LHHH	H	H	L	7Chex	
L	H	H	7	LHHH	H	H	H	7Ehex	
L	C	C	0	LHHH	L	L	L	70hex	8Ehex
H	L	L	8	HLLL	L	L	L	80hex	
H	L	C	9	HLLL	L	L	H	82hex	
H	L	H	10	HLLL	L	H	L	84hex	
H	C	L	11	HLLL	L	H	H	86hex	
H	C	H	12	HLLL	H	L	L	88hex	
H	H	L	13	HLLL	H	L	H	8Ahex	
H	H	C	14	HLLL	H	H	L	8Chex	
H	C	C	8	HLLL	L	L	L	80hex	

L : Low level
C: Center level
H: High level

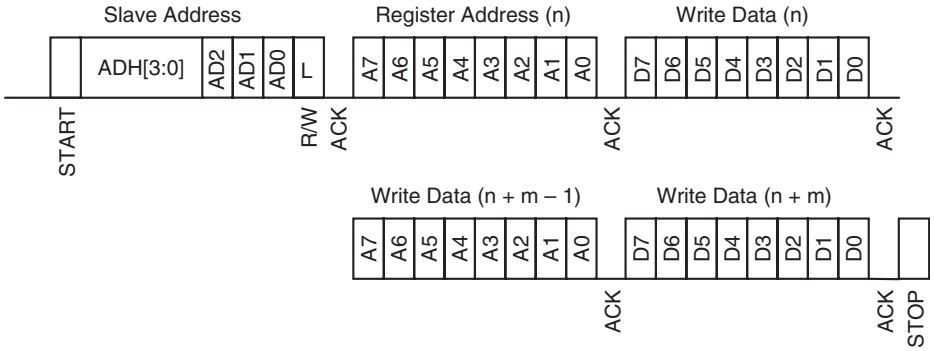
Note) See the “Pin Description” for the external pin ADDR0 and ADDR1 settings.

5. Byte Write Operation

When an 8-bit device address word with the R/W code set Low is input following the Start condition, this IC outputs an ACK response in the 9th bit and enters write mode. Thereafter, when an 8-bit register address is input followed by write data input in 8-bit units, an ACK response is output in each 9th bit and the data is written in this IC.
ACK: In write mode, output Low level on the IC side SDA.

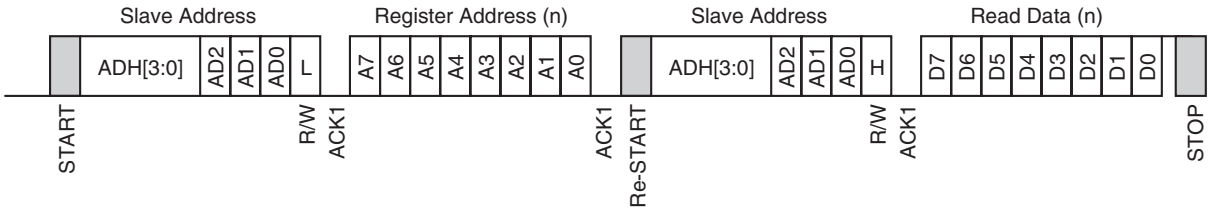
6. Continuous Write Operation

This IC can also write data continuously. Continuous write operation allows continuous write by writing the write data in the same way as byte write operation, and then continuing and transmitting the next write data before transmitting the Stop condition. In continuous write mode, the write data address is automatically incremented each time a single write operation finishes.
After auto incrementing reaches address 255h, it wraps and auto incrementing is repeated again from address 0h.



7. Byte Read Operation

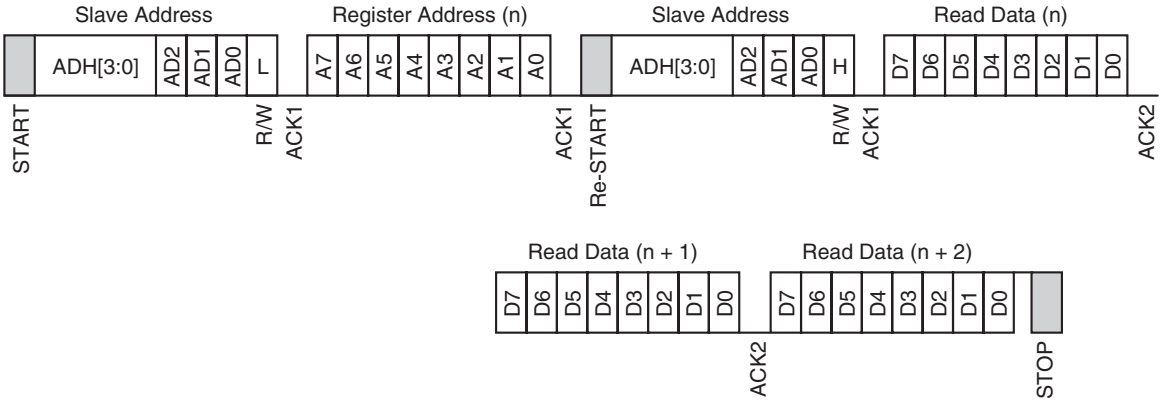
Write the read start register address with write operation.
Then, when the read flag is raised and operation restarts, this IC outputs an ACK response in the 9th bit and enters read mode.
After that, 8 bits of the data written in the designated register is read. Note that an ACK (ACK2*) response is transmitted from the host side after 8 bits of read data in read mode. When an ACK (ACK2*) response is not returned from the host side at the ACK response timing, the circuit automatically stops read operation.



"0" data: Low level output
"1" data: Output at the pulled-up level

8. Continuous Read Operation

This IC can also read data continuously.
Continuous read operation allows continuous read by reading the read data in the same way as byte read operation, and then returning an ACK (ACK2*) from the host side at the ACK response timing. In continuous read mode, the read data address is automatically incremented each time a single read operation finishes. After auto incrementing reaches address 255h, it wraps and auto incrementing is repeated again from address 0h.

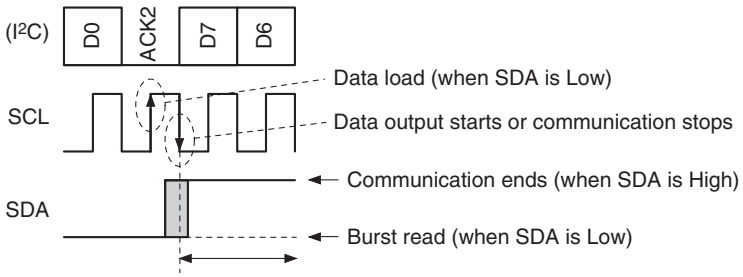


"0" data: Low level output
"1" data: Output at the pulled-up level

◆ **ACK2**

In read mode the CXA7009R does not set SDA Low at the ACK2 timing shown above, so the host side must return Low level when continuing communication. When the host side does not return Low level, the communication automatically ends.

In addition, the following processes are performed during the ACK2 period.
When SCL changes from Low to High while (1) the SDA line is Low, the next address data is loaded (for burst read).
When SCL changes from High to Low while (1) the SDA line is Low, the data is output (burst read).
When SCL changes from High to Low while (2) the SDA line is High, communication ends (automatically set to stop mode).



I²C Control Register

Addr.	Function	D7	D6	D5	D4	D3	D2	D1	D0	Preset
00	Mode1	ALON[1]	M/S	CKPOL	SLSD	DIRCR	FRINV	SIDON	ALON[0]	10
01	CAL control1	OUTDLY	CALON	CALL11	CALL10	CALL9	CALL8	CALL7	CALL6	60
02	CAL control2			CALL5	CALL4	CALL3	CALL2	CALL1	CALL0	00
03	CAL control3			CALMD	CALN	CALP3	CALP2	CALP1	CALP0	20
04	SIG center			SIGC5	SIGC4	SIGC3	SIGC2	SIGC1	SIGC0	04
05	Gain control	G7	G6	G5	G4	G3	G2	G1	G0	70
06	Bright control	B7	B6	B5	B4	B3	B2	B1	B0	00
07	VCOM control		VC6	VC5	VC4	VC3	VC2	VC1	VC0	7F
08	SID control A	SIDA7	SIDA6	SIDA5	SIDA4	SIDA3	SIDA2	SIDA1	SIDA0	AA
09	SID control B	SIDB7	SIDB6	SIDB5	SIDB4	SIDB3	SIDB2	SIDB1	SIDB0	AA
0A	Mode2								OUTENB	00

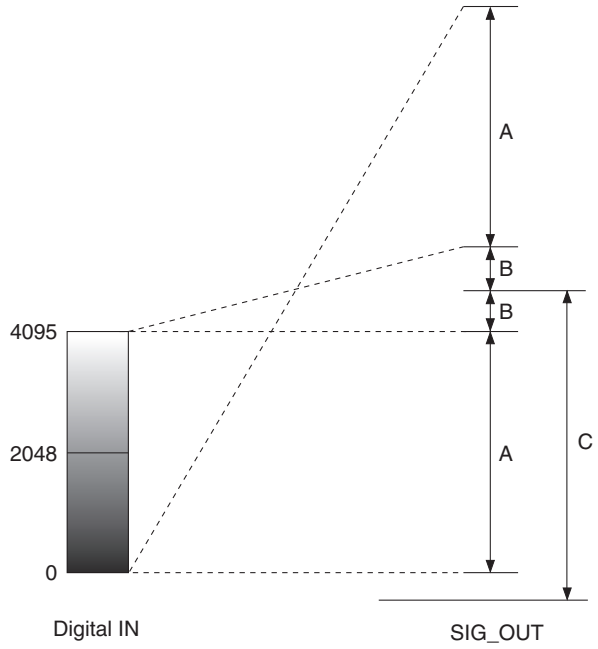
Mode : Various function settings
CAL control : Calibration level and mode settings
SIG center : Signal center voltage setting
Gain control : Voltage amplitude setting between SIG_OUT black and white levels
Brightness control : Offset adjustment from the SIG_OUT signal center voltage
VCOM control : VCOM voltage setting
SID control A : Precharge signal voltage setting A
SID control B : Precharge signal voltage setting B

Note) Always write “0” to the blanks.
Do not write addresses after OB.

Description of Operation

The flow of internal operations is described below.
The digital signals input to DA (B)_IN0 to DA (B)_IN11 are internally demultiplexed into 12 parallel, and then data processed according to the various mode settings. After that, the signals are D/A converted into analog signals for each channel, amplified at the rear end, and output.

The output level relative to the digital input changes according to the following settings.
A: Register Gain control setting
B: Register Brightness control setting
C: SIG_C voltage



◆ Signal center voltage adjustment (C)

The SIG_C voltage is determined by the register setting SIG center.
The signal center voltage can be adjusted in 35mV/LSB steps from 00h: 6.5V to 3Fh: 8.5V.

◆ Offset adjustment relative to the signal center voltage (B)

The output voltage at digital input FFFh is determined by the SIG_C voltage and the register setting Brightness control.
The offset relative to the SIG_C voltage can be adjusted in 4mV/LSB steps from 00h: SIG_C ± 0.2V to FFh: SIG_C ± 1V.

◆ Black-white amplitude gain adjustment (A)

The black-white voltage amplitude when the digital input is varied from 000h to FFFh is determined by the register setting Gain control in the condition with the FFFh level fixed.
The gain relative to the SIG_C voltage can be adjusted in 16mV/LSB steps from 00h: SIG_C ± 2V to FFh: SIG_C ± 5.5V.

Other settings are as follows.

1. Digital Block

The CXA7009R can be set to parallel mode, single mode, right/left inversion, etc. This makes it possible to support various systems.

2. Timing Generator (TG) Block

The internal timing generator operates by the clock input, horizontal sync signal input (PRG), LCD panel AC drive inversion timing input (FRP), and the register settings, and generates the timing signals needed by the digital block. The various mode settings can be designated by the registers and the external pins.

The various operating modes that can be set by the timing generator block are described below.

◆ Operating mode setting <SLSD>

Single mode can be set by setting the Mode setting: SLSD to Low level, or parallel mode can be set by setting SLSD to High level. In single mode, the A port data only is expanded to 12 parallel. In parallel mode, the A port and B port data are expanded to odd output and even output with 6 parallel each. In addition, the output order switches between ascending order and descending order according to the right/left inversion control signal, the DIRC pin (Pin 7) and the register setting DIRCR to support the right/left inversion mode of the LCD panel.
Fix the B port inputs (DB_IN0 to DB_IN11) to GND in single mode.

	DIRC ex-or DIRCR: H	DIRC ex-or DIRCR: L
SLSD: L	SIG_OUT1: A1, SIG_OUT2: A2, SIG_OUT3: A3, SIG_OUT4: A4, SIG_OUT5: A5, SIG_OUT6: A6, SIG_OUT7: A7, SIG_OUT8: A8, SIG_OUT9: A9, SIG_OUT10: A10, SIG_OUT11: A11, SIG_OUT12: A12	SIG_OUT1: A12, SIG_OUT2: A11, SIG_OUT3: A10, SIG_OUT4: A9, SIG_OUT5: A8, SIG_OUT6: A7, SIG_OUT7: A6, SIG_OUT8: A5, SIG_OUT9: A4, SIG_OUT10: A3, SIG_OUT11: A2, SIG_OUT12: A1
SLSD: H	SIG_OUT1: A1, SIG_OUT2: B1, SIG_OUT3: A2, SIG_OUT4: B2, SIG_OUT5: A3, SIG_OUT6: B3, SIG_OUT7: A4, SIG_OUT8: B4, SIG_OUT9: A5, SIG_OUT10: B5, SIG_OUT11: A6, SIG_OUT12: B6	SIG_OUT1: A6, SIG_OUT2: B6, SIG_OUT3: A5, SIG_OUT4: B5, SIG_OUT5: A4, SIG_OUT6: B4, SIG_OUT7: A3, SIG_OUT8: B3, SIG_OUT9: A2, SIG_OUT10: B2, SIG_OUT11: A1, SIG_OUT12: B1

◆ Clock polarity setting <CKPOL>

The polarity of the internal circuit operation clock (MCLK) is determined by the Mode setting: CKPOL. The internal circuits operate at reverse polarity from CLK when CKPOL is High, and at the same polarity as CLK when CKPOL is Low. Normally set Low.

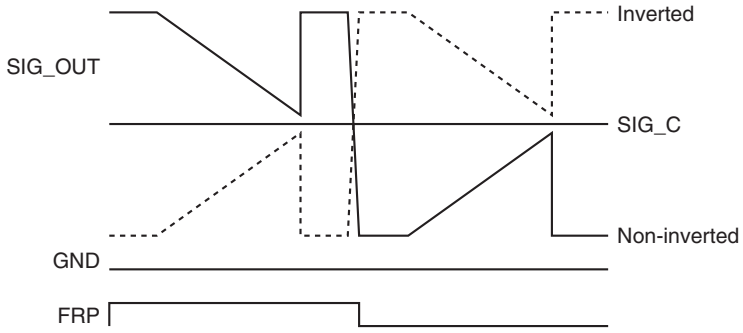
◆ SIG_OUT output delay setting <OUTDLY>

OUTDLY sets analog delay of SIG_OUT1 to SIG_OUT12.
The delay function is OFF when OUTDLY is High or ON when OUTDLY is Low, and SIG_OUT1 to SIG_OUT12 output are delayed compared to when OUTDLY = High.

◆ LCD panel AC drive inversion timing setting <FRINV>

Output polarity inversion/non-inversion relative to the signal center voltage is set by the FRP input and the register bit FRINV (1 bit). When set to the combinations shown in the table below, SIG_OUT is output non-inverted (solid line) when FRINV = Low or inverted (dotted line) when FRINV = High relative to FRP.

	FRINV: H	FRINV: L
FRP: H	Non-inverted	Inverted
FRP: L	Inverted	Non-inverted



◆ Offset calibration system

The CXA7009R is equipped with a calibration system for reducing the deviation between SIG_OUT output channels. This system automatically adjusts the output level so that the deviation between channels is constantly minimized.
This system operates to correct the channel fluctuation after IC mounting or due to the temperature characteristics or other factors so that the deviation between channels is constantly minimized.
The signals and settings related to this operation are as follows.

VD pulse : This is the external pin that inputs the trigger pulse for performing the offset calibration operation. Input a pulse with a width of 24 CLK or more during the V blanking period.

CALON : This is the calibration function ON/OFF setting. When this register is set High, the calibration function operates.

CALMD : This is the calibration mode setting. When this register is set High while CALON is High, the calibration function is forcibly applied continuously regardless of VD and the other register settings. When set Low, calibration is performed during the V blanking period using the VD pulse as the trigger according to the CALN setting below.

CALN : This sets the number of channels to be calibrated at once when CALMD is set Low. When this register is set High, calibration is performed for two channels at a time. When set Low, calibration is performed one channel at a time.

CALP : This is the calibration start position adjustment function. The calibration start position relative to the externally input VD can be adjusted in 1H units by 4 bits.

CALL : This is the calibration level setting. The offset calibration operation is performed at the level set by this register, and operation is performed to minimize the deviation between channels at that level. Set to the position with the highest optical response sensitivity relative to the LCD panel voltage.

M/S : When using two or more CXA7009Rs with one panel, this sets the main and sub ICs in order to interlock the offset cancel timing between multiple ICs. When this register is set High, that IC becomes the main IC and the sync pulse is output from the RET pin (Pin 6). When set Low for the remaining ICs, those ICs become sub ICs and the RET pin functions as an input pin.
Set High when using only one CXA7009R.

◆ Description of calibration operation

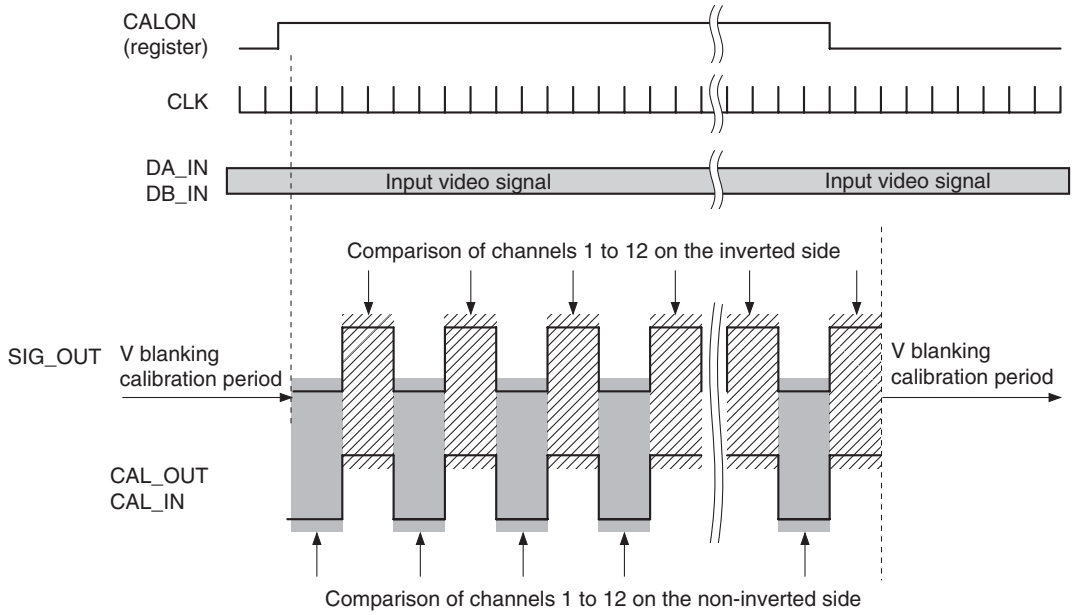
In the calibration system, feedback is applied to minimize the respective SIG_OUT1 to SIG_OUT12 offsets relative to the voltage input to CAL_IN. Operation is performed to minimize the offset between channels at the video input level set by CALL.

A video signal of the same level as the video input level set by CALL is output from CAL_OUT.
This CAL_OUT signal from the CAL_IN input is shared by multiple ICs. During the calibration period, this CALL equivalent level signal is inserted to the video signal inside the IC, and the size relationship between this output and the CAL_IN input is detected. This operation is repeated on the inverted side and the non-inverted side, and the gain and offset are adjusted by the fine-adjustment DAC (internal) for each channel based on these results.

In continuous calibration mode, the above calibration operation is repeated continuously while CALON is High. After power-on, initialize the registers and then perform continuous calibration operation for 3 seconds or more. Note that the offset cancel function may not be reflected properly when initialization and continuous calibration are not performed.

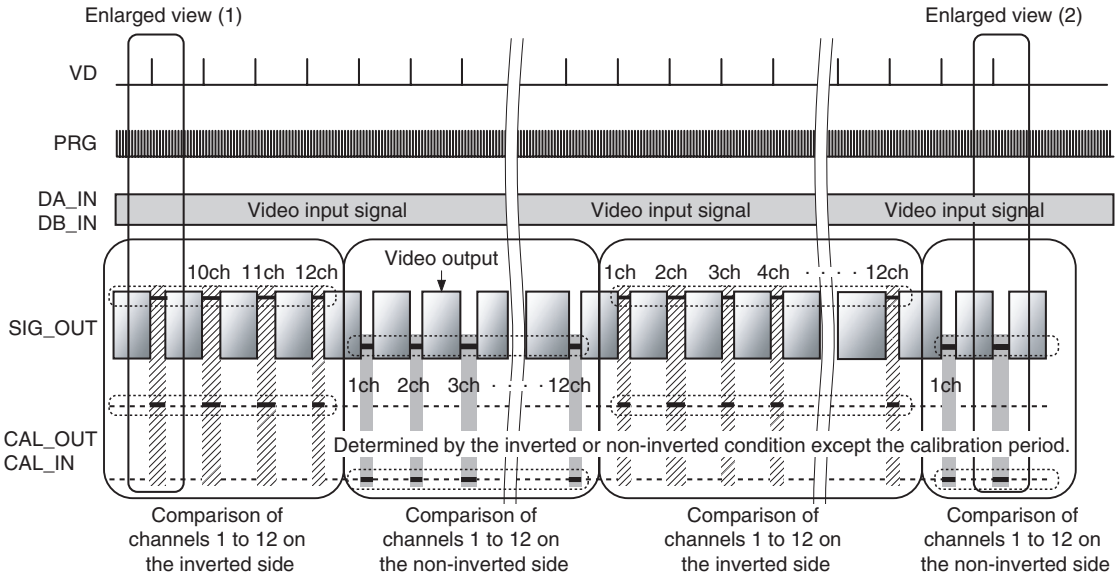
◆ Calibration timing charts

Continuous calibration mode

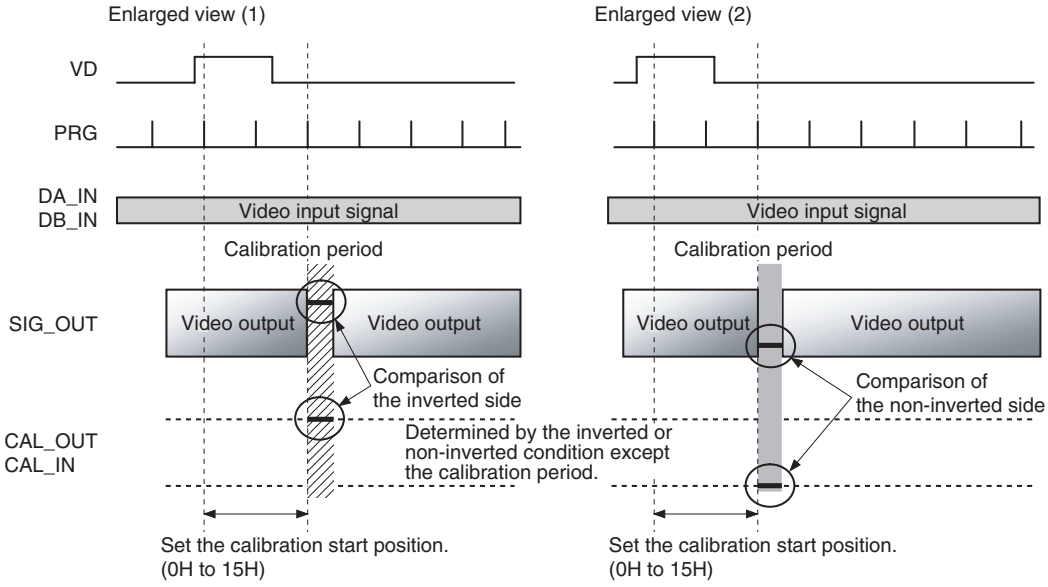


Note) CALON should be set High to validate the V blanking calibration period.

V blanking calibration mode

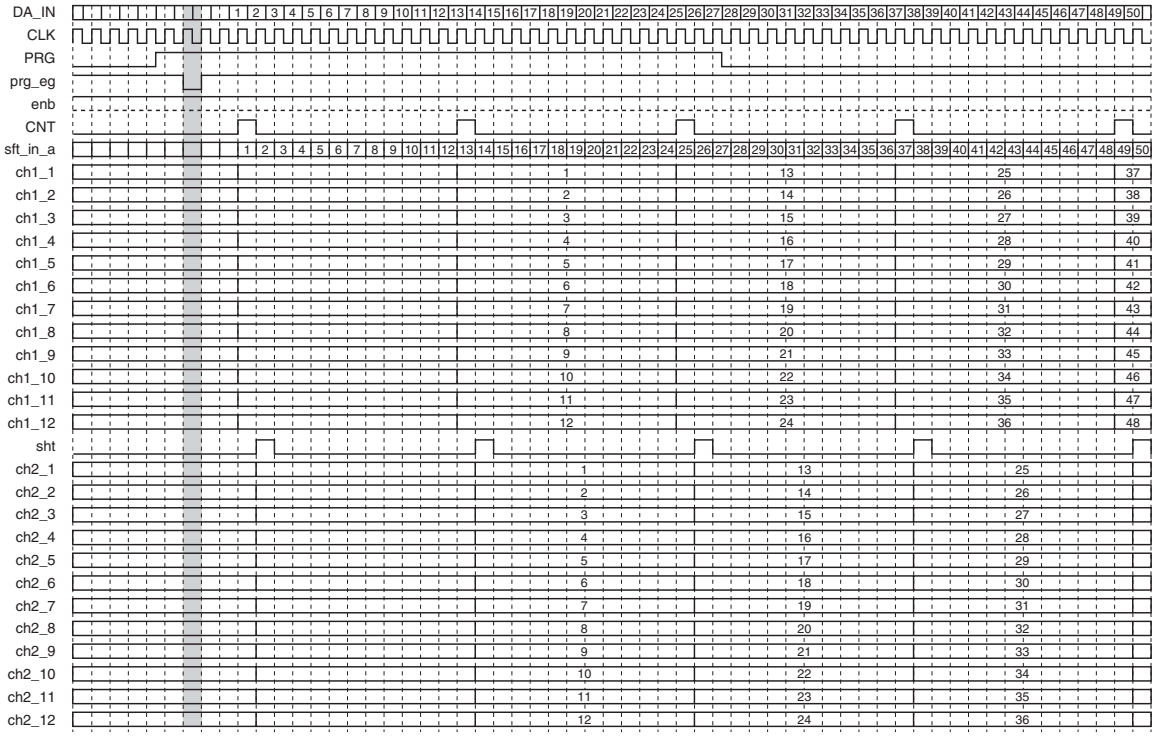


V blanking calibration mode (Enlarged view)

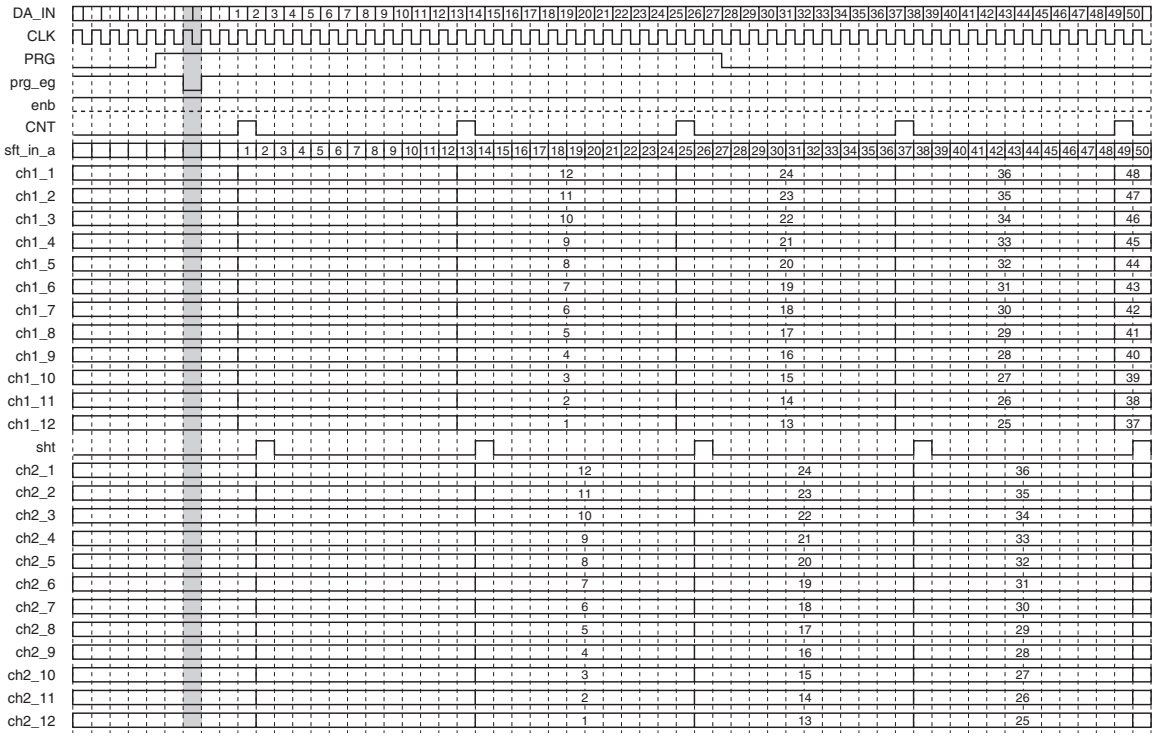


Input PRG during VD High period to perform the calibration normally.
And it means the start of the V blanking calibration.
The calibration start position can be delayed by 0H to 15H from the first rising edge of PRG during VD High period by changing CALP from 0h to Fh.

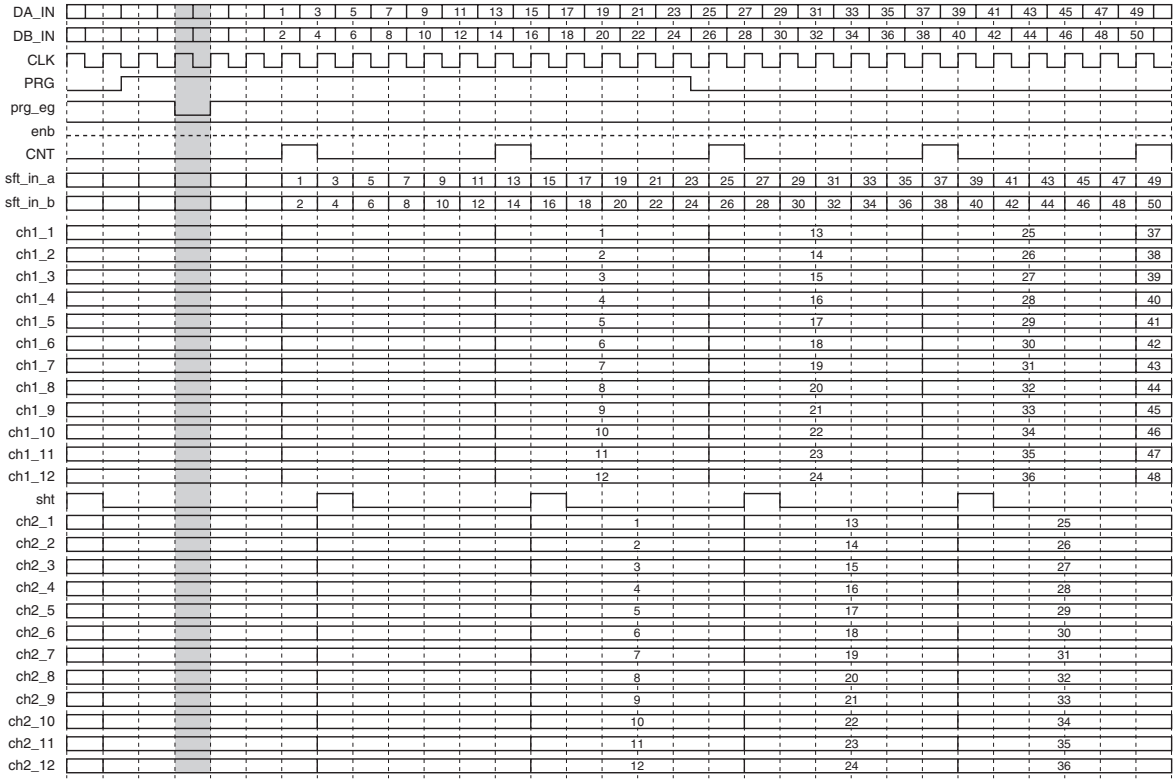
SLSD: L
DIRC ex-or DIRCR: H



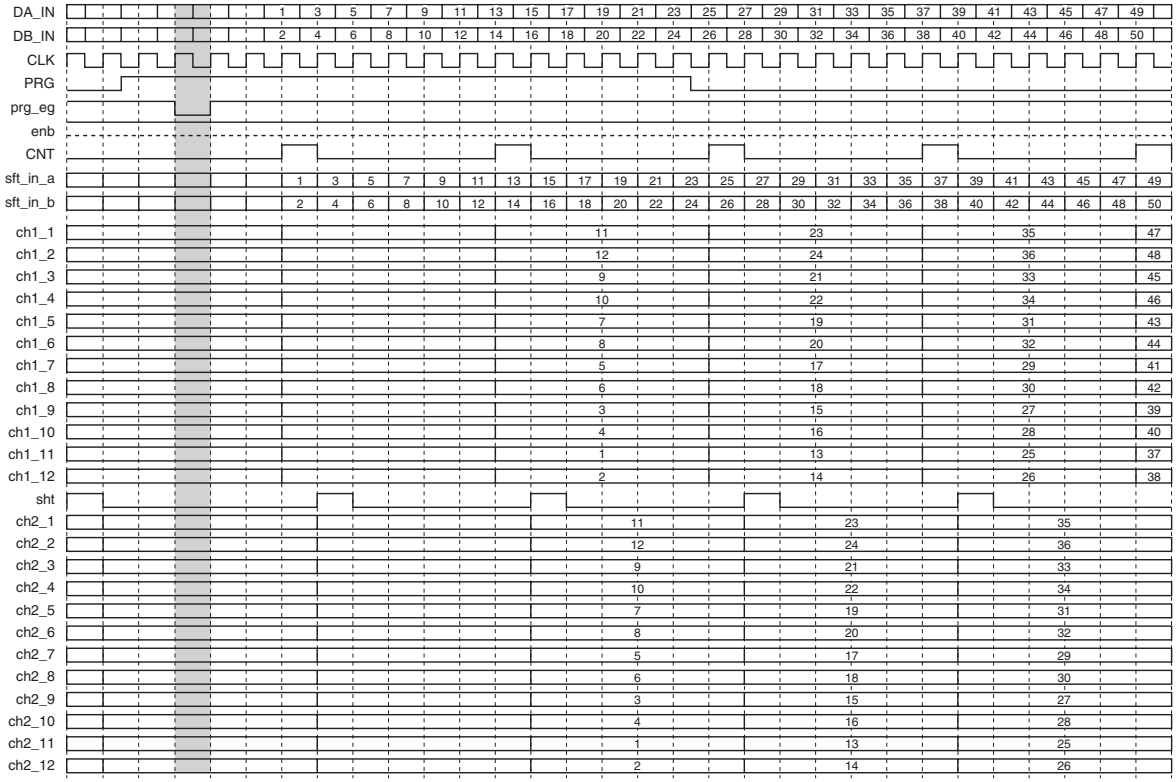
SLSD: L
DIRC ex-or DIRCR: L



SLSD: H
DIRC ex-or DIRCR: H



SLSD:
H DIRC ex-or DIRCR: L



3. SID Signal Generator Block

This circuit generates the precharge signal waveform used by the LCD panel.

The SID_OUT output level 1-step/2-step switching function is set by the Mode setting: SIDON.

When SIDON is Low level, 1-step precharge mode results, and operations (1) and (2) can be switched by ALON[1:0]. Operation (1) results when ALON[1:0] is set to any of “0h”, “1h” or “2h”, and operation (2) results when ALON[1:0] is set to “3h”.
The inverted side level is adjusted by the register setting: SID control A, and the non-inverted side level is adjusted by the register setting: SID control B.
During operation (1), SID_OUT is output in-phase with the SIG_OUT output. That is to say, when SIG_OUT is non-inverted, SID_OUT is also non-inverted output, and when SIG_OUT is inverted, SID_OUT is also inverted output.
During operation (2), SID_OUT is output at the reverse phase of the SIG_OUT output. That is to say, when SIG_OUT is non-inverted, SID_OUT is inverted output, and when SIG_OUT is inverted, SID_OUT is non-inverted output.

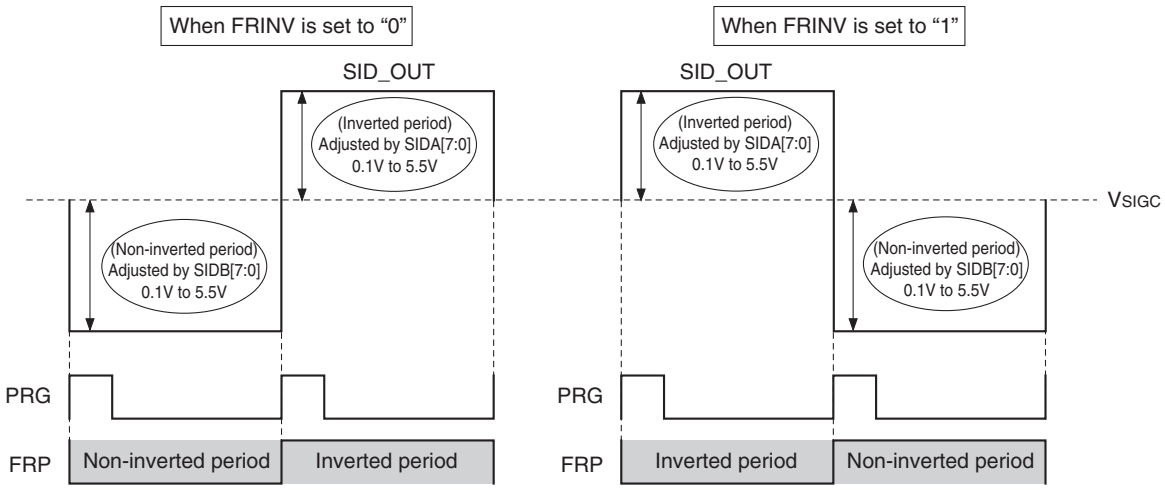
In addition, when SIDON is High level, 2-step precharge mode results, and operations (3), (4) and (5) can be switched by ALON[1:0].
When the register setting ALON[1:0] is set to “0h”, operation (3) results. In this mode the level during the PRG pulse High period is adjusted by the register setting: SID control A, and the level during the PRG pulse Low period is adjusted by the register setting: SID control B.
When the register setting ALON[1:0] is set to “1h”, operation (4) results. In this mode the level during the PRG pulse High period is output on the non-inverted side regardless of the FRP polarity.
When the register setting ALON[1:0] is set to “2h” or “3h”, operation (5) results. In this mode when PRG is High during the inverted period, the SIDB[7:0] value is output instead of the SIDA[7:0] value.

Each SID control setting can be adjusted in approximately 25mV/LSB steps from 00h: SIG_C $\pm$ 5.5V to FFh: SIG_C $\pm$ 0.1V. In addition, SID_OUT cannot directly drive the precharge signal input of an LCD panel when a load of 1nF or more. In this case connect SID_OUT via a buffer with sufficient current supply capacity.

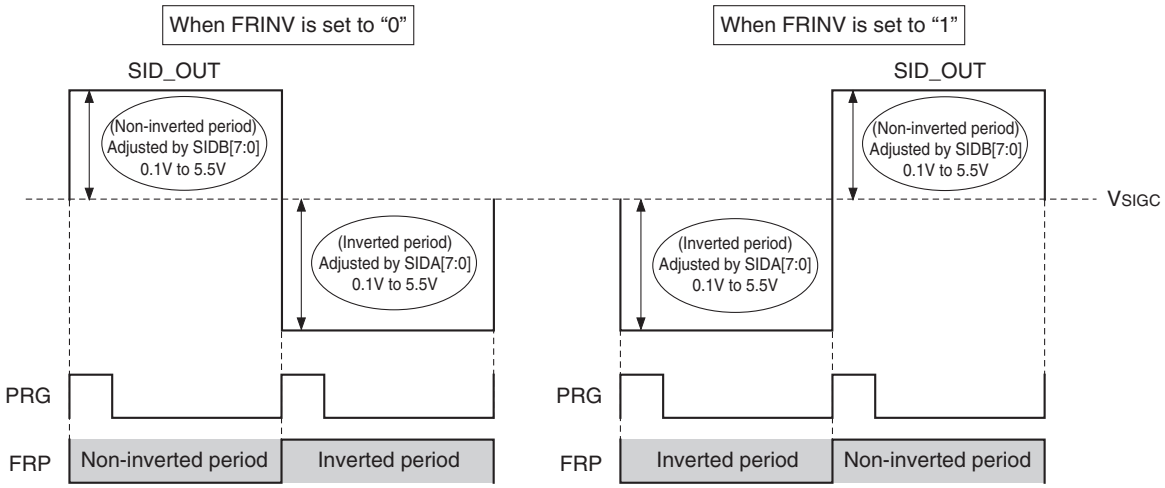
◆ **List of precharge settings (Difference between the CXA7009R and CXA7007R settings)**

	CXA7009R		CXA7007R	
	SIDON	ALON[1:0]	SIDON	ALON
Precharge operation (1)	L	0h/1h/2h	L	L
Precharge operation (2)	L	3h	No mode setting	
Precharge operation (3)	H	0h	H	L
Precharge operation (4)	H	1h	H	H
Precharge operation (5)	H	2h/3h	No mode setting	

◆ **Precharge operation (1) (SIDON = 0 and ALON[1:0] = 0h/1h/2h)**

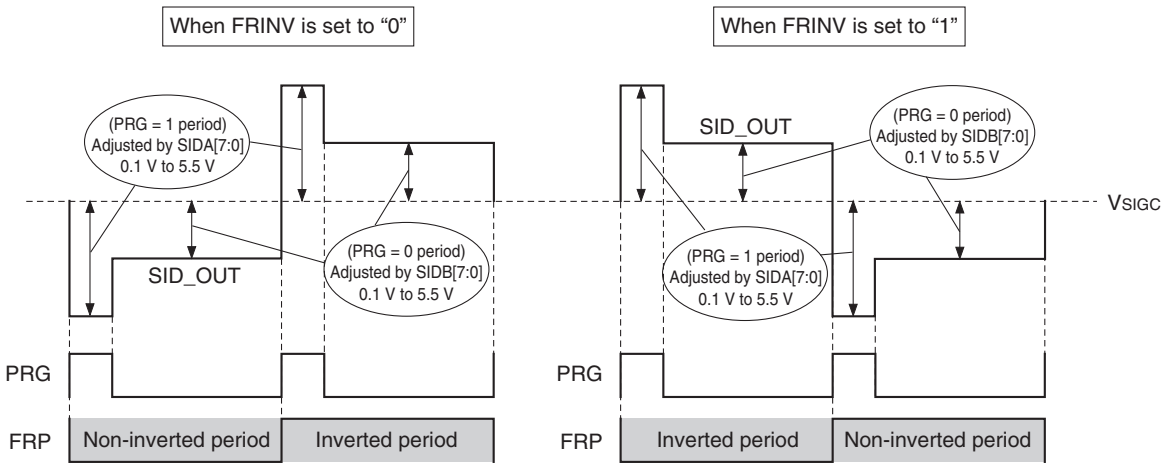


◆ **Precharge operation (2) (SIDON = 0 and ALON[1:0] = 3h)**

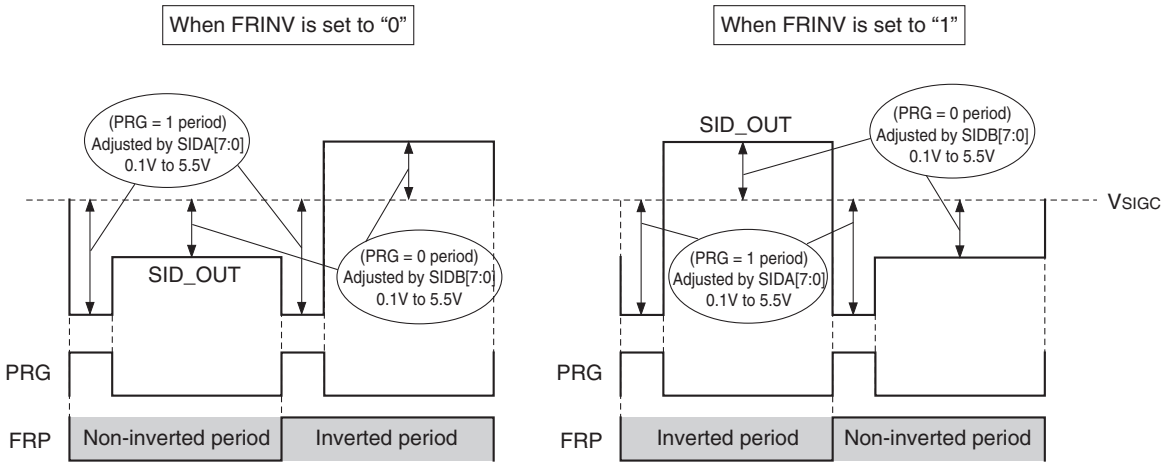


Note) Precharge operation (2) outputs the inverted waveform of precharge operation (1) on the SID_OUT output. At this time only the SID_OUT output is inverted, and the SIG_OUT output polarity is unaffected.

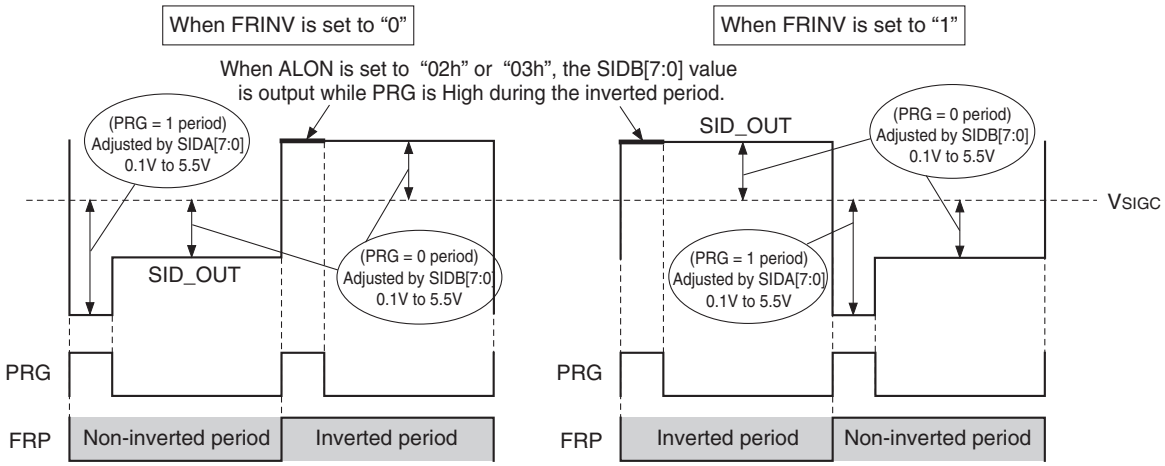
◆ **Precharge operation (3) (SIDON = 1 and ALON[1:0] = 0h)**



◆ **Precharge operation (4) (SIDON = 1 and ALON[1:0] = 1h)**



◆ **Precharge operation (5) (SIDON = 1 and ALON[1:0] = 2h/3h)**



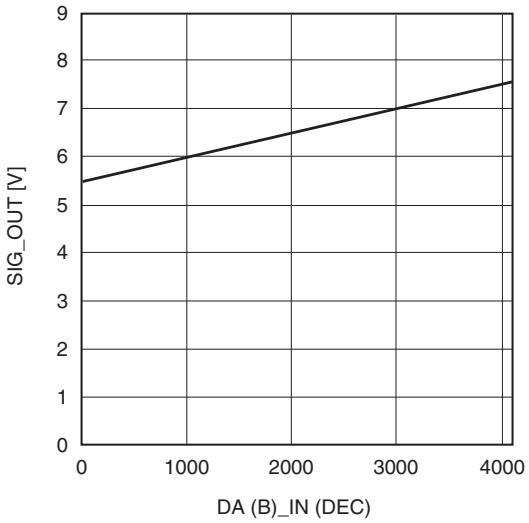
4. VCOM Voltage Generation Block

This block sets the DC common potential for the LCD panel.
The offset from the SIG_OUT center voltage can be adjusted by the register setting: VCOM control.
Adjustment is possible in 17.5mV/LSB steps from 00h: SIG_C – 2V to 7Fh: SIG_C – 0.1V.

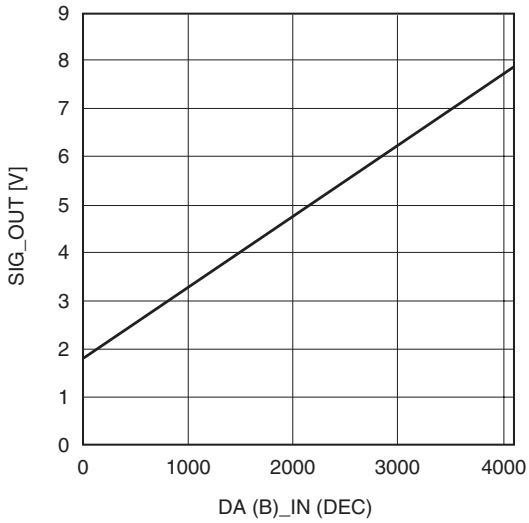
Example of Representative Characteristics

(V_{CC} = 15.5V, V_{DD} = 3.3V, Ta = 25°C)

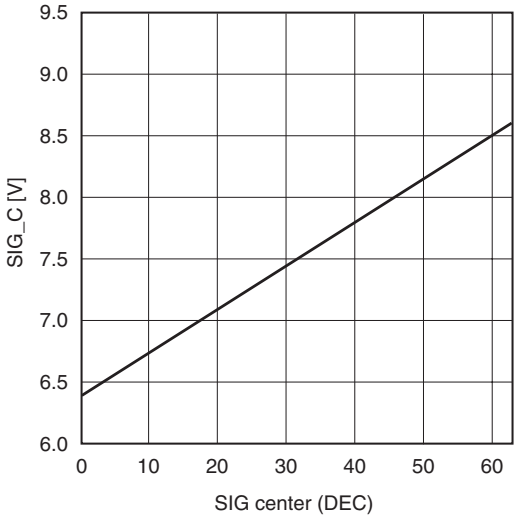
SIG_OUT characteristics (Gain control: 00h)



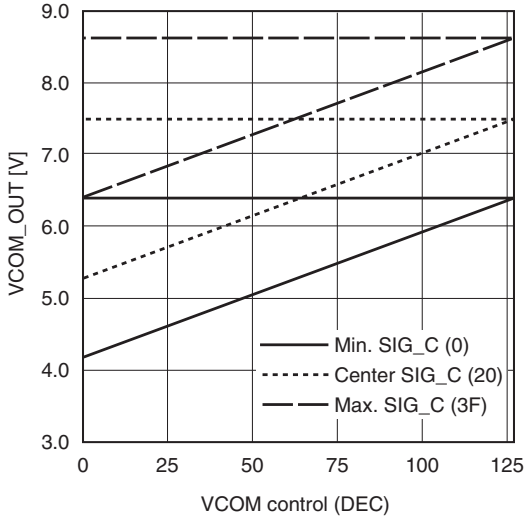
SIG_OUT characteristics (Gain control: FFh)



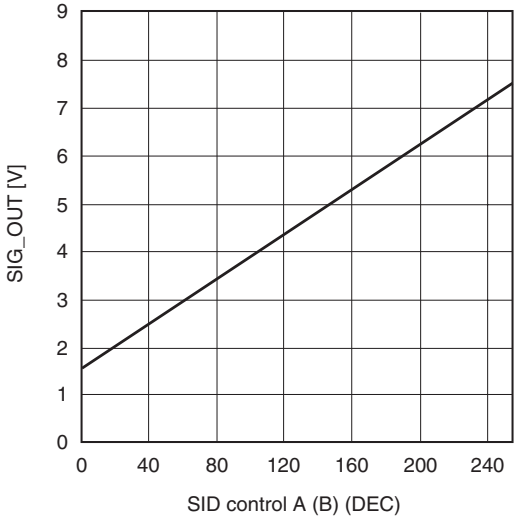
SIG center voltage



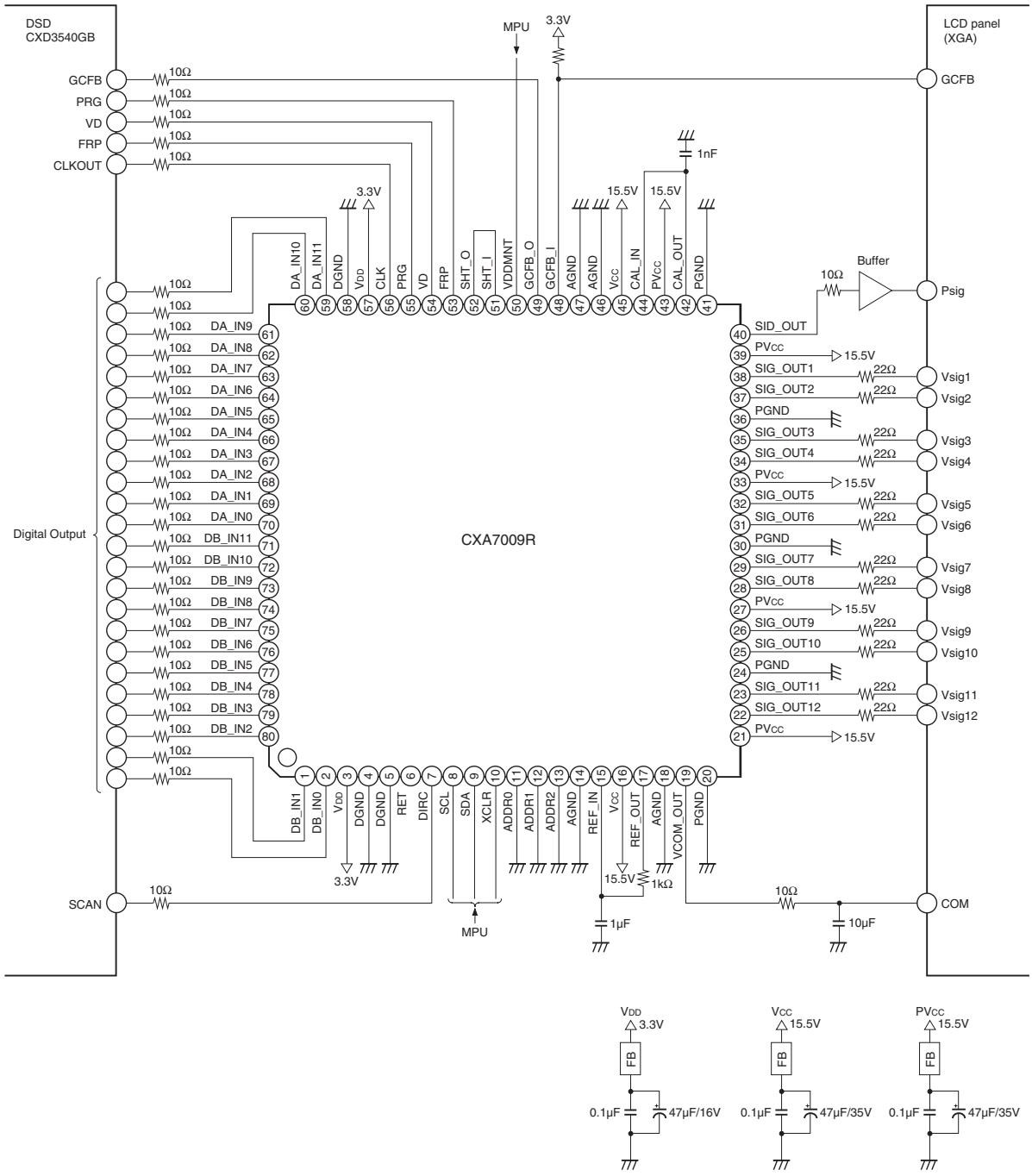
SIG_VCOM voltage



SID_OUT characteristics

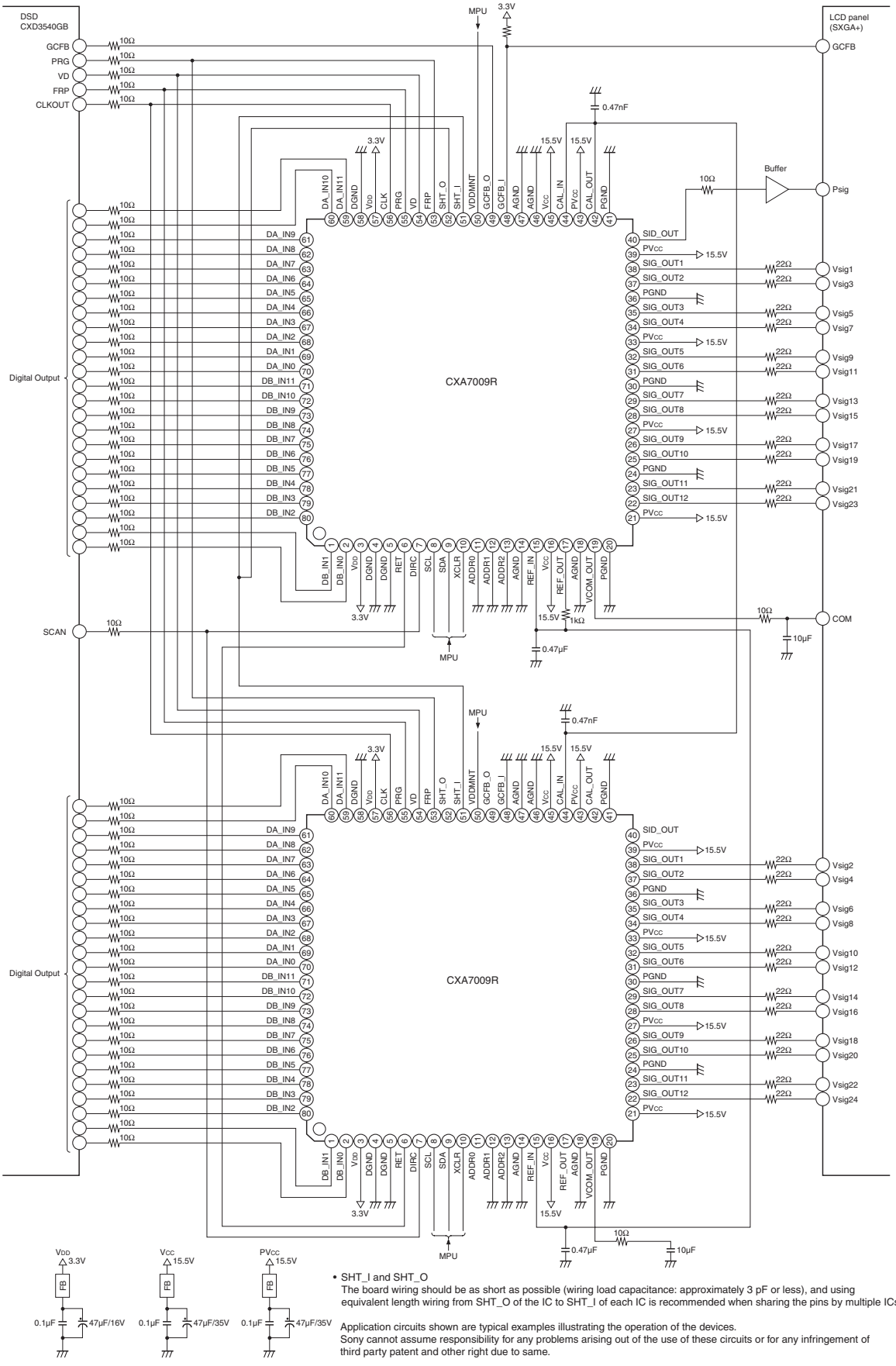


Application Circuit 1 – Application Circuit to XGA Panel



Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 – Application Circuit to SXGA+ Panel



• SHT_I and SHT_O
The board wiring should be as short as possible (wiring load capacitance: approximately 3 pF or less), and using equivalent length wiring from SHT_O of the IC to SHT_I of each IC is recommended when sharing the pins by multiple ICs.

Application circuits shown are typical examples illustrating the operation of the devices.
Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Board Design

The CXA7009R consumes a large current to drive the LCD panel load at high speed. Therefore, the structure emits heat from the PGND pin to the board in order to suppress the temperature rise due to heat generation. When designing the board, take the following points into account and provide the highest heat radiation effects possible.

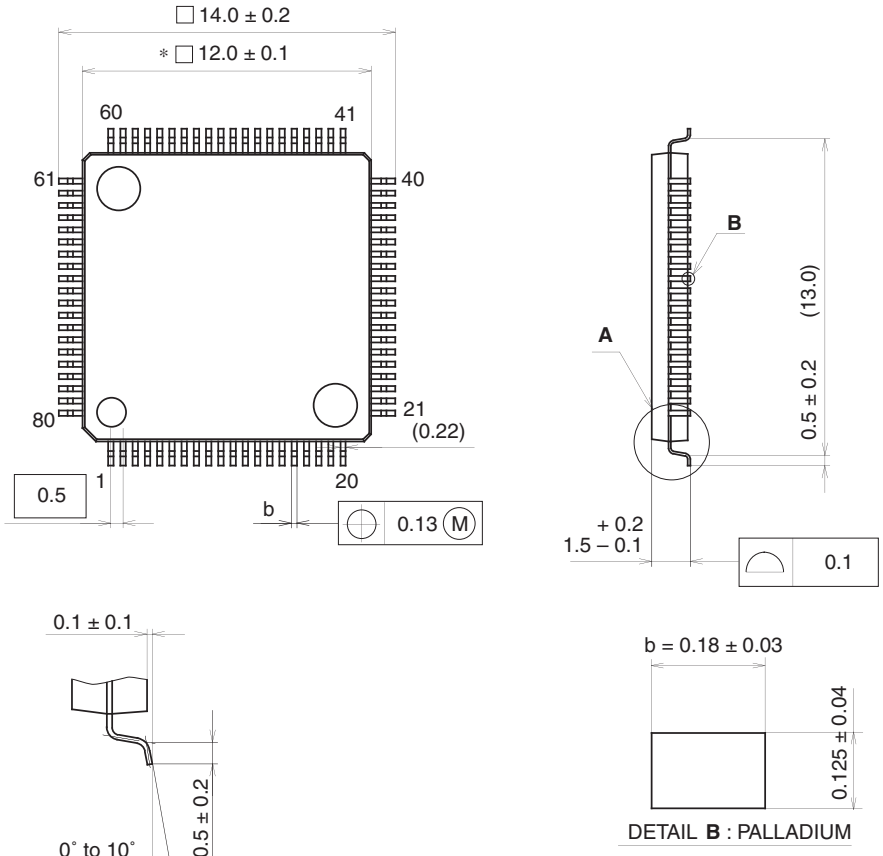
- ◆ Provide the widest GND possible on the IC rear surface pattern, and connect to the inner layer GND using through the via.
- ◆ PGND also functions as a thermal radiation pin. Connect PGND to the surface layer GND with the thickest wiring possible, and also connect to the GND pattern below the IC.
- ◆ Heat escapes to the board GND, so heat radiation effects may not be obtained when the board itself has heat. Avoid locating heat sources around this IC as much as possible.

In addition, connect each power supply pin to GND through a 0.1μF ceramic capacitor located on the pin side. When whiskers synchronized with the parallel expansion pulses appear in the output, connect a 1000 to 2000pF capacitor in parallel with the 0.1μF capacitor. (Recommended)

Package Outline

(Unit: mm)

80PIN LQFP (PLASTIC)



DETAIL **B** : PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

SONY CODE	LQFP-80P-L01
EIAJ CODE	P-LQFP80-12x12-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g