DS14C88 Quad CMOS Line Driver

Check for Samples: DS14C88

FEATURES

- **Meets EIA-232D and CCITT V.28 Standards**
- **LOW Power Consumption**
- **Wide Power Supply Range: ±5V to ±12V**
- **Available in SOIC Package**

DESCRIPTION

The DS14C88, pin-for-pin compatible to the DS1488/MC1488, is a quad line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device translates standard TTL/CMOS logic levels to levels conforming to EIA-232-D and CCITT V.28 standards.

The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to its bipolar equivalents: 500 µA (DS14C88) versus 25 mA (DS1488).

The DS14C88 simplifies designs by eliminating the need for external slew rate control capacitors. Slew rate control in accordance with EIA-232D is provided on-chip, eliminating the output capacitors.

Connection Diagram

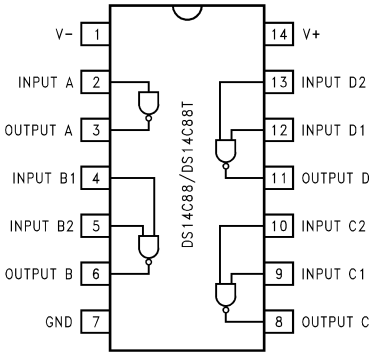


Figure 1. SOIC or PDIP Package- Top View
See Package Number NFF0014A or D0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2][3][4]

Supply Voltage	
V^+ Pin	+13V
V^- Pin	−13V
Driver Input Voltage	(V^+) +0.3V to GND −0.3V
Driver Output Voltage	$\lvert(V^+) - V_O\rvert \le 30V$
	$\lvert(V^-) - V_O\rvert \le 30V$
Continuous Power Dissipation @+25°C[5]	
NFF0014A Package	1513 mW
D0014A Package	1063 mW
Junction Temperature	+150°C
Lead Temperature (Soldering 4 seconds)	+260°C
Storage Temperature Range	−65°C to +150°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be Ensured. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) This Product does not meet 2000V ESD rating.
(4) ESD Rating (HBM, 1.5 kΩ, 100 pF) ≥ 1.0 kV.
(5) Derate NFF0014A Package 12.1 mW/°C, and D0014A Package 8.5 mW/°C above +25°C.

Recommended Operating Conditions

	Min	Max	Units
V^+ Supply (GND = 0V)	+4.5	+12.6	V
V^- Supply (GND = 0V)	−4.5	−12.6	V
Operating Free Air Temp. (T_A)			
DS14C88	0	+75	°C

Electrical Characteristics

Over Recommended Operating Conditions, unless otherwise specified

Parameter		Test Conditions		Min	Typ	Max	Units
I_{IL}	Maximum Low Input Current	V_{IN} = GND				+10	µA
I_{IH}	Maximum High Input Current	$V_{IN} = V^+$		−10			µA
V_{IL}	Low Level Input Voltage	$V^+ \ge +7V$, $V^- \le -7V$		GND		0.8	V
		$V^+ < +7V$, $V^- > -7V$		GND		0.6	V
V_{IH}	High Level Input Voltage			2.0		V^+	V
V_{OL}	Low Level Output Level	$V_{IN} = V_{IH}$, R_L = 3 kΩ or 7 kΩ	V^+ = 4.5V, V^- = −4.5V		−4.0	−3.0	V
			V^+ = 9V, V^- = 9V		−8.0	−6.5	V
			V^+ = 12V, V^- = −12V		−10.5	−9.0	V
V_{OH}	High Level Output Level	$V_{IN} = V_{IL}$, R_L = 3 kΩ or 7 kΩ	V^+ = 4.5V, V^- = −4.5V	3.0	4.0		V
			V^+ = 9V, V^- = −9V	6.5	8.0		V
			V^+ = 12V, V^- = −12V	9.0	10.5		V
I_{OS+}	High Level Output Short Circuit Current[1]	V_{IN} = 0.8V, V_O = GND	V^+ = +12V, V^- = −12V	−45			mA
I_{OS-}	Low Level Output Short Circuit Current[1]	V_{IN} = 2.0V, V_O = GND				+45	mA
R_{OUT}	Output Resistance	$V^+ = V^- = GND = 0V$, $-2V \le V_O \le +2V$[2] (Figure 2)		300			Ω

(1) I_{OS+} and I_{OS-} values are for one output at a time. If more than one output is shorted simultaneously, the device dissipation may be exceeded.
(2) Power supply (V^+, V^-) and GND pins are connected to ground for the Output Resistance Test (R_O).

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Electrical Characteristics (continued)

Over Recommended Operating Conditions, unless otherwise specified

Parameter		Test Conditions		Min	Typ	Max	Units
I_{CC+}	Positive Supply Current	$V_{IN} = V_{ILmax}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$			10	µA
			$V^+ = 9V$, $V^- = -9V$			30	µA
			$V^+ = 12V$, $V^- = -12V$			60	µA
		$V_{IN} = V_{IHmin}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$			50	µA
			$V^+ = 9V$, $V^- = -9V$			300	µA
			$V^+ = 12V$, $V^- = -12V$			500	µA
I_{CC-}	Negative Supply Current	$V_{IN} = V_{ILmax}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$			−10	µA
			$V^+ = 9V$, $V^- = -9V$			−10	µA
			$V^+ = 12V$, $V^- = -12V$			−10	µA
		$V_{IN} = V_{IHmin}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$			−30	µA
			$V^+ = 9V$, $V^- = -9V$			−30	µA
			$V^+ = 12V$, $V^- = -12V$			−60	µA

Switching Characteristics[1][2]

Over Recommended Operating Conditions, unless otheriwse specified (Figure 3, Figure 4)

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	$V^+ = +4.5V$, $V^- = -4.5V$		1.5	6.0	µs
		$V^+ = +9.0V$, $V^- = -9.0V$		1.2	5.0	µs
		$V^+ = +12V$, $V^- = -12V$		1.2	4.0	µs
t_{PHL}	Propagation Delay High to Low	$V^+ = +4.5V$, $V^- = -4.5V$		1.5	6.0	µs
		$V^+ = +9.0V$, $V^- = -9.0V$		1.35	5.0	µs
		$V^+ = +12V$, $V^- = -12V$		1.3	4.0	µs
t_r	Rise Time[3]		0.2	1.0		µs
t_f	Fall Time[3]		0.2	1.0		µs
tsk	Typical Propagation Delay Skew	$V^+ = +4.5V$, $V^- = -4.5V$		250		ns
		$V^+ = +9.0V$, $V^- = -9.0V$		200		ns
		$V^+ = +12V$, $V^- = -12V$		150		ns
S_R	Output Slew Rate[3]	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF			30	V/µs

(1) AC input test waveforms for test purposes: $t_r = t_f \leq 20$ ns, $V_{IH} = 2V$, $V_{IL} = 0.8V$ (0.6V at $V^+ = 4.5V$, $V^- = -4.5V$)
(2) Input rise and rall times must not exceed 5 µs.
(3) The output slew rate, rise time, and fall time are measured from the +3.0V to the −3.0V level on the output waveform.

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Parameter Measure Information

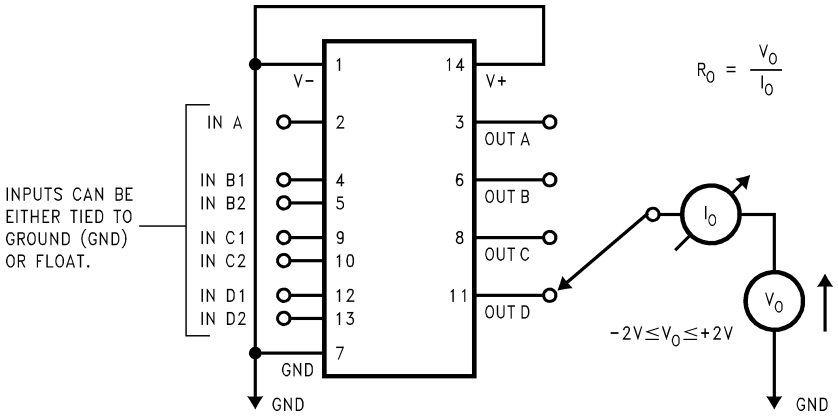


Figure 2. Output Resistance Test Circuit (Power-Off)

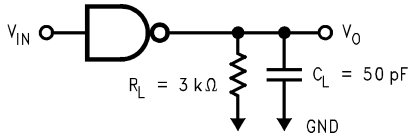


Figure 3. Driver Load Circuit(4)

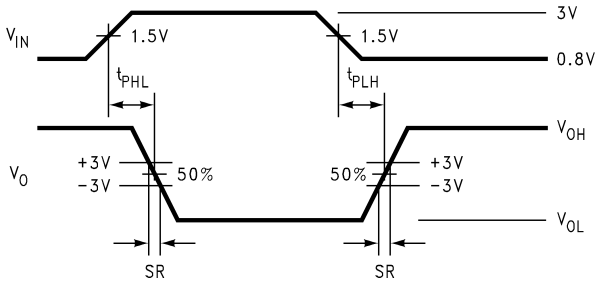


Figure 4. Driver Switching Waveform

(4) C_L include jig and probe capacitances.

TYPICAL APPLICATION INFORMATION

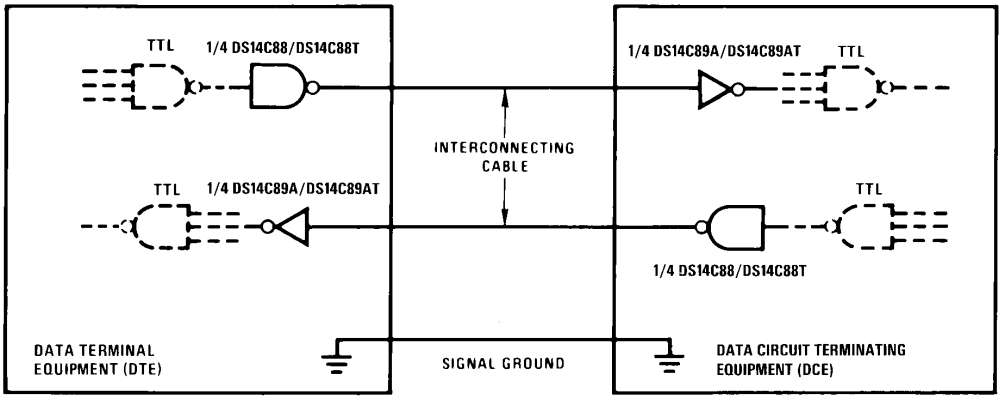


Figure 5. EIA-232D Data Transmission

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	4

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS14C88M/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M	Samples
DS14C88MX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	DS14C88M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

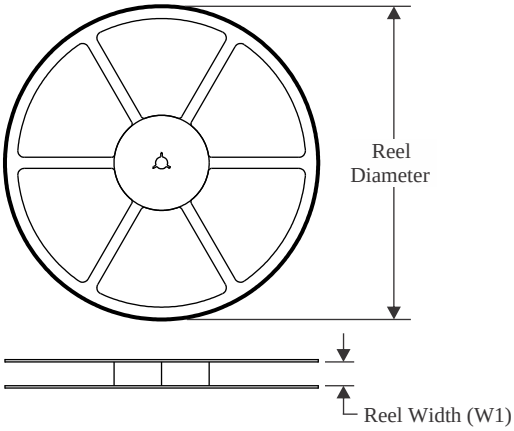
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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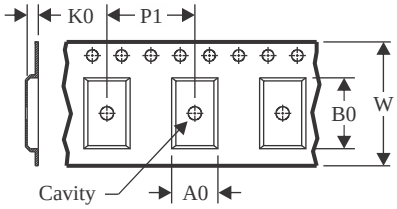
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

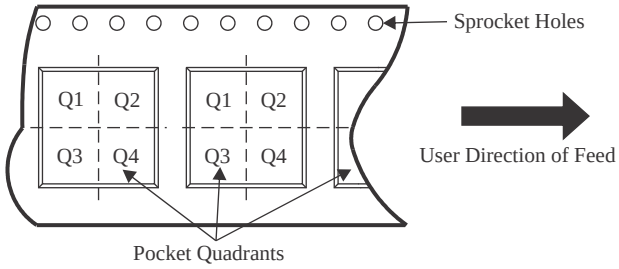


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

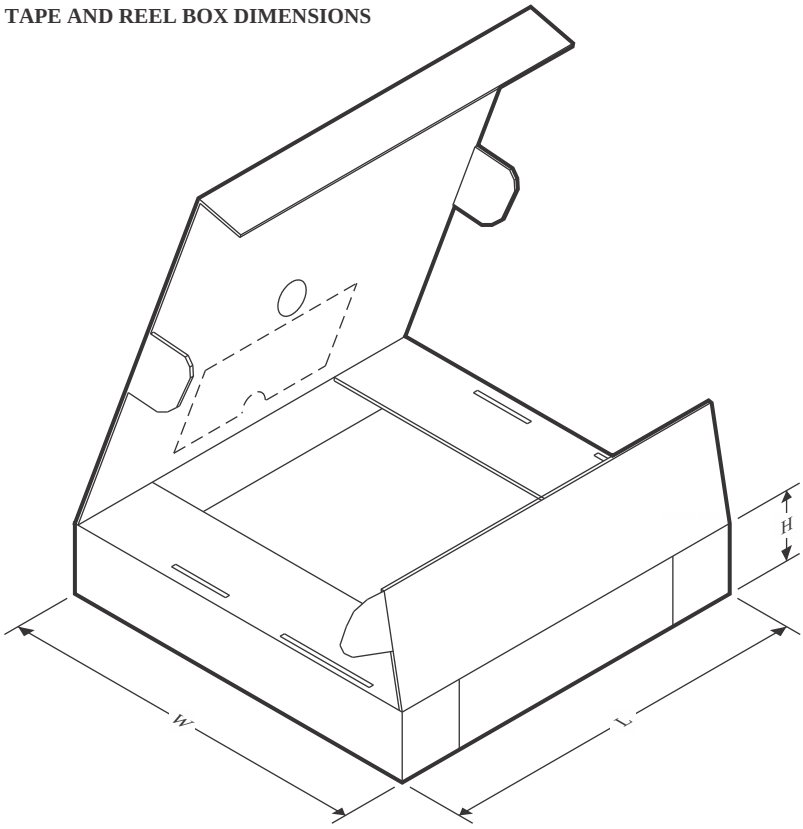
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS14C88MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

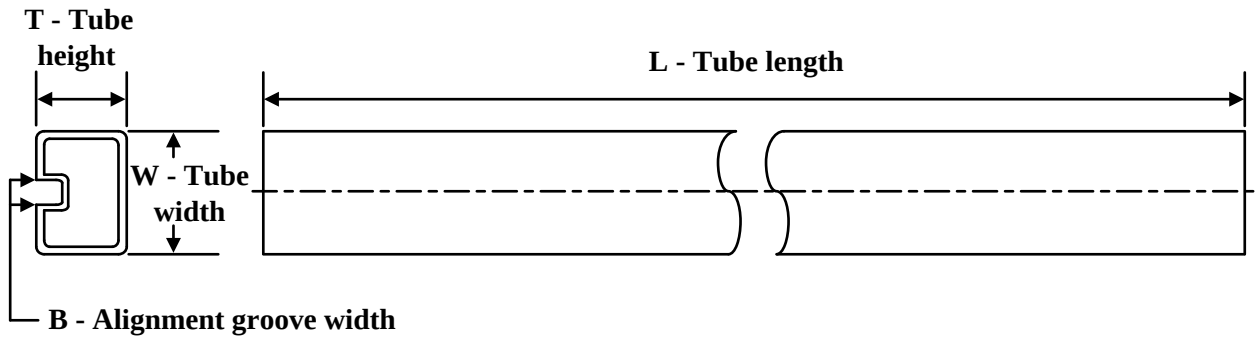
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

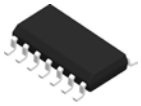
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS14C88MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS14C88M/NOPB	D	SOIC	14	55	495	8	4064	3.05

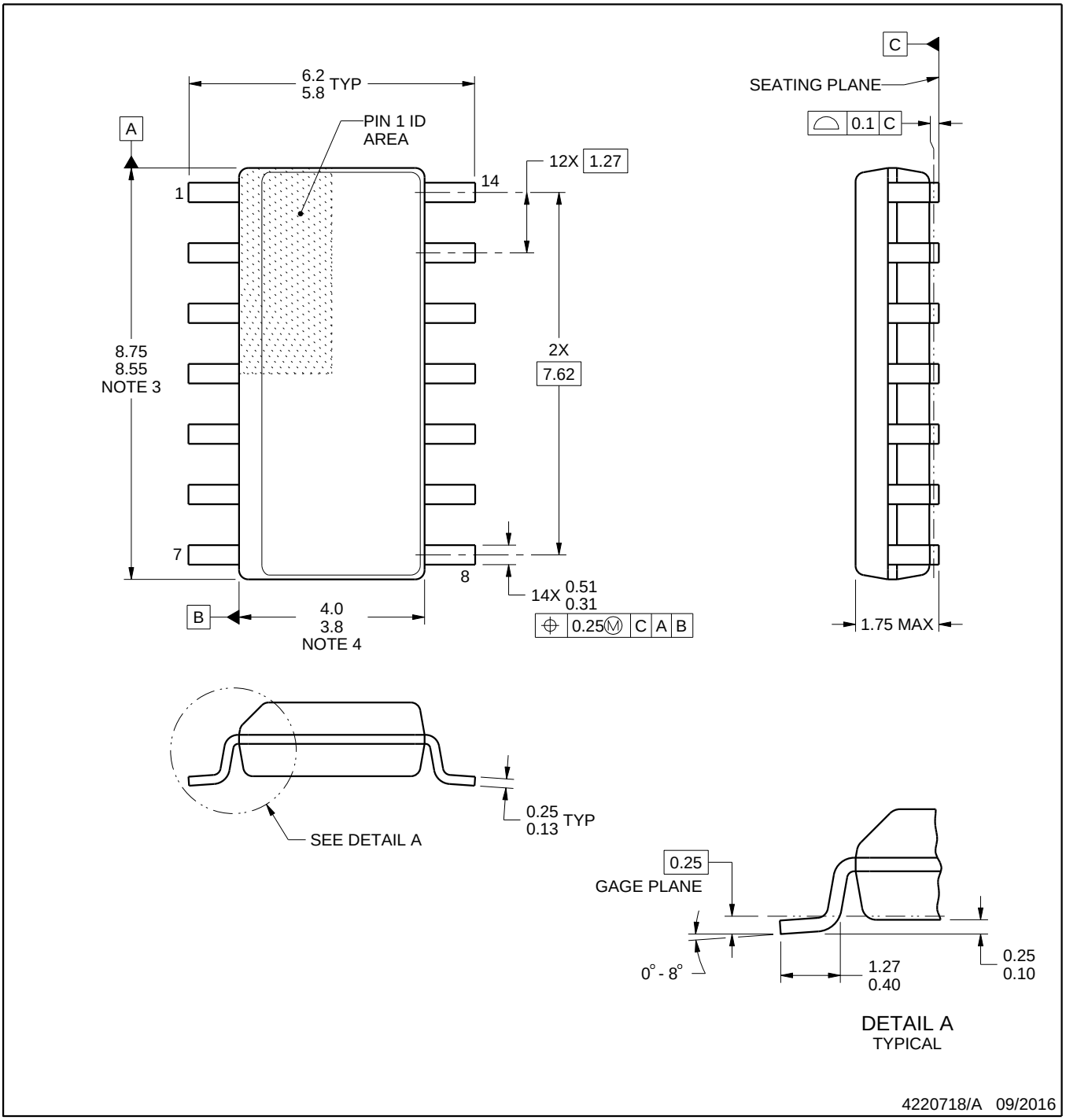


PACKAGE OUTLINE

D0014A

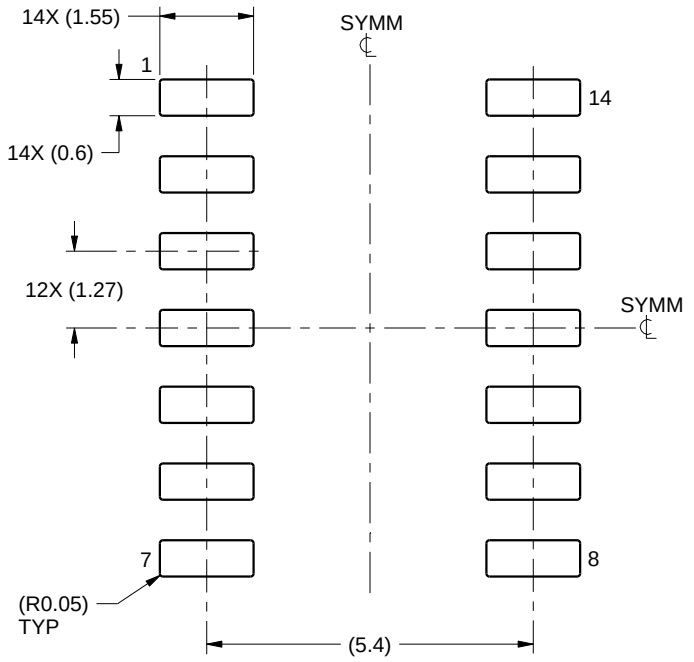
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

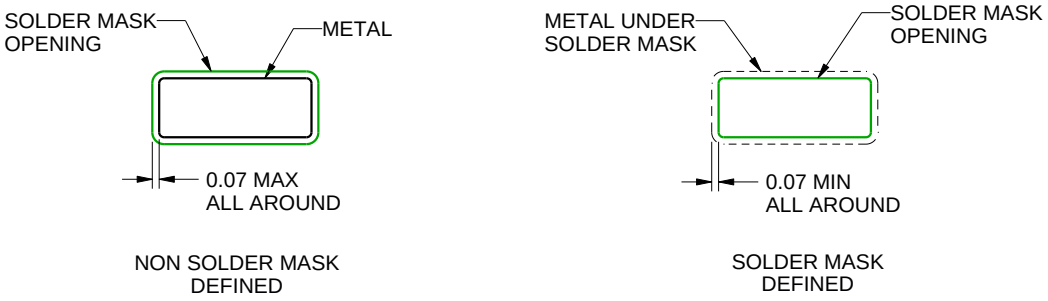


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

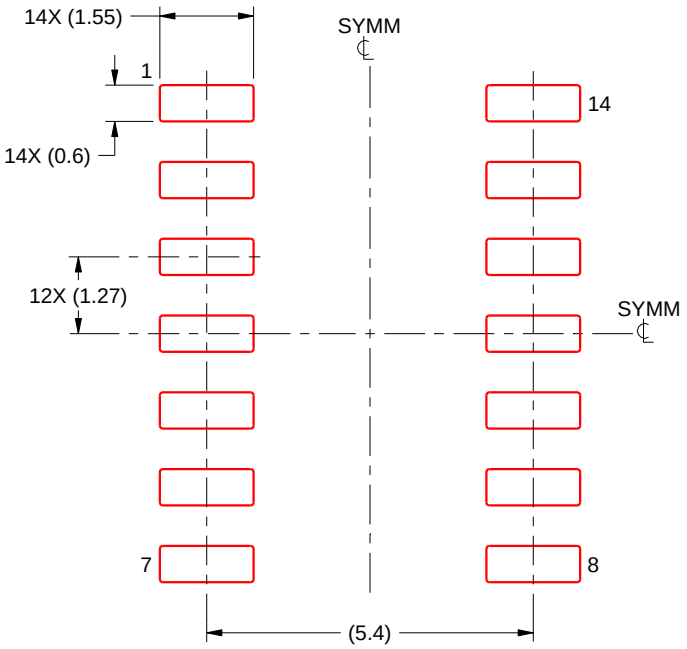
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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