



## DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

### GENERAL DESCRIPTION

The ALD1103 is a monolithic dual N-channel and dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1101 N-channel MOSFET pair and an ALD1102 P-channel MOSFET pair in one package.

The ALD1103 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1103 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1103 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is  $= 5\text{mA}/50\text{pA} = 100,000,000$ .

### FEATURES

- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low  $V_{os}$  -- 10mV
- High input impedance --  $10^{13}\Omega$  typical
- Low input and output leakage currents
- Negative current ( $I_{DS}$ ) temperature coefficient
- Enhancement mode (normally off)
- DC current gain  $10^9$
- Matched N-channel and matched P-channel in one package

### ORDERING INFORMATION

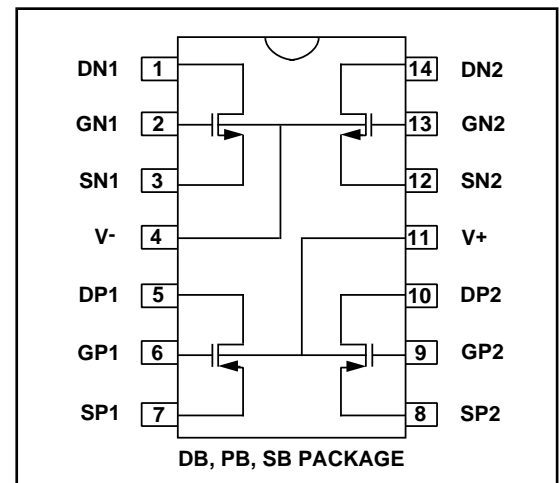
Operating Temperature Range*		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Plastic Dip Package	14-Pin SOIC Package
ALD1103 DB	ALD1103 PB	ALD1103 SB

\* Contact factory for industrial temperature range.

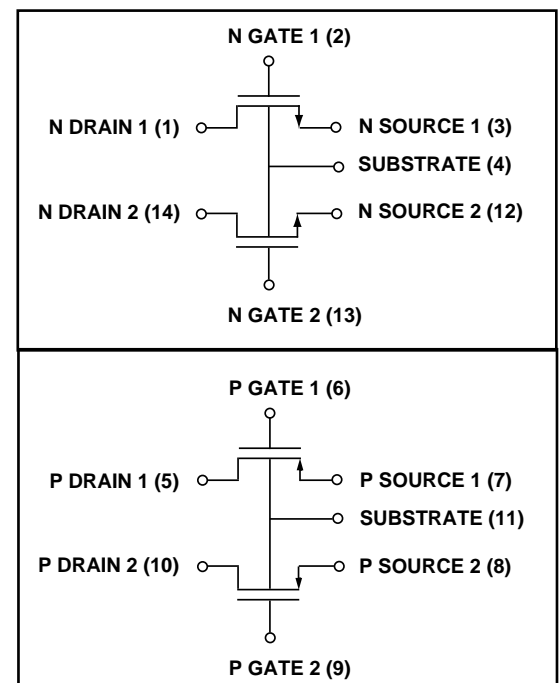
### APPLICATIONS

- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

### PIN CONFIGURATION



### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Drain-source voltage, $V_{DS}$	_____	13.2V
Gate-source voltage, $V_{GS}$	_____	13.2V
Power dissipation	_____	500 mW
Operating temperature range	PB, SB package	0°C to +70°C
	DB package	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C
Lead temperature, 10 seconds	_____	+260°C

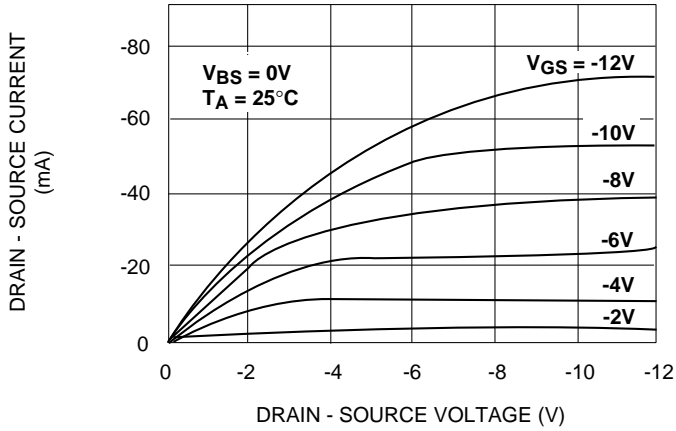
## OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$  unless otherwise specified

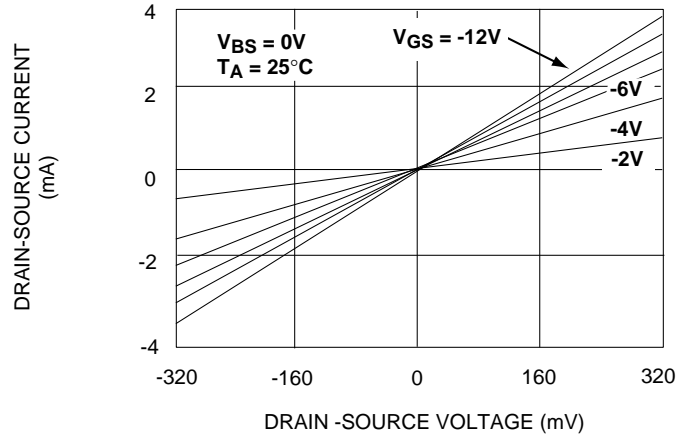
Parameter	Symbol	N - Channel			Unit	Test Conditions	P - Channel			Unit	Test Conditions
		Min	Typ	Max			Min	Typ	Max		
Gate Threshold Voltage	$V_T$	0.4	0.7	1.0	V	$I_{DS} = 10\mu\text{A}$ $V_{GS} = V_{DS}$	-0.4	-0.7	-1.2	V	$I_{DS} = -10\mu\text{A}$ $V_{GS} = V_{DS}$
Offset Voltage $V_{GS1} - V_{GS2}$	$V_{OS}$			10	mV	$I_{DS} = 100\mu\text{A}$ $V_{GS} = V_{DS}$			10	mV	$I_{DS} = -100\mu\text{A}$ $V_{GS} = V_{DS}$
Gate Threshold Temperature Drift	$TC_{VT}$		-1.2		mV/°C			-1.3		mV/°C	
On Drain Current	$I_{DS(ON)}$	25	40		mA	$V_{GS} = V_{DS} = 5V$	-8	-16		mA	$V_{GS} = V_{DS} = -5V$
Trans-. conductance	$G_{fs}$	5	10		mmho	$V_{DS} = 5V$ $I_{DS} = 10\text{mA}$	2	4		mmho	$V_{DS} = -5V$ $I_{DS} = -10\text{mA}$
Mismatch	$\Delta G_{fs}$		0.5		%			0.5		%	
Output Conductance	$G_{OS}$		200		$\mu\text{mho}$	$V_{DS} = 5V$ $I_{DS} = 10\text{mA}$		500		$\mu\text{mho}$	$V_{DS} = -5V$ $I_{DS} = -10\text{mA}$
Drain Source ON Resistance	$R_{DS(ON)}$		50	75	$\Omega$	$V_{DS} = 0.1V$ $V_{GS} = 5V$		180	270	$\Omega$	$V_{DS} = -0.1V$ $V_{GS} = -5V$
Drain Source ON Resistance Mismatch	$\Delta R_{DS(ON)}$		0.5		%	$V_{DS} = 0.1V$ $V_{GS} = 5V$		0.5		%	$V_{DS} = -0.1V$ $V_{GS} = -5V$
Drain Source Breakdown Voltage	$BV_{DSS}$	12			V	$I_{DS} = 10\mu\text{A}$ $V_{GS} = 0V$	-12			V	$I_{DS} = -10\mu\text{A}$ $V_{GS} = 0V$
Off Drain Current	$I_{DS(OFF)}$		0.1	4 4	nA $\mu\text{A}$	$V_{DS} = 12V$ $I_{GS} = 0V$ $T_A = 125^\circ\text{C}$		0.1	4 4	nA $\mu\text{A}$	$V_{DS} = -12V$ $V_{GS} = 0V$ $T_A = 125^\circ\text{C}$
Gate Leakage Current	$I_{GSS}$		1	50 10	pA nA	$V_{DS} = 0V$ $V_{GS} = 12V$ $T_A = 125^\circ\text{C}$		1	50 10	pA nA	$V_{DS} = 0V$ $V_{GS} = -12V$ $T_A = 125^\circ\text{C}$
Input Capacitance	$C_{ISS}$		6	10	pF			6	10	pF	

# P- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

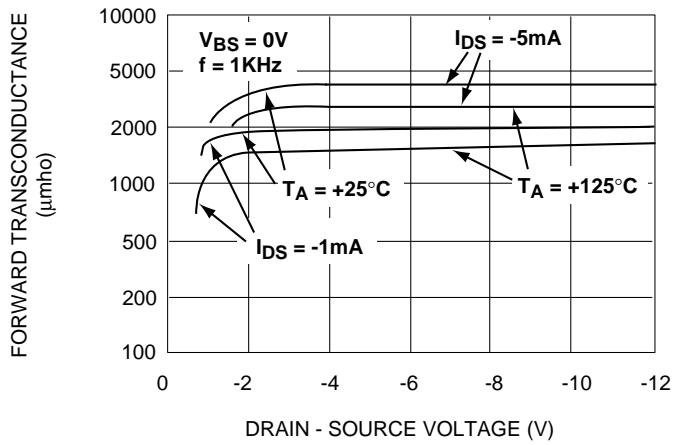
## OUTPUT CHARACTERISTICS



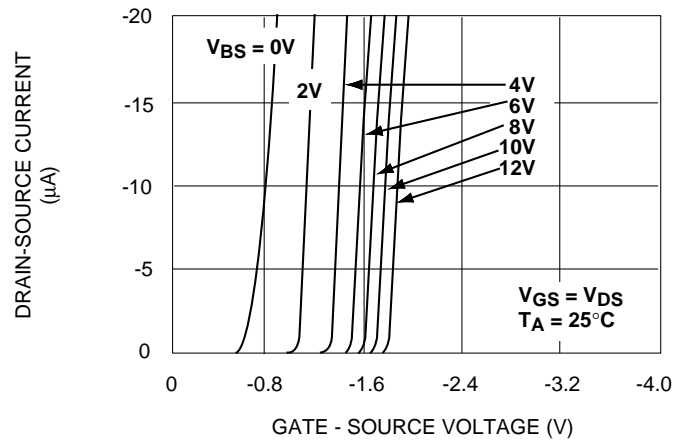
## LOW VOLTAGE OUTPUT CHARACTERISTICS



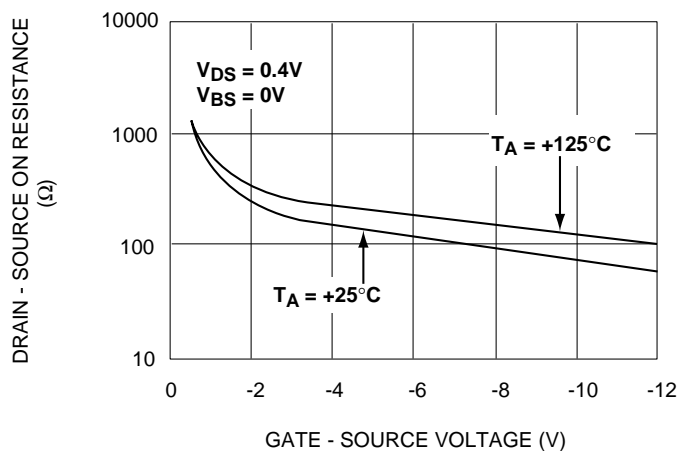
## FORWARD TRANSCONDUCTANCE vs. DRAIN - SOURCE VOLTAGE



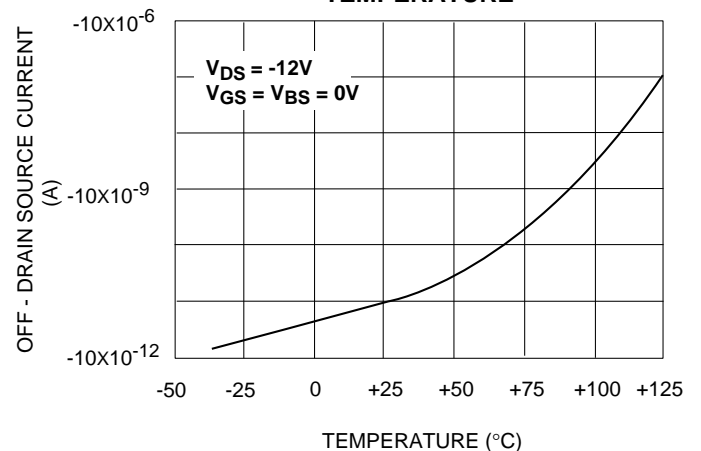
## TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



## RDS (ON) vs. GATE - SOURCE VOLTAGE

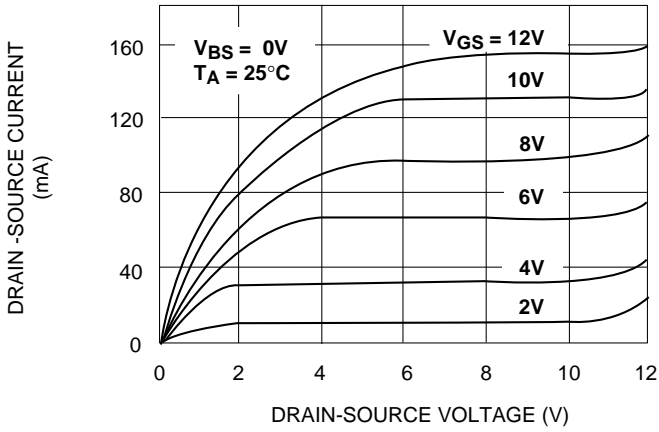


## OFF DRAIN - CURRENT vs. TEMPERATURE

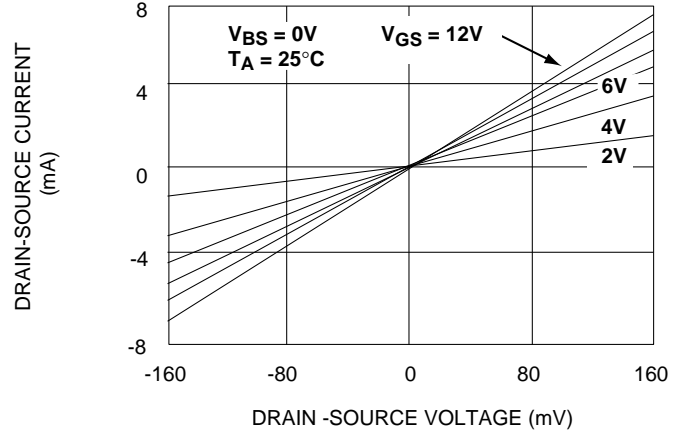


# N- CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

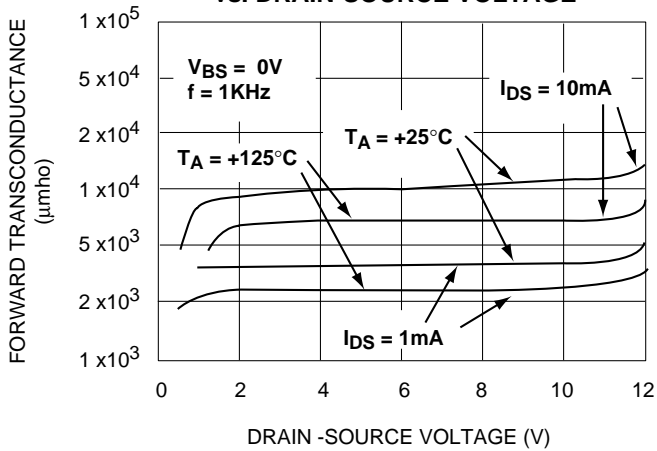
## OUTPUT CHARACTERISTICS



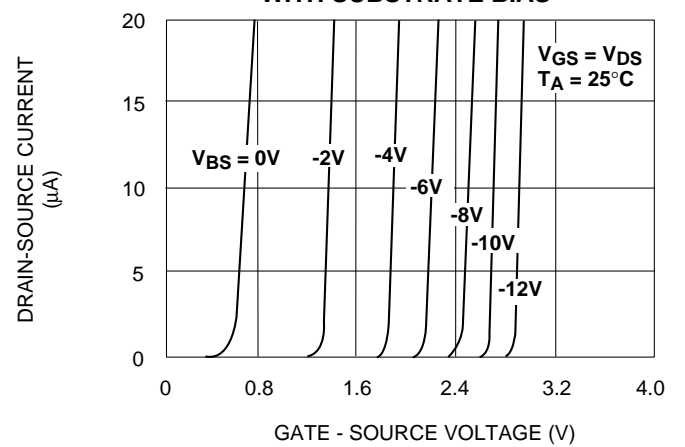
## LOW VOLTAGE OUTPUT CHARACTERISTICS



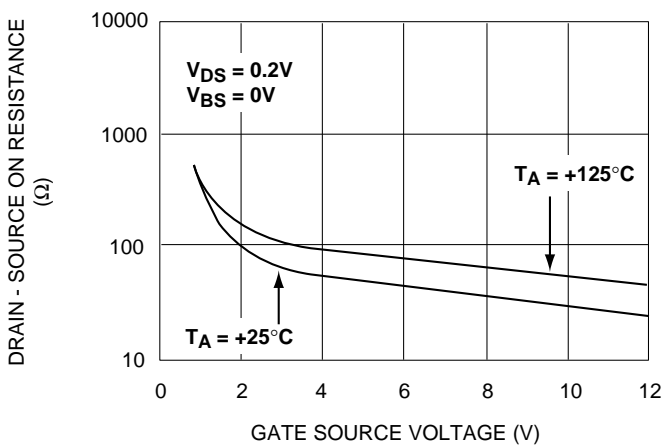
## FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE



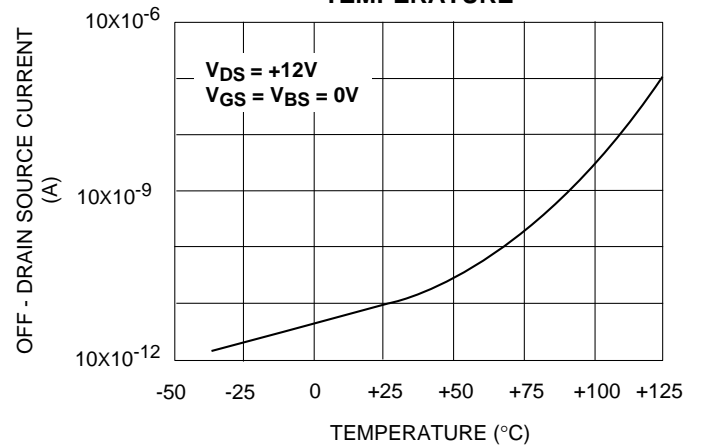
## TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS



## RDS (ON) vs. GATE - SOURCE VOLTAGE

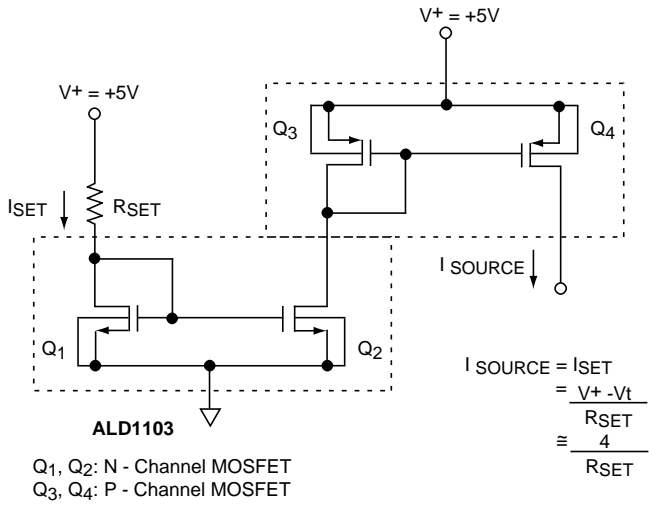


## OFF DRAIN - CURRENT vs. TEMPERATURE

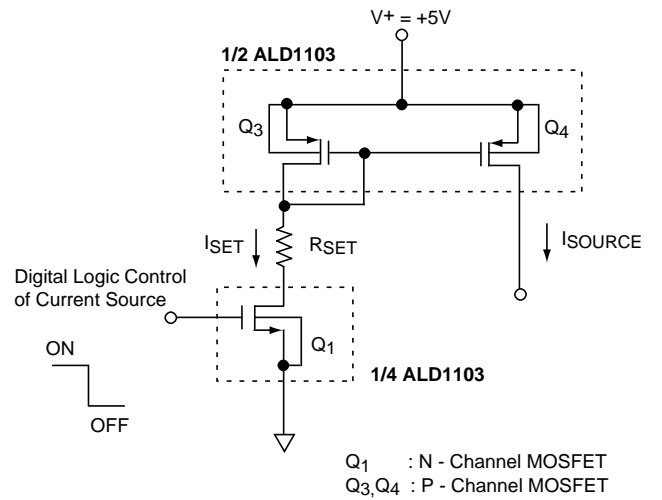


# TYPICAL APPLICATIONS

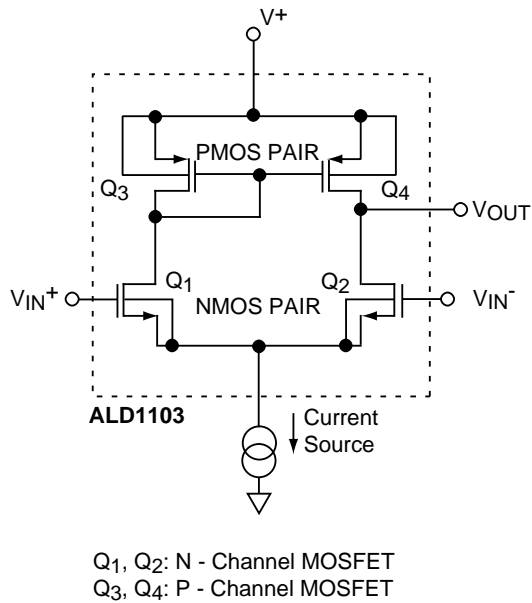
## CURRENT SOURCE MIRROR



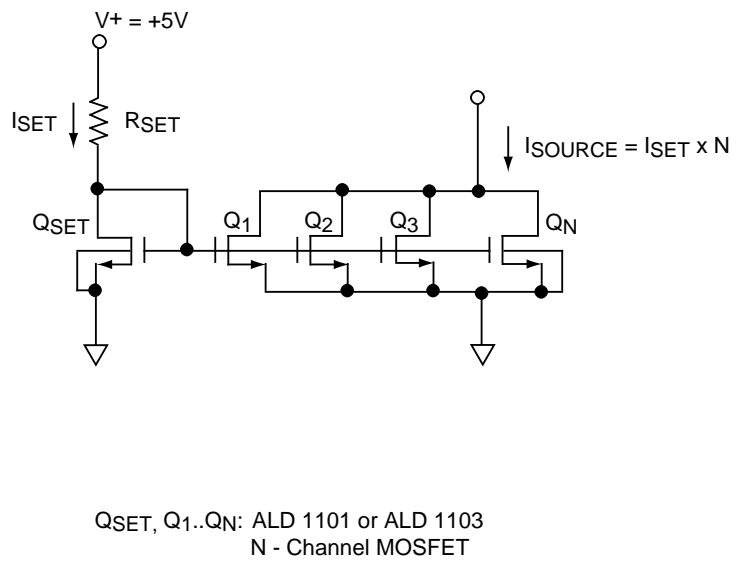
## CURRENT SOURCE WITH GATE CONTROL



## DIFFERENTIAL AMPLIFIER



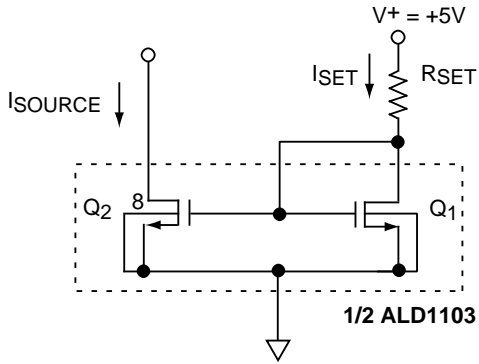
## CURRENT SOURCE MULTIPLICATION



# TYPICAL APPLICATIONS

## BASIC CURRENT SOURCES

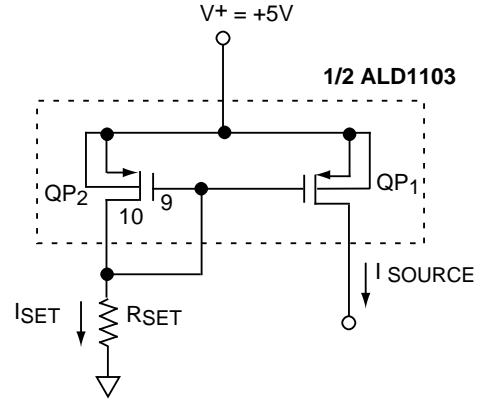
### N- CHANNEL CURRENT SOURCE



$$I_{SOURCE} = I_{SET} = \frac{V^+ - V_t}{R_{SET}} \cong \frac{V^+ - 1.0}{R_{SET}} \cong \frac{4}{R_{SET}}$$

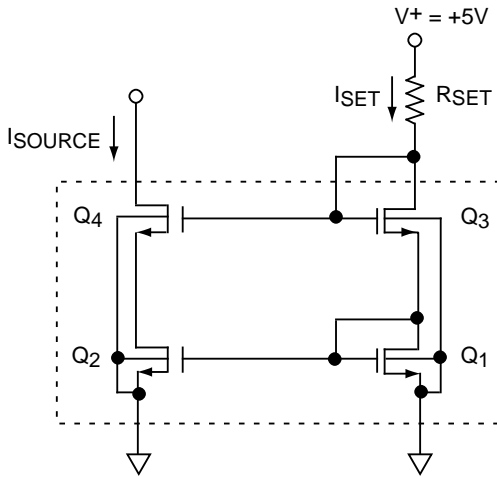
Q<sub>1</sub>, Q<sub>2</sub> : N - Channel MOSFET

### P- CHANNEL CURRENT SOURCE

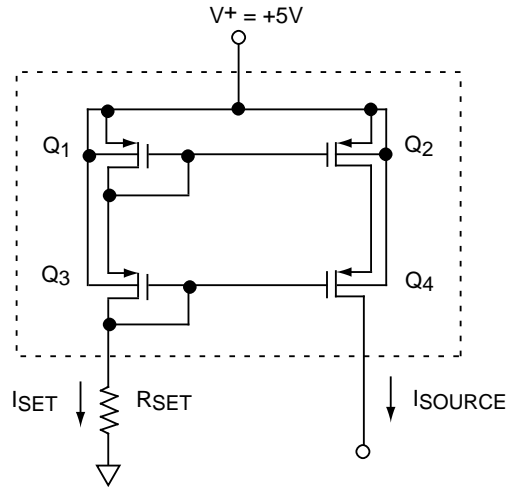


QP<sub>1</sub>, QP<sub>2</sub>: P - Channel MOSFET

## CASCODE CURRENT SOURCES



Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, Q<sub>4</sub>: N - Channel MOSFET  
(ALD1101 or ALD1103)



$$I_{SOURCE} = I_{SET} = \frac{V^+ - 2V_t}{R_{SET}} \cong \frac{3}{R_{SET}}$$

Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>3</sub>, Q<sub>4</sub>: P - Channel MOSFET  
(ALD1102 or ALD1103)