QUAD/DUAL N-CHANNEL ZERO THRESHOLD™ EPAD®
MATCHED PAIR MOSFET ARRAY

$V_{GS(th)}$= +0.0V

GENERAL DESCRIPTION

ALD110800A/ALD110800/ALD110900A/ALD110900 are monolithic quad/dual N-Channel MOSFETs matched at the factory using ALD's proven EPAD® CMOS technology. These devices are intended for low voltage, small signal applications. The ALD110800/ALD110900 features zero threshold voltage, which reduces or eliminates input to output voltage level shift, including circuits where the signal is referenced to GND or V+. This feature greatly reduces output signal voltage level shift and enhances signal operating range, especially for very low operating voltage environments. With these zero threshold devices an analog circuit with multiple stages can be constructed to operate at extremely low supply or bias voltage levels. As an example, an input amplifier stage operating at 0.2V supply voltage has been demonstrated.

ALD110800A/ALD110800/ALD110900A/ALD110900 matched pair MOSFETs are designed for exceptional device electrical characteristics matching. As these devices are on the same monolithic chip, they also exhibit excellent tempco tracking characteristics. They are versatile as design components for a broad range of analog applications such as basic building blocks for current sources, differential amplifier input stages, transmission gates, and multiplexer applications.

Besides matched pair electrical characteristics, each individual MOSFET also exhibits well controlled parameters, enabling the user to depend on tight design limits. Even units from different batches and different date of manufacture have correspondingly well matched characteristics.

These devices are built for minimum offset voltage and differential thermal response, and they are designed for switching and amplifying applications in +0.2V to +10V systems where low input bias current, low input capacitance and fast switching speed are desired. The $V_{GS(th)}$ of these devices are set at +0.0V, which classify them as both enhancement mode and depletion mode devices. When the gate is set at 0.0V, the drain current = +1μA @ V_{DS} =1+0.1V, which allow a class of circuits with output voltage level biased at or near input voltage level without voltage level shift. These devices exhibit same well controlled turn-off and sub-threshold characteristics as standard enhancement mode MOSFETs.

The ALD110800A/ALD110800/ALD110900A/ALD110900 are MOSFET devices that feature high input impedance ($10^{12}\Omega$) and high DC current gain (>10^8). A sample calculation of the DC current gain at a drain current of 3mA and input leakage current of 30pA at 25°C is = 3mA/30pA = 100,000,000. For most applications, connect V+ pin to the most positive voltage potential (or left open unused) and V- and N/C pins to the most negative voltage potential in the system. All other pins must have voltages within these voltage limits.

ORDERING INFORMATION

Operating Temperature Range* 0°C to +70°C		Operating Temperature Range* 0°C to +70°C	
16-Pin Plastic Dip Package	16-Pin SOIC Package	8-Pin Plastic Dip Package	8-Pin SOIC Package
ALD110800APC	ALD110800ASC	ALD110900APA	ALD110900ASA
ALD110800PC	ALD110800SC	ALD110900PA	ALD110900SA

* Contact factory for industrial temp. range or user-specified threshold voltage values

FEATURES

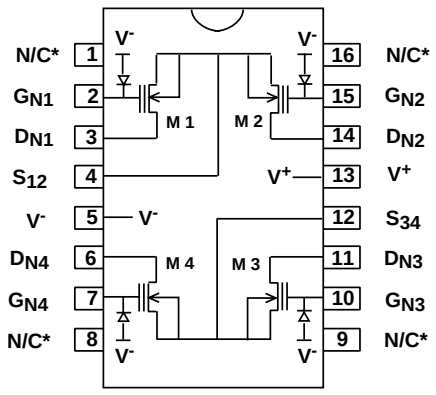
- Precision zero threshold voltage mode
- Nominal $R_{DS(ON)}$ @V_{GS}=0.0V of 104KΩ
- Matched MOSFET to MOSFET characteristics
- Tight lot to lot parametric control
- $V_{GS(th)}$ match (V_{OS}) to 2mV and 10mV
- Positive, zero, and negative $V_{GS(th)}$ tempco
- Low input capacitance
- Low input/output leakage currents

APPLICATIONS

- Very low voltage analog and digital circuits
- Zero power fail safe circuits
- Backup battery circuits & power failure detector
- Low level voltage clamp & zero crossing detector
- Source followers and buffers
- Precision current mirrors and current sources
- Capacitives probes and sensor interfaces
- Charge detectors and charge integrators
- Differential amplifier input stage
- High side switches
- Peak detectors and level shifters
- Sample and Hold
- Current multipliers
- Analog switches / multiplexers
- Voltage comparators and level shifters

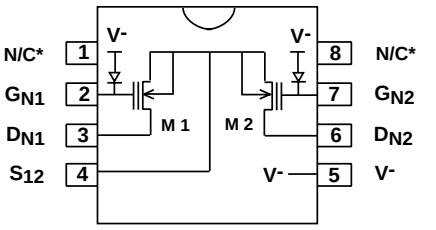
PIN CONFIGURATION

ALD110800



PC, SC PACKAGES

ALD110900



PA, SA PACKAGES

*N/C pins are internally connected.
Connect to V- to reduce noise

ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS} — 10.6V
Gate-Source voltage, V_{GS} — 10.6V
Power dissipation — 500 mW
Operating temperature range PA, SA, PC, SC package — 0°C to +70°C
Storage temperature range — -65°C to +150°C
Lead temperature, 10 seconds — +260°C

OPERATING ELECTRICAL CHARACTERISTICS

V^+ = +5V (or open) V- = GND T_A = 25°C unless otherwise specified

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

		ALD110800A / ALD110900A			ALD110800/ ALD110900				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Gate Threshold Voltage	$V_{GS(th)}$	-0.01	0.00	0.01	-0.02	0.00	0.02	V	I_{DS} =1μA, V_{DS} = 0.1V
Offset Voltage $V_{GS(th)1}$-$V_{GS(th)2}$	V_{OS}		1	2		2	10	mV	
Offset Voltage Tempco	TCV_{OS}		5			5		μV/°C	V_{DS1} = V_{DS2}
GateThreshold Voltage Tempco	$TCV_{GS(th)}$		-1.7 0.0 +1.6			-1.7 0.0 +1.6		mV/°C	I_D = 1μA, V_{DS} = 0.1V I_D = 20μA, V_{DS} = 0.1V I_D = 40μA, V_{DS} = 0.1V
On Drain Current	$I_{DS\ (ON)}$		12.0 3.0			12.0 3.0		mA	V_{GS} = +9.5V, V_{DS} = +5V V_{GS} = +4.0V, V_{DS} = +5V
Forward Transconductance	G_{FS}		1.4			1.4		mmho	V_{GS} = +4.0V V_{DS} = +9.0V
Transconductance Mismatch	ΔG_{FS}		1.8			1.8		%	
Output Conductance	G_{OS}		68			68		μmho	V_{GS} = +4.0V V_{DS} = +9.0V
Drain Source On Resistance	$R_{DS\ (ON)}$		500			500		Ω	V_{DS} = +0.1V V_{GS} = +4.0V
Drain Source On Resistance	$R_{DS\ (ON)}$		104			104		KΩ	V_{DS} = +0.1V V_{GS} = +0.0V
Drain Source On Resistance Tolerance	$\Delta R_{DS\ (ON)}$		5			5		%	V_{DS} = +0.1V V_{GS} = +4.0V
Drain Source On Resistance Mismatch	$\Delta R_{DS\ (ON)}$		0.5			0.5		%	
Drain Source Breakdown Voltage	BV_{DSX}	10			10			V	I_{DS} = 1.0μA V^-= V_{GS} = -1.0V
Drain Source Leakage Current[1]	$I_{DS\ (OFF)}$		10	400 4		10	400 4	pA nA	V_{GS} = -1.0V, V_{DS} =+5V V^- = -5V T_A = 125°C
Gate Leakage Current[1]	I_{GSS}		5	30 1		5	30 1	pA nA	V_{DS} = 0V V_{GS} = +10V T_A =125°C
Input Capacitance	C_{ISS}		2.5			2.5		pF	
Transfer Reverse Capacitance	C_{RSS}		0.1			0.1		pF	
Turn-on Delay Time	t_{on}		10			10		ns	V^+ = 5V R_L= 5KΩ
Turn-off Delay Time	t_{off}		10			10		ns	V^+ = 5V R_L= 5KΩ
Crosstalk			60			60		dB	f = 100KHz

Notes: [1] Consists of junction leakage currents