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DEVICES, INC.

ALD8100XX/ALD9100XX FAMILY of SUPERCAPACITOR AUTO BALANCING (SAB™) MOSFET ARRAYS

GENERAL DESCRIPTION

The ALD8100xx/ALD9100xx family of Supercapacitor Auto Balancing MOSFET Arrays, or SAB™ MOSFETs, are designed to address voltage and leakage current balancing of supercapacitors connected in series. Supercapacitors, also known as ultracapacitors or supercaps, connected in series can be balanced with single or multiple ALD8100xx/ALD9100xx packages. These SAB MOSFETs are built with ALD production proven EPAD® MOSFET technology.

SAB MOSFETs have unique electrical characteristics for superior active continuous leakage current regulation and self-balancing of stacked series-connected supercapacitors while dissipating near zero leakage currents, practically eliminating extra power consumption. For many applications, SAB MOSFET automatic charge balancing offers a simple, economical and effective method to balance and regulate supercapacitor voltages. With SAB MOSFETs, each supercapacitor in a series-connected stack is continuously monitored and automatically controlled for precise, effective balancing of its voltage and leakage current.

The SAB MOSFET regulates the voltage across a supercapacitor cell by increasing its drain current exponentially across the supercapacitor when its voltage increases, and by decreasing its drain current exponentially across the supercapacitor when its voltage decreases. When a supercapacitor cell is charged to a voltage less than 90% of the desired voltage limit, the SAB MOSFET across the supercap is turned off and there is zero leakage current contribution from the SAB MOSFET. On the other hand, when the voltage across the supercapacitor is over the desired voltage limit, the SAB MOSFET is turned on to increase its drain currents to keep the supercapacitor voltage from rising. Simultaneously, the voltages and leakages of other supercapacitors in the series stack are lowered to result in a near zero net increase in leakage current.

The ALD8100xx/ALD9100xx SAB MOSFET family offers a selection of different threshold devices for various supercapacitor maximum operating voltage values and desired leakage balancing characteristics as well as different temperature range environments. A list of the available ALD part numbers can be found in the tables on pages 6 and 7 of this document. For individual datasheets and specifications, please visit www.aldinc.com under “SAB MOSFET”.

SUPERCAPACITORS

Supercapacitors are typically rated with a nominal recommended working voltage established for long life at their maximum rated operating temperature. When a supercapacitor cell voltage exceeds its rated voltage for a prolonged time period, it experiences reduced lifetime and eventual rupture and catastrophic failure. To prevent such an occurrence, in most applications having two or more supercapacitors connected in series, a means of automatically monitoring and adjusting charge-balancing at their maximum operating voltages is required. This is due to different internal leakage currents in each specific cell.

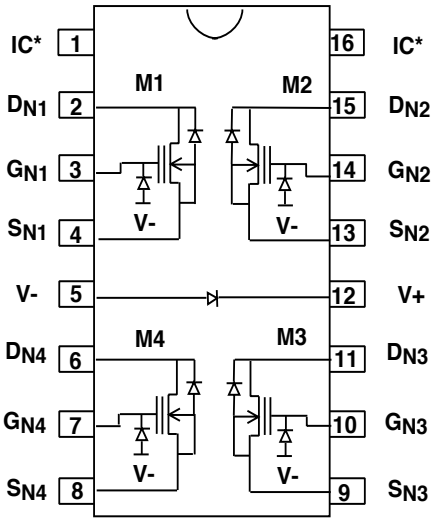
The supercapacitor’s leakage current is a variable function of many parameters such as aging, initial leakage current at zero input voltage, material and construction of the supercapactor, its chemistry composition, its leakage as a function of the charging voltage and the charging current and temperature, operating temperature range, and the rate of change of many of these parameters. Supercapacitor balancing must correct for these changing effects automatically, with minimal added leakage currents or power consumption.

SAB MOSFET ADVANTAGES

The ALD8100xx/ALD9100xx family of SAB MOSFETs are designed for automatic supercapacitor balancing. They are replacements for many other passive or active supercapacitor balancing methods where cost, board space, efficiency, simplicity and power dissipation are important design considerations. For example, in applications where supercapacitors require minimum long-term power dissipation (internal leakage currents) as a primary goal, ALD8100xx/ALD9100xx SAB MOSFETs are simpler and more effective in performing the leakage balancing function, using significantly less board space and contributing no additional charge loss beyond the supercapacitor’s own leakages. Other common methods of charge

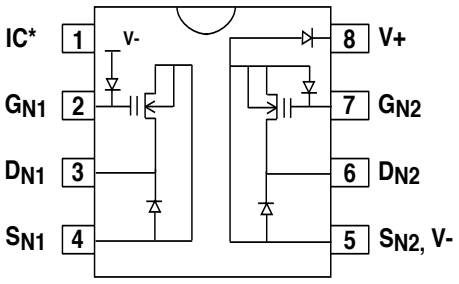
PIN CONFIGURATIONS

ALD8100xx



SCL PACKAGES

ALD9100xx



SAL PACKAGES

*IC pins are internally connected, connect to V-

balancing generally contribute additional continuous power dissipation due to linear currents at all supercapacitor voltage levels, whereas SAB MOSFET leakages decrease exponentially with decreased supercapacitor voltages. In many cases, the additional leakage charge loss is near zero.

UNDERSTANDING SUPERCAPACITOR AUTO BALANCING USING SAB™ MOSFETS

The principle behind the SAB MOSFET in balancing supercapacitors is simple. It is based on the natural threshold characteristics of a MOSFET device. The threshold voltage of a MOSFET is the voltage at which a MOSFET turns on and starts to conduct a current. The drain current of the MOSFET, at or below its threshold voltage, is an exponential function of its gate voltage. Hence, for small changes in the MOSFET's gate voltage, its drain-source on-current can vary greatly, by orders of magnitude. ALD's SAB MOSFETs are designed to take advantage of this fundamental device characteristic.

SAB MOSFETs are connected in the V_t mode, meaning that the Gate-to-Source and the Drain-to-Source terminals of each MOSFET are always connected. In this mode V_{GS} is always equal to V_{DS} and when this joint terminal is connected across a supercapacitor, it is also referred to as an Input Voltage, V_{IN}. Each SAB MOSFET has a well defined Drain-to-Source Current, $I_{DS(ON)}$, for different values of V_{IN} Voltages. This current is also referred to as the Output Current, I_{OUT}, of the SAB MOSFET.

SAB MOSFETs can be connected in parallel or in series, to suit the desired leakage current characteristics, in order to charge-balance an array of supercapacitors connected in series. The array of combined SAB MOSFETs and supercapacitors would be automatically self-regulating with various leakage mismatches and environmental temperature changes. The SAB MOSFETs can also be used entirely in the subthreshold mode, meaning the SAB MOSFET is used at min., nominal and max. operating voltages in voltage ranges below its specified threshold voltage.

With the ALD8100xx/ALD9100xx family, the threshold voltage V_t of an SAB MOSFET is defined as its drain-gate source voltage at a drain-source ON current, $I_{DS(ON)} = 1\mu A$, when its gate and drain terminals are connected together ($V_{GS} = V_{DS}$). This voltage is specified as xx, where the threshold voltage is in 0.10V increments. Two examples are: the ALD810025 features a precise threshold voltage of $V_t = 2.500V$ at $I_{DS(ON)} = 1\mu A$ and the ALD810017 has $V_t = 1.700V$ at $I_{DS(ON)} = 1\mu A$.

As all ALD8100xx/ALD9100xx devices operate similarly, with linear voltage shifts, an ALD810025 is used as an illustration of its characteristics. At voltages below its threshold voltage, the ALD810025 rapidly turns off at a rate of approximately one decade of current per 104mV of voltage drop. Hence, at $V_{IN} = 2.396V$, the ALD810025 I_{OUT} is $0.1\mu A$. At $V_{IN} = 2.292V$, its I_{OUT} becomes $0.01\mu A$. When V_{IN} drops further to 2.188V, its I_{OUT} becomes $0.001\mu A$. It should be apparent that at $V_{IN} \leq 2.10V$, the ALD810025 $I_{OUT} \leq 0.00014\mu A$, which is near zero when compared to $1\mu A$ at $V_{IN} = 2.50V$. At V_{IN} below 1.9V, the SAB MOSFET Output Current, I_{OUT}, goes to essentially zero (~70pA). The $I_{OUT} \leq 0.00014\mu A$ is controlled and repeatable for different units from various production batches.

This exponential relationship between the SAB MOSFET's V_{IN} and I_{OUT} can be an important consideration in replacing certain supercapacitor charge balancing applications currently using fixed resistors, operational amplifier circuits or other forms of charge balancing. These other conventional charge-balancing methods continue to dissipate a significant amount of current, even after the voltage across the supercapacitors has dropped, because the current dissipated is a linear function, rather than an exponential function, of the supercapacitor voltage (I = V/R). For supercapacitor series stacks with more than two cells, the challenge of leakage balancing becomes even more onerous.

With most other passive or active circuits that offer charge balancing, active power is still being consumed even if the supercapacitor voltage falls much below its operating voltage. For a four-cell supercapacitor stack, for example, this translates into a 2.0V x 4 ~= 8.0V power supply for an IC charge-balancing circuit. As the number of cells increase, adding components to the charge balancing circuit, increased circuit complexity and power dissipation becomes a greater challenge. A supercapacitor stack using the SAB MOSFET charge-balancing method, on the other hand, would not cause extra power dissipation when the number of cells increase. This method provides an exponentially decreasing amount of charge loss with time, and helps preserve, by far, the greatest amount of charge on each of the supercapacitors.

If V_{IN} of the ALD810025 is greater than its V_t threshold voltage, its Output Current, I_{OUT}, behavior has the opposite near-exponential effect. At $V_{IN} = 2.60V$, for example, the ALD810025 I_{OUT} increases tenfold to $10\mu A$. Similarly, I_{OUT} becomes $100\mu A$ at a V_{IN} of 2.74V, and $300\mu A$ at V_{IN} of 2.84V. (See Table 1.)

As I_{OUT} changes rapidly with the applied V_{IN}, the SAB MOSFET device acts like a voltage limiting regulator with self-adjusting current levels. When the SAB MOSFET is connected across a supercapacitor cell, the total leakage current equals the two in combination automatically compensate and correct for each other.

Consider the case when two supercapacitor cells are connected in series, each with an SAB MOSFET connected across it, charged by a power supply to a voltage equal to 2 x V_S.

If the top supercapacitor has a higher internal leakage current than the bottom supercapacitor, the voltage $V_{S(top)}$ across it tends to drop lower than that of the bottom supercapacitor. The SAB MOSFET I_{OUT} across the top supercapacitor, sensing this voltage drop, drops off rapidly. Meanwhile, the bottom supercapacitor $V_{S(bottom)}$ voltage tends to rise, as $V_{S(bottom)} = (2 \times V_S) - V_{S(top)}$. This tendency for the voltage rise also increases V_{IN} voltage of the SAB MOSFET across the bottom supercapacitor. This increased V_{IN} voltage would cause the I_{OUT} of the bottom SAB MOSFET to increase rapidly as well. The excess leakage current of the top supercapacitor would now leak across the bottom SAB MOSFET, reducing the voltage rise tendency of the lower supercapacitor. With this automatic self-regulating mechanism, the top supercapacitor voltage tends to rise while the bottom supercapacitor voltage tends to drop, creating simultaneously opposing actions to the supercapacitor leakage currents.

With appropriate design and selection of a specific SAB MOSFET device for a given pair of supercapacitors, it is now possible to regulate and balance two series-connected supercapacitors with essentially no extra leakage current, since the SAB MOSFET only conducts the difference in leakage current between the two supercapacitors.

Likewise, the case of the bottom supercapacitor having a higher leakage current than that of the top supercapacitor works in similar fashion, where the bottom supercapacitor voltage tends to drop, compensated by the tendency of the top supercap voltage to drop as well, effected by the top SAB MOSFET. This SAB MOSFET charge balancing scheme also works with four, eight or more supercapacitors in series by using an equivalent number of SAB MOSFETs in multiple package(s).

Ambient temperature increases cause supercapacitor leakage currents to increase. The SAB MOSFET threshold voltage is reduced

with temperature increase, which causes its I_{OUT} to increase with temperature as well. This current increase compensates for the leakage current increase within the supercapacitor, reducing the overall supercapacitor temperature leakage effect and preserving charge balancing effectiveness. This temperature compensation assumes that all supercapacitors and SAB MOSFETs operate in the same temperature environments.

SAB MOSFET LIMITATIONS

During supercapacitor charging, consideration must be paid to limit the rate of charging so that excessive voltage and current does not build up across any two pins of the SAB MOSFETs, even momentarily, to exceed their absolute maximum ratings in voltage, operating current, and power dissipation. In most cases though, this is not an issue, as other design constraints elsewhere limit the rate of charging or discharging of the supercapacitors. For many applications, no further action, other than checking the voltage and current excursions, or including a simple current-limiting charging resistor, is necessary.

For each SAB MOSFET, its V+ pin must be connected to the most positive voltage and its V- and IC pins to the most negative voltage within the package. SAB MOSFETs have numerous pins required for its manufacturing process, which must be connected to the supercapacitors when in use, for proper circuit operation. Multiple packages can be cascaded for higher system voltages as long as absolute maximum ratings are observed for each individual package.

Note that each Drain pin of a SAB MOSFET has an internal reverse biased diode to its Source pin, which can become forward-biased if the Drain voltage should become negative relative to its Source voltage. This forward-biased diode clamps the Drain voltage to limit the negative voltage relative to its Source voltage, and is limited to a 80mA max. rated current between any two pins.

Each Gate pin also has a reverse biased diode to V-. When forward biased, the maximum diode current must be within the absolute maximum ratings. All other pins must have voltages within V+ and V- voltage limits. Standard ESD protection facilities and handling procedures for static sensitive devices must also be followed before the SAB MOSFETs are installed. Once the SAB MOSFET is permanently connected to the supercapacitors, ESD concerns are relieved because any extraneous electrostatic charge would be absorbed by the supercapacitor and would not cause exessive voltage increase.

EXTENDED TEMPERATURE RANGE OPERATION

SAB MOSFETs are built with solid state integrated circuit tehcnology. They are available for operation over a wide temperature range, with appropriate derating, screening and packaging. Standard commercial grade devices are rated for operation at 0°C to +70°C. Industrial temperature range (“I” suffix) units are rated for -40°C to +85°C. Custom versions are also available for military temperature ranges (“M” suffix), -55°C to +125°C.

MATCHING SAB™ MOSFETS TO SUPERCAPACITORS

Figure 1 shows a basic connection diagram of two SAB MOSFETs connected across two supercapacitors, powered by a V+ power supply with an external (or internal) resistor, with basic equations of SAB MOSFET and supercapacitor voltages and currents.

The proess of selecting SAB MOSFETs to match specific models of supercapacitors begins by analyzing the parameters and the requirements of a given set of supercapacitors:

1) For better leakage current matching results, pick the same make and model of supercapacitors to be connected in a series. If possible, select supercapacitors from the same production batch. (Note: SAB MOSFETs are precisely set at the factory and specified such that their unit-to-unit variation is not a concern.)

2) Determine the max. leakage current of each supercapacitor.

3) Determine the desired nominal operating voltage of the supercapacitor.

4) Determine the maximum operating voltage rating of the supercapacitor.

5) Calculate or measure the maximum leakage current of the supercapacitor at its maximum rated operating voltage.

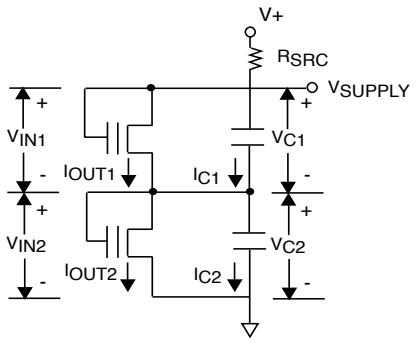
6) Determine the operating temperature range of the supercapacitor.

7) Determine any additional level of operating leakage current in the system.

Next, determine the normalized I_{OUT} of an SAB MOSFET at a preselected V_{IN} operating voltage.

For example, the ALD810025 has a rated Drain Current of 1μA at applied V_{IN} of 2.50V. If the desired normalized I_{OUT} is 0.01μA, then the ALD810025 would give a bias V_{IN} voltage of approximately 2.3V at that current, which produces an equivalent ON resistance of 2.3V/0.01μA ~= 230MΩ (using the rule of thumb: one decade of I_{OUT} change per 0.10V of V_{IN} change).

FIGURE 1



Basic Equations:

$V^+ = V_{C1} + V_{C2} + R_{SRC}\,(I_{C1} + I_{OUT1})$

$V^+ = V_{C1} + V_{C2} + R_{SRC}\,(I_{C2} + I_{OUT2})$

$V_{C1} = V_{IN1}$

$V_{C2} = V_{IN2}$

$I_{C1} + I_{OUT1} = I_{C2} + I_{OUT2}$

$V_{SUPPLY} = V_{C1} + V_{C2}$

CHOOSING A SPECIFIC SAB MOSFET

In choosing SAB MOSFETs for a specific application, go to the SAB MOSFET selection table, (Table 1 for ALD8100xx devices, Table 2 for ALD9100xx devices) where each SAB MOSFET Part Number and its respective parameters are listed. First, select an SAB MOSFET I_{OUT} Current horizontally across the top row of the Table(s). Next, look down that column to the row that contains the maximum desired V_{IN} voltage. The appropriate ALD part number is in the first column of that row. The part number of an SAB MOSFET references its rated threshold voltage, but that is not necessarily the desired operating voltage where the auto-balancing supercapacitor operates. Generally, the recommended maximum supercapacitor I_{OUT} auto-balancing for the ALD8100xx/ALD9100xx family is about 1mA. When supercapacitor leakage current exceeds 1mA, the effectiveness of the SAB MOSFET auto-balancing gradually diminishes and there is additional leakage current contribution from the SAB MOSFET itself as its V_{IN} increases. Please contact techsupport@aldinc.com for more information or technical assistance.

A DESIGN EXAMPLE

A single 5V power supply using two 2.7V rated supercapacitors connected in series and a single ALD810026 SAB MOSFET array package (using two of the four devices in the package).

For a supercapacitor with:

1) max. operating voltage = 2.70V and
2) max. leakage current = 10μA at 70°C.
3) At 2.50V, the supercapacitor max. leakage current = 2.5μA at 25°C.

Next, pick ALD810026, a SAB MOSFET with V_t = 2.60V. For this device, at V_{IN} = 2.60V, the nominal I_{OUT} = 1μA. See Table 1, at V_{IN} = 2.50V, I_{OUT} ~= 0.1μA.

At a nominal V_{IN} of 2.50V, the additional leakage current contribution by the ALD810026 is therefore ~= 0.1μA. The total leakage current for the supercapacitor and the SAB MOSFET = 2.5μA + 0.1μA ~= 2.6μA @ 2.50V operating voltage. When operating voltage becomes 2.40V, additional ALD810026 leakage current contribution decreases to about 0.01μA.

At V_{IN} of 2.70V across the ALD810026 SAB MOSFET, I_{OUT} = 10μA. 10μA is also the max. leakage current design margin, the difference between top and bottom supercapacitor leakage currents that can be compensated.

If a higher max. leakage current margin is desired, then SAB MOSFET selection may need to go to the next SAB MOSFET part down in Table 1, which is ALD810025. For ALD810025 operating at a max. rated voltage of 2.70V, the max. leakage current margin is ~= 50μA. For this device, I_{OUT} at 2.50V is ~= 1μA, which is the average current consumption for the series-connected stack. The total current for the supercapacitor and the SAB MOSFET is = 2.5μA + 1μA ~= 3.5μA @ 2.50V operating voltage.

Because an SAB MOSFET is always active and always in “on” mode, there is no circuit switching or sleep mode involved. This may become an important factor when the time interval between the supercap discharging or recharging, and other events happening in the application, is long, unknown or variable. The circuit operation is also greatly simplified.

In real life situations, the actual circuit behavior is a little different, further reducing overall leakage currents from both supercapacitors and SAB MOSFETs, due to the automatic compensation for different leakage currents from the supercapacitors by themselves and in combination with the SAB MOSFETs. Take an example of two supercapacitors in series, assuming that the top supercapacitor is leaking 10μA and the bottom one is leaking 4μA (both at the rated 2.7V max.) while the power supply remains at 5V DC. The actual voltage across the top supercapacitor tends to be less than 2.5V (50% of 5.0V), due to its higher internal leakage current, and results in a lowered current level than 10μA because the current tends to be lower at less than 2.7V. As the total voltage across both supercapacitors is still 5.0V, each supercapacitor would experience a lowered voltage than its maximum rated voltage of 2.7V, thereby resulting in reduced overall leakage currents in each of the two supercapacitors.

These leakage currents are then further regulated by the SAB MOSFETs connected across each of the supercapacitors. The end result is a compensated condition where, for example, the top supercapacitor has V_{IN} of ~2.4V across it and the bottom supercapacitor has V_{IN} of ~2.6V. The excess leakage current of the top supercapacitor is bypassed across the bottom SAB MOSFET. Meanwhile the top SAB MOSFET, with ~2.4V across it, is biased to conduct very little I_{OUT}. Note also that the top supercapacitor is now biased at ~2.4V and, therefore, would experience less current leakage than when it is at 2.7V. The key point here is that this process of leakage current balancing is fully automatic and works for a variety of supercapacitors, each with its own different leakage current characteristic profile.

A second factor to note is that with ~2.4V and ~2.6V across the two supercapacitors, as in this example, the actual current level difference between the top and the bottom SAB MOSFETs is at about a 100:1 ratio (~2 orders of magnitude). The net additional leakage current contributed by the ALD810026 in the design example above would, therefore, be approximately 0.01μA. In this case, leakage currents between the two supercapacitors can be at a ratio of 100:1 and still experience charge balancing and voltage regulation. If a range of supercapacitor leakge currents can be determined or selected for a particular model of supercapacitor across different production batches, then a SAB MOSFET part can be specified that further minimizes any SAB leakage currents and still maintains balanced supercapacitor voltages within a narrow range.

The dynamic response of a SAB MOSFET circuit is very fast, and the typical response time is determined by the RC time constant of the equivalent ON resistance value R_{ON} of the SAB MOSFET and the capacitance value C of the supercapacitor. In many cases the R_{ON} value is small initially, responding rapidly to a large voltage transient by having a smaller $R_{ON}C$ time constant. As the voltages settle down, the equivalent R_{ON} increases. As these R_{ON} and C values can become very large, it can take a long time for the voltages across the supercaps to settle down to steady state levels. The direction of the voltage movements across the supercapacitor, however, can indicate that the supercapacitor voltages are moving away from the voltage limits.

A HIGH LEAKAGE CURRENT DESIGN EXAMPLE

A nominal 12V DC power supply connects across a supercapacitor series stack consisting of six 2.0V supercapacitor cells. Each cell has a nominal operating voltage of 2.0V and is rated at 2.5V max. Maximum voltage across the stack is 13.92V, which results in a per-cell voltage of 2.32V. The max. leakage current for the supercapacitor is rated at 1mA at 2.5V.

Next, we choose a maximum acceptable supercapacitor in-balance stack voltage of 2.42V, which allows for temperature and aging effects, among other factors. When we look down the column of 1000μA (1mA) in Table 1 to locate a V_{IN} voltage of 2.42V, we find the corresponding ALD part number to be ALD810019.

In the graph titled “Input Voltage vs. Output Current”, locate the V_{IN} point as follows. First, find the V_t of the ALD810019 from the SAB MOSFET Selection Table, which is 1.90V. Next, subtract 1.90V from 2.42V, which is 0.52V. Check the I_{OUT} current variation and voltage variation as a function of temperature. If the temperature variation allowance is 60mV, then the maximum supercap inbalance voltage is 2.48V (2.42V + 0.06V) across temperature.

In cases where the supercapacitor leakage current is 1mA max., the ALD810019 is suggested. In cases where supercapacitor leakage currents are up to 3mA, then a part such as the ALD81016 can be used, although this may cause increased leakage current through the SAB MOSFET itself. Another way to reduce leakage currents would be to parallel connect mulitple ALD810019 devices to auto-balance leakage currents greater than 1mA.

A 4.2V SUPERCAPACITOR STACK DESIGN EXAMPLE

A supply voltage of 4.2V across two supercapacitors gives 2.1V across each supercapacitor cell. With a maximum leakage current of 100μA for each cell at 2.22V maximum V_{IN} cell voltage, the corresponding ALD part number is ALD910020SAL, a dual 8L SOIC package.

The ALD910020 would support an I_{OUT} (supercapacitor leakage current) of 300μA at V_{IN} = 2.30V; 100μA at V_{IN} = 2.22V; 10μA at V_{IN} = 2.10V and 1μA at V_{IN} = 2.00V, respectively. An inbalance leakage current ratio between two supercapacitor cell units of 100μA to 1μA, a 100 to 1 ratio, would produce one cell voltage of 2.22V and the other cell voltage of 1.98V, which adds up to 4.20V. Similarly, a lower supply voltage than 4.2V would be divided between the two supercapacitors corresponding to their respective leakage currents. Consider the case when the supply voltage is 4.10V, each with an ALD910020 connected to it. If the leakage current ratio between the supercapacitors remains the same, then one cell would be biased at 2.22V (100μA) and the other would be biased at 1.88V (4.10V - 2.22V). This would cause the ALD910020 to have a max. leakage current contribution of less than 0.1μA.

PARALLEL-CONNECTED AND SERIES-CONNECTED SAB MOSFETS

In the first design example on the previous page, note that the ALD810026 is a quad pack, with four SAB MOSFETs in a single SOIC package. For applications where two supercapacitors are connected in series, the ALD9100xx dual SAB MOSFET is recommended for charge balancing. If a two-stack supercapacitor requires charge balancing, then there is also an option to parallel-connect two additional SAB MOSFETs of the quad ALD8100xx for each of the two supercapacitors. Parallel-connection means that the drain, gate and source terminals of each of the two SAB MOSFETs are connected together to form a single MOSFET with twice the output current and twice the output current sensitivity to voltage change. In this case, at an operating V_{IN} voltage of 2.50V, the additional I_{OUT} current contribution by the SAB MOSFET is equal to 2 x 0.1μA = 0.2μA. The total current for the combined supercapacitor and SAB MOSFET is = 2.5μA + 0.2μA ~= 2.7μA @ 2.50V operating voltage. At max. voltage of 2.70V across the SAB MOSFET, V_{IN} = 2.70V results in a I_{OUT} of 2 x 10μA = 20μA. So this configuration would be chosen to increase max. supercapacitor charge balancing leakage current at 2.70V to 20μA, at the expense of an additional 0.1μA I_{OUT} leakage at 2.50V.

For stacks of series-connected supercapacitors consisting of more than three or four cells, it is possible to use a single SAB MOSFET array for every supercapacitor stack (up to 4 cells) connected in series. Multiple SAB MOSFET arrays can be arrayed across multiple supercapacitor stacks to operate at higher operating voltages. It is only important to limit the voltage across any two pins within a single SAB MOSFET array package to be less than its absolute maximum voltage and current ratings.

LOW LEAKAGE ENERGY HARVESTING APPLICATIONS

Supercapacitors offer an important benefit in energy harvesting applications with a high impedance energy source, in buffering and storing such energy to drive a higher power load.

For energy harvesting applications, supercapacitor leakage currents are a critical design parameter, as the average energy harvesting input charge must exceed the average supercapacitor internal leakage currents in order for any net energy to be harvested. When the input energy is a variable, meaning that its input voltage and current magnitude is not constant and dependent upon other parameters such as the source energy availability (energy sensor conversion efficiency, etc.), the energy harvested and stored must supply and exceed the necessary leakage currents, which tend to be steady DC currents.

In these types of applications, in order to minimize the amount of energy loss due to leakage currents, it is essential to choose supercapacitors with low leakage specifications and to use SAB MOSFETs to balance them.

For the first 90% of the initial voltages of a supercapacitor used in energy harvesting applications, supercapacitor charge loss is lower than its maximum leakage rating, at less than its max. rated voltage. SAB MOSFETs, used for charge balancing, would be completely turned off, consuming zero leakage current while the supercapacitor is being charged, maximizing any energy harvesting gathering efforts. The SAB MOSFET would not become active until the supercapacitor is already charged to over 90% of its max. rated voltage. The trickle charging of supercapacitors with energy harvesting techniques tends to work well with SAB MOSFETs as charge balancing devices, as it is less likely to have high transient energy spurts resulting in excessive voltage or current excursions.

If an energy harvesting source only provides a few μA of current, the power budget would not allow wasting any of this current on capacitor leakage currents, and on many other conventional charge balancing methods. Resistors or operational amplifiers used as charge-balancing circuits would dissipate far more energy than desired. It may also be an important consideration to reduce long term DC leakage currents as energy harvesting charging at low levels may take up to many days.

In summary, in order for an energy harvesting application to be successful, the input energy harvested must exceed all the energy spent, due to the leakages of the supercapacitors and the charge-balancing circuits, plus any load requirements. With their unique balancing characteristics and near-zero charge loss, SAB MOSFETs are ideal devices to use for supercapacitor charge-balancing within energy harvesting applications.

LONG TERM BACKUP BATTERY APPLICATIONS

Similar to energy harvesting applications, any low leakage long-term application, such as a long-term backup battery requiring supercapacitors at the output to reduce output impedance and to boost its output power, would benefit from SAB MOSFET deployment. Over a long time span, reducing leakge currents is an important design parameter. For example, a low DC leakage current of just 1μA over 5 years translates into 44.8mAhr of energy lost.

TABLE 1. ALD 8100XX SUPERCAPACITOR AUTO BALANCING (SAB™) MOSFETS EQUIVALENT ON RESISTANCE AT DIFFERENT INPUT VOLTAGES AND OUTPUT CURRENTS

ALD Part Number	Gate-Threshold Voltage V_t (V)	V_{IN} (V) [2] Equivalent ON Resistance (MΩ)	OUTPUT CURRENT I_{OUT} = $I_{DS(ON)}$ (μA) [1] TA = 25°C										
			0.0001	0.001	0.01	0.1	1	10	100	300	1000	3000	10000
ALD810028	2.80	V_{IN} (V)	2.40	2.50	2.60	2.70	2.80	2.90	3.04	3.14	3.32	3.62	4.22
		$R_{DS(ON)}$ (MΩ)	24000	2500	260	27	2.8	0.29	0.030	0.01	0.003	0.001	0.0004
ALD810027	2.70	V_{IN} (V)	2.30	2.40	2.50	2.60	2.70	2.80	2.94	3.04	3.22	3.52	4.12
		$R_{DS(ON)}$ (MΩ)	23000	2400	250	26	2.7	0.28	0.029	0.01	0.003	0.001	0.0004
ALD810026	2.60	V_{IN} (V)	2.20	2.30	2.40	2.50	2.60	2.70	2.84	2.94	3.12	3.42	4.02
		$R_{DS(ON)}$ (MΩ)	22000	2300	240	25	2.6	0.27	0.028	0.01	0.003	0.001	0.0004
ALD810025	2.50	V_{IN} (V)	2.10	2.20	2.30	2.40	2.50	2.60	2.74	2.84	3.02	3.32	3.92
		$R_{DS(ON)}$ (MΩ)	21000	2200	230	24	2.5	0.26	0.027	0.01	0.003	0.001	0.0004
ALD810024	2.40	V_{IN} (V)	2.00	2.10	2.20	2.30	2.40	2.50	2.64	2.74	2.92	3.22	3.82
		$R_{DS(ON)}$ (MΩ)	20000	2100	220	23	2.4	0.25	0.026	0.009	0.003	0.001	0.0004
ALD810023	2.30	V_{IN} (V)	1.90	2.00	2.10	2.20	2.30	2.40	2.54	2.64	2.82	3.12	3.72
		$R_{DS(ON)}$ (MΩ)	19000	2000	210	22	2.3	0.24	0.025	0.009	0.003	0.001	0.0004
ALD810022	2.20	V_{IN} (V)	1.80	1.90	2.00	2.10	2.20	2.30	2.44	2.54	2.72	3.02	3.62
		$R_{DS(ON)}$ (MΩ)	18000	1900	200	21	2.2	0.23	0.024	0.008	0.003	0.001	0.0004
ALD810021	2.10	V_{IN} (V)	1.70	1.80	1.90	2.00	2.10	2.20	2.34	2.44	2.62	2.92	3.52
		$R_{DS(ON)}$ (MΩ)	17000	1800	190	20	2.1	0.22	0.023	0.008	0.003	0.001	0.0004
ALD810020	2.00	V_{IN} (V)	1.60	1.70	1.80	1.90	2.00	2.10	2.24	2.34	2.52	2.82	3.42
		$R_{DS(ON)}$ (MΩ)	16000	1700	180	19	2.0	0.21	0.022	0.008	0.003	0.001	0.0003
ALD810019	1.90	V_{IN} (V)	1.50	1.60	1.70	1.80	1.90	2.00	2.14	2.24	2.42	2.72	3.32
		$R_{DS(ON)}$ (MΩ)	15000	1600	170	18	1.9	0.20	0.021	0.007	0.002	0.001	0.0003
ALD810018	1.80	V_{IN} (V)	1.40	1.50	1.60	1.70	1.80	1.90	2.04	2.14	2.32	2.62	3.22
		$R_{DS(ON)}$ (MΩ)	14000	1500	160	17	1.8	0.19	0.020	0.007	0.002	0.001	0.0003
ALD810017	1.70	V_{IN} (V)	1.30	1.40	1.50	1.60	1.70	1.80	1.94	2.04	2.22	2.52	3.12
		$R_{DS(ON)}$ (MΩ)	13000	1400	150	16	1.7	0.18	0.019	0.007	0.002	0.001	0.0003
ALD810016	1.60	V_{IN} (V)	1.20	1.30	1.40	1.50	1.60	1.70	1.84	1.94	2.12	2.42	3.02
		$R_{DS(ON)}$ (MΩ)	12000	1300	140	15	1.6	0.17	0.018	0.007	0.002	0.001	0.0003

Selection of an SAB MOSFET device depends on a set of desired voltage vs. current characteristics that closely match the supercapacitor operating V_{IN} voltage and I_{OUT} currents that provide the best leakage and regulation profile of a supercapacitor load. The table lists V_{IN} which corresponds to different supercapacitor load voltages. At each $V_{IN} = V_{GS} = V_{DS}$ bias voltage, a corresponding I_{OUT}, Drain Source ON Current, $I_{DS(ON)}$, is produced by a specific SAB MOSFET, which is equal to the amount of current available to compensate for supercapacitor leakage current inbalances. This current results in an Equivalent ON Resistance $R_{DS(ON)}$ across a supercapacitor cell. Selection of an SAB MOSFET part number operating at maximum supercapacitor operating voltage at an I_{OUT} that corresponds to the maximum supercapacitor leakage current offer the best possible tradeoff between leakage current balancing and voltage regulation.

Notes: 1) The SAB MOSFET Output Current (I_{OUT}) = Drain Source ON Current ($I_{DS(ON)}$) and is the maximum current available to offset the supercapacitor leakage current.
2) The Input Voltage (V_{IN}) = Drain Gate Source Voltage ($V_{GS} = V_{DS}$) and is normally the same as the voltage across the supercapacitor.

TABLE 2. ALD 9100XX SUPERCAPACITOR AUTO BALANCING (SAB™) MOSFETS EQUIVALENT ON RESISTANCE AT DIFFERENT INPUT VOLTAGES AND OUTPUT CURRENTS

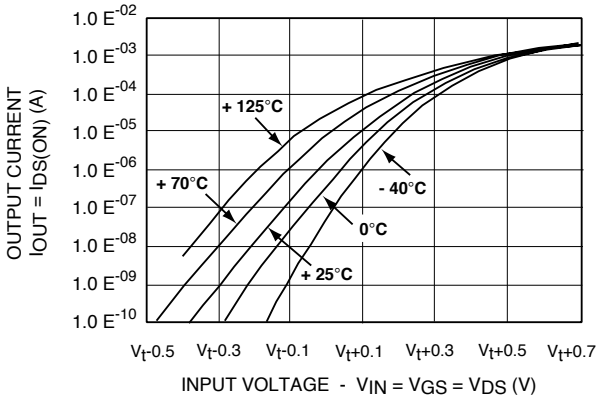
ALD Part Number	Gate-Threshold Voltage V_t (V)	V_{IN} (V)[2] Equivalent ON Resistance (MΩ)	OUTPUT CURRENT I_{OUT} = $I_{DS(ON)}$ (μA)[1] TA = 25°C										
			0.0001	0.001	0.01	0.1	1	10	100	300	1000	3000	10000
ALD910028	2.80	V_{IN} (V)	2.40	2.50	2.60	2.70	2.80	2.90	3.02	3.10	3.24	3.30	3.80
		$R_{DS(ON)}$ (MΩ)	24000	2500	260	27	2.8	0.29	0.030	0.01	0.003	0.001	0.0004
ALD910027	2.70	V_{IN} (V)	2.30	2.40	2.50	2.60	2.70	2.80	2.92	3.00	3.14	3.20	3.70
		$R_{DS(ON)}$ (MΩ)	23000	2400	250	26	2.7	0.28	0.029	0.01	0.003	0.001	0.0004
ALD910026	2.60	V_{IN} (V)	2.20	2.30	2.40	2.50	2.60	2.70	2.82	2.90	3.04	3.10	3.60
		$R_{DS(ON)}$ (MΩ)	22000	2300	240	25	2.6	0.27	0.028	0.01	0.003	0.001	0.0004
ALD910025	2.50	V_{IN} (V)	2.10	2.20	2.30	2.40	2.50	2.60	2.72	2.80	2.94	3.00	3.50
		$R_{DS(ON)}$ (MΩ)	21000	2200	230	24	2.5	0.26	0.027	0.01	0.003	0.001	0.0004
ALD910024	2.40	V_{IN} (V)	2.00	2.10	2.20	2.30	2.40	2.50	2.62	2.70	2.84	2.90	3.40
		$R_{DS(ON)}$ (MΩ)	20000	2100	220	23	2.4	0.25	0.026	0.009	0.003	0.001	0.0003
ALD910023	2.30	V_{IN} (V)	1.90	2.00	2.10	2.20	2.30	2.40	2.52	2.60	2.74	2.80	3.30
		$R_{DS(ON)}$ (MΩ)	19000	2000	210	22	2.3	0.24	0.025	0.009	0.003	0.001	0.0003
ALD910022	2.20	V_{IN} (V)	1.80	1.90	2.00	2.10	2.20	2.30	2.42	2.50	2.64	2.70	3.20
		$R_{DS(ON)}$ (MΩ)	18000	1900	200	21	2.2	0.23	0.024	0.008	0.003	0.001	0.0003
ALD910021	2.10	V_{IN} (V)	1.70	1.80	1.90	2.00	2.10	2.20	2.32	2.40	2.54	2.60	3.10
		$R_{DS(ON)}$ (MΩ)	17000	1800	190	20	2.1	0.22	0.023	0.008	0.003	0.001	0.0003
ALD910020	2.00	V_{IN} (V)	1.60	1.70	1.80	1.90	2.00	2.10	2.22	2.30	2.44	2.50	3.00
		$R_{DS(ON)}$ (MΩ)	16000	1700	180	19	2.0	0.21	0.022	0.008	0.002	0.001	0.0003
ALD910019	1.90	V_{IN} (V)	1.50	1.60	1.70	1.80	1.90	2.00	2.12	2.20	2.34	2.40	2.90
		$R_{DS(ON)}$ (MΩ)	15000	1600	170	18	1.9	0.20	0.021	0.007	0.002	0.001	0.0003
ALD910018	1.80	V_{IN} (V)	1.40	1.50	1.60	1.70	1.80	1.90	2.02	2.10	2.24	2.30	2.80
		$R_{DS(ON)}$ (MΩ)	14000	1500	160	17	1.8	0.19	0.020	0.007	0.002	0.001	0.0003
ALD910017	1.70	V_{IN} (V)	1.30	1.40	1.50	1.60	1.70	1.80	1.92	2.00	2.14	2.20	2.70
		$R_{DS(ON)}$ (MΩ)	13000	1400	150	16	1.7	0.18	0.019	0.007	0.002	0.001	0.0003
ALD910016	1.60	V_{IN} (V)	1.20	1.30	1.40	1.50	1.60	1.70	1.82	1.90	2.04	2.10	2.60
		$R_{DS(ON)}$ (MΩ)	12000	1300	140	15	1.6	0.17	0.018	0.007	0.002	0.001	0.0003

Selection of an SAB MOSFET device depends on a set of desired voltage vs. current characteristics that closely match the supercapacitor operating V_{IN} voltage and I_{OUT} currents that provide the best leakage and regulation profile of a supercapacitor load. The table lists V_{IN} which corresponds to different supercapacitor load voltages. At each $V_{IN} = V_{GS} = V_{DS}$ bias voltage, a corresponding I_{OUT}, Drain Source ON Current, $I_{DS(ON)}$, is produced by a specific SAB MOSFET, which is equal to the amount of current available to compensate for supercapacitor leakage current inbalances. This current results in an Equivalent ON Resistance $R_{DS(ON)}$ across a supercapacitor cell. Selection of an SAB MOSFET part number operating at maximum supercapacitor operating voltage at an I_{OUT} that corresponds to the maximum supercapacitor leakage current offer the best possible tradeoff between leakage current balancing and voltage regulation.

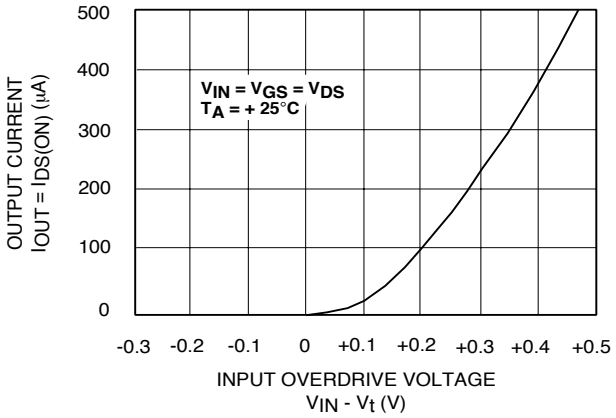
Notes: 1) The SAB MOSFET Output Current (I_{OUT}) = Drain Source ON Current ($I_{DS(ON)}$) and is the maximum current available to offset the supercapacitor leakage current.
2) The Input Voltage (V_{IN}) = Drain Gate Source Voltage ($V_{GS} = V_{DS}$) and is normally the same as the voltage across the supercapacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

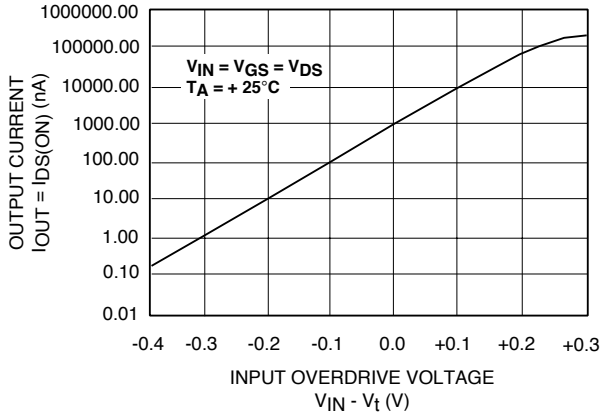
ALD8100xx INPUT VOLTAGE vs. OUTPUT CURRENT



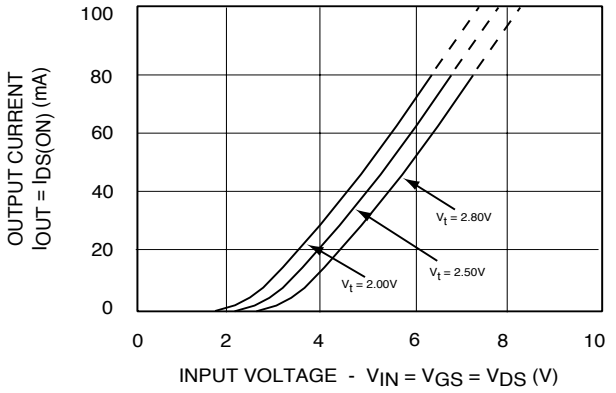
ALD8100xx FORWARD TRANSFER CHARACTERISTICS - LOW VOLTAGE



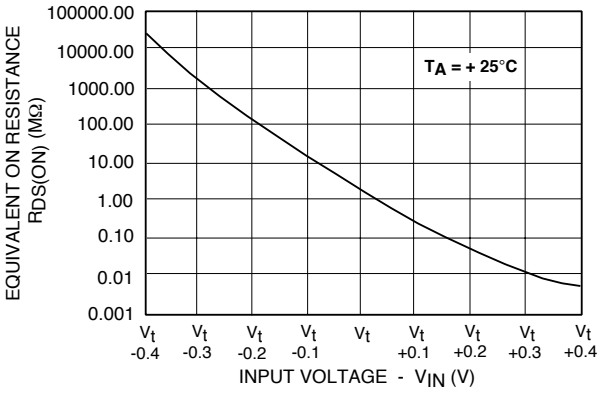
ALD8100xx FORWARD TRANSFER CHARACTERISTICS EXPANDED (SUBTHRESHOLD)



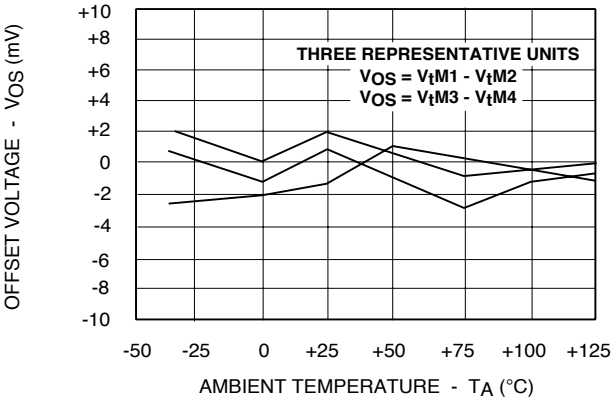
ALD8100xx OUTPUT CHARACTERISTICS



ALD8100xx EQUIVALENT ON RESISTANCE vs. INPUT VOLTAGE

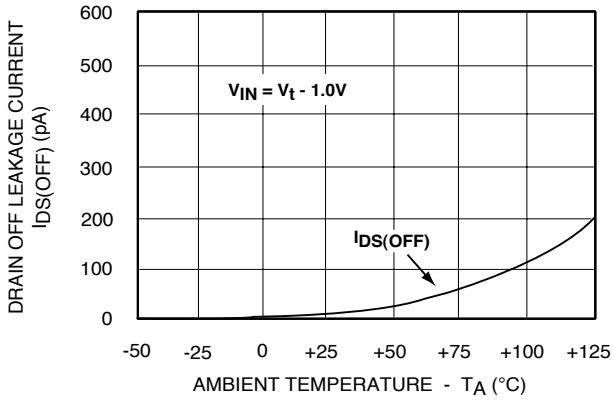


ALD8100xx OFFSET VOLTAGE vs. AMBIENT TEMPERATURE

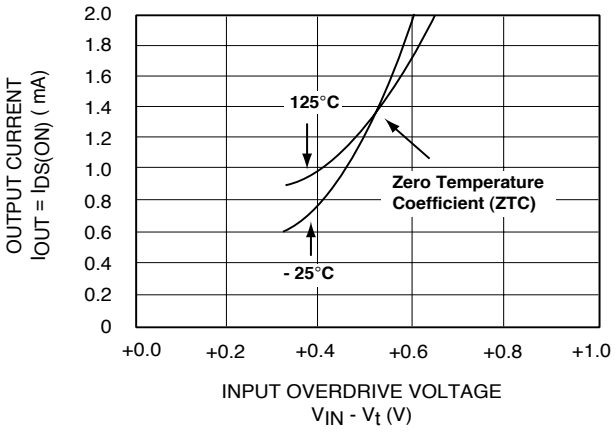


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

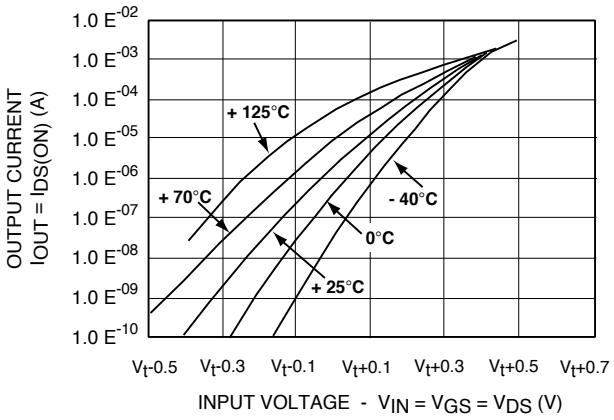
ALD8100xx DRAIN OFF LEAKAGE CURRENT vs. AMBIENT TEMPERATURE



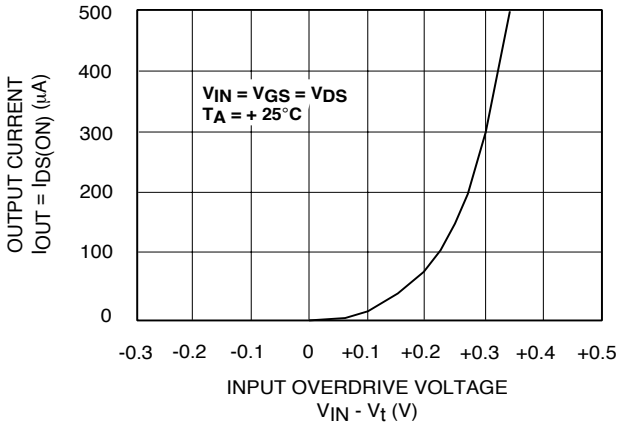
ALD8100xx OUTPUT CURRENT vs. AMBIENT TEMPERATURE



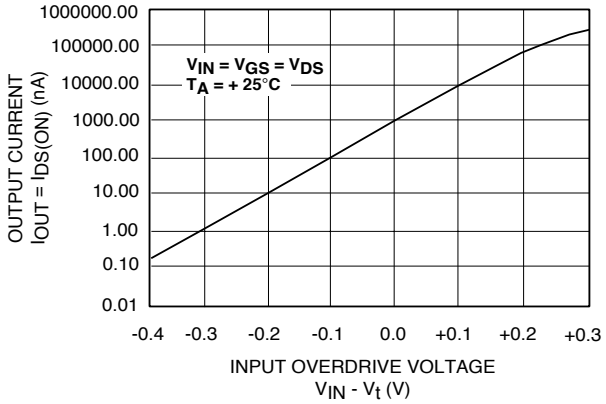
ALD9100xx INPUT VOLTAGE vs. OUTPUT CURRENT



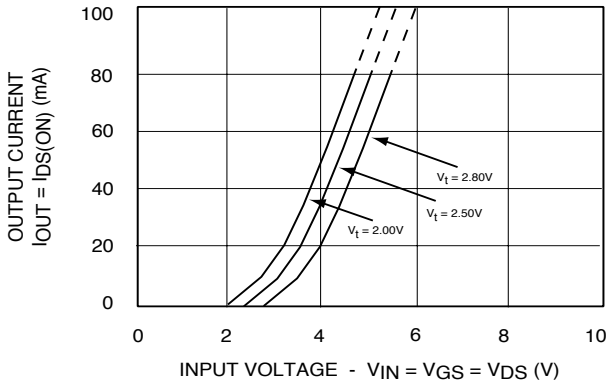
ALD9100xx FORWARD TRANSFER CHARACTERISTICS - LOW VOLTAGE



ALD9100xx FORWARD TRANSFER CHARACTERISTICS EXPANDED (SUBTHRESHOLD)

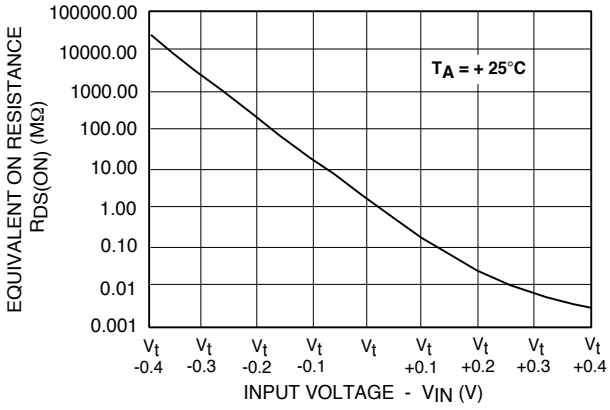


ALD9100xx OUTPUT CHARACTERISTICS

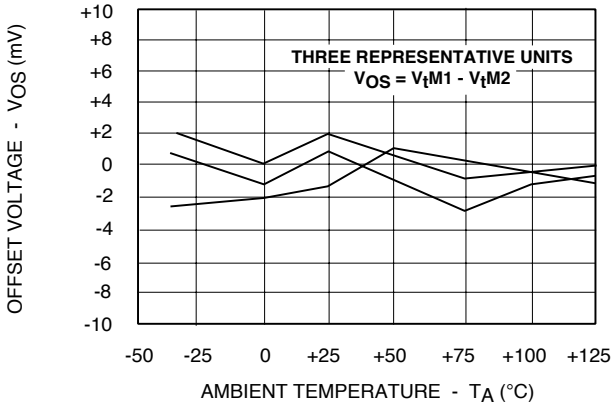


TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

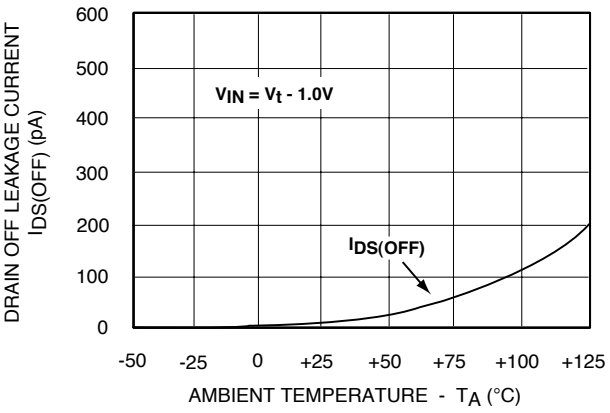
ALD9100xx EQUIVALENT ON RESISTANCE vs. INPUT VOLTAGE



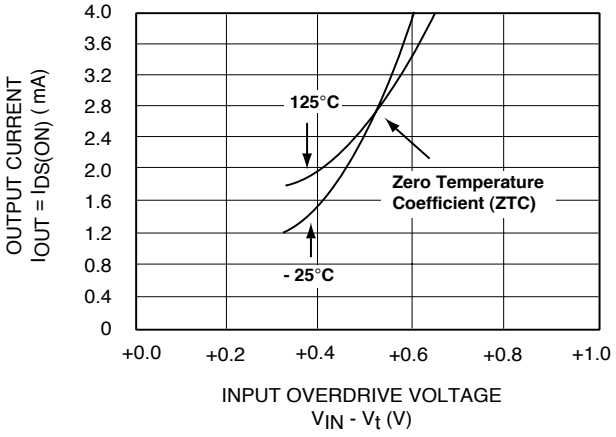
ALD9100xx OFFSET VOLTAGE vs. AMBIENT TEMPERATURE



ALD9100xx DRAIN OFF LEAKAGE CURRENT vs. AMBIENT TEMPERATURE

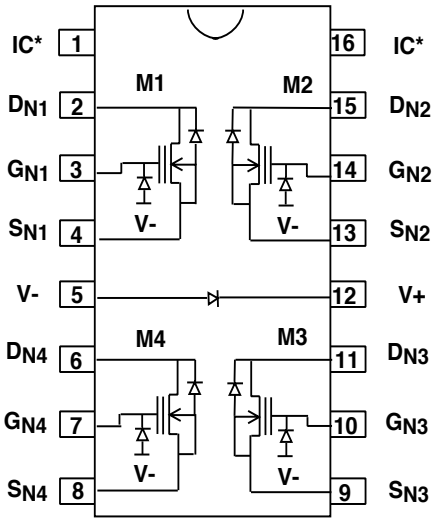


ALD9100xx OUTPUT CURRENT vs. AMBIENT TEMPERATURE

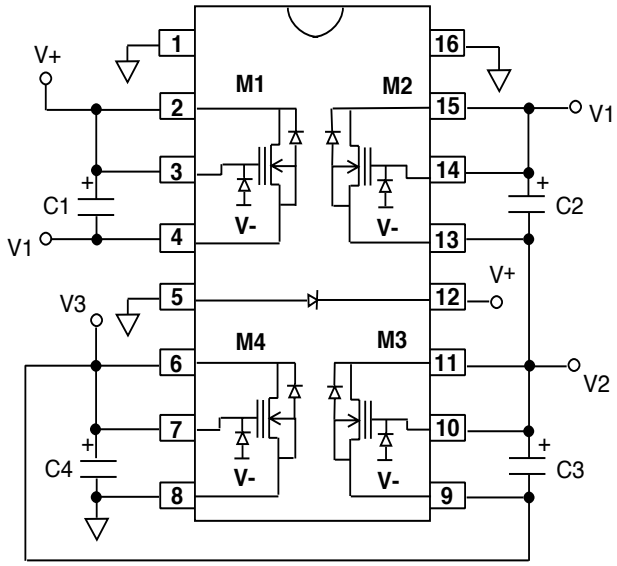


TYPICAL ALD8100XX APPLICATIONS

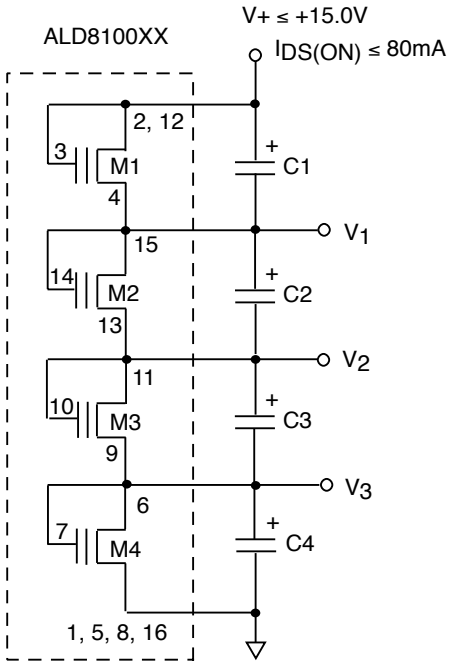
ALD8100xx PIN DIAGRAM



TYPICAL CONNECTION FOR A FOUR-SUPERCAP STACK

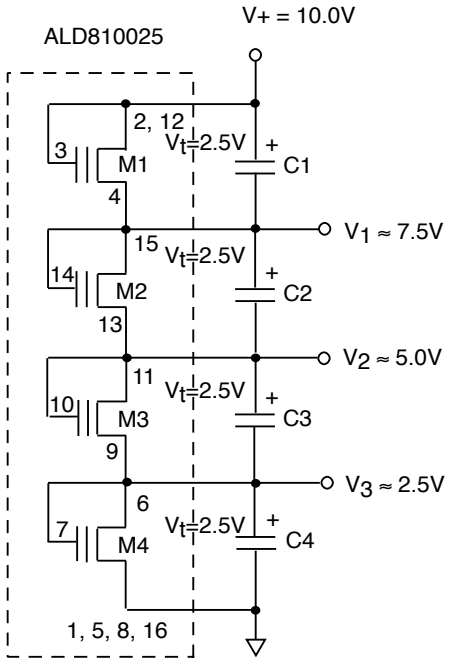


SCHEMATIC DIAGRAM OF A TYPICAL CONNECTION FOR A FOUR-SUPERCAP STACK



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C4 DENOTES SUPERCAPACITORS

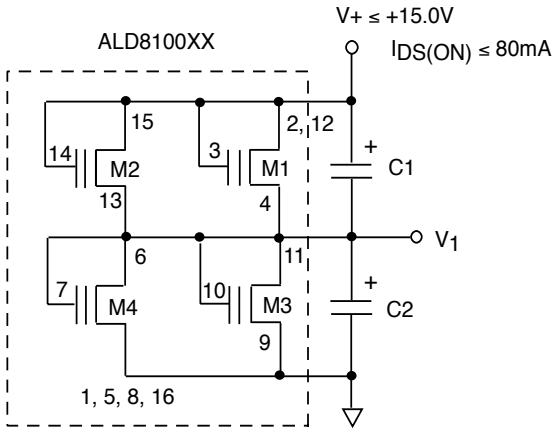
EXAMPLE OF ALD810025 CONNECTION ACROSS FOUR SUPERCAPS IN SERIES



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C4 DENOTES SUPERCAPACITORS

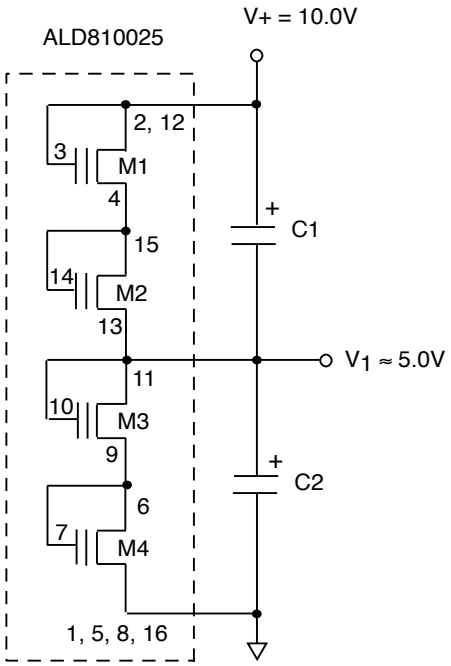
TYPICAL ALD8100XX APPLICATIONS (cont.)

TYPICAL PARALLEL CONNECTION OF SAB MOSFETS WITH TWO SUPERCAPS



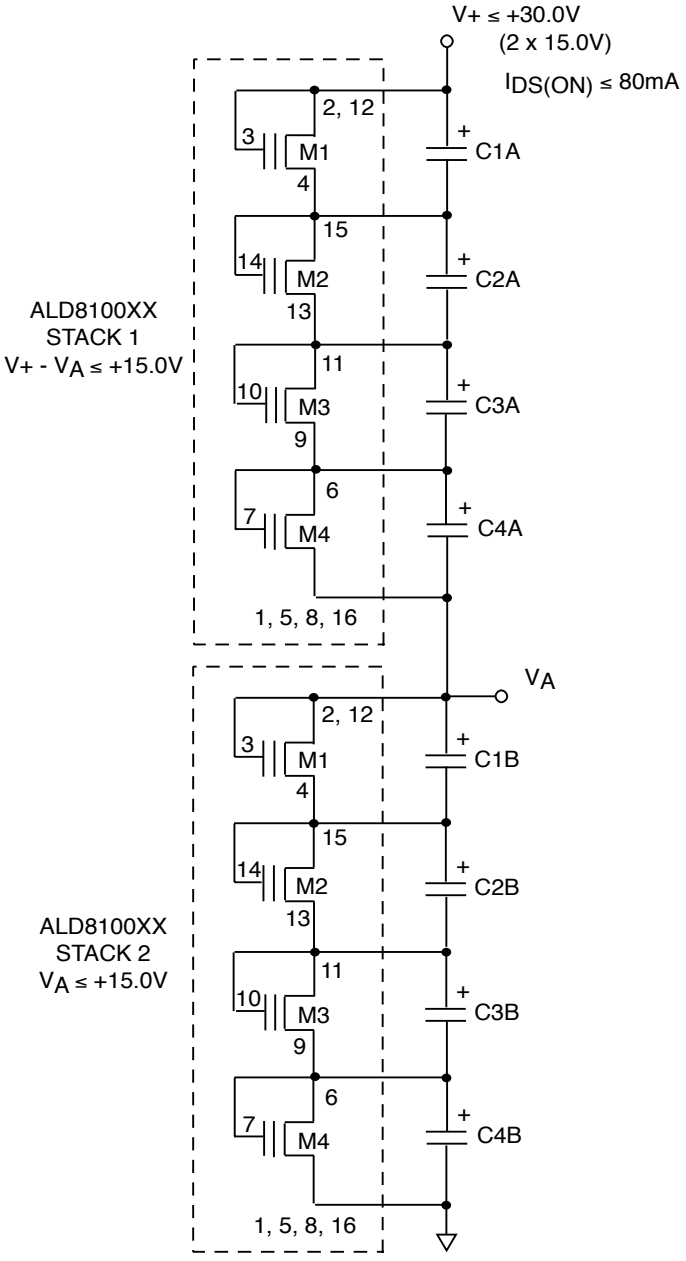
1-16 DENOTES PACKAGE PIN NUMBERS
C1-C2 DENOTES SUPERCAPACITORS

EXAMPLE OF ALD810025 CONNECTION ACROSS TWO SUPERCAPS IN SERIES



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C2 DENOTES SUPERCAPACITORS

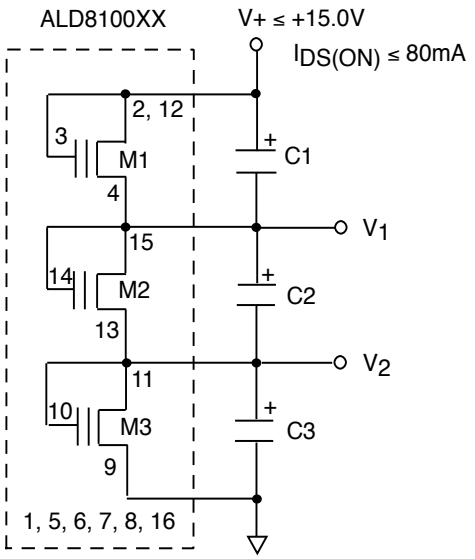
SERIES CONNECTION OF TWO FOUR-SUPERCAP STACKS EACH WITH A SEPARATE SAB MOSFET PACKAGE



1-16 DENOTES PACKAGE PIN NUMBERS
C1A-C4B DENOTES SUPERCAPACITORS

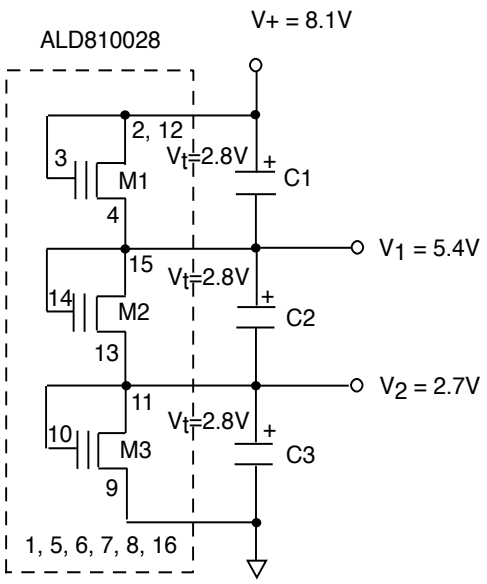
TYPICAL ALD8100XX APPLICATIONS (cont.)

TYPICAL SERIES CONNECTION OF SAB MOSFETS WITH THREE SUPERCAPS



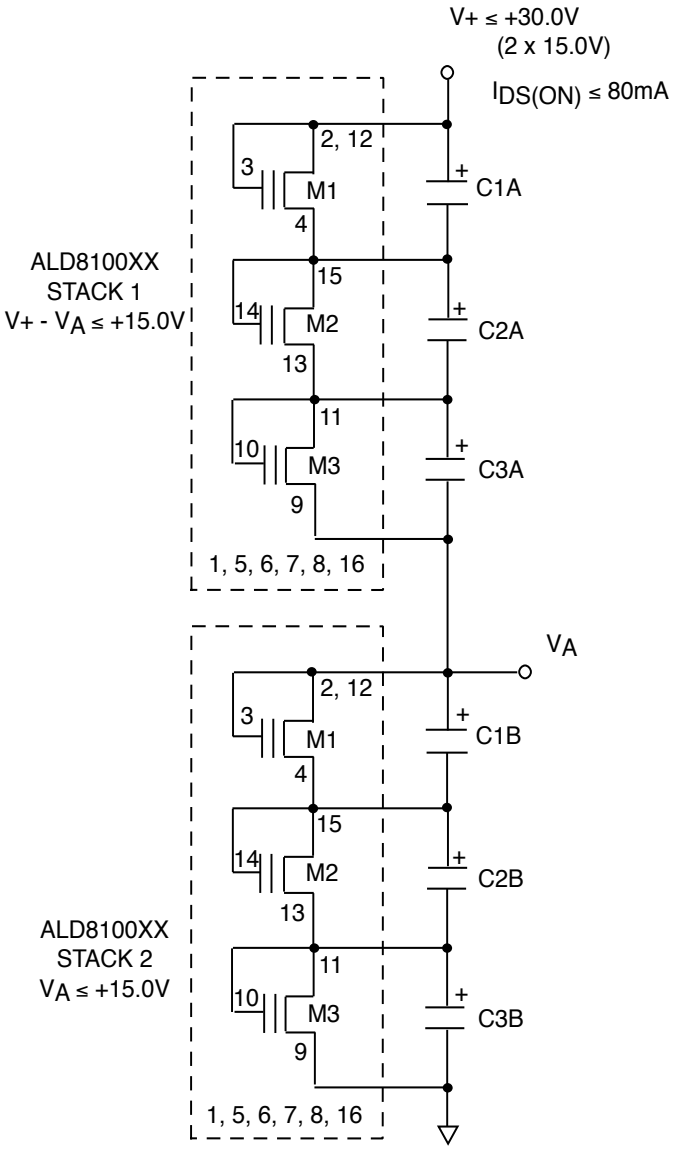
1-16 DENOTES PACKAGE PIN NUMBERS
C1-C3 DENOTES SUPERCAPACITORS

EXAMPLE OF ALD810028 CONNECTION ACROSS THREE SUPERCAPS IN SERIES



1-16 DENOTES PACKAGE PIN NUMBERS
C1-C3 DENOTES SUPERCAPACITORS

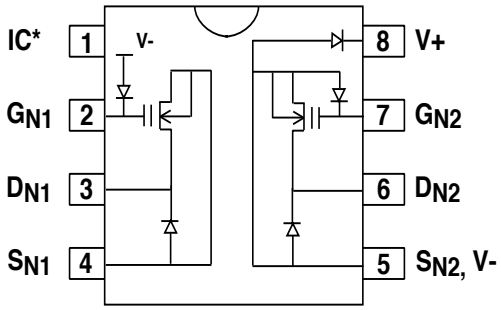
SERIES CONNECTION OF TWO THREE-SUPERCAP STACKS EACH WITH A SEPARATE SAB MOSFET PACKAGE



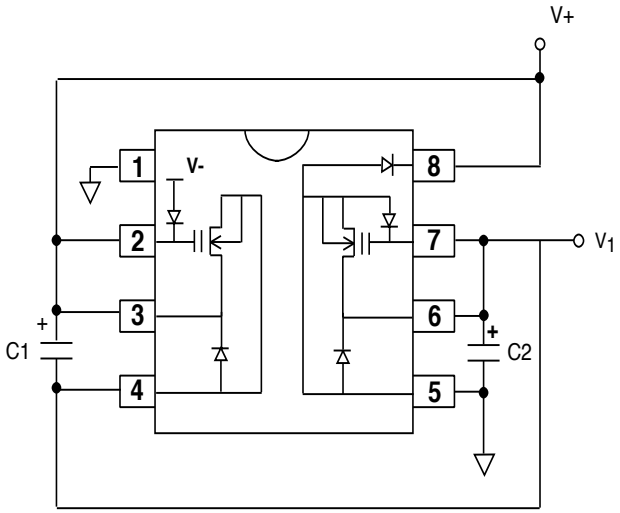
1-16 DENOTES PACKAGE PIN NUMBERS
C1A-C3B DENOTES SUPERCAPACITORS

TYPICAL ALD9100XX APPLICATIONS

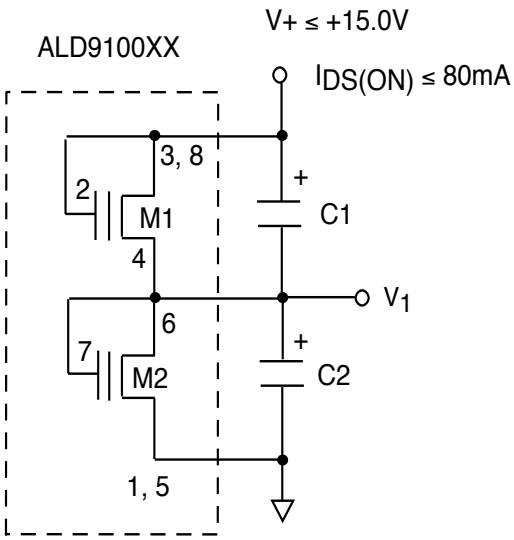
ALD9100XX PIN DIAGRAM



TYPICAL CONNECTION FOR A TWO-SUPERCAP STACK

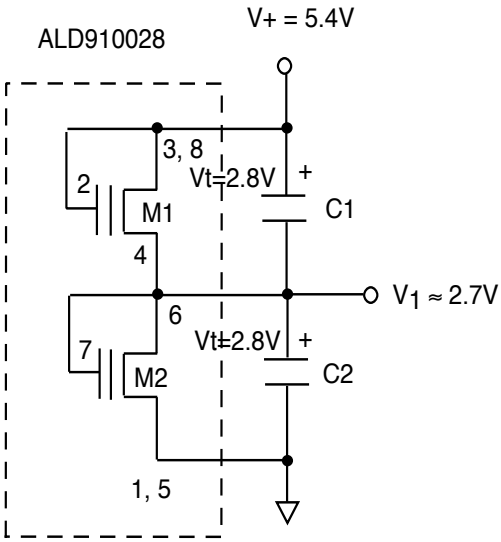


SCHEMATIC DIAGRAM OF A TYPICAL CONNECTION FOR A TWO-SUPERCAP STACK



1-8 DENOTES PACKAGE PIN NUMBERS
C1-C2 DENOTES SUPERCAPACITORS

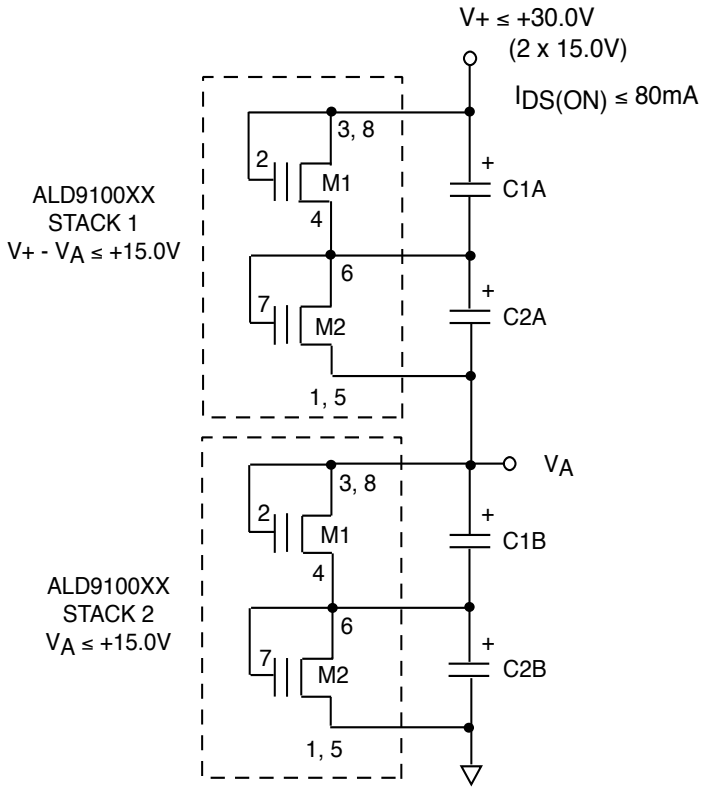
EXAMPLE OF ALD910028 CONNECTION ACROSS TWO SUPERCAPS IN SERIES



1-8 DENOTES PACKAGE PIN NUMBERS
C1-C2 DENOTES SUPERCAPACITORS

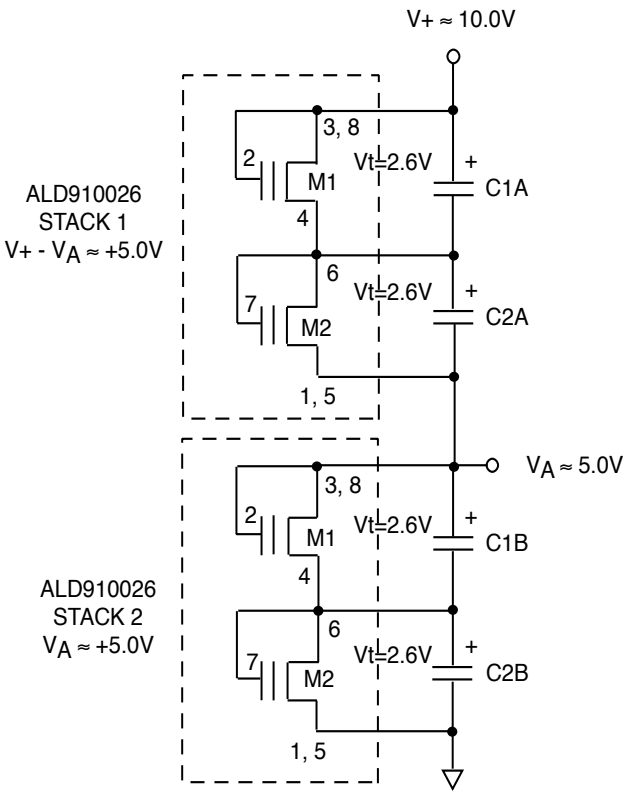
TYPICAL ALD9100XX APPLICATIONS (cont.)

SERIES CONNECTION OF TWO TWO-SUPERCAP STACKS EACH WITH A SEPARATE SAB MOSFET PACKAGE



1-8 DENOTES PACKAGE PIN NUMBERS
C1A-C2B DENOTES SUPERCAPACITORS

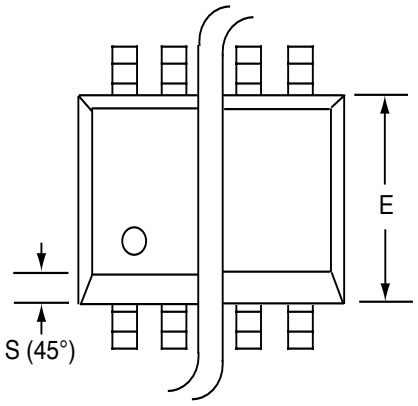
EXAMPLE OF ALD910026 CONNECTION ACROSS TWO TWO-SUPERCAP STACKS EACH WITH A SEPARATE SAB MOSFET PACKAGE

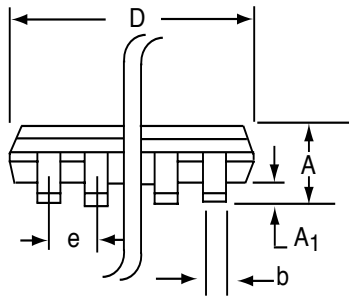


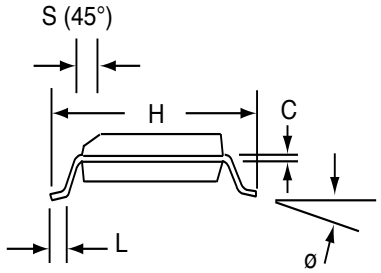
1-8 DENOTES PACKAGE PIN NUMBERS
C1A-C2B DENOTES SUPERCAPACITORS

SOIC-16 PACKAGE DRAWING

16 Pin Plastic SOIC Package



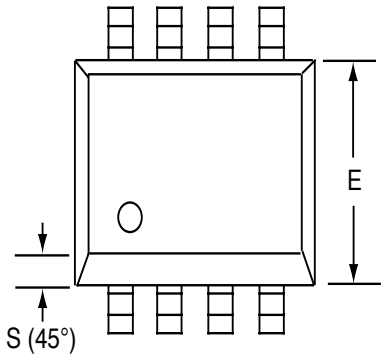


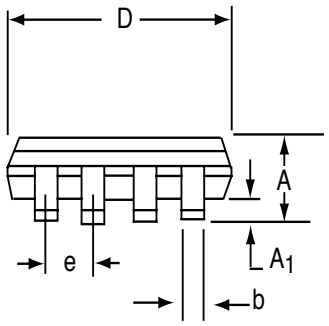


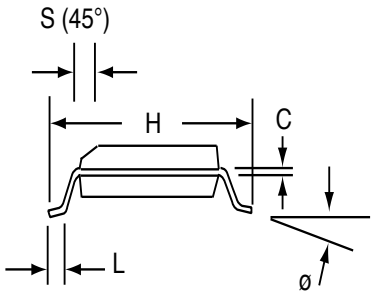
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-16	9.80	10.00	0.385	0.394
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package







Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020