A1373 and A1374

High Precision, Output Pin Programmable Linear Hall Effect Sensor ICs

Discontinued Product

These devices are no longer in production. The devices should not be purchased for new design applications. Samples are no longer available.

Date of status change: October 31, 2011

Recommended Substitutions:

Contact Allegro Sales for more information.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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A1373 and A1374

High Precision, Output Pin Programmable Linear Hall Effect Sensor ICs

Features and Benefits

- Output pin programming
- Field-programmable for optimal application integration
- Selectable coarse and fine gain and quiescent output voltage
- Selectable sensitivity temperature coefficient
- Selectable output clamp voltage level, including no-clamp (rail-to-rail)
- Selectable output polarity
- Unipolar or bipolar operation
- Ratiometric sensitivity, clamps, and quiescent output voltage
- Chopper-stabilized Hall technique
- Wide operating temperature range
- On-chip regulator for over/under voltage protection
- On-chip regulator provides EMI robustness
- Wide lead-spacing with KB package

Package: 3 pin SIP (suffix KB)

Not to scale

Description

The A1373 and A1374 high precision linear Hall effect sensor ICs are sensitive, temperature stable, linear devices with externally programmable features. This device family incorporates a chopper-stabilized amplifier, voltage regulator, programming logic, and an output amplifier on a single IC. The patented dynamic offset cancellation used with a chopper-stabilization technique provides extremely low offset and minimal temperature drift. A high frequency clock is used for chopping, to ensure high frequency signal processing capability. The A1373 and A1374 are ideal for use in automotive and industrial linear position-sensing applications that require increased reliability and accuracy over conventional contacting-potentiometer solutions. Key applications include: throttle position sensors, pedal position sensors, and suspension height sensors.

The design and manufacturing flexibility of the A1373 and A1374 complement the Allegro linear Hall effect family of devices by offering programmable gain, quiescent offset voltage for unipolar or bipolar operation, temperature coefficient, clamps, and polarity. The device can be set up in a magnetic circuit and programmed with a train of serial pulses via the output

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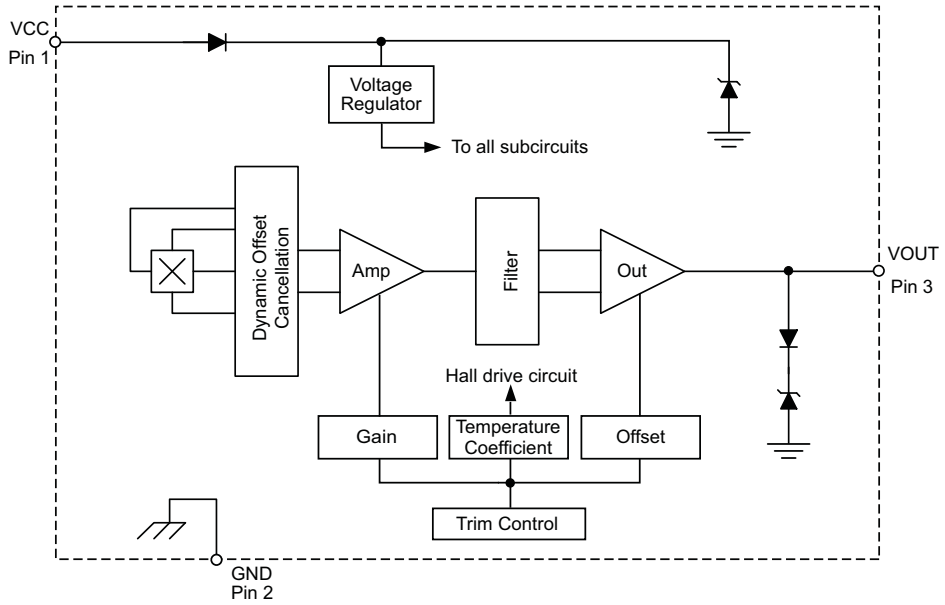
Functional Block Diagram



Description (continued)

pin. Once the right combination of gain, quiescent output voltage, and temperature coefficient has been selected, the codes can be locked for one-time programming. In this manner, manufacturing tolerances can be reduced and the assembly process can be simplified.

These devices are available in the KB package, a 3-pin SIP (single inline package). The lead (Pb) free version has a 100% matte tin plated leadframe.

Selection Guide

Part Number	Packing*	Ambient, T_A (ºC)
A1373EKB–T	Bulk, 500 pieces / bag	–40 to 85
A1373LKB–T	Bulk, 500 pieces / bag	–40 to 150
A1374EKB–T	Bulk, 500 pieces / bag	–40 to 85
A1374LKB–T	Bulk, 500 pieces / bag	–40 to 150

*Contact Allegro for additional packing options.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		16	V
Reverse Supply Voltage	V_{RCC}		–16	V
Output Voltage	V_{OUT}	When blowing fuses during device programming, a voltage of 28 V may be applied to VOUT.	16	V
Reverse-Output Voltage	V_{ROUT}		–0.1	V
Output Source Current	$I_{OUTSOURCE}$		3	mA
Output Sink Current	$I_{OUTSINK}$		10	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

CHARACTERISTIC PARAMETERS

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max	Units
ELECTRICAL CHARACTERISTICS over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted							
Supply Voltage	V_{CC}	Operation within specification, T_j < 165°C		4.5	5.0	5.5	V
Supply Current	I_{CC}			–	8.2	10	mA
Reverse-Supply Current	I_{RCC}	V_{CC} = –16 V, T_A = 25°C		–	–	16	mA
Power-On Time[1]	t_{PO}	C_{LOAD} = 10 nF, 90% full scale V_{OUT}		–	–	300	µs
Chopping Frequency	f_C			–	200	–	kHz
Internal Bandwidth	BW	A1373	Small signal -3 dB	–	2.5	–	kHz
		A1374		–	20	–	kHz
OUTPUT CHARACTERISTICS over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted							
Noise[2,3]	V_N	A1373	peak-to-peak, C_{LOAD} > 1 nF, 2.5 mV/G	–	6	16	mV
		A1374		–	14	26	mV
Output Capacitance Load	C_{LOAD}	VOUT pin to GND pin		–	–	10	nF
Output Resistive Load	R_{LOAD}			4700	–	–	Ω
Phase Shift	ΔΦ	A1373	Magnetic signal freq. = 100 Hz	–	3	–	(°)
		A1374	Magnetic signal freq. = 1000 Hz	–	3	–	(°)
Output Voltage	$V_{OUT(Sat)HIGH}$	$I_{OUTSOURCE}$ = 1.2 mA, B(kG) > (V_{CC}–$V_{OUT(Q)}$) / Sens (mV/G)		4.65	4.7	–	V
	$V_{OUT(Sat)LOW}$	$I_{OUTSINK}$ = 1.2 mA, B(kG) < $V_{OUT(Q)}$ / Sens (mV/G)		–	0.2	0.25	V
Output Resistance	R_{OUT}			–	1.5	–	Ω
MAGNETIC CHARACTERISTICS							
Magnetic Slew Rate	SLR	V / ms / Sens		–	20	–	G/µs
PRE-PROGRAMMING TARGET (Prior to coarse and fine trim) over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted							
Pre-Programming Quiescent Output Voltage	$V_{OUT(Q)PRE}$	B = 0 G, T_A = 25°C		1.62	1.80	1.98	V
Pre-Programming Sensitivity	$Sens_{PRE}$	T_A = 25°C		1.05	1.31	1.75	mV/G
Pre-Programming Sensitivity Temperature Coefficient	TC_{PRE}	T_A relative to 25°C		–0.016	0.05	0.104	%/°C
INITIAL COARSE PROGRAMMING over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted							
Initial Coarse Quiescent Output Voltage	$V_{OUT(Q)INITLOW}$	T_A = 25°C		–	0.55	–	V
	$V_{OUT(Q)INITMID}$	Reference $V_{OUT(Q)PRE}$		–	––	–	V
	$V_{OUT(Q)INITHIGH}$	T_A = 25°C		–	3.25	–	V
Initial Coarse Sensitivity	$Sens_{INITLOW}$	Reference $Sens_{PRE}$		–	–	–	mV/G
	$Sens_{INITMID}$	T_A = 25°C		–	2.8	–	mV/G
	$Sens_{INITHIGH}$	T_A = 25°C		–	5.5	–	mV/G

Continued on the next page...

CHARACTERISTIC PARAMETERS (continued)

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max	Units
QUIESCENT OUTPUT VOLTAGE PROGRAMMING over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted							
Quiescent Output Voltage Range	$V_{OUT(Q)LOW}$	B = 0 G, T_A = 25°C		0.7	–	1.9	V
	$V_{OUT(Q)MID}$			2.0	–	3.2	V
	$V_{OUT(Q)HIGH}$			3.5	–	4.5	V
Average Quiescent Output Voltage Step Size[4,5,6]	$Step_{VOUT(Q)}$	T_A = 25°C		3.0	3.275	3.5	mV
Quiescent Output Voltage Programming Resolution	$Err_{PROGVOUT(Q)}$	Fine programming value selection accuracy		–	±0.5 × $Step_{VOUT(Q)}$	–	mV
Quiescent Output Voltage Drift Over Operating Temperature Range	$\Delta V_{OUT(Q)}$	$V_{OUT(Q)}$ = $V_{OUT(Q)LOW}$		–	–	±40	mV
		$V_{OUT(Q)}$ = $V_{OUT(Q)MID}$		–	–	±40	mV
		$V_{OUT(Q)}$ = $V_{OUT(Q)HIGH}$		–	–	±55	mV
Quiescent Output Voltage Programming Bits	–	Coarse (Range selection)		–	2	–	Bit
		Fine (Value selection)		–	9	–	Bit
10% Output Clamp Option[7]	$V_{OUTCLP10HIGH}$	A1373	High-side output clamp	4.350	–	4.565	V
		A1374		4.300	–	4.650	V
	$V_{OUTCLP10LOW}$	A1373	Low-side output clamp	0.4	–	0.6	V
		A1374		0.3	–	0.6	V
20% Output Clamp Option[7]	$V_{OUTCLP20HIGH}$	A1373	High-side output clamp	3.925	–	4.125	V
		A1374		3.900	–	4.200	V
	$V_{OUTCLP20LOW}$	A1373	Low-side output clamp	0.9	–	1.1	V
		A1374		0.8	–	1.1	V
Delay to Clamp	t_{CLP}	A1373		–	–	2	µs
		A1374		–	–	100	µs
SENSITIVITY PROGRAMMING over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted							
Sensitivity Range[8]	$Sens_{LOW}$	T_A = 25°C		1.75	–	2.8	mV/G
	$Sens_{MID}$			3.5	–	5.7	mV/G
	$Sens_{HIGH}$			7.0	–	11.25	mV/G
Average Sensitivity Step Size[4,5,6]	$Step_{SENSLOW}$	T_A = 25°C		6	9.5	14	µV/G
	$Step_{SENSMID}$			12	18.7	28	µV/G
	$Step_{SENSHIGH}$			22	37.0	56	µV/G
Sensitivity Programming Resolution	$Err_{PROGSENS}$	Fine programming value selection accuracy		–	±0.5 × $Step_{SENS}$	–	µV/G
Sensitivity Programming Bits	–	Coarse (Range selection)		–	2	–	Bit
		Fine (Value selection)		–	8	–	Bit
POLARITY PROGRAMMING							
Polarity Programming Bit	–	Negative Sensitivity		–	1	–	Bit

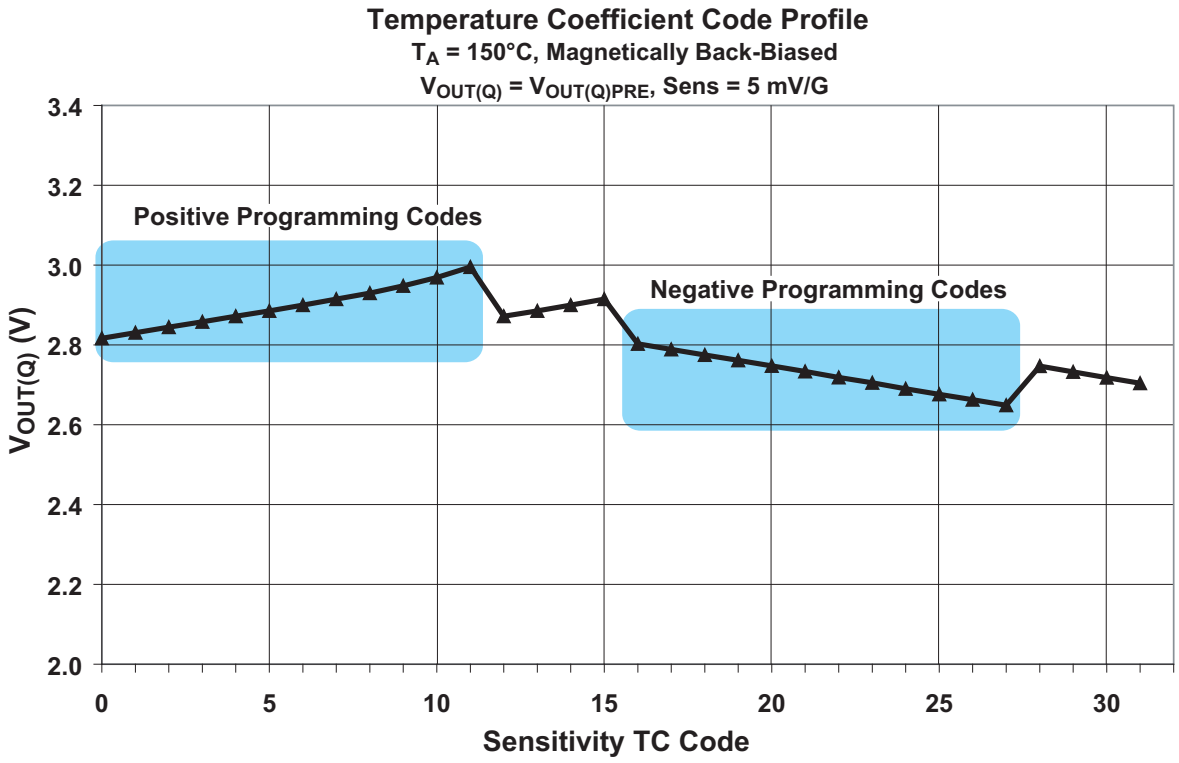
Continued on the next page...

CHARACTERISTIC PARAMETERS (continued)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max	Units
SENSITIVITY TEMPERATURE COEFFICIENT PROGRAMMING over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted						
Sensitivity Temperature Coefficient Range	TC	*Sensitivity T/C* codes 0 to 11, minimum (absolute) positive temperature coefficient attainable	–	0.07	–	%/°C
		Sensitivity T/C codes 16 to 27, minimum (absolute) negative temperature coefficient attainable	–	–0.016	–	%/°C
Average Sensitivity Temperature Coefficient Step Size[4,5,6]	$Step_{TC}$	T_A = 150°C	–	0.01	–	%/°C
Sensitivity Temperature Coefficient Programming Bits	–		–	5	–	Bit
ONE-TIME PROGRAMMING						
Device Programming Lock Bit	–		–	1	–	Bit
RATIOMETRY over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted						
Quiescent Voltage Error	$Rat_{VOUT(Q)}$	V_{CC} at $V_{OPERATING}$	–	±0.25	–	%
Sensitivity Error	Rat_{SENS}	V_{CC} at $V_{OPERATING}$	–	±1.0	–	%
Clamp Error	$Rat_{VOUTCLP}$	V_{CC} at $V_{OPERATING}$	–	±1.5	–	%
LINEARITY over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted						
Positive Linearity Error	Lin+	V_{CC} at $V_{OPERATING}$	–	±0.5	–	%
Negative Linearity Error	Lin–	V_{CC} at $V_{OPERATING}$	–	±0.5	–	%
SYMMETRY over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted						
Symmetry Error	Sym	V_{CC} at $V_{OPERATING}$ – V_{CC}	–	±0.35	–	%
ADDITIONAL CHARACTERISTICS						
Sensitivity Drift[9]	ΔSens		–	–	±2	%
Package Thermal Resistance	$R_{\theta JA}$	1 layer PCB with copper limited to solder pads; see Allegro web site for additional thermal information	–	177	–	°C/W
FAULT CONDITIONS over operating temperature range, V_{CC} = 5.0 V, unless otherwise noted						
Shorted Output Wire	I_{OUTSHT}	VOUT pin to VCC pin	–	–	18	mA
		VOUT pin to GND pin	–	–	4	mA

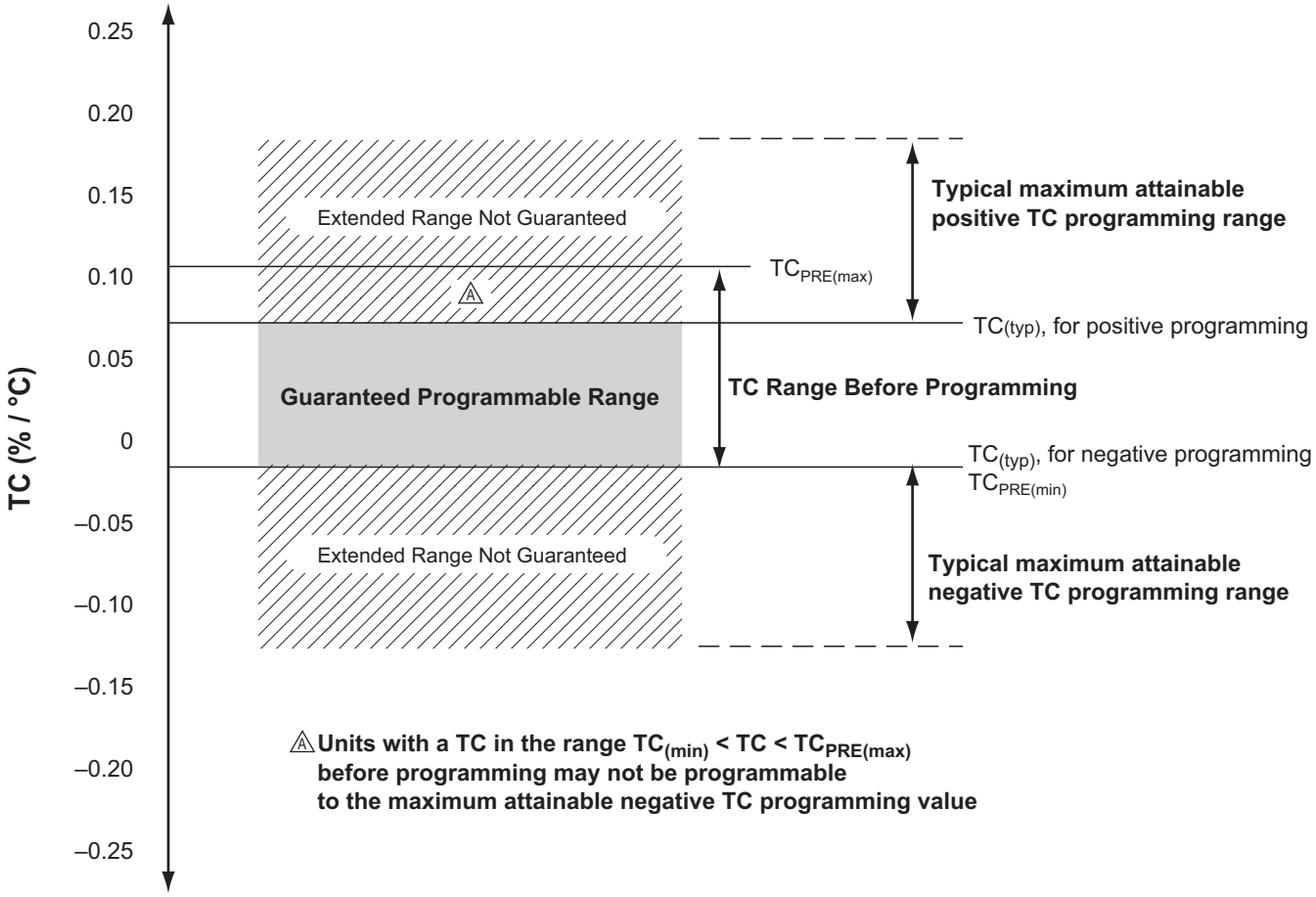
[1] t_{PO} does not include t_{CLP}, specified in the Quiescent Programming section of this table.
[2] Peak to peak value exceeded: 0.3% (6σ).
[3] For A1373, no digital noise is present at the output.
[4] Step size is larger than required for the specified range, to take into account manufacturing spread.
[5] Individual code step sizes can be greater than 2× larger than the step size at each significant bit rollover.
[6] Average fine code step size in a given range = (Output value at highest fine code in the range – Output value at code 0 of the range) / Total quantity of steps (codes) in the range.
[7] Values indicated are valid if any additional magnetic field does not exceed B(kG)= ±2 (V)/Sens (mv/G), after V_{OUTCLP} is reached.
[8] Program the *Sensitivity T/C* register before programming *Sensitivity Coarse* and *Sensitivity Fine*, due to a worst case shift of ±3% in sensitivity at 25°C at the maximum values for *Sensitivity T/C: Positive T/C* and *Sensitivity T/C: Negative T/C*. The Programming Guidelines section in this document lists a complete recommended order for programming individual values.
[9] Drift due to temperature cycling is due to package effects on the Hall transducer. The stress is reduced when the package is baked. However, it will recover over time after removal from the bake.

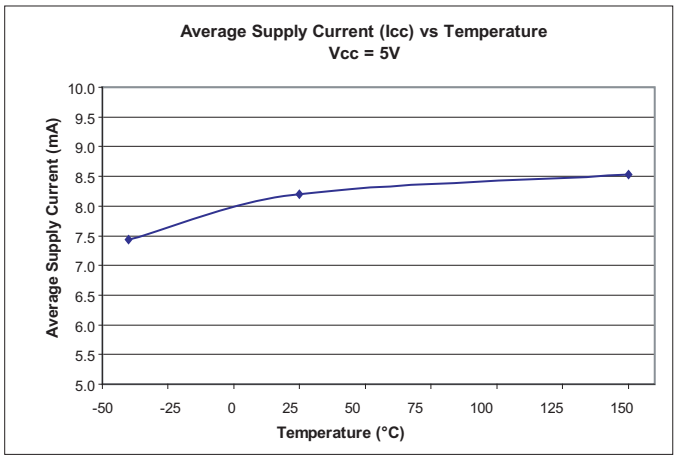
Typical Characteristics

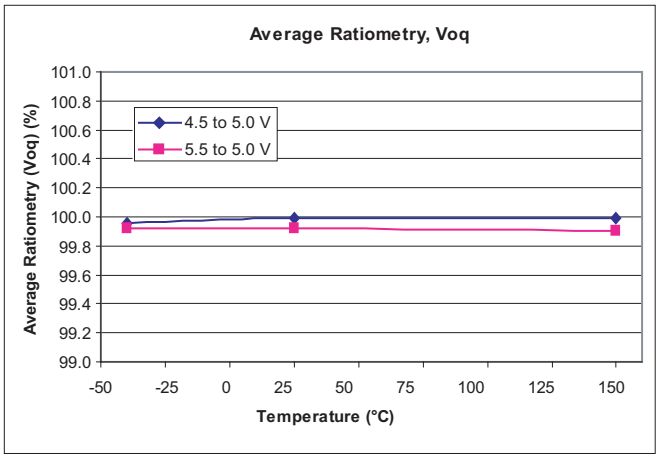


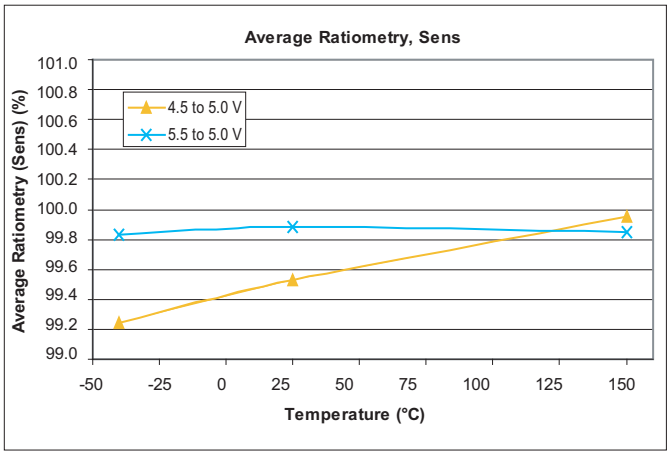
Code	Application
0	Initial code
1 – 11	Positive TC codes, use to increase TC value
12 – 15	[Unused, same effect as 4 – 7, respectively]
16 – 27	Negative TC codes, use to decrease TC value
28 – 31	[Unused, same effect as 20 – 23, respectively]

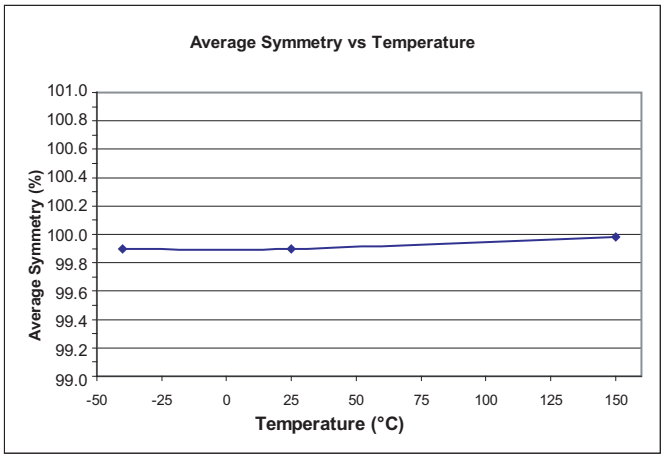
Sensitivity Temperature Coefficient Range, TC

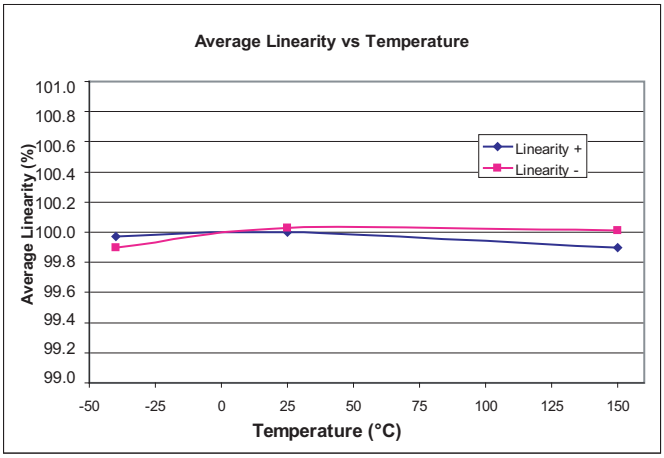


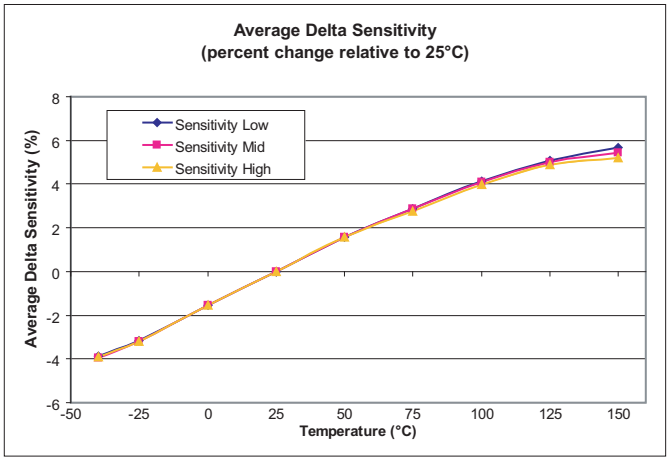

Average Supply Current (Icc) vs Temperature
Vcc = 5V
Average Supply Current (mA)
10.0
9.5
9.0
8.5
8.0
7.5
7.0
6.5
6.0
5.5
5.0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)

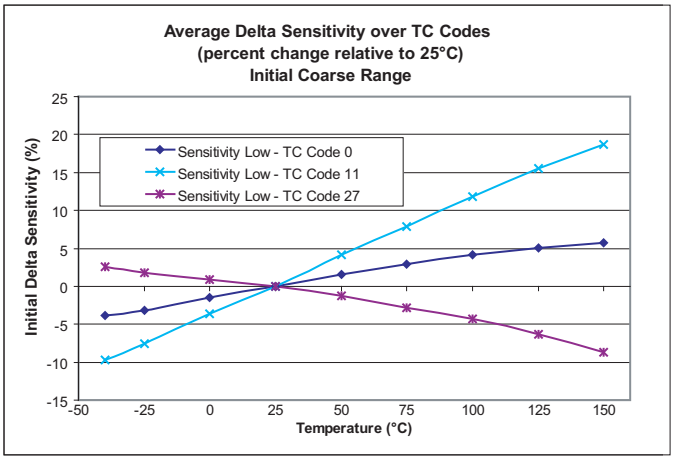

Average Ratiometry, Voq
Average Ratiometry (Voq) (%)
4.5 to 5.0 V
5.5 to 5.0 V
101.0
100.8
100.6
100.4
100.2
100.0
99.8
99.6
99.4
99.2
99.0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)

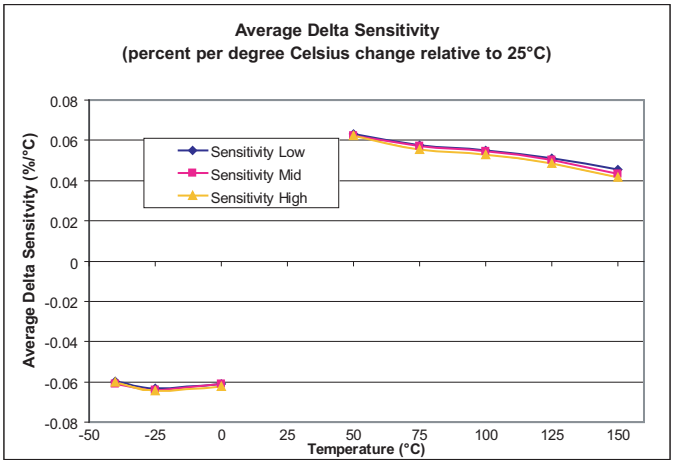

Average Ratiometry, Sens
Average Ratiometry (Sens) (%)
4.5 to 5.0 V
5.5 to 5.0 V
101.0
100.8
100.6
100.4
100.2
100.0
99.8
99.6
99.4
99.2
99.0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)

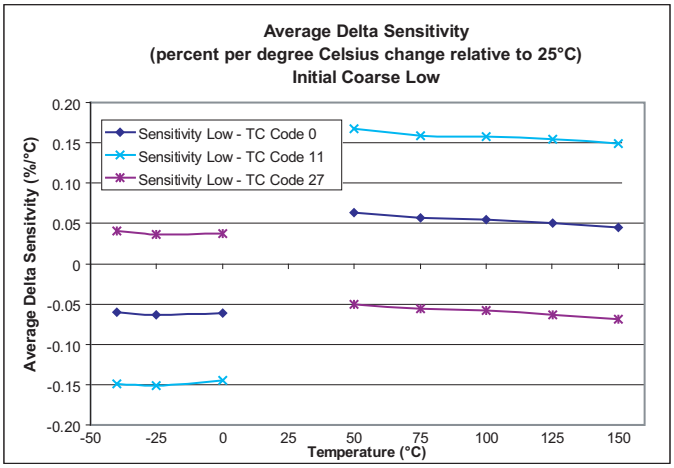

Average Symmetry vs Temperature
Average Symmetry (%)
101.0
100.8
100.6
100.4
100.2
100.0
99.8
99.6
99.4
99.2
99.0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)

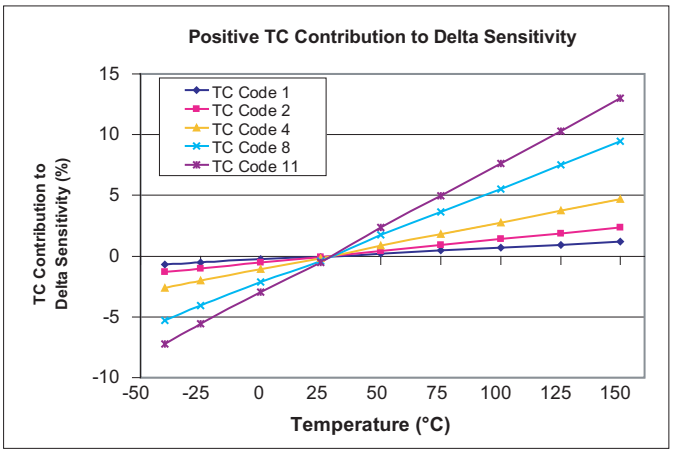

Average Linearity vs Temperature
Average Linearity (%)
Linearity +
Linearity -
101.0
100.8
100.6
100.4
100.2
100.0
99.8
99.6
99.4
99.2
99.0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)

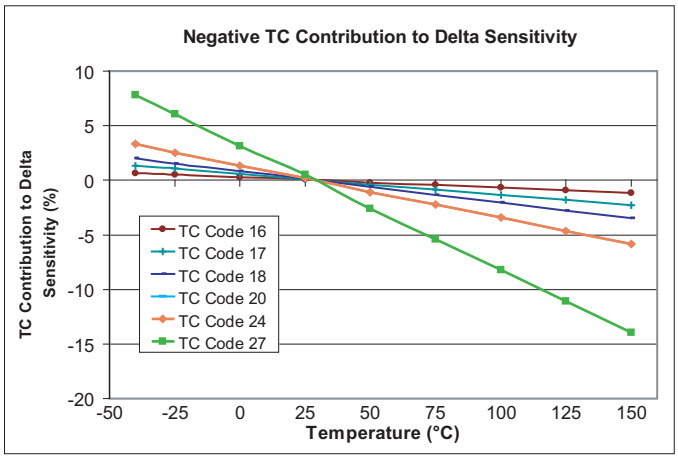

Average Delta Sensitivity
(percent change relative to 25°C)
Sensitivity Low
Sensitivity Mid
Sensitivity High
Average Delta Sensitivity (%)
Temperature (°C)

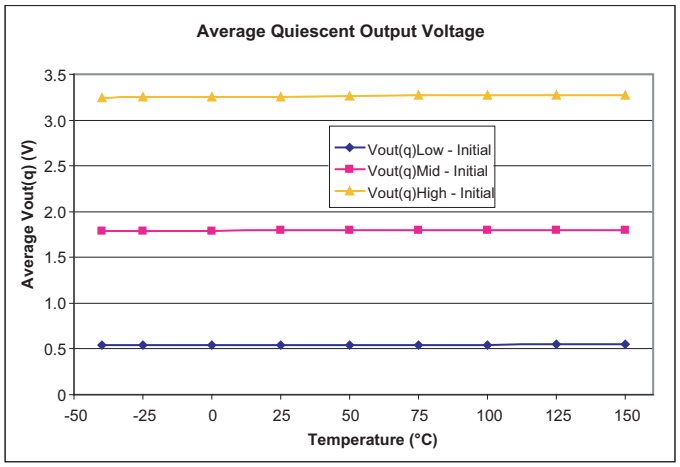

Average Delta Sensitivity over TC Codes
(percent change relative to 25°C)
Initial Coarse Range
Sensitivity Low - TC Code 0
Sensitivity Low - TC Code 11
Sensitivity Low - TC Code 27
Initial Delta Sensitivity (%)
Temperature (°C)

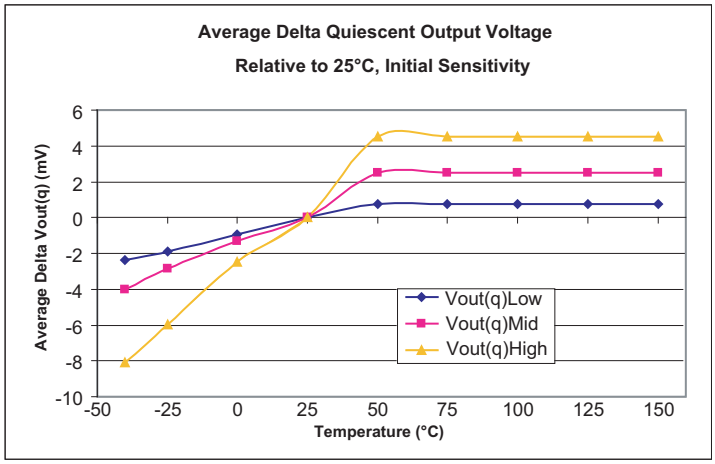

Average Delta Sensitivity
(percent per degree Celsius change relative to 25°C)
Sensitivity Low
Sensitivity Mid
Sensitivity High
Average Delta Sensitivity (%/°C)
Temperature (°C)

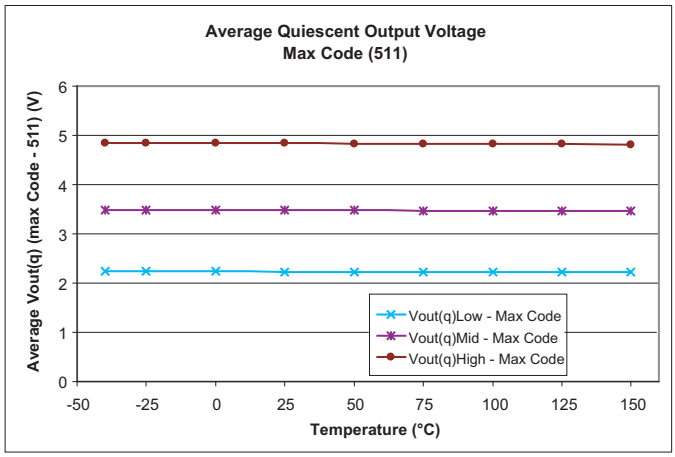

Average Delta Sensitivity
(percent per degree Celsius change relative to 25°C)
Initial Coarse Low
Sensitivity Low - TC Code 0
Sensitivity Low - TC Code 11
Sensitivity Low - TC Code 27
Average Delta Sensitivity (%/°C)
Temperature (°C)

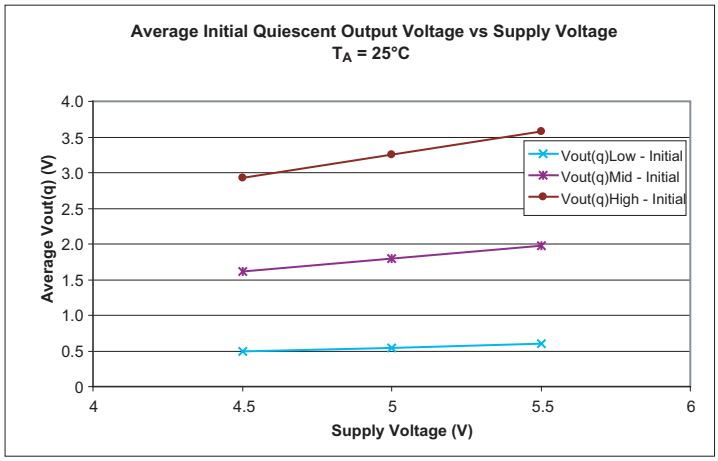

Positive TC Contribution to Delta Sensitivity
TC Code 1
TC Code 2
TC Code 4
TC Code 8
TC Code 11
TC Contribution to Delta Sensitivity (%)
Temperature (°C)

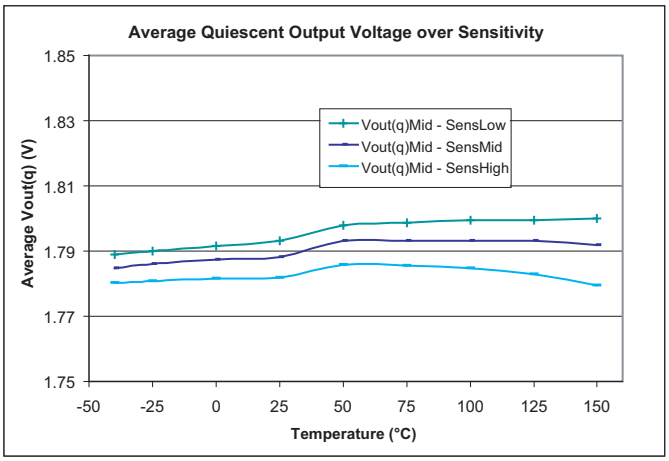

Negative TC Contribution to Delta Sensitivity
TC Code 16
TC Code 17
TC Code 18
TC Code 20
TC Code 24
TC Code 27
TC Contribution to Delta Sensitivity (%)
Temperature (°C)

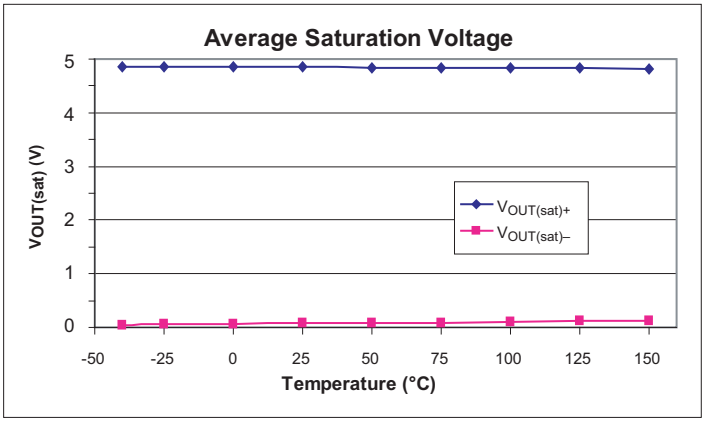

Average Quiescent Output Voltage
Average Vout(q) (V)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)
Vout(q)Low - Initial
Vout(q)Mid - Initial
Vout(q)High - Initial

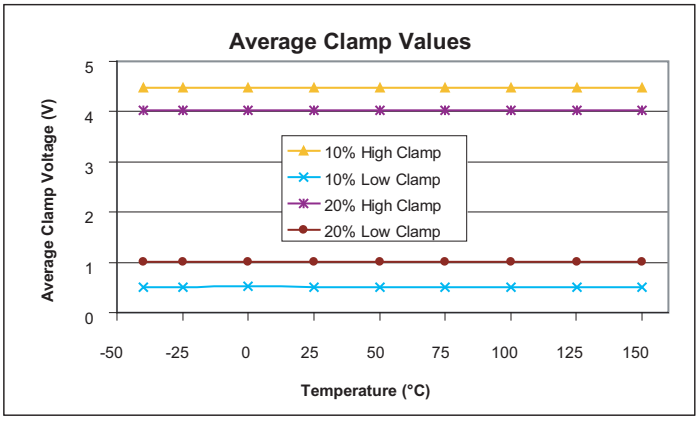

Average Delta Quiescent Output Voltage
Relative to 25°C, Initial Sensitivity
Average Delta Vout(q) (mV)
6
4
2
0
-2
-4
-6
-8
-10
-50
-25
0
25
50
75
100
125
150
Temperature (°C)
Vout(q)Low
Vout(q)Mid
Vout(q)High


Average Quiescent Output Voltage
Max Code (511)
Average Vout(q) (max Code - 511) (V)
6
5
4
3
2
1
0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)
Vout(q)Low - Max Code
Vout(q)Mid - Max Code
Vout(q)High - Max Code


Average Initial Quiescent Output Voltage vs Supply Voltage
T_A = 25°C
Average Vout(q) (V)
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
4
4.5
5
5.5
6
Supply Voltage (V)
Vout(q)Low - Initial
Vout(q)Mid - Initial
Vout(q)High - Initial


Average Quiescent Output Voltage over Sensitivity
Average Vout(q) (V)
1.85
1.83
1.81
1.79
1.77
1.75
-50
-25
0
25
50
75
100
125
150
Temperature (°C)
Vout(q)Mid - SensLow
Vout(q)Mid - SensMid
Vout(q)Mid - SensHigh


Average Saturation Voltage
VOUT(sat) (V)
5
4
3
2
1
0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)
VOUT(sat)+
VOUT(sat)–


Average Clamp Values
Average Clamp Voltage (V)
5
4
3
2
1
0
-50
-25
0
25
50
75
100
125
150
Temperature (°C)
10% High Clamp
10% Low Clamp
20% High Clamp
20% Low Clamp

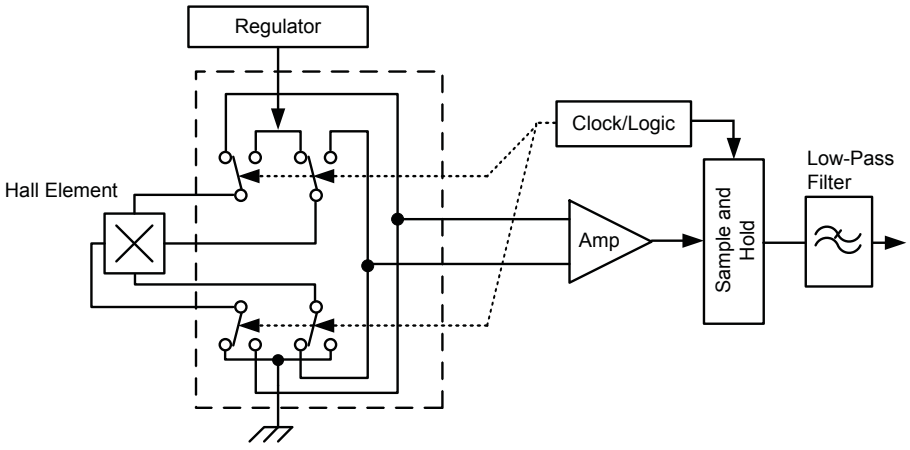
Chopper Stabilization Technique

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation.

The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field-induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic-sourced signal then can pass through a low-pass filter, while the modulated dc offset is suppressed.

The chopper stabilization technique uses a 200 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability.

This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

Definitions of Terms

Linear: A type of Hall-Effect device that produces an analog output voltage proportional to the strength of a sensed magnetic field.

Ratiometric: A linear Hall-Effect device that, when not subjected to a significant magnetic field, has an output that is a ratio of its supply voltage. A ratiometric performance of 100% indicates the output follows the supply with no percentage error.

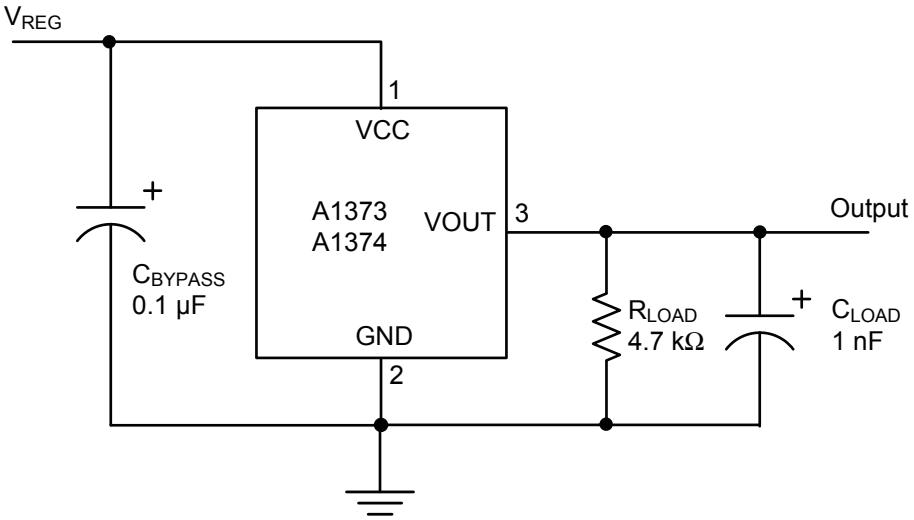
Gauss: Standard unit of measuring magnetic flux density. 1 gauss is equal to 1 Maxwell per square centimeter or 10^{-4} tesla. (For reference, the earth's magnetic field is approximately 0.5 gauss.)

Blowing: Applying a pulse of sufficient voltage and duration to permanently set a bit, by blowing a fuse internal to the device. Once a bit (fuse) has been blown, it cannot be reset. The terms *trimming* and *programming* can be used interchangeably with *blowing* in this context.

Programming modes: Testing the results is the only valid method to guarantee successful programming, and multiple modes are provided to support this. The programming modes are described in the section Mode Selection State.

Code: The number used to identify the register and the bitfield to be programmed, expressed as the decimal equivalent of the binary value. The LSB of a register is denoted as bit 0.

Typical Application Drawing



Characteristic Definitions

Quiescent Output Voltage. In the quiescent state (no significant magnetic field: B = 0), the output, V_{OUTQ}, equals a ratio of the supply voltage, V_{CC}, throughout the entire operating ranges of V_{CC} and ambient temperature, T_A. Due to internal component tolerances and thermal considerations, there is a tolerance on the quiescent output voltage, ΔV_{OUTQ}, which is a function of both ΔV_{CC} and ΔT_A. For purposes of specification, the quiescent output voltage as a function of temperature, $\Delta V_{OUTQ(\Delta T_A)}$, is defined as:

$$\Delta V_{OUTQ(\Delta T_A)} = \frac{V_{OUTQ(T_A)} - V_{OUTQ(25°C)}}{Sens_{(25°C)}} \quad (1)$$

where Sens is in mV/G, and the result is the device equivalent accuracy, in gauss (G), applicable over the entire operating temperature range.

Sensitivity. The presence of a south-polarity (+B) magnetic field, perpendicular to the branded face of the device package, increases the output voltage, V_{OUT}, in proportion to the magnetic field applied, from V_{OUTQ} toward the V_{CC} rail. Conversely, the application of a north polarity (–B) magnetic field, in the same orientation, proportionally decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity of the device and is defined as:

$$Sens = \frac{V_{OUT(-B)} - V_{OUT(+B)}}{2B} \quad (2)$$

The stability of the device magnetic sensitivity as a function of ambient temperature, $\Delta Sens_{(\Delta T_A)}$ (%) is defined as:

$$\Delta Sens_{(\Delta T_A)} = \frac{Sens_{(T_A)} - Sens_{(25°C)}}{Sens_{(25°C)}} \times 100\% \quad (3)$$

Ratiometric. The A1373 and A1374 feature ratiometric output. This means that the quiescent voltage output, V_{OUTQ}, magnetic sensitivity, Sens, and clamp voltage, V_{OUTCLP}, are proportional to the supply voltage, V_{CC}.

The ratiometric change in the quiescent output voltage, $RAT_{VOUT(Q)}$ (%), is defined as:

$$RAT_{VOUT(Q)} = \frac{V_{OUTQ(V_{CC})} \,/\, V_{OUTQ(5V)}}{V_{CC} \,/\, 5\ V} \times 100\% \quad (4)$$

the ratiometric change in sensitivity is defined as:

$$RAT_{Sens} = \frac{Sens_{(V_{CC})} \,/\, Sens_{(5V)}}{V_{CC} \,/\, 5\ V} \times 100\% \quad (5)$$

and the ratiometric change in clamp voltage is defined as:

$$RAT_{VCLP} = \frac{V_{CLP(V_{CC})} \,/\, V_{CLP(5V)}}{V_{CC} \,/\, 5\ V} \times 100\% \quad (6)$$

Note that clamping effect is applicable only when clamping is enabled by programming of the device.

Linearity and Symmetry. The on-chip output stage is designed to provide linear output at a supply voltage of 5 V. Although the application of very high magnetic fields does not damage these devices, it does force their output into a nonlinear region. Linearity in percent is measured and defined as:

$$Lin+ = \frac{V_{OUT(+B)} - V_{OUTQ}}{2\,(V_{OUT(+B½)} - V_{OUTQ})} \quad 100\% \quad (7)$$

$$Lin- = \frac{V_{OUT(-B)} - V_{OUTQ}}{2(V_{OUT(-B½)} - V_{OUTQ})} \times 100\% \quad (8)$$

and output symmetry as:

$$Sym = \frac{V_{OUT(+B)} - V_{OUTQ}}{V_{OUTQ} - V_{OUT(-B)}} \times 100\% \quad (9)$$

Pulse Generation

Several parameters can be field-programmed. To do so, a coded series of voltage pulses through the VOUT pin is used to set bitfields in onboard registers. The effect on the device output can be monitored, and the registers can be cleared and set repeatedly until the required output results are achieved. To make the setting permanent, bitfield-level solid state fuses are blown, and finally, a device-level fuse is blown, blocking any further coding.

Although any programmable variable power supply can be used to generate the pulsed waveforms, Allegro highly recommends using the Allegro Sensor IC Evaluation Kit, available on the Allegro Web site On-line Store. The manual for that kit is available for download free of charge, and provides additional information on programming these devices.

There are three voltage levels that must be taken into account when programming. For purposes of explanation in this document, the signal levels are referred to simply as *high* programming voltage, V_{PH}, *mid*, V_{PM}, and *low*, V_{PL}.

The rising edge of the high level, V_{PH}, pulse generates a state change. The falling edge of the high level, V_{PH}, pulse increments the mode, register, or bitfield selection by one, when allowed to drop below the low level, V_{PL}, threshold. A delay on the falling edge, at the mid level, V_{PM}, range is required to guarantee proper programming level recognition. When it is not desirable to increment these fields further, it is acceptable to hold the signal at the mid level, V_{PM}, range and then transition to another high level, V_{PH}, pulse. Referring to the Programming State Machine diagram, when using Blow Fuse mode the fourth high level, V_{PH}, pulse (including the key sequence to enable Blow Fuse mode), will blow the selected key-code combination. If fuse blowing is not desired, it is recommended to reset the A137x by toggling the supply pin. If the high level, V_{PH}, pulse is not generated, and the A137x is not reset, then the next key sequence to change states will blow the unwanted key-code combination. For multiple register addressing without fuse blowing, Try Value mode must be used.

PROGRAMMING PROTOCOL CHARACTERISTICS, over operating temperature range, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Programming Voltage[1]	V_{PL}	Low voltage range, for addressing registers and bitfields	0	–	5	V
	V_{PM}	Mid voltage range, for addressing bitfields and for separating programming signals	14	–	16	V
	V_{PH}	High voltage range, for enabling state changes and for fuse blowing	25	26	27	V
Programming Current[2]	I_{PP}	t_r = 11 µs; 5 V → 28 V; C_{PROG} = 0.1 µF	–	209	–	mA
Pulse Width	t_{PHE}	High pulse duration for enabling state change	20	–	–	µs
	t_{PHP}	High pulse duration for blowing fuses	100	–	–	µs
	t_{PLA}	Low pulse duration for bitfield addressing	6	–	–	µs
	t_{PME}	Mid pulse delay on falling edge of high pulse, V_{PH}	15	–	–	µs
	t_{PMA}	Mid pulse duration for bitfield addressing	6	–	–	µs
Pulse Rise Time	t_r	V_{PL} to V_{PH} or V_{PM}; maximum may be application dependent	5	–	100	µs
Pulse Fall Time	t_f	V_{PH} or V_{PM} to V_{PL}; maximum may be application dependent	5	–	100	µs

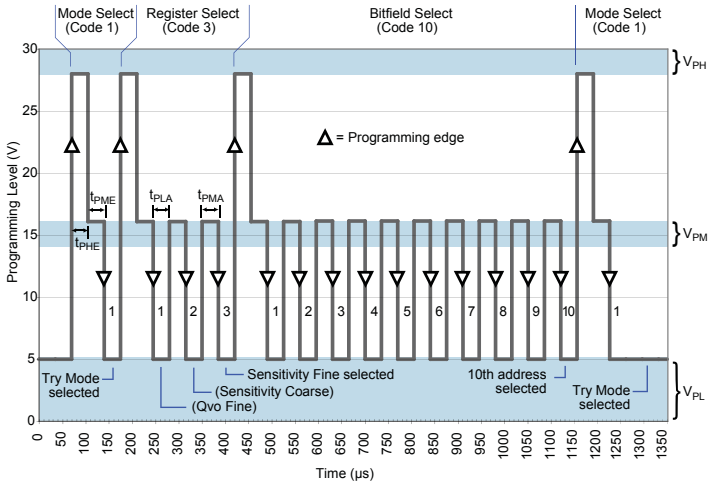
[1]Programming voltages are measured at pin #3, VOUT, of the A137x.
[2]A minimum capacitance of 0.1 µF must be connected from VOUT to the GND pin of the A137x in order to provide the current necessary to blow the fuse.

The mid voltage range, V_{PM}, is a neutral level used to separate V_{PH} and V_{PL} pulses from each other.

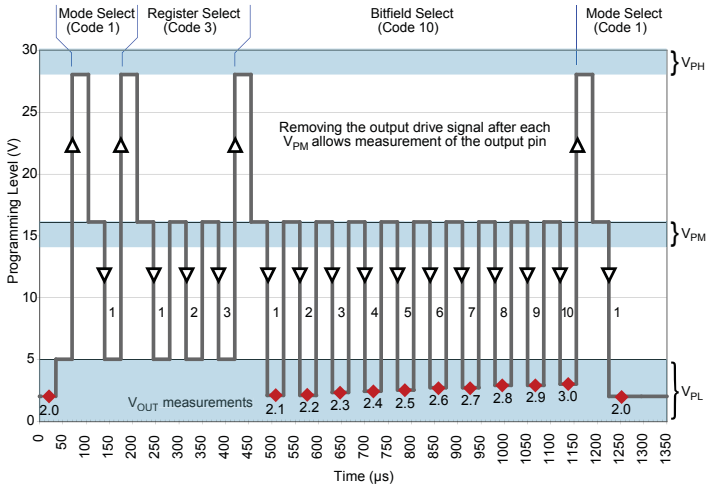
The low level, V_{PL}, pulse is used to increment the mode, register, and bitfield addresses that are to be set. The device generates a V_{PL} pulse on the falling edge of the mid-level to low-level transition, V_{PM} to V_{PL}.

In Try Value mode,the programming drive signal can be held at 5 V or less if no code search is required. If a code search is required, then the output drive signal must be released to allow the output level to be read for each bitfield increment (see panels A and B, below).

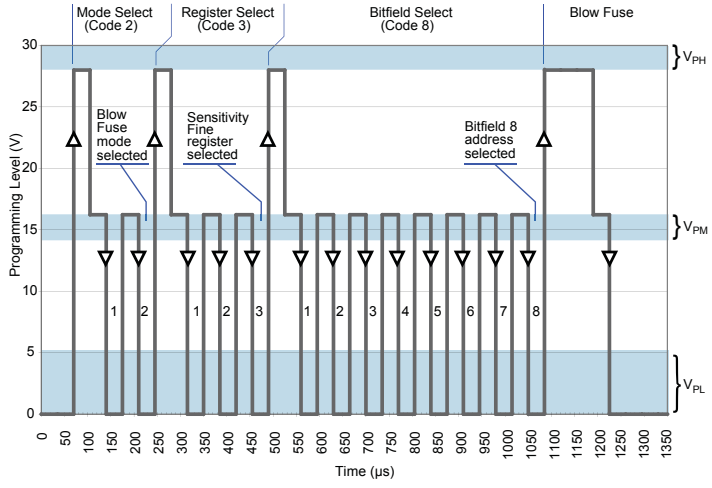
To guarantee proper pulse recognition, each level must be held for the predefined durations specified in the Programming Protocol Characteristics table. Failure to follow the specifications may produce undefined results. Examples of common pulse trains are shown in panels C and D, below.



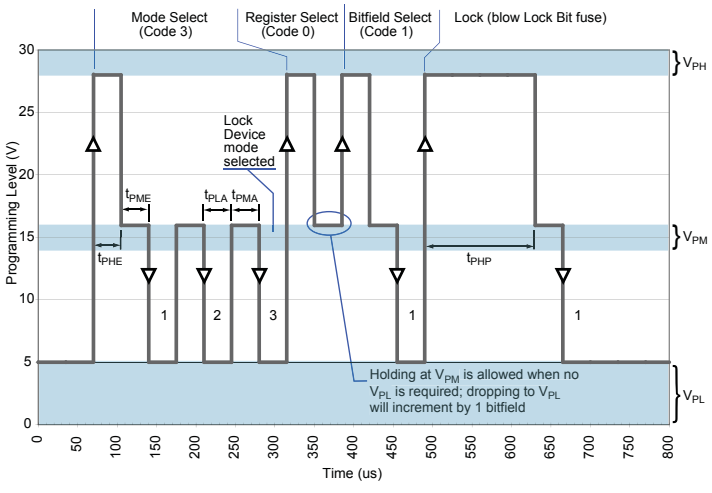
A. Try Value Mode. Code search with drive signal held at 5 V.



B. Try Value Mode. Code search with drive signal released after each V_{PM}, allows output to be measured after each code increment.

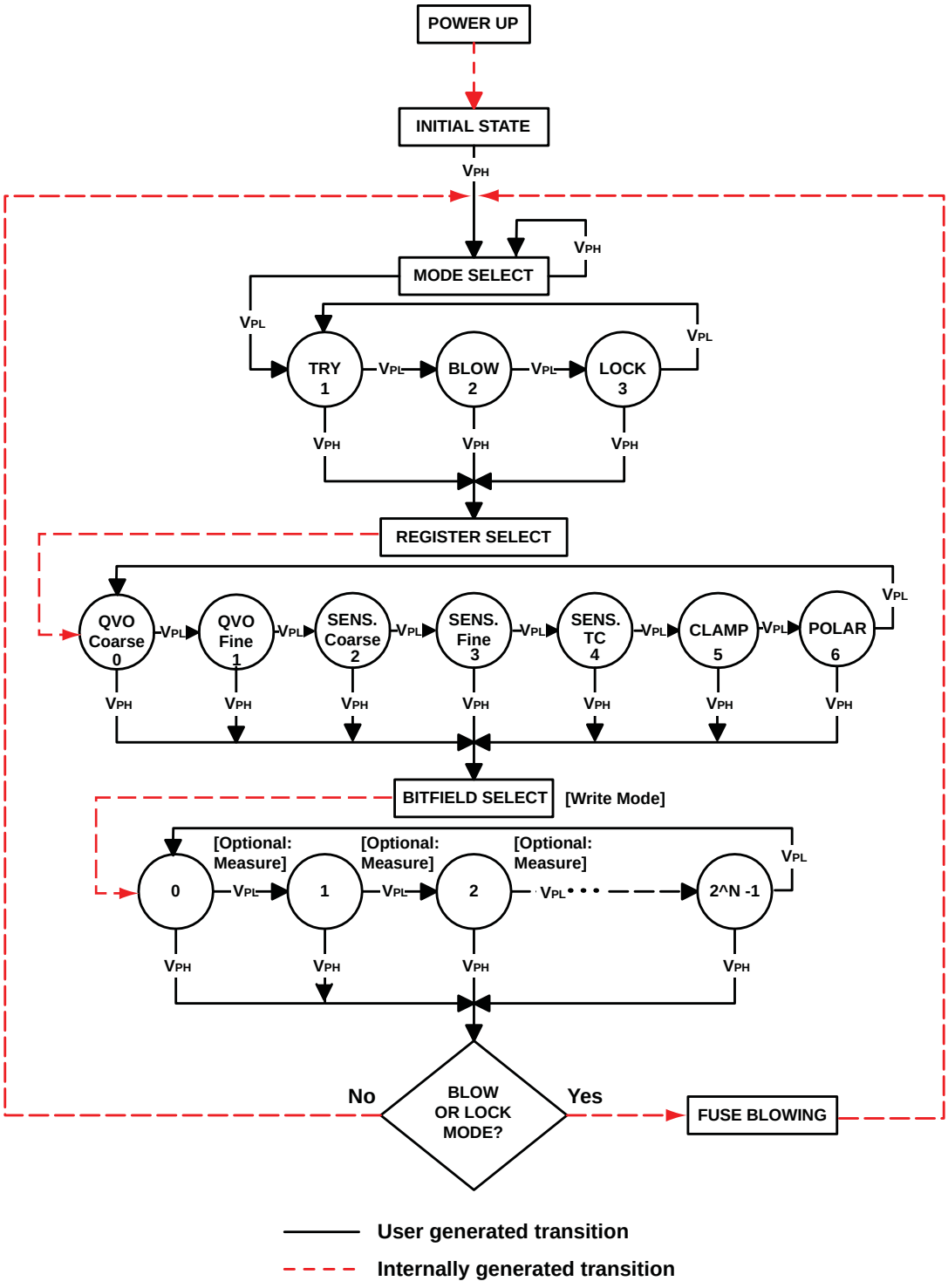


C. Blow Fuse Mode: Code 8 / bit 4 is programmed.



D. Lock Device Mode. Device-level Lock Bit is programmed; device programming is then permanently disabled.

Programming State Machine



Programming Protocol and State Machine Description

INITIAL STATE

After system power-up, the programming logic is reset to a known state. This is referred to as the Initial state. All the registers that have intact fuses are set to logic 0.

While in the Initial state, any V_{PL} pulses on the VOUT pin are ignored.

To enter the Mode Selection state, send one V_{PH} pulse on the VOUT pin.

MODE SELECTION STATE

This state allows the selection of the programming mode:

- Try Value Mode. In this mode, the user provisionally downloads settings to the device registers, without blowing the bits. The user can increment through the codes of each parameter, and evaluate the results of various code settings.
- Blow Fuse Mode. In this mode, after downloading the settings, the user can blow the fuses in specific registers.
- Lock Device Mode. This mode is similar to Blow Fuse mode, except that the fuse that is blown permanently prevents any further programming of any bits in the device.

To select a mode, increment through the register bitfields by sending V_{PL} pulses on the VOUT pin, as follows:

0 pulses – No effect
1 pulse – Try Value mode
2 pulses – Blow Fuse mode
3 pulses – Lock Device mode

This register wraps by default. This means that sending additional VPL pulses traverses the register again.

Any V_{PH} pulse sent before a V_{PL} pulse has no effect.

To enter the Register Selection state, after sending a valid quantity of V_{PL} pulses, send one V_{PH} pulse on the VOUT pin.

REGISTER SELECTION STATE

This state allows the selection of the register containing the bitfields to be programmed. Selecting the register corresponds to selecting the parameter to be set. For bit codes, see the section Programming Logic.

- QVO [$V_{OUT(Q)}$] Coarse. Register for setting the range of the operating dc point (2 bits)
- QVO Fine. Register for setting the value within the range set in the QVO Coarse register (9 bits)
- Sens. [Sensivity] Coarse. Register for setting the overall gain of the device (2 bits)
- Sens. Fine. Register for setting the value within the range set in the Sens. Coarse register (8 bits)
- [Sensitivity] TC Register. Register for setting the temperature coefficient for the device (5 bits).
- Clamp [V_{OUTCLP}] Bit. Register for setting the clamping voltage of the output (2 bits)
- Polarity Bit. Register setting the polarity of the output (1 bit)

To select a register, increment through the register bitfields by sending V_{PL} pulses on the VOUT pin. Note that the programming of registers should follow the order shown in item 7 in the section Programming Guidelines, not the bitfield selection order shown here. The bitfield selection order is:

0 pulses – QVO Coarse register
1 pulse – QVO Fine register
2 pulses – Sens. Coarse register
3 pulses – Sense Fine register
4 pulses – TC Register register
5 pulses – Clamp Bit register
6 pulses – Polarity Bit register

This register wraps by default.

To enter the Bitfield Selection state, send one V_{PH} pulse on the VOUT pin.

BITFIELD SELECTION STATE (Write Mode)

This state allows the selection of the individual bitfields to be programmed, in the register selected in the Register Selection state.

In Try Value mode, the total value of the bitfields selected increments by 1 with each V_{PL} pulse on the VOUT pin. The parameter being programmed changes with each additional pulse, so measurements can be taken after each pulse to determine if the desired result has been acquired.

In Blow Fuses mode, each bitfield to be blown must be selected individually.

For bit codes and wrapping for these registers, see the section Programming Logic.

To leave this state, send one V_{PH} pulse on the VOUT pin. If the current mode is Try Value, the bitfields remain set and the device reverts to the Mode Selection state. If the current mode is Blow Fuse, the selected bitfield fuse is blown, and the device reverts to the Mode Selection state.

Programming Logic

Binary Bitfield Address	Decimal Equivalent Code	Description
QVO Coarse register		
00	0	$V_{OUT(Q)}$ mid range
01	1	$V_{OUT(Q)}$ low range
10	2	$V_{OUT(Q)}$ high range
11	3	Register wraps to 00
QVO Fine register		
000000000	0	Initial value in selected QVO Coarse range
111111111	511	Maximum value in selected QVO Coarse range
Sens. Coarse register		
00	0	Sens low range
01	1	Sens mid range
10	2	Sens high range
11	3	Register wraps to 00
Sens. Fine register		
00000000	0	Initial value in selected Sens. Coarse range
11111111	255	Maximum value in selected Sens. Coarse range
TC Register register (See also chart Sensitivity Temperature Coefficient Code Profile in Typical Characteristics section)		
00000	0	initial TC
00001 through 01011	1 through 11	Positive TC programming range
01100 through 01111	12 through 15	Unused: equal to codes 4 to 7, respectively
10000 through 11011	16 through 27	Negative TC prgramming range; Value for 16 equals 1 step less than the value for the Initial TC Value (00000)
11100 through 11111	28 through 31	Unused: equal to codes 20 to 23, respectively
Clamp Bit register		
00	0	Rail-to-rail output swing
01	1	0.5 V and V_{CC}– 0.5V rails
10	2	1 V and V_{CC} – 1 V rails
00	3	Register wraps to 00
Polarity Bit register		
0	0	Positive (V_{OUT} increases when a positive (south) magnetic field is applied to the device)
1	1	Negative (V_{OUT} increases when a negative (north) magnetic field is applied to the device)
Lock Bit register		
0	0	Unlocked
1	1	Locked (register 0, bitfield 1)

Programming Guidelines

• A bypass capacitor rated at 0.1µF must be mounted between the VOUT pin and the GND pin during programming. The power supply used for programming should be capable of delivering 28 V and 300 mA.

• Before beginning any Blow Fuse mode or Lock Device mode code sequence, the device MUST be reset by cycling V_{CC} power-off and power-on again. Cycling power resets the device by setting all bitfields that have intact fuses to 0. Bitfields with blown fuses are unaffected.

In Try Value mode, to retain register settings from previous code sequences, do not cycle power between sequences.

When a register is selected in Register Selection mode, when the V_{PH} pulse is sent to enter the Bitfield Selection mode, the bitfields with intact fuses in that register are reset to 0.

• In Try Value mode, all bits in the register can be set in one code sequence. For example, setting the binary value 0110 and sending a V_{PH} pulse sets code 6. However, because of the power requirement, blowing fuses in Blow Fuse mode must be performed one bitfield at a time. In order to program (blow fuses) for binary 0110, the bitfields MUST be programmed (blown) in two different code sequences:one setting the 0100 bit, and the other setting the 0010 bit (in either order). Power must be cycled before each of the two sequences.

• Although a bitfield cannot be reset once its fuse is blown, additional bitfields can be blown at any time, until the device is locked by setting the Lock bit. For example, if bit 1 (0010) has been blown, it is possible to blow bit 0 (0001). Because bit 1 was already blown, the end result will be 0011 (code 3).

• Before powering down the device after programming, observe the recommended delay at the mid voltage level, to ensure that the last V_{PH} pulse has decayed before voltage drops to the V_{PL} voltage. This will avoid the generation of overlapping V_{PL} and V_{PH} pulses. At the end of a Lock Device mode code sequence, the delay is not necessary.

• Programming order is important in both Try Value mode and in Blow Fuse mode. There will be a slight parametric shift in sensitivity after programming the temperature coefficient, and a slight quiescent voltage shift with polarity. Subsequent changes to sensitivity can cause a shift in the quiescent output voltage.

The following order is recommended:

a. Polarity
b. TC Register
c. Sens Coarse
d. QVO Coarse
e. Sens Fine
g. QVO Fine

The Clamp Bit register can be programmed at any point in the order, as no parametric shift is observed due to clamps.

• The actual distribution of parametric programming ranges are wider than the specified programming ranges, in order to take in to account manufacturing spread. The maximum possible attainable range can be used with the understanding that other specified parameters might be out of datasheet specification in the extended range. (For an example, see the chart Sensitivity Temperature Coefficient Range, in the Typical Characteristics section.)

Programming Example

This example demonstrates the programming of the devices by setting the register for Sensitivity Temperature Coefficient to 00110.

1. Power-on the system. This will reset the unprogrammed bits in all registers to 0. The device enters the Initial state.
2. Send one V_{PH} pulse to enter the Mode Selection state.
3. Send one V_{PL} pulse to select Try Value mode.
4. Send one V_{PH} pulse to enter the Register Selection state.
5. Send four V_{PL} pulses to select the TC register.
6. Send one V_{PH} pulse to enter Bitfield Selection state (Write mode). The TC register is reset to 00000 (assuming all of those bitfields have intact fuses).
7. Send five V_{PL} pulses to set bitfields 0 and 2 (00101).

Now we can measure the device output to see if this is the desired value. We may find that the value we programmed is not correct. So we will proceed to change it, as follows:

8. Send one V_{PL} pulse to increase the code to 6 (setting bitfields 1 and 2: 00110).

We measure the device and find that this is the correct TC we require. We are finished with trying values, and now want to set the value permanently. In the following steps, remember that blowing fuses is done one bit at a time.

9. Send one V_{PH} pulse to exit Bitfield Selection mode. (The device returns to the Mode Selection state.)
10. RESET the device by powering it off and on.
11. Send one V_{PH} pulse to enter the Mode Selection state.
12. Send two V_{PL} pulses to select Blow Fuse mode.
13. Send one V_{PH} pulse to enter the Register Selection state.
14. Send four V_{PL} pulses to select the TC register.
15. Send one V_{PH} pulse to enter Bitfield Selection state (Write Mode). The TC register is reset to 00000.
16. Send four V_{PL} pulses to set bit 2 (00100, decimal 4).
17. Send one V_{PH} pulse to exit Bitfield Selection state. The bitfield fuse is blown, and the device returns to the Mode Selection state.

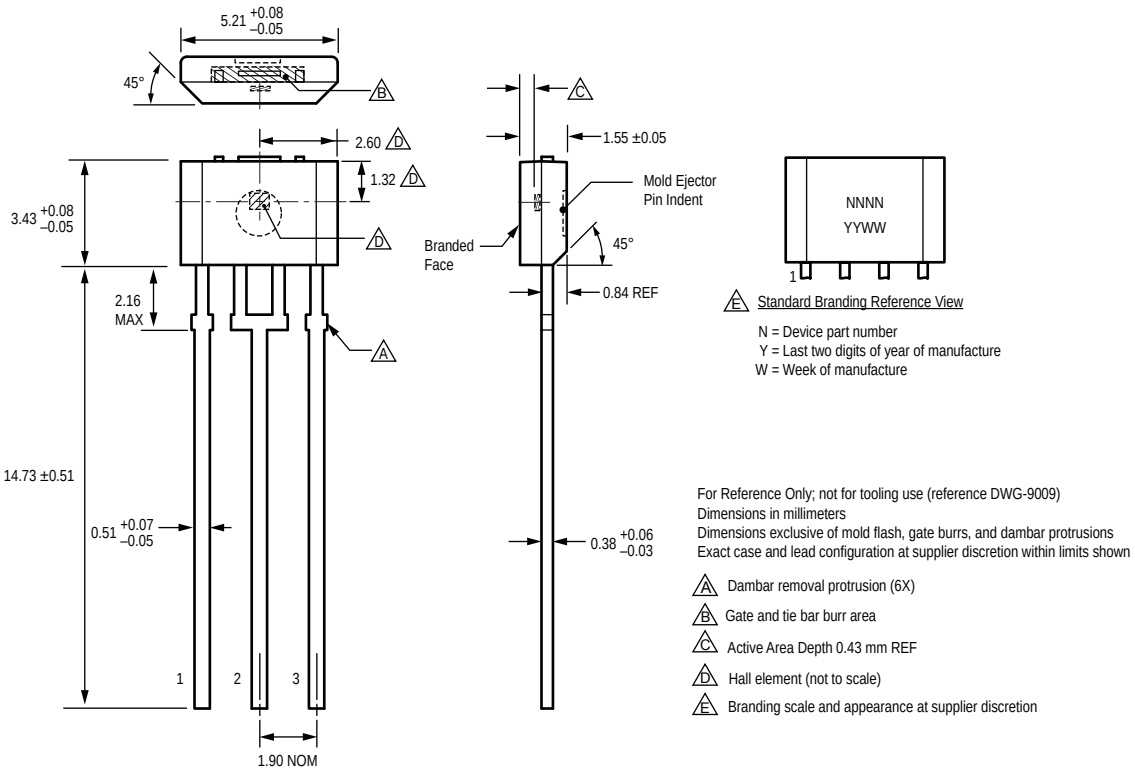
One of the two bitfields is programmed. Now we program the other bitfield.

18. Repeat steps 10 to 15 to select the TC register again. This time, however, the register resets to 00100, because bit 2 has been permanently set.
19. Send two V_{PL} pulses to set bit 1 (00010, decimal 2).
20. Send one V_{PH} pulse to exit Bitfield Selection state. The bitfield fuse is blown, and the device returns to the Mode Selection state.

After repeating the above steps to program all parameters, we can lock the device:

21. RESET the device by powering it off and on.
22. Send one V_{PH} pulse to enter the Mode Selection state.
23. Send three V_{PL} pulses to select Lock Device mode.
24. Send one V_{PH} pulse to enter the Bitfield Selection state. (We do not need to select a register for locking the device).
25. Send one V_{PL} pulse to set the Lock bit to 1.
26. Send one V_{PH} pulse to exit Bitfield Selection state. The bitfield fuse is blown, and the device returns to the Mode Selection state.
27. Programming the device is complete. Optionally, test the results, or power-off the device.

Package KB, 3-Pin SIP



Terminal List

Name	Number	Description
VCC	1	Connects power supply to chip
GND	2	Ground
VOUT	3	Output from circuit, terminal for programming pluses

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