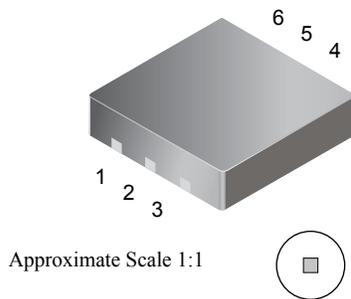


Low-Voltage Full-Bridge Brushless DC Motor Driver with Hall Element Commutation

Features and Benefits

- Single-chip solution for high reliability
- Chopper stabilization technique for precise signal response over operating range
- 2.0 to 4.0 V operation
- Sleep mode pin allowing external logic signal enable/disable to reduce average power consumption
- Restart feature
- Small package size

Package: 6 Contact MLP/DFN/SO8 (suffix EL)



Description

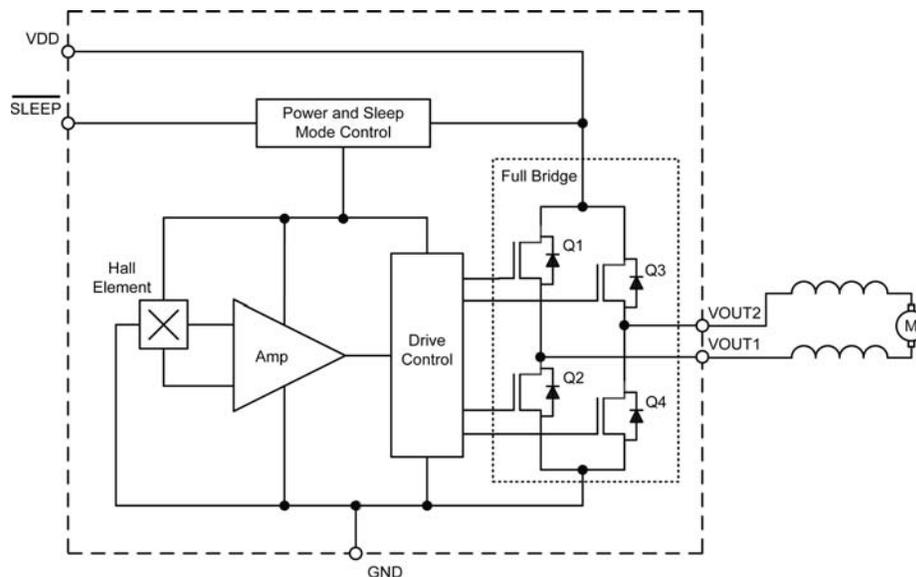
The A1441 is a full-bridge motor driver designed to drive low-voltage bipolar brushless dc motors. Commutation of the motor is achieved by use of a single Hall element sensor to detect the position of an alternating-pole ring magnet. A high density merged Bipolar-CMOS semiconductor process allows the integration of the Hall element on the same IC as the motor control circuitry, providing a single-chip solution for enhanced reliability. All necessary circuitry is incorporated within the device package, eliminating the need for any external support components.

A micropower sleep mode can be enabled by an external signal, to reduce current consumption for battery management in portable electronic devices. In addition, the device offers an active function for motor braking.

The A1441 is optimized for vibration motor applications such as cellular phones, pagers, electronic toothbrushes, and hand-held video game controllers. These devices also drive low power fan motors designed with cogging plates.

Continued on the next page...

Functional Block Diagram



Description (continued)

The small package outlines and low profiles make this device ideally suited for use in applications where printed circuit board area and component headroom are at a premium. It is available in

a lead (Pb) free (leadframe plating 100% matte tin) 6-pin surface mount MLP (microleadframe: DFN) package, with exposed pad for enhanced thermal dissipation.

Selection Guide

| Part Number | Package | Packing ¹ |
|---------------------------|---------------------------------|-------------------------|
| A1441EELLT-T | MLP 2x2 mm; 0.50 mm nom. height | 3000 pieces/ 7-in. reel |
| A1441SEKLT-T ² | | |



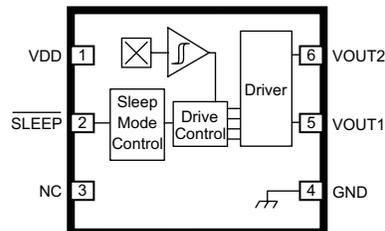
¹For additional packing options, contact Allegro.

²These variants are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 1, 2006.

Absolute Maximum Ratings

| Characteristic | Symbol | Notes | Rating |
|-------------------------------|----------------|---|----------------------------|
| Supply Voltage | V_{DD} | | 5.0 V |
| Reverse Battery Voltage | V_{RDD} | | -0.3 V |
| Output Voltage | V_{OUT} | | -0.3 V to $V_{DD} + 0.3$ V |
| Control Input Voltage | $V_{IN(High)}$ | | -0.3V to $V_{DD} + 0.3$ V |
| Load Current | I_{LOAD} | Positive I_{LOAD} flow is from VOUT1 to VOUT2 | ± 150 mA |
| Magnetic Flux Density | B | | Unlimited |
| Operating Ambient Temperature | T_A | Range E | -40°C to 85°C |
| Maximum Junction | $T_J(max)$ | | 165°C |
| Storage Temperature | T_{stg} | | -65°C to 170°C |

Pin-out Diagram



Terminal List Table

| Name | Number | Function |
|-------|------------|----------------------------|
| | EL Package | |
| VDD | 1 | Supply voltage |
| SLEEP | 2 | Toggle Sleep/Enabled modes |
| NC | 3 | No connection |
| GND | 4 | Ground |
| VOUT1 | 5 | First output |
| VOUT2 | 6 | Second output |

DEVICE CHARACTERISTICS over the voltage and temperature operating range, unless otherwise specified

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Units | |
|--|-----------------|---|--------------|------|------|---------------|---|
| Supply Voltage | V_{DD} | Running | 2.0 | – | 4.0 | V | |
| Total Output Saturation Voltage ¹ | $V_{OUT(Sat)}$ | $I_{LOAD} = 100 \text{ mA}, V_{DD} = 3.6 \text{ V}$ | – | – | 500 | mV | |
| | | $I_{LOAD} = 70 \text{ mA}, V_{DD} = 2.2 \text{ V}$ | – | – | 400 | mV | |
| Sleep Mode Supply Current | $I_{DD(Sleep)}$ | | – | – | 10 | μA | |
| Load Current Rise Time ² | $t_{r(ILOAD)}$ | $V_{DD} = 3.6 \text{ V}$ | – | 10 | – | μs | |
| Chopping Settling Time ³ | $t_{s(CHOP)}$ | | – | 30 | – | μs | |
| $\overline{\text{SLEEP}}$ Input Threshold | V_{INLO} | | – | – | 0.5 | V | |
| | V_{INHI} | | $V_{DD}-0.7$ | – | – | V | |
| $\overline{\text{SLEEP}}$ Input Current | I_{IN} | | – | – | 1 | μA | |
| Crossover Dead Time ⁴ | t_{DT} | VOUT switching | – | 2 | – | μs | |
| Restart Delay ⁵ | t_{RS} | | – | – | 225 | ms | |
| Magnetic Switchpoints | B_{OP} | | – | 35 | 75 | G | |
| | B_{RP} | | –75 | –35 | – | G | |
| | B_{HYS} | $B_{OP} - B_{RP}; B_{OP} > B_{RP}$ | – | 70 | – | G | |
| Startup Polarity | V_{OUT1} | $B < B_{rp}$ | | LOW | | – | |
| | | $B > B_{op}$ | | HIGH | | – | |
| | V_{OUT2} | $B < B_{rp}$ | | | HIGH | | – |
| | | $B > B_{op}$ | | | LOW | | – |

¹Either $V_{OUT(Sat)} = V_{Q1(Sat)} + V_{Q4(Sat)}$ or $V_{OUT(Sat)} = V_{Q2(Sat)} + V_{Q3(Sat)}$. Total output saturation voltage is a sum of the voltages across the active output transistors.

²Time period required for current to change from 10% to 90% of it's value.

³Chopping settling time is the required time to have valid device output after power up of the device.

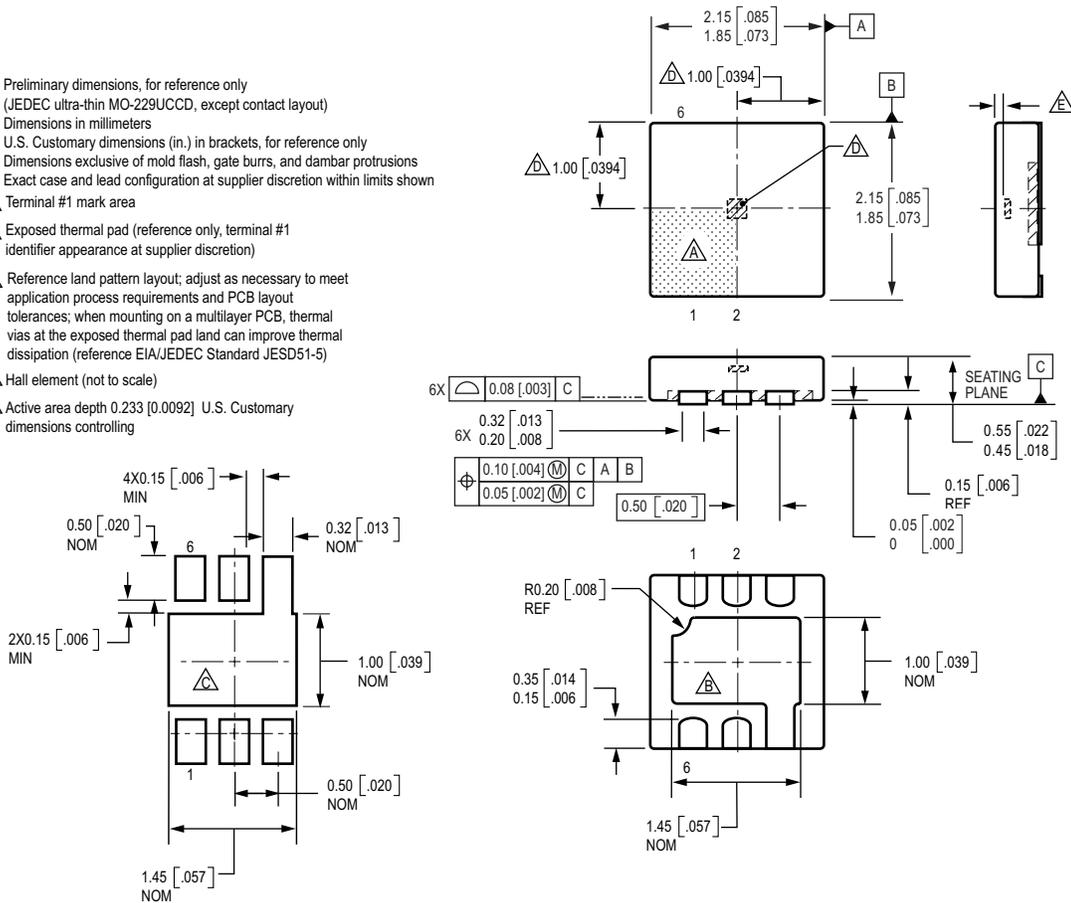
⁴Crossover dead time is a time period during which all output transistors are switched off.

⁵Restart delay is a time period during which only one pair of the output transistors is switched on.

Low-Voltage Full-Bridge Brushless DC Motor Driver with Hall Element Commutation

Package EL, 6 pin MLP/DFN/SO8

- Preliminary dimensions, for reference only
(JEDEC ultra-thin MQ-229UCCD, except contact layout)
Dimensions in millimeters
- U.S. Customary dimensions (in.) in brackets, for reference only
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
-  Terminal #1 mark area
-  Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
-  Reference land pattern layout; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
-  Hall element (not to scale)
-  Active area depth 0.233 [0.0092] U.S. Customary dimensions controlling



The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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