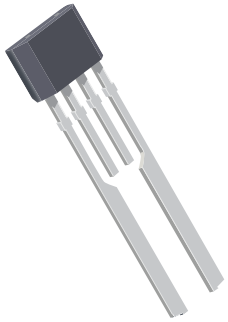
Two-Wire True Zero-Speed Miniature Differential Peak-Detecting Sensor IC with Continuous Calibration

Features and Benefits

- Running mode calibration for continuous optimization
- Single chip IC for high reliability
- Internal current regulator for 2-wire operation
- Precise duty cycle signal over operating temperature range
- Large operating air gaps
- Automatic Gain Control (AGC) for air gap independent switchpoints
- Automatic Offset Adjustment (AOA) for signal processing optimization
- True zero-speed operation
- Undervoltage lockout
- Wide operating voltage range
- Wide-lead package suitable for welding external components directly to the package leads or for welding the device to a leadframe.

Package: 4-pin SIP (Suffix KN)



Not to scale

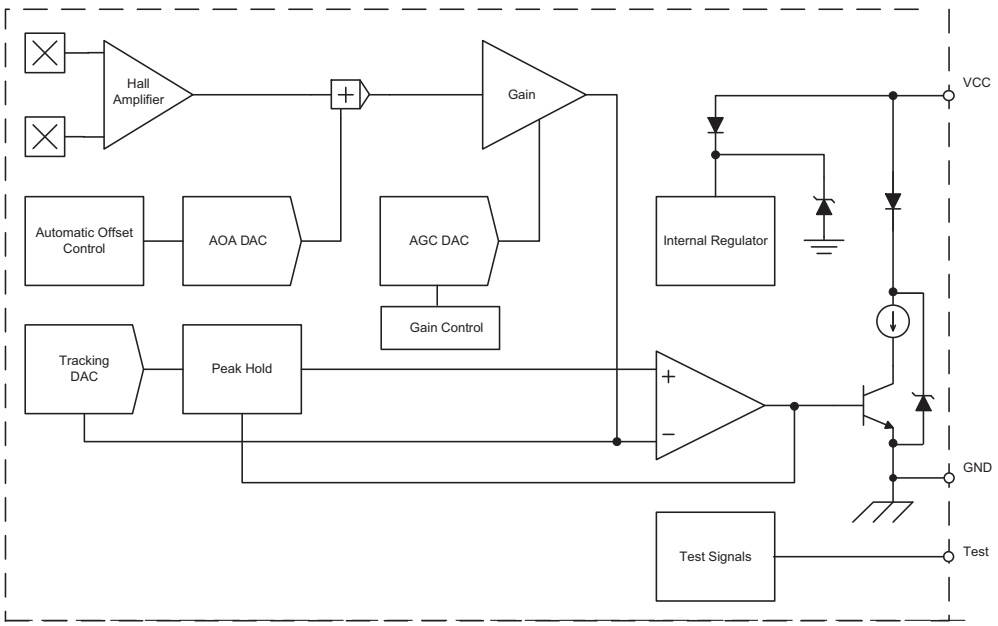
Description

The A1642 is an optimized Hall effect sensing integrated circuit that provides a user-friendly solution for true zero-speed digital ring-magnet sensing in two-wire applications. This small package can be easily assembled and used in conjunction with a wide variety of target shapes and sizes.

The integrated circuit incorporates dual Hall effect elements and signal processing that switches in response to differential magnetic signals created by ring magnet poles. The circuitry contains a sophisticated digital circuit to reduce system offsets, to calibrate the gain for air-gap–independent switchpoints, and to achieve true zero-speed operation. Signal optimization occurs at power-on through the combination of offset and gain adjust and is maintained throughout the operating time with the use of a running-mode calibration. The running-mode calibration allows immunity to environmental effects such as micro-oscillations of the target or sudden air gap changes.

The regulated current output is configured for two-wire applications and the A1642 is ideally suited for obtaining speed and duty cycle information in ABS (antilock braking systems). The 1.5 mm spacing between the dual Hall elements is optimized for fine pitch ring-magnet–based configurations. For applications requiring sensing of rotating ferrous gears and targets, refer to the Allegro ATS series of products. The package is lead (Pb) free, with 100% matte tin leadframe plating.

Functional Block Diagram



Selection Guide

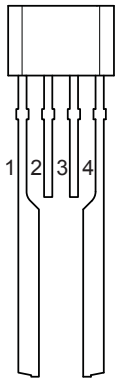
Part Number	I_{CC} Range	Packing*
A1642LKNTN-I1-T	4.0 mA Low to 16.0 mA High	Tape and reel, 13-inch reel 4000 pieces per reel
A1642LKNTN-I2-T	5.9 mA Low to 16.8 mA High	
A1642LKNTN-I3-T	5.9 mA Low to 16.0 mA High	

*Contact Allegro for additional packing options

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A	Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-out Diagram



Terminal List Table

Number	Name	Function
1	VCC	Connects power supply to chip
2	NC	No connection
3	Test	Float or tie to GND
4	GND	Ground connection

OPERATING CHARACTERISTICS T_A and V_{CC} within specification, unless otherwise noted

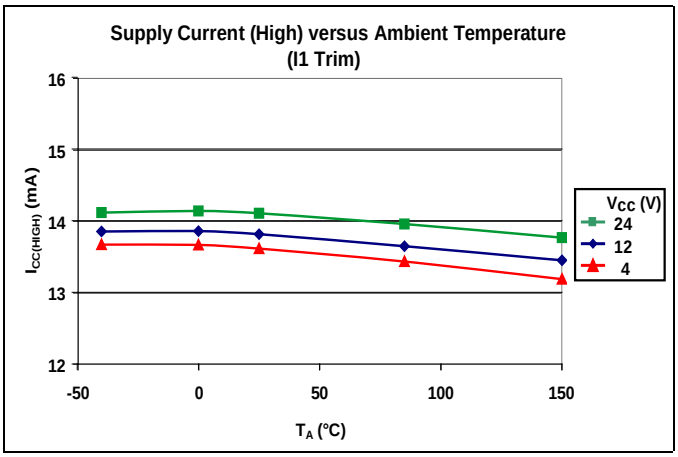
CHARACTERISTIC	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage[2]	V_{CC}	Operating; T_J < 165°C	4.0	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} 0 → 5 V and 5 → 0 V	–	–	4.0	V
Supply Zener Clamp Voltage	V_Z	$I_{CC} = I_{CC(max)}$ + 3 mA; T_A = 25°C	28	–	–	V
Supply Zener Current	I_Z	Test conditions only; V_Z = 28 V	–	–	$I_{CC(max)}$+ 3 mA	mA
Supply Current	$I_{CC(Low)}$	A1642LKN-I1	4.0	6.0	8.0	mA
		A1642LKN-I2, A1642LKN-I3	5.9	7.0	8.4	mA
	$I_{CC(High)}$	A1642LKN-I1, A1642LKN-I3	12.0	14.0	16.0	mA
		A1642LKN-I2	11.8	14.0	16.8	mA
Supply Current Ratio	$I_{CC(High)}/I_{CC(Low)}$	Ratio of high current to low current	1.85	–	3.05	–
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V	–	–	–5	mA
POWER-ON STATE CHARACTERISTICS						
Power-On State[3]	POS	t > t_{PO}	–	$I_{CC(High)}$	–	–
Power-On Time[4]	t_{PO}	f_{OP} < 100 Hz	–	1	2	ms
OUTPUT STAGE						
Output Slew Rate[5]	dI/dt	R_{LOAD} = 100 Ω, C_{LOAD} = 10 pF	–	14	–	mA/µs

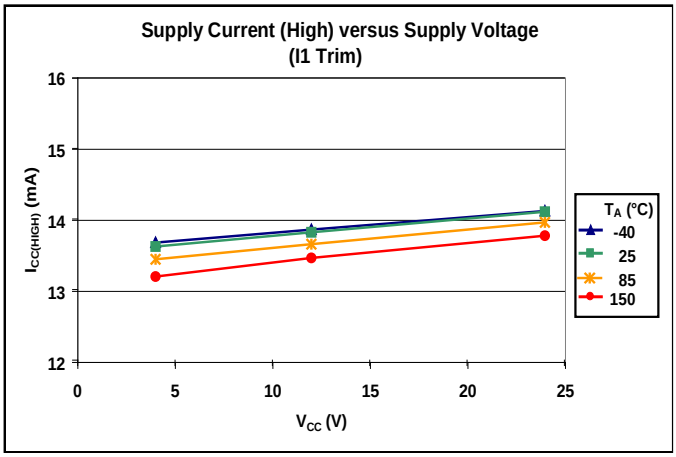
Continued on the next page.

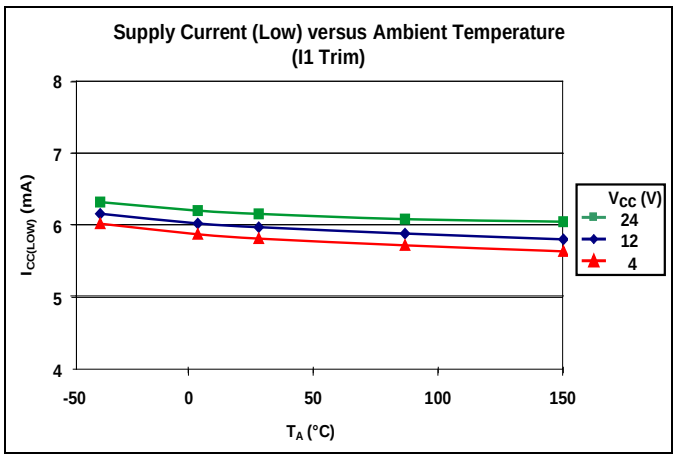
OPERATING CHARACTERISTICS (continued) T_A and V_{CC} within specification, unless otherwise noted						
Characteristic	**Symbol**	**Test Conditions**	**Min.**	**Typ.[1]**	**Max.**	**Units**
SWITCHPOINT CHARACTERISTICS						
Operating Speed	f_{OP}		0	–	8,000	Hz
Analog Signal Bandwidth	BW	Equivalent to f – 3 dB	20	40	–	kHz
Operate Point	B_{OP}	Transitioning from $I_{CC(High)}$ to $I_{CC(Low)}$; positive peak referenced; AG < AG_{MAX}	–	120	–	mV
Release Point	B_{RP}	Transitioning from $I_{CC(Low)}$ to $I_{CC(High)}$; negative peak referenced; AG < AG_{MAX}	–	120	–	mV
CALIBRATION						
Initial Calibration	C_I	Quantity of rising output (current) edges required for accurate edge detection	–	–	3	Edge
DAC CHARACTERISTICS						
Allowable User-Induced Differential Offset		Operating within specification	–	–	±90	G
FUNCTIONAL CHARACTERISTICS[6]						
Operating Signal Range[7]	Sig	Operating within specification	30	–	1000	G
Minimum Operating Signal	$Sig_{OP(min)}$	Output switching (no missed edges); ΔDC not guaranteed	20	–	–	G

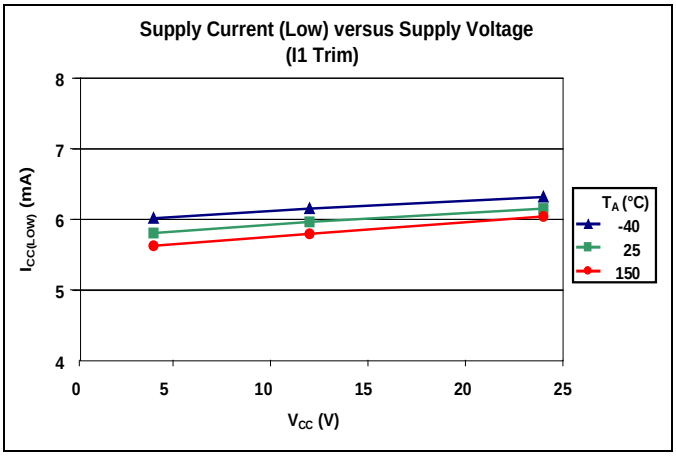
[1]Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2]Maximum voltage must be adjusted for power dissipation and junction temperature; see *Power Derating* section.
[3]Please refer to Device Operation section.
[4]Power-On Time includes the time required to complete the internal automatic offset adjust. The DAC is then ready for peak acquisition.
[5]dI is the difference between 10% of $I_{CC(Low)}$ and 90% of $I_{CC(High)}$, and dt is the time period between those two points.
Note: dI/dt is dependent upon the value of the bypass capacitor, if one is used.
[6]Functional characteristics valid only if magnetic offset is within the specified range for Allowable User Induced Differential Offset.
[7]In order to remain in specification, the magnetic gradient must induce an operating signal greater than the minimum value specified. This includes the effect of target wobble.

Characteristic Data

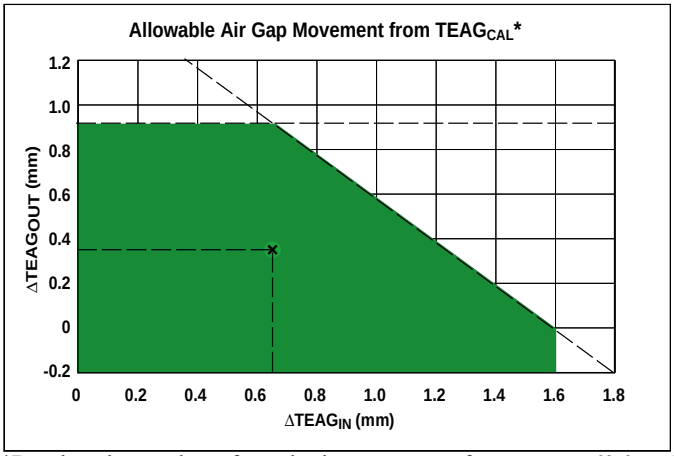








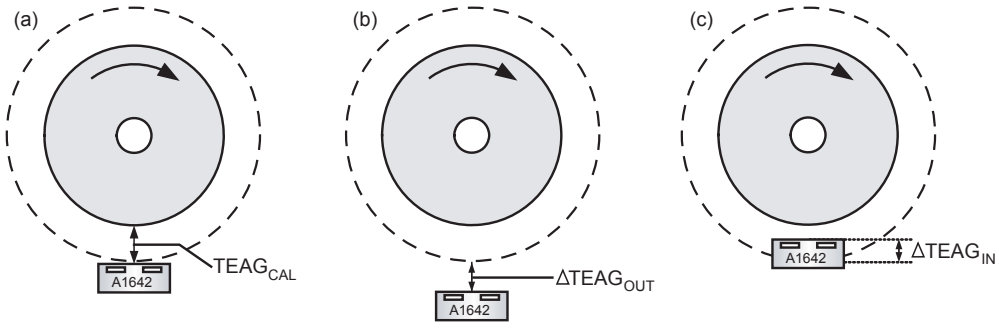
Characteristic Allowable Air Gap Movement



*Data based on study performed using spur gear reference target 60-0, and applicable to ring magnet targets with similar magnetic characteristics.

The colored area in the chart above shows the region of allowable air gap movement within which the device will continue output switching. The output duty cycle is wholly dependent on the target's magnetic signature across the air gap range of movement, and may not always be within specification throughout the entire operating region (to $AG_{(OPmax)}$).

The axis parameters for the chart are defined in the drawings below. As an example, assume the case where the air gap is allowed to vary from the nominal installed air gap ($TEAG_{CAL}$, panel a) within the range defined by an increase of $\Delta TEAG_{OUT}$ = 0.35 mm (shown in panel b), and a decrease of $\Delta TEAG_{IN}$ = 0.65 mm (shown in panel c). This case is plotted with an "**x**" in the chart above.

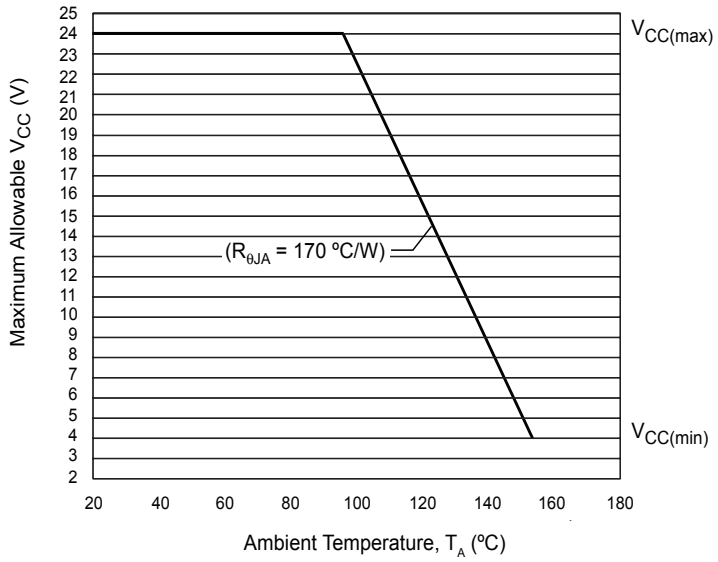


THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

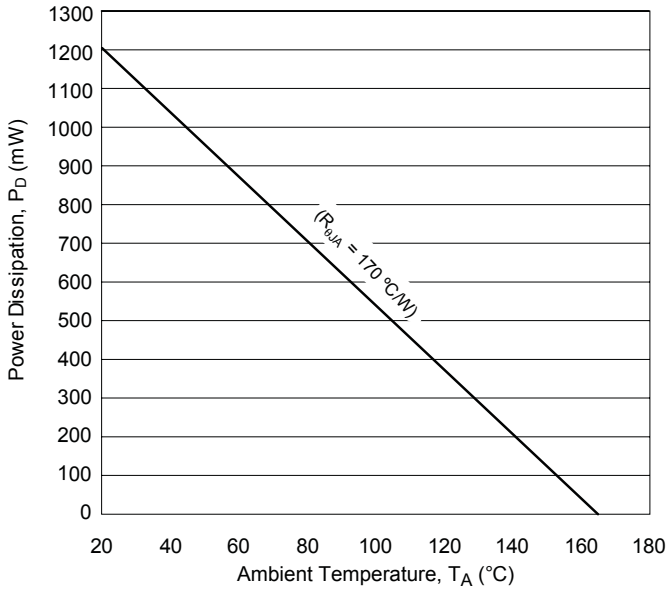
CHARACTERISTIC	Symbol	TEST CONDITIONS*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	170	ºC/W

*Additional information is available on the Allegro Web site.

Power Derating Curve



Power Dissipation versus Ambient Temperature



Functional Description

Sensing Technology

The single-chip differential Hall effect sensor IC possesses two Hall elements, which sense the magnetic profile of the ring magnet simultaneously, but at different points (spaced at a 1.5 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature compensated amplifier and offset compensation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset compensation circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling

An operating device is capable of providing digital information that is representative of the magnetic features on a rotating target. The waveform diagram shown in figure 3 presents the automatic translation of the magnetic profile to the digital output signal of the device.

Output Polarity

Figure 3 shows the output polarity for the orientation of target and device shown in figure 2. The target direction of rotation shown is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 4 side. This results in the device output switching from high, $I_{CC(High)}$, to low $I_{CC(Low)}$, as the leading edge of a north magnetic pole passes the device face. In this configuration, the device output current switches to its low polarity when a north pole is the target feature nearest to the device. If the direction of rotation is reversed, then the output polarity inverts.

Note that output voltage polarity is dependent on the position of the sense resistor, R_{SENSE} (see figure 4).

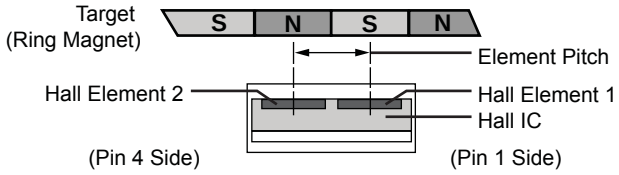


Figure 1. Relative motion of the target is detected by the dual Hall elements mounted on the Hall IC.

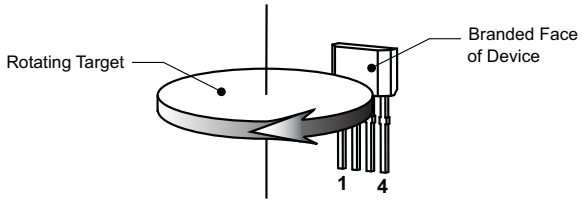


Figure 2. This left-to-right (pin 1 to pin 4) direction of target rotation results in a low output signal when a magnetic north pole of the target is nearest the face of the device (see figure 3). A right-to-left (pin 4 to pin 1) rotation inverts the output signal polarity.

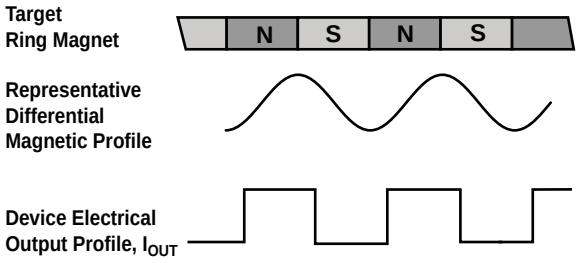


Figure 3. Output Profile of a ring magnet target for the polarity indicated in figure 2.

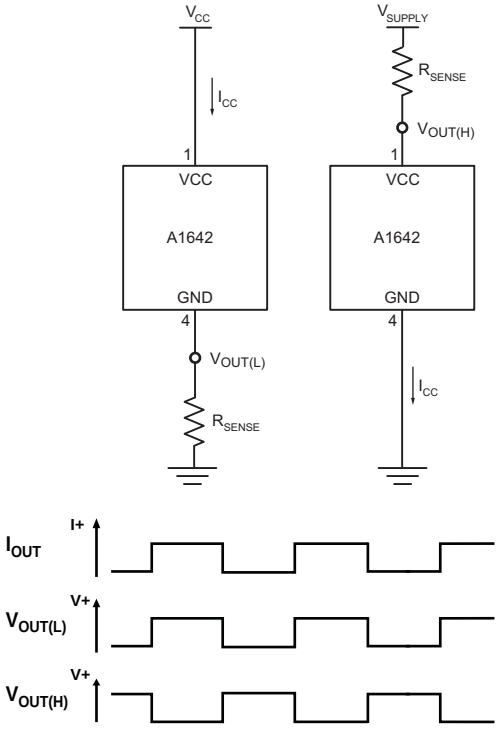


Figure 4: Voltage profiles for high side and low side two-wire sensing.

Automatic Gain Control (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). During calibration, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain of the device is then automatically adjusted. Figure 5 illustrates the effect of this feature.

Automatic Offset Adjust (AOA)

The AOA is patented circuitry that automatically compensates for the effects of chip, magnet, and installation offsets. (For capability, see Dynamic Offset Cancellation, in the Operating Characteristics table.) This circuitry is continuously active, including both during calibration mode and running mode, compensating for offset drift. Continuous operation also allows it to compensate for offsets induced by temperature variations over time.

Digital Peak Detection

A digital DAC tracks the internal analog voltage signal V_{PROC}, and is used for holding the peak value of the internal analog signal. In the example shown in figure 6, the DAC would first track up with the signal and hold the upper peak's value. When V_{PROC} drops below this peak value by B_{OP}, the device hysteresis, the output would switch and the DAC would begin tracking the signal downward toward the negative V_{PROC} peak. Once the DAC acquires the negative peak, the output will again switch states when V_{PROC} is greater than the peak by the value B_{RP}. At this point, the DAC tracks up again and the cycle repeats. The digital tracking of the differential analog signal allows the device to achieve true zero-speed operation.

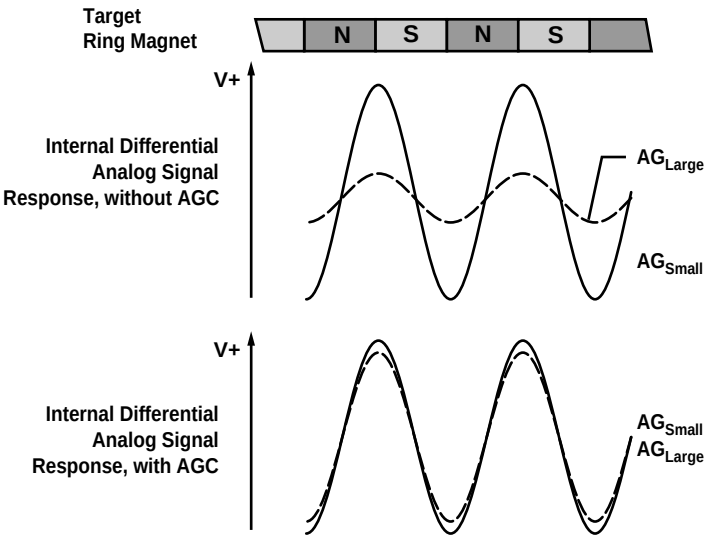


Figure 5. Automatic Gain Control (AGC). The AGC function corrects for variances in the air gap. Differences in the air gap affect the magnetic gradient, but AGC prevents that from affecting device performance, as shown in the lowest panel.

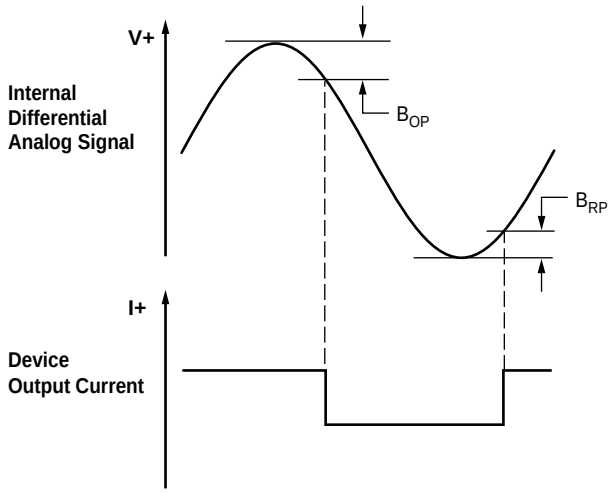


Figure 6: Peak Detecting Switchpoint Detail

Power Supply Protection

The device contains an on-chip regulator and can operate over a wide V_{CC} range. For devices that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro Microsystems for information on the circuitry needed for compliance with various EMC specifications. Refer to figure 7 for an example of a basic application circuit.

Undervoltage Lockout

When the supply voltage falls below the undervoltage lockout voltage, $V_{CC(UV)}$, the device enters Reset, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied. I_{CC} levels may not meet datasheet limits when $V_{CC} < V_{CC(min)}$.

Assembly Description

This device is integrally molded into a plastic body that has been optimized for size, ease of assembly, and manufacturability. High operating temperature materials are used in all aspects of construction.

Diagnostics

The regulated current output is configured for two wire applications, requiring one less wire for operation than do switches with the more traditional open-collector output. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges, shown in figure 8 as $I_{CC(High)}$ and $I_{CC(Low)}$. Any current level not within these ranges indicates a fault condition. If $I_{CC} > I_{CC(High)max}$, then a short condition exists, and if $I_{CC} < I_{CC(low)min}$, then an open condition exists. Any value of I_{CC} between the allowed ranges for $I_{CC(High)}$ and $I_{CC(Low)}$ indicates a general fault condition.

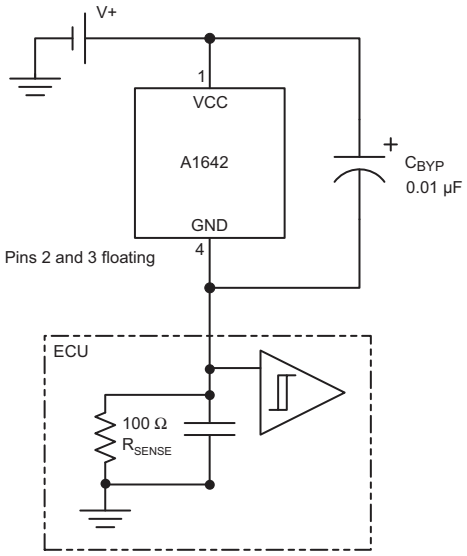


Figure 7: Typical Application Circuit

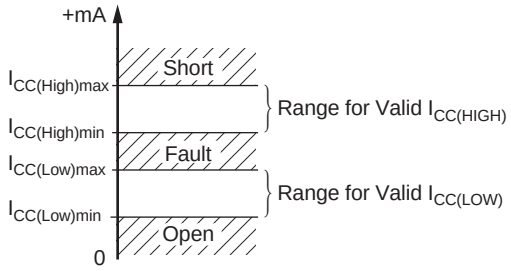


Figure 8: Diagnostic Characteristics of Supply Current Values

DEVICE OPERATION

Each operating mode is described in detail below.

Power-On

When power ($V_{CC} > V_{CC(Min)}$) is applied to the device, a short period of time is required to power the various portions of the IC. During this period, the A1642 powers-on in the high current state, $I_{CC(High)}$. After power-on, there are conditions that could induce a change in the output state. Such an event could be caused by thermal transients, but would require a static applied magnetic field, proper signal polarity, and particular direction and magnitude of internal signal drift.

Initial Offset Adjust

The device initially cancels the effects of chip, magnet, and installation offsets. Once offsets have been cancelled, the digital tracking DAC is ready to track the signal and provide output switching. The period of time required for both Power-On and Initial Offset Adjust is defined as the Power-On Time.

Calibration Mode

The calibration mode allows the device to automatically select the proper signal gain and continue to adjust for offsets. The AGC is active, and selects the optimal signal gain based on the amplitude of the V_{PROC} signal. Following each adjustment to the AGC DAC, the Offset DAC is also adjusted to ensure the internal analog signal is properly centered.

During this mode, the tracking DAC is active and output switching occurs, but the duty cycle is not guaranteed to be within specification.

Running Mode

After the Initial Calibration period, C_I, establishes a signal gain, the device moves to Running mode. During Running mode, the device tracks the input signal and gives an output edge for every peak of the signal. AOA remains active to compensate for any offset drift over time.

The A1642 incorporates a novel algorithm for adjusting the signal gain during Running mode. This algorithm is designed to optimize the V_{PROC} signal amplitude in instances where the magnetic signal "seen" during the calibration period is not representative of the amplitude of the magnetic signal for the installed device air gap (see figure 9).

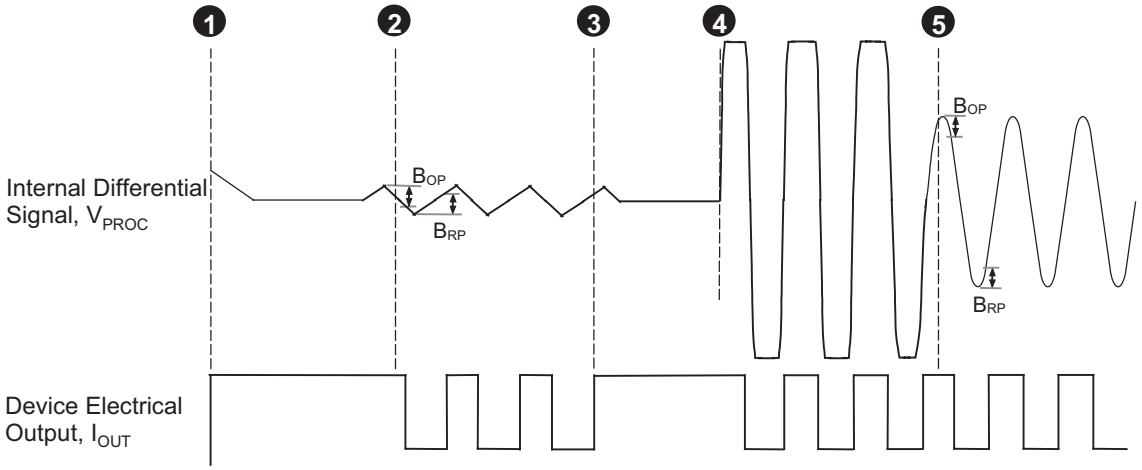


Figure 9: Operation of Running Mode Gain Adjust.

Position 1. The device is initially powered-on. Self-calibration occurs.

Position 2. Small amplitude oscillation of the target sends an erroneously small differential signal to the device. The amplitude of V_{PROC} is greater than the switching hysteresis (B_{OP} and B_{RP}), and the device output switches.

Position 3. The calibration period completes on the third rising output edge, and the device enters Running mode.

Position 4. True target rotation occurs and the correct magnetic signal is generated for the installation air gap. The established signal gain is too large for the target's rotational magnetic signal at the given air gap.

Position 5. Running Mode Calibration corrects the signal gain to an optimal level for the installation air gap.

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 6 mA, and $R_{\theta JA}$ = 170 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 6\ mA = 72\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 72\ mW \times 170\ °C/W = 12.2°C$$

$$T_J = T_A + \Delta T = 25°C + 12.2°C = 37.2°C$$

A worst-case estimate, $P_D(max)$, represents the maximum allowable power level ($V_{CC}(max)$, $I_{CC}(max)$), without exceeding $T_J(max)$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package KN (I1 trim), using 1-layer PCB

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=170 °C/W, $T_J(max)$=165°C, $V_{CC}(max)$=24 V, and $I_{CC}(max)$ = 16 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 170\ °C/W = 88.2\,mW$$

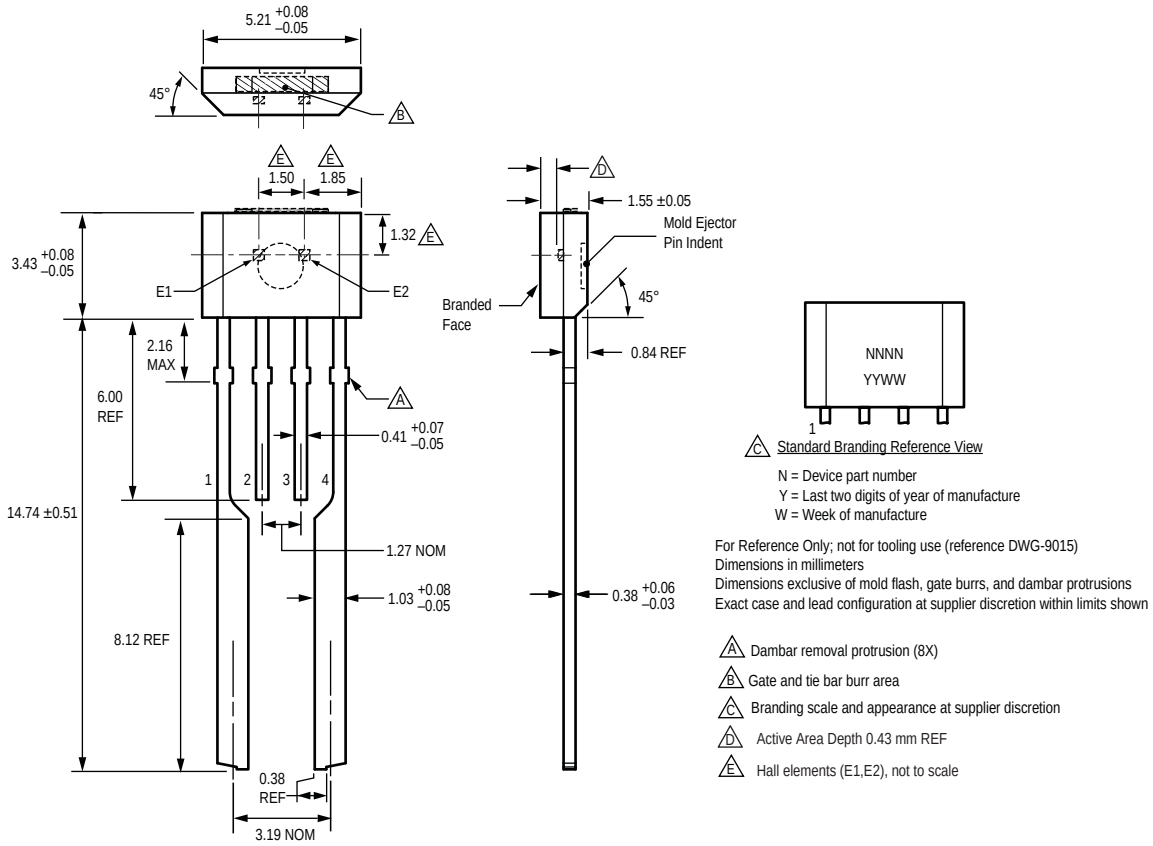
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_D(max) \div I_{CC}(max) = 88.2\,mW \div 16\,mA = 5.5\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC}(max)$. If $V_{CC(est)} \leq V_{CC}(max)$, then reliable operation between $V_{CC(est)}$ and $V_{CC}(max)$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC}(max)$, then operation between $V_{CC(est)}$ and $V_{CC}(max)$ is reliable under these conditions.

Package KN, 4-Pin SIP



Revision History

Revision	Revision Date	Description of Revision
Rev. 4	January 16, 2012	Update product variants offered

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www.allegromicro.com