2981 and 2982

8-Channel Source Drivers

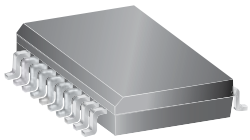
Features and Benefits

- TTL, DTL, PMOS, or CMOS compatible inputs
- 500 mA output source current capability
- Transient-protected outputs
- Output breakdown voltage to 50 V
- DIP or SOIC packaging

Packages:

Not to scale

18-pin DIP (Package A)



20-pin SOICW (package LW)
(drop-in replacement for discontinued 18-pin SOIC variants)

Description

Recommended for high-side switching applications that benefit from separate logic and load grounds, these devices encompass load supply voltages to 50 V and output currents to -500 mA. These 8-channel source drivers are useful for interfacing between low-level logic and high-current loads. Typical loads include relays, solenoids, lamps, stepper and/or servo motors, print hammers, and LEDs.

All devices may be used with 5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. The device packages offered are electrically interchangeable, and will withstand a maximum output off voltage of 50 V, and operate to a minimum of 5 V. All devices in this series integrate input current limiting resistors and output transient suppression diodes, and are activated by an active high input.

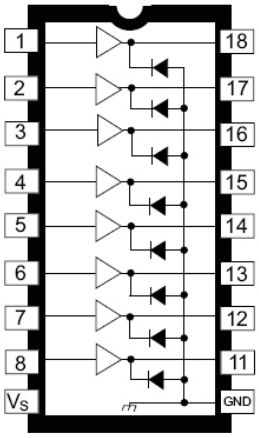
The suffix "A" indicates an 18-lead plastic dual in-line package with copper lead frame for optimum power dissipation. Under normal operating conditions, these devices will sustain 120 mA continuously for each of the eight outputs at an ambient temperature of +50°C and a supply of 15 V.

The suffix "LW" package is provided in a 20-pin wide-body SOIC package with improved thermal characteristics compared to the 18-pin SOIC version it replaces (100% pin-compatible electrically). The A2982ELW driver is available for operation over an extended temperature range, down to -40°C.

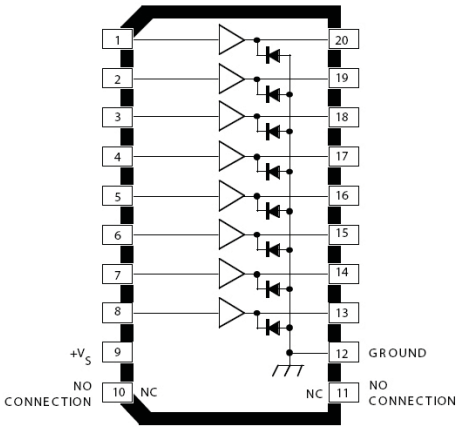
These packages are lead (Pb) free, with 100% matte-tin leadframe plating.

Simplified Block Diagrams

18-pin DIP (A Package)



20-pin SOICW (LW Package)



(NC pins, 10 and 11, not present on discontinued 18-pin LW package)

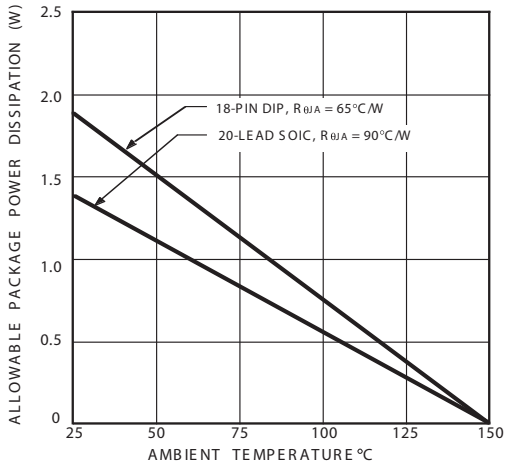
Selection Guide

Part Number	Package	Packing	Ambient Temperature T_A (°C)
A2982ELWTR-T*	20-pin SOICW	1000 per reel	–40 to 85
A2982SLWTR-T	20-pin SOICW	1000 per reel	–20 to 85
UDN2981A-T	18-pin DIP	21 per tube	
UDN2982A-T	18-pin DIP	21 per tube	

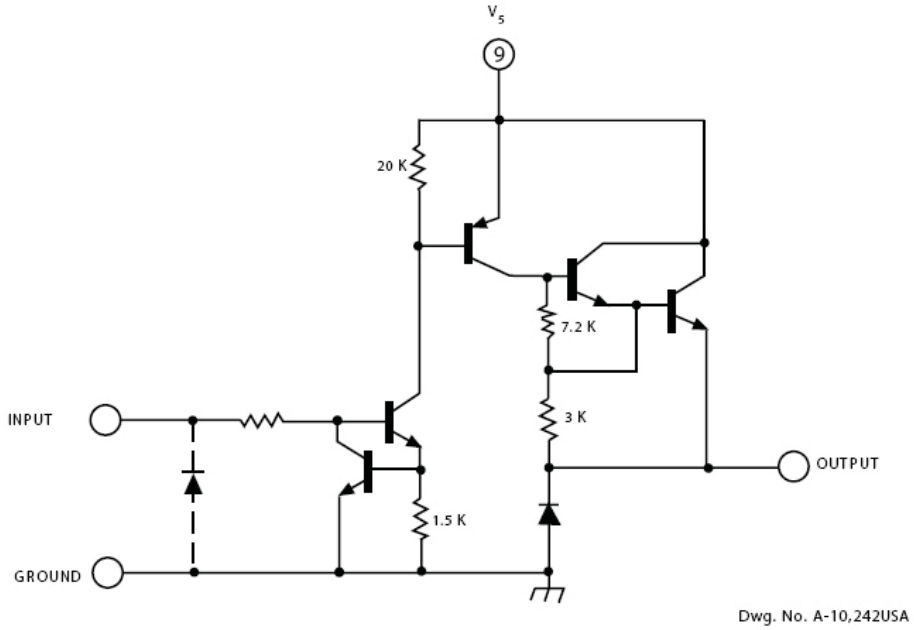
*Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Output Voltage Range	V_{CE}		5 to 50	V
Input Voltage	V_{IN}	UDN2981	25	V
		A2982, UDN2982	20	V
Output Current	I_{OUT}		–500	mA
Package Power Dissipation	P_D	See graph	–	–
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range S	–20 to 85	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C

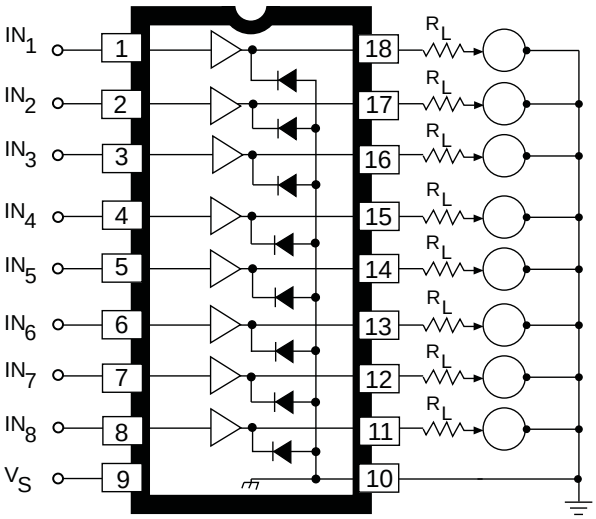


One of Eight Drivers

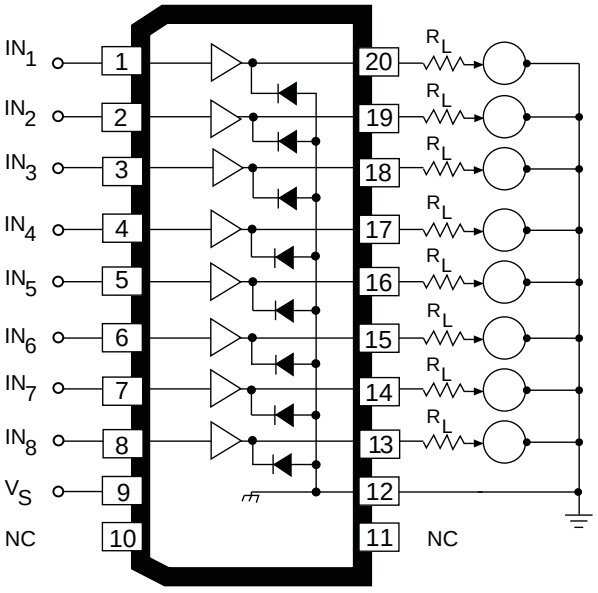


Typical electrosensitive printer application

18-pin DIP (A Package)



20-pin SOICW (LW Package)



Pins 10 and 11 can float; other pins match discontinued 18-pin SOIC: 1 to 9 same, pins 12 to 20 match pins 10 to 18

ELECTRICAL CHARACTERISTICS[1,2] at T_A = +25°C (unless otherwise specified).

Characteristic	Symbol	Variant	Test Conditions	Test Fig.	Min.	Typ.	Max.	Units
Output Leakage Current[3]	I_{CEX}	All	V_{IN} = 0.4 V, V_S = 50 V	1	—	—	20	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	All	I_{OUT} = -45 mA	—	35	—	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	V_{IN} = 2.4 V, I_{OUT} = -100 mA	2	—	1.6	1.8	V
			V_{IN} = 2.4 V, I_{OUT} = -225 mA	2	—	1.7	1.9	V
			V_{IN} = 2.4 V, I_{OUT} = -350 mA	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	2981	V_{IN} = 2.4 V	3	—	140	200	µA
			V_{IN} = 3.85 V	3	—	310	450	µA
		2982	V_{IN} = 2.4 V	3	—	140	200	µA
			V_{IN} = 12 V	3	—	1.25	1.93	mA
Output Source Current (Outputs Open)	I_{OUT}	2981	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	-350	—	—	mA
		2982	V_{IN} = 2.4 V, V_{CE} = 2.0 V	2	-350	—	—	mA
Supply Current Leakage Current	I_S	All	V_{IN} = 2.4 V*, V_S = 50 V	4	—	—	10	mA
Clamp Diode Current	I_R	All	V_R = 50 V, V_{IN} = 0.4 V*	5	—	—	50	µA
Clamp Diode Forward Voltage	V_F	All	I_F = 350 mA	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V	—	—	0.3	2.0	µs
Turn-Off Delay[4]	t_{OFF}	All	0.5 E_{IN} to 0.5 E_{OUT}, R_L = 100Ω, V_S = 35 V, See Note	—	—	2.0	10	µs

[1]Negative current is defined as coming out of (sourcing) the specified device terminal.

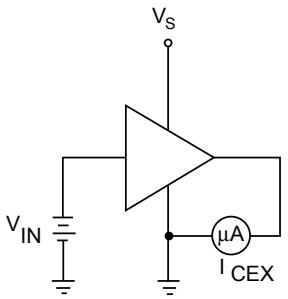
[2]All unused inputs must be connected to ground. Pull-down resistors (approximately 10 kΩ) are recommended for inputs that are allowed to float while power is being applied to V_S.

[3]All inputs simultaneously.

[4]Turn-off delay is influenced by load conditions. Systems applications well below the specified output loading may require timing considerations for some designs, i.e., multiplexed displays or when used in combination with sink drivers in a totem pole configuration.

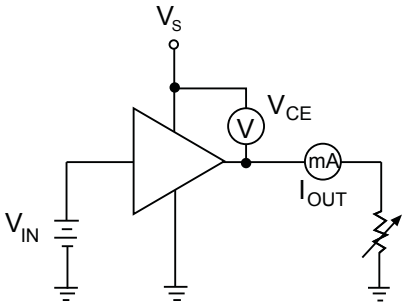
TEST FIGURES

Figure 1



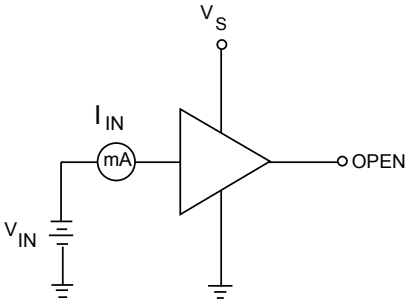
Dwg. No. A-11,083

Figure 2



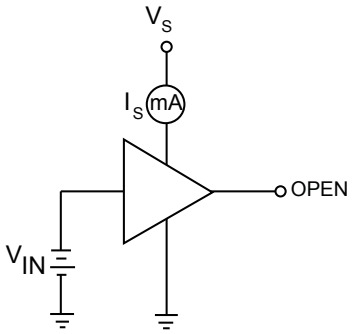
Dwg. No. A-11,084

Figure 3



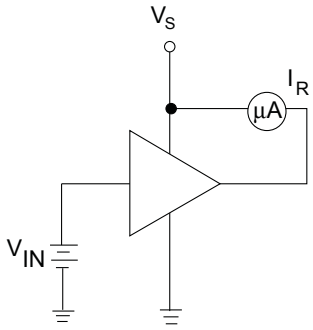
Dwg. No. A-11,085

Figure 4



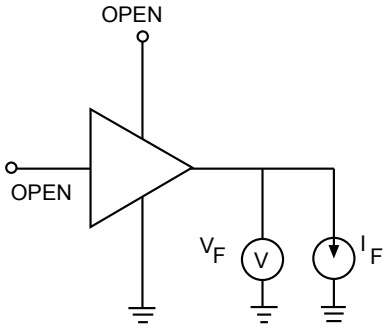
Dwg. No. A-11,086

Figure 5



Dwg. No. A-11,087

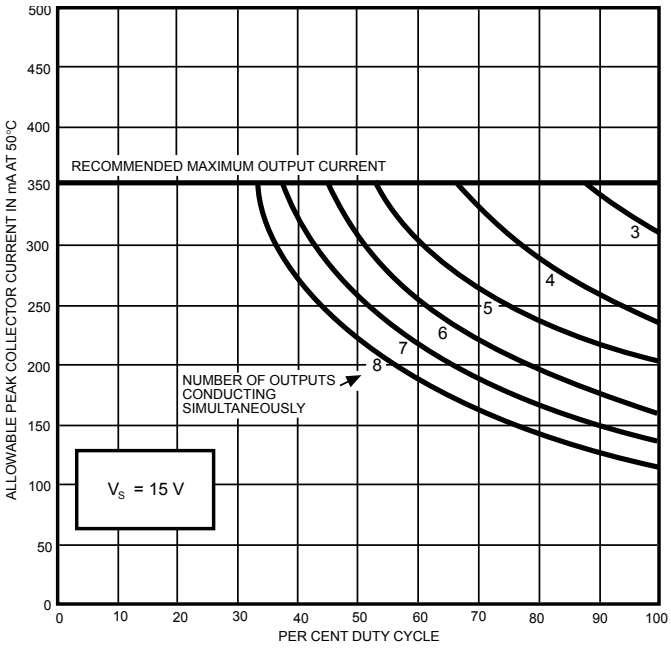
Figure 6



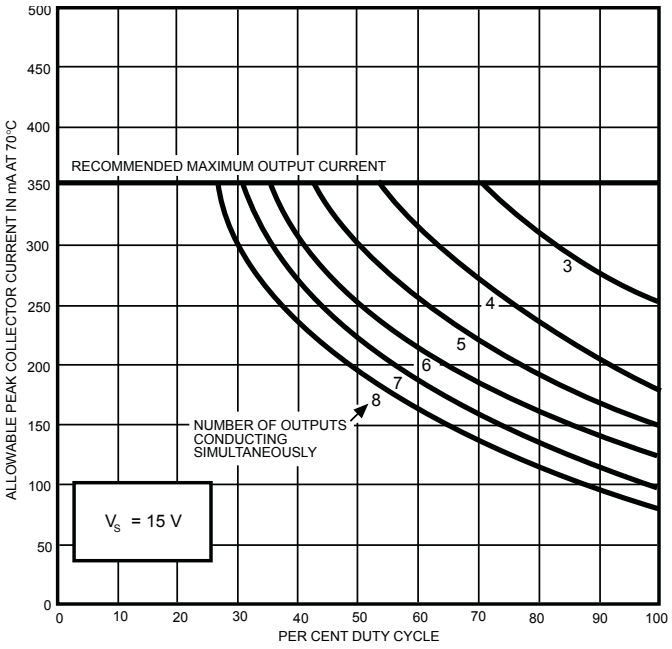
Dwg. No. A-11,088

Allowable peak collector current as a function of duty cycle

UDN2981A and UDN2982A

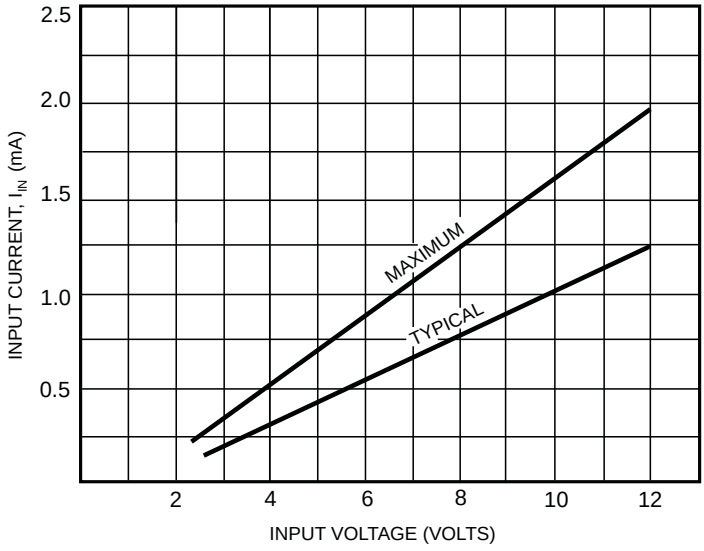


Dwg. No. A-11,107B



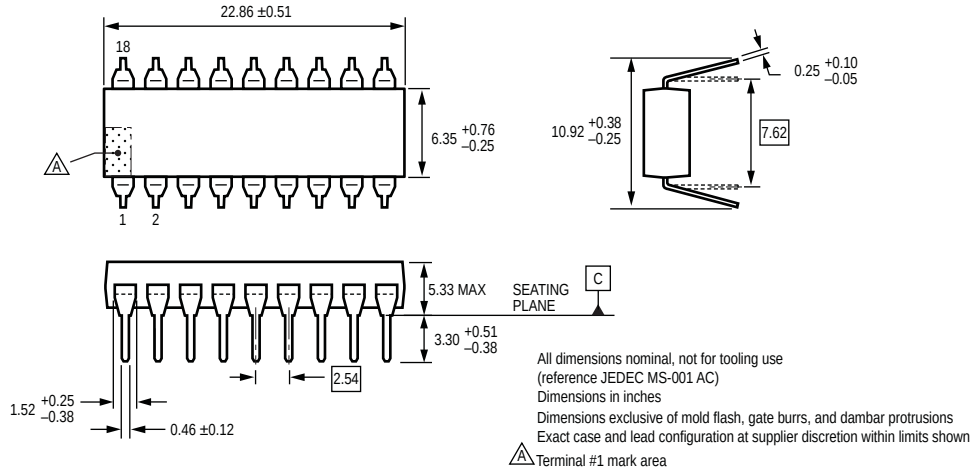
Dwg. No. A-11,108B

Input current as a function of input voltage



Dwg. No. A-11,115B

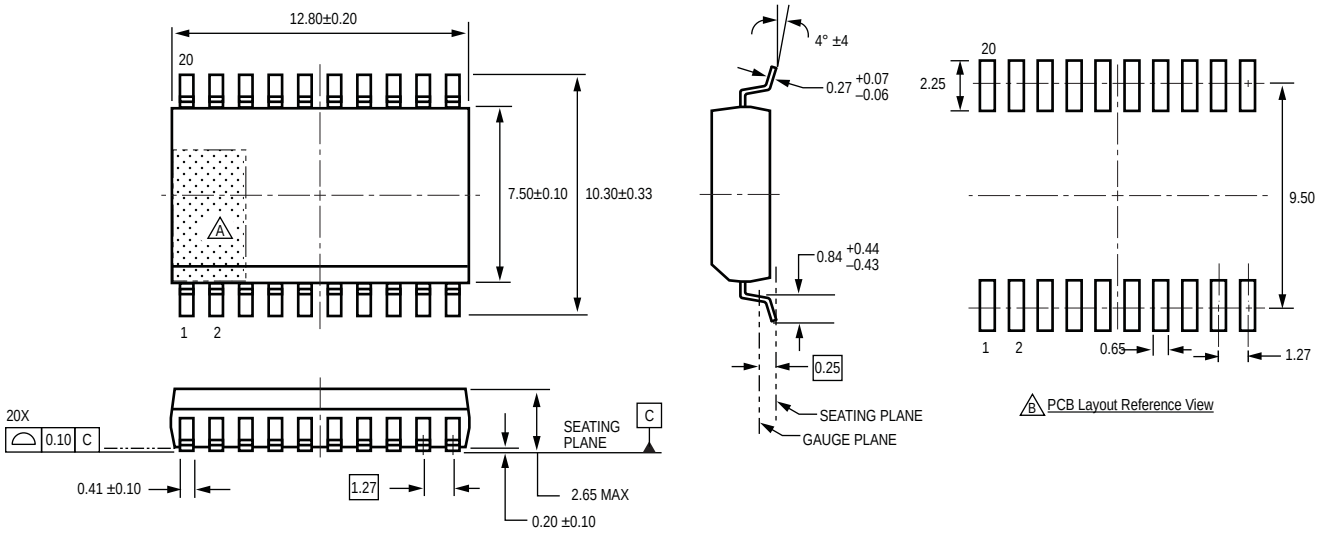
A Package, 18-Pin DIP



All dimensions nominal, not for tooling use
(reference JEDEC MS-001 AC)
Dimensions in inches
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

LW Package, 20-Pin SOICW



For Reference Only
Dimensions in millimeters
(Reference JEDEC MS-013 AC)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-20M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
to meet application process requirements and PCB layout tolerances

For the latest version of this document, visit our website:
www.allegromicro.com