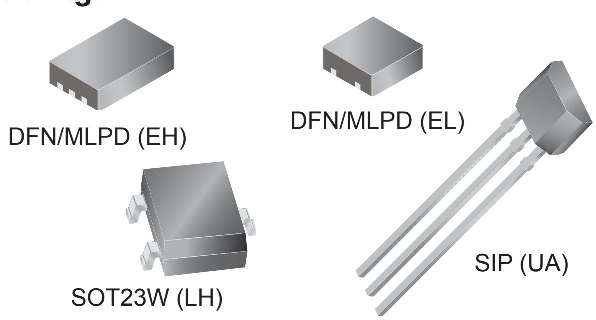
A3211 and A3212

Micropower, Ultra-sensitive Hall-effect Switches

Features and Benefits

- Micropower operation
- Operation with north or south pole
- 2.5 to 3.5 V battery operation
- Chopper stabilized
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- High ESD protection
- Solid-state reliability
- Small size
- Easily manufacturable with magnet pole independence

Packages:



Not to scale

Description

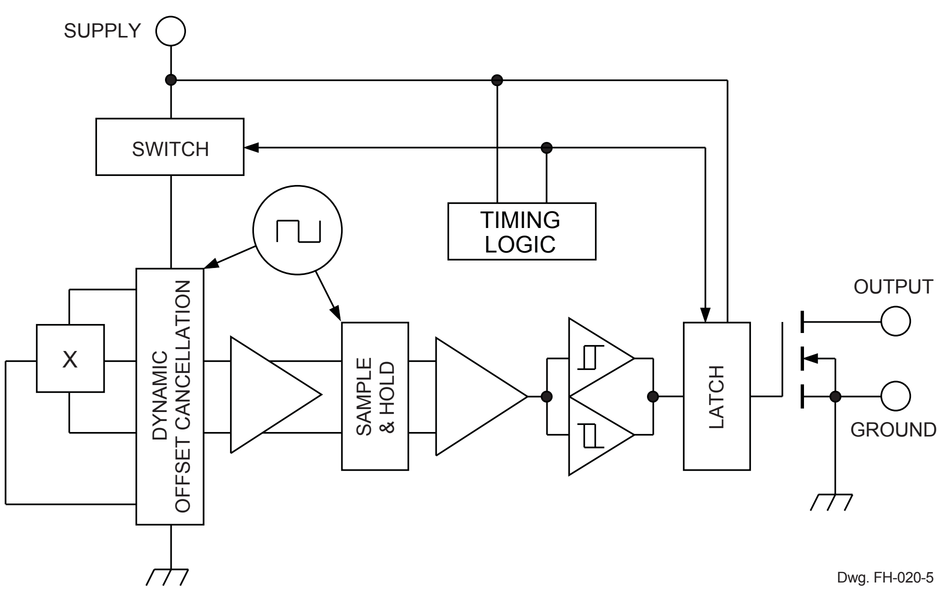
The A 3211 and A3212 integrated circuits are ultra-sensitive, pole independent Hall-effect switches with latched digital output. These sensors are especially suited for operation in battery-operated, hand-held equipment such as cellular and cordless telephones, pagers, and palmtop computers. A 2.5 volt to 3.5 volt operation and a unique clocking scheme reduce the average operating power requirements to less than 15 μW with a 2.75 volt supply.

Unlike other Hall-effect switches, either a north or south pole of sufficient strength will turn the output on in the A3212, and in the absence of a magnetic field, the output is off. The A3211 provides an inverted output. The polarity independence and minimal power requirements allow these devices to easily replace reed switches for superior reliability and ease of manufacturing, while eliminating the requirement for signal conditioning.

Improved stability is made possible through chopper stabilization (dynamic offset cancellation), which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

Continued on the next page…

Functional Block Diagram



Description (continued)

This device includes on a single silicon chip a Hall-voltage generator, small-signal amplifier, chopper stabilization, a latch, and a MOSFET output. Advanced BiCMOS processing is used to take advantage of low-voltage and low-power requirements, component matching, very low input-offset errors, and small component geometries.

Four package styles provide magnetically optimized solutions for most applications. Miniature low-profile surface-mount package types *EH* and *EL* (0.75 and 0.50 mm nominal height) are leadless, *LH* is a leaded low-profile SMD, and *UA* is a three-lead SIP for through-hole mounting. Packages are available in lead (Pb) free versions (suffix, *–T*) with 100% matte tin plated leadframe. EL package for limited release, engineering samples available.

Selection Guide

Part Number	Pb-free[1]	Packing[2] (Units/Pack)	Package	Ambient Temperature T_A (°C)
A3211EEHLT–T	Yes	Tape and Reel (3000)	Leadless Surface Mount	–40 to 85
A3211EELLT–T	Yes	Tape and Reel (3000)		
A3211ELHLT–T	Yes	Tape and Reel (3000)	3-Pin Surface Mount	
A3212EEHLT–T	Yes	Tape and Reel (3000)	Leadless Surface Mount	–40 to 85
A3212EELLT–T	Yes	Tape and Reel (3000)		
A3212ELHLT–T	Yes	Tape and Reel (3000)	3-Pin Surface Mount	
A3212EUA–T	Yes	Bulk Pack (500)	SIP-3 Through Hole, Straight Lead	
A3212LLHLT–T	Yes	Tape and Reel (3000)	3-Pin Surface Mount	–40 to 150
A3212LUA–T	Yes	Bulk Pack (500)	SIP-3 Through Hole, Straight Lead	

[1]Pb-based variants are being phased out of the product line.

a. Certain variants cited in this footnote are in production but have been determined to be LAST TIME BUY. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2006. Deadlilne for receipt of LAST TIME BUY ORDERS: April 27, 2007. These variants include: A3212LLHLT and A3212LUA.

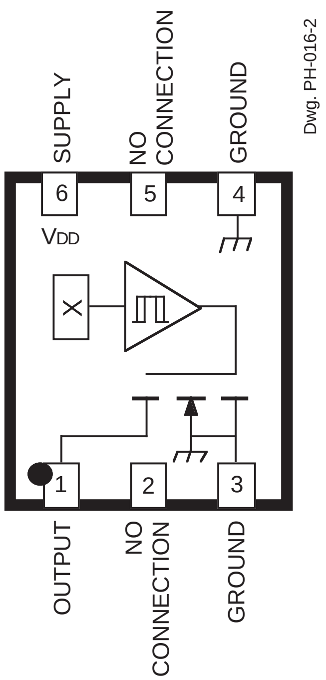
b. Certain variants cited in this footnote are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The variants should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 1, 2006 for A3212EEHLT, A3212ELHLT, and A3212EUA.

[2]Contact Allegro for additional packaging and handling options.

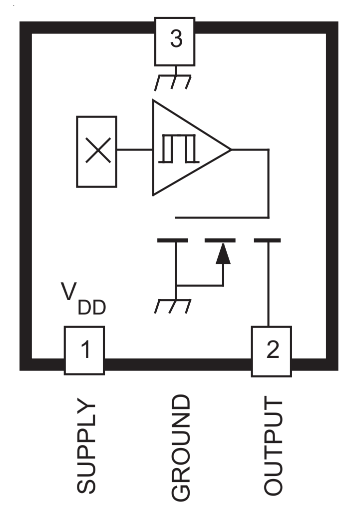
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{DD}		5	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	V_{OUT}		5	V
Output Current	I_{OUT}		1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Package Suffix 'EH' Pinning
(Leadless Chip Carrier)



Package Suffix 'EL' Pinning
(Leadless Chip Carrier)



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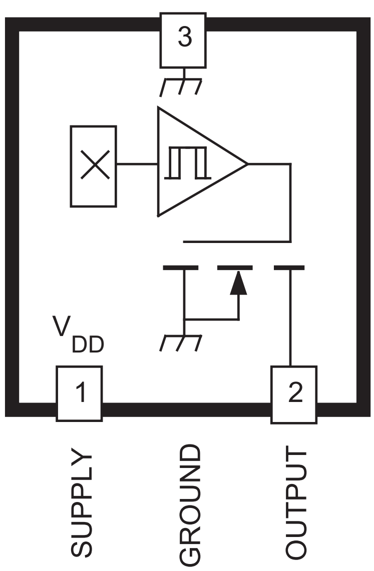
Package Suffix 'LH' Pinning
(SOT23W)



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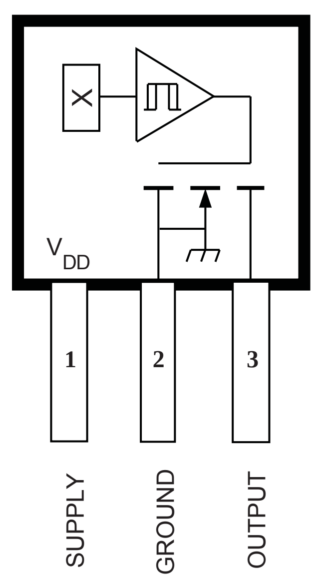
Package Suffix 'UA' Pinning
(SIP)



Dwg. PH-016

Pinning is shown viewed from branded side.

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ELECTRICAL CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.*	Max.	Units
Supply Voltage Range	V_{DD}	Operating	2.5	2.75	3.5	V
Output Leakage Current	I_{OFF}	V_{OUT} = 3.5 V, Output off	–	<1.0	1.0	µA
Output On Voltage	V_{OUT}	I_{OUT} = 1 mA, V_{DD} = 2.75 V	–	100	300	mV
Awake Time	t_{awake}		–	45	90	µs
Period	t_{period}		–	45	90	ms
Duty Cycle	d.c.		–	0.1	–	%
Chopping Frequency	f_C		–	340	–	kHz
Supply Current	$I_{DD(EN)}$	Chip awake (enabled)	–	–	2.0	mA
	$I_{DD(DIS)}$	Chip asleep (disabled)	–	–	8.0	µA
	$I_{DD(AVG)}$	V_{DD} = 2.75 V	–	5.1	10	µA
		V_{DD} = 3.5 V	–	6.7	10	µA

* Typical data is at T_A = 25°C and V_{DD} = 2.75 V, and is for design information only.

3211 MAGNETIC CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Points	B_{OPS}	South pole to branded side; B > B_{OP}, V_{OUT} = High (Output Off)	–	37	55	G
	B_{OPN}	North pole to branded side; B > B_{OP}, V_{OUT} = High (Output Off)	–55	–40	–	G
Release Points	B_{RPS}	South pole to branded side; B < B_{RP}, V_{OUT} = Low (Output On)	10	31	–	G
	B_{RPN}	North pole to branded side; B < B_{RP}, V_{OUT} = Low (Output On)	–	–34	–10	G
Hysteresis	B_{HYS}	$\|B_{OPx} - B_{RPx}\|$	–	5.9	–	G

NOTES: 1. Negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.
2. B_{OPx} = operate point (output turns off); B_{RPx} = release point (output turns on).
3. Typical Data is at T_A = +25°C and V_{DD} = 2.75 V and is for design information only.
4. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).

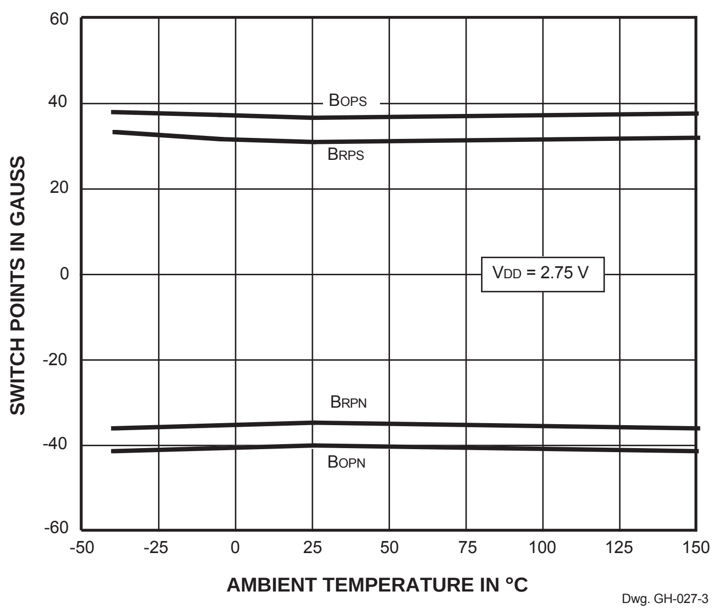
3212 MAGNETIC CHARACTERISTICS over operating voltage and temperature range (unless otherwise specified)

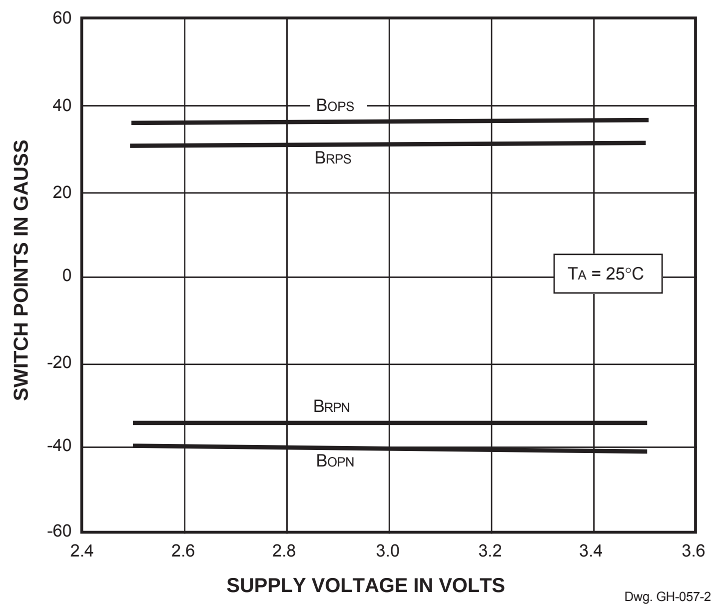
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Points	B_{OPS}	South pole to branded side; B > B_{OP}, V_{OUT} = Low (Output On)	–	37	55	G
	B_{OPN}	North pole to branded side; B > B_{OP}, V_{OUT} = Low (Output On)	–55	–40	–	G
Release Points	B_{RPS}	South pole to branded side; B < B_{RP}, V_{OUT} = High (Output Off)	10	31	–	G
	B_{RPN}	North pole to branded side; B < B_{RP}, V_{OUT} = High (Output Off)	–	–34	–10	G
Hysteresis	B_{HYS}	$\|B_{OPx} - B_{RPx}\|$	–	5.9	–	G

NOTES: 1. Negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.
2. B_{OPx} = operate point (output turns on); B_{RPx} = release point (output turns off).
3. Typical Data is at T_A = +25°C and V_{DD} = 2.75 V and is for design information only.
4. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).

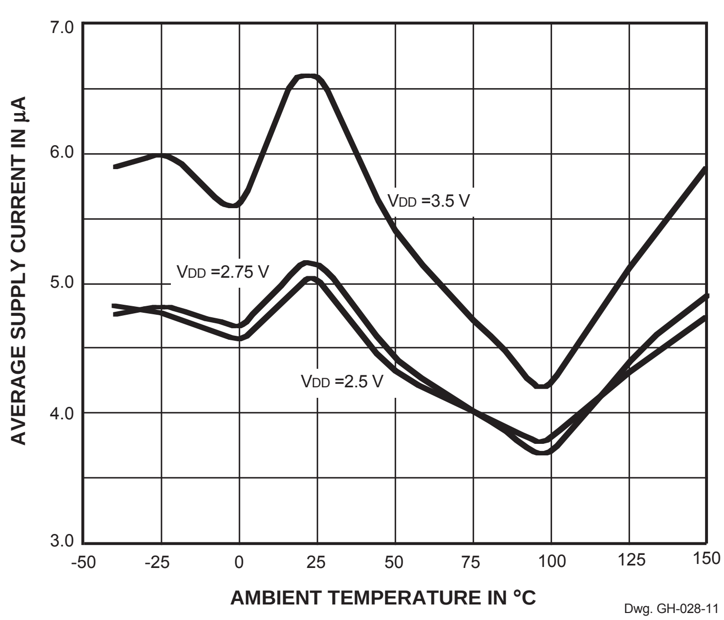
TYPICAL OPERATING CHARACTERISTICS

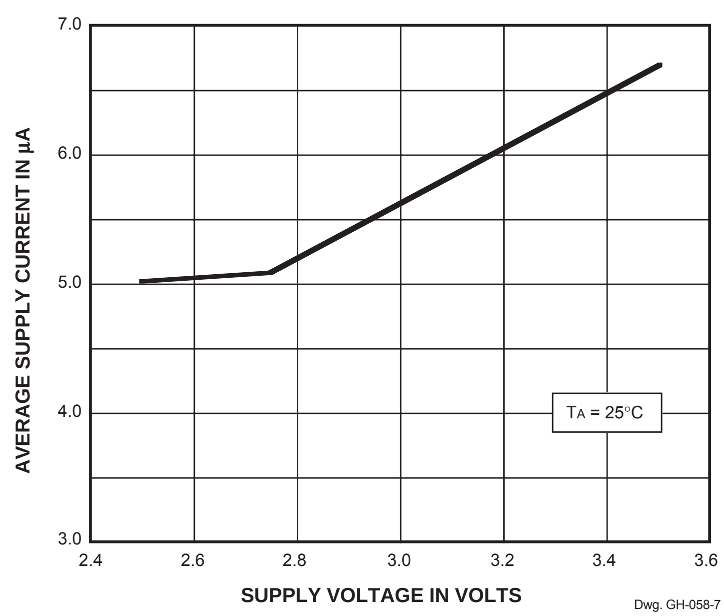
SWITCH POINTS





SUPPLY CURRENT





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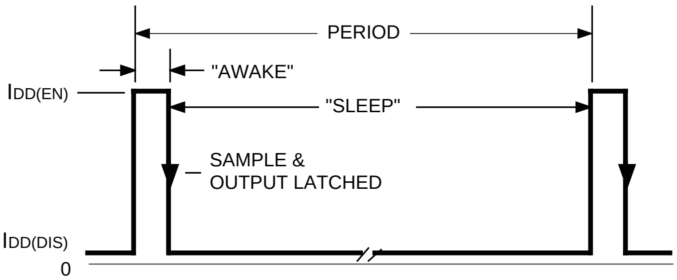
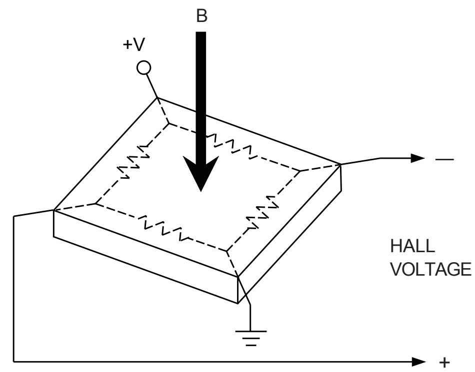
FUNCTIONAL DESCRIPTION

Low Average Power. Internal timing circuitry activates the sensor for 45 µs and deactivates it for the remainder of the period (45 ms). A short "awake" time allows for stabilization prior to the sensor sampling and data latching on the falling edge of the timing pulse. The output during the "sleep" time is latched in the last sampled state. The supply current is not affected by the output state.



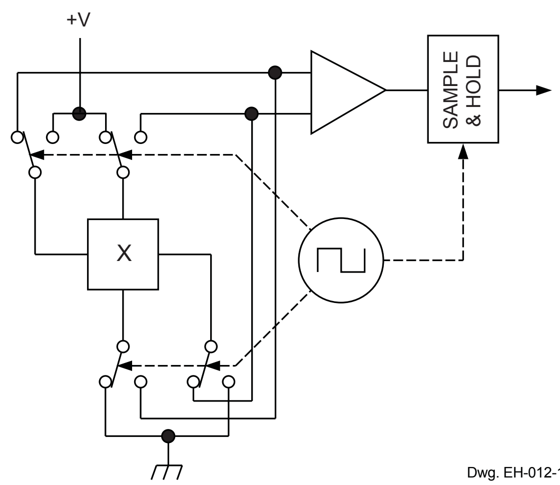
Dwg. WH-017-2



Dwg. AH-011-2

Chopper-Stabilized Technique. The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaing the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. A relatively high sampling frequency is used for faster signal processing capability can be processed.

More detailed descriptions of the circuit operation can be found in: Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensor Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.



Dwg. EH-012-1

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FUNCTIONAL DESCRIPTION (cont'd)

Operation. The output of the A3212 switches low (turns on) when a magnetic field perpendicular to the Hall sensor exceeds the operate point B_{OPS} (or is less than B_{OPN}). After turn-on, the output is capable of sinking up to 1 mA and the output voltage is $V_{OUT(ON)}$. When the magnetic field is reduced below the release point B_{RPS} (or increased above B_{RPN}), the device output switches high (turns off). The difference in the magnetic operate and release points is the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The A3211 functions in the same manner, except the output voltage is reversed from the A3212, as shown in the figures to the right.

As used here, negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.

Applications. Allegro's pole-independent sensing technique allows for operation with either a north pole or south pole magnet orientation, enhancing the manufacturability of the device. The state-of-the-art technology provides the same output polarity for either pole face.

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. This is especially true due to the relatively high impedance of battery supplies.

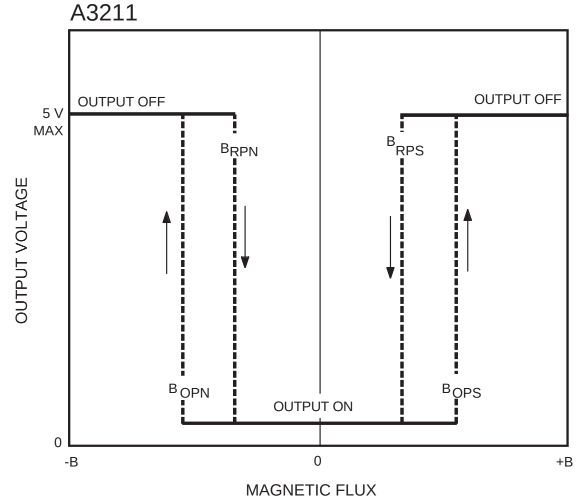
The simplest form of magnet that will operate these devices is a bar magnet with either pole near the branded surface of the device. Many other methods of operation are possible. Extensive applications information for Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide*, Application Note 27701;
- *Hall-Effect Devices: Soldering, Gluing, Potting, Encapsulating, and Lead Forming*, Application Note 27703.1;
- *Soldering of Through-Hole Hall-Sensor Dervices*, Application Note 27703; and
- *Soldering of Surface-Mount Hall-Sensor Devices*, Application Note 27703.2.

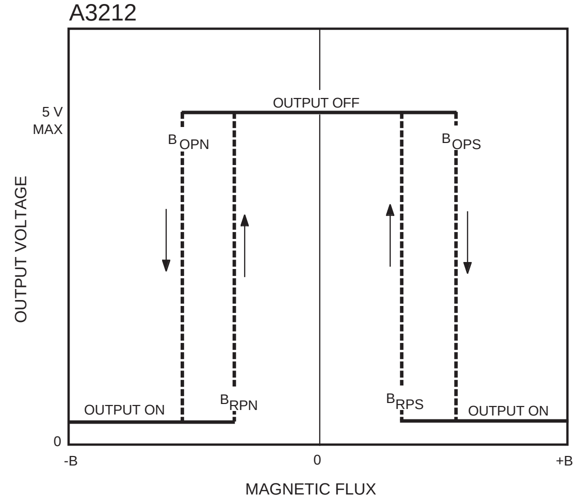
All are provided at

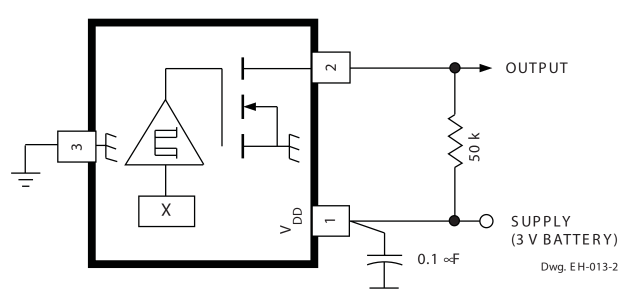
www.allegromicro.com

A3211



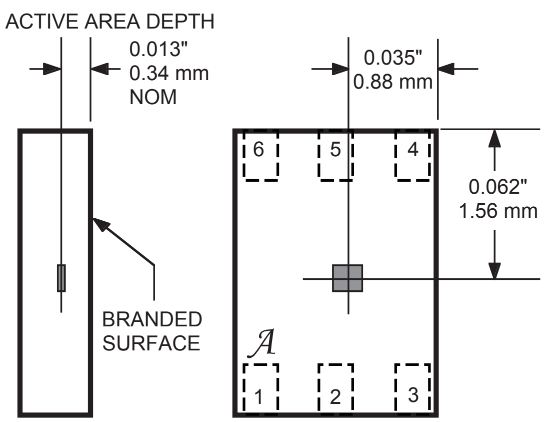
A3212



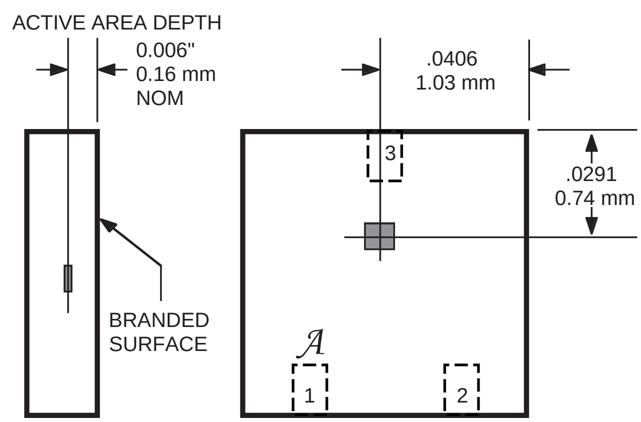


SENSOR LOCATIONS

Package Designator 'EH'

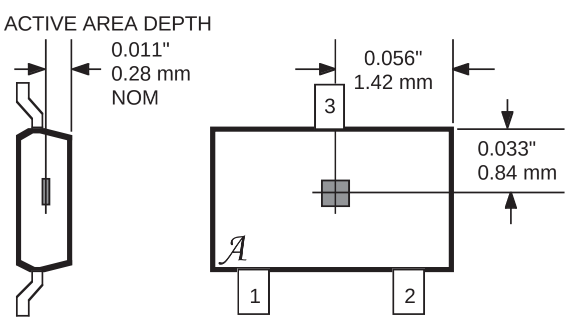


Package Designator 'EL'



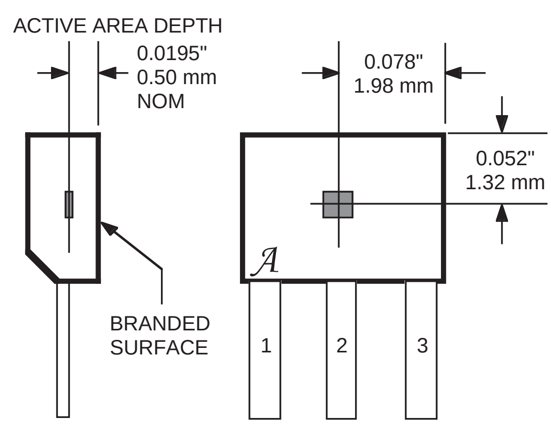
Dwg. MH-030

Package Designator 'LH'



Dwg. MH-025-2

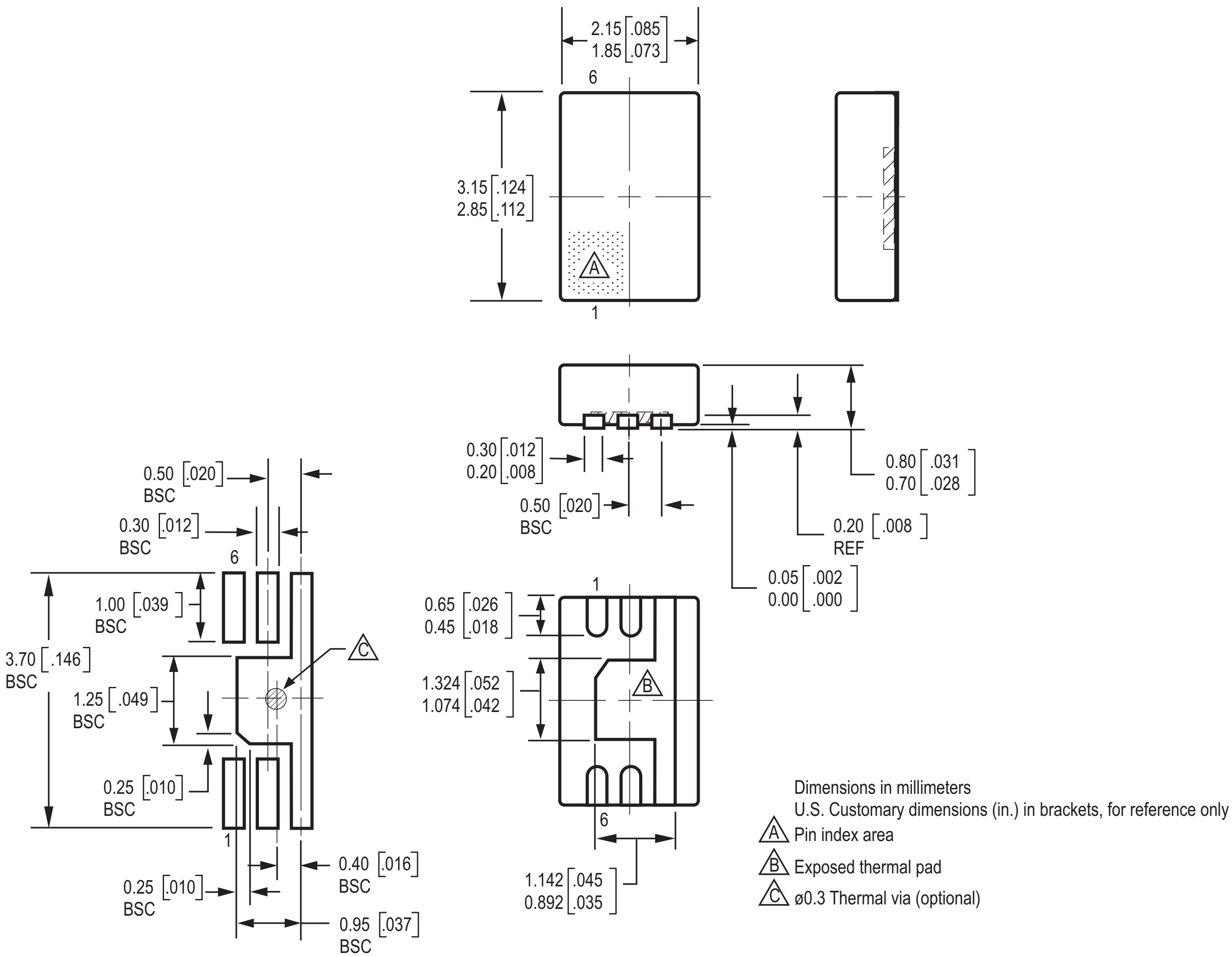
Package Designator 'UA'



Dwg. MH-011-13

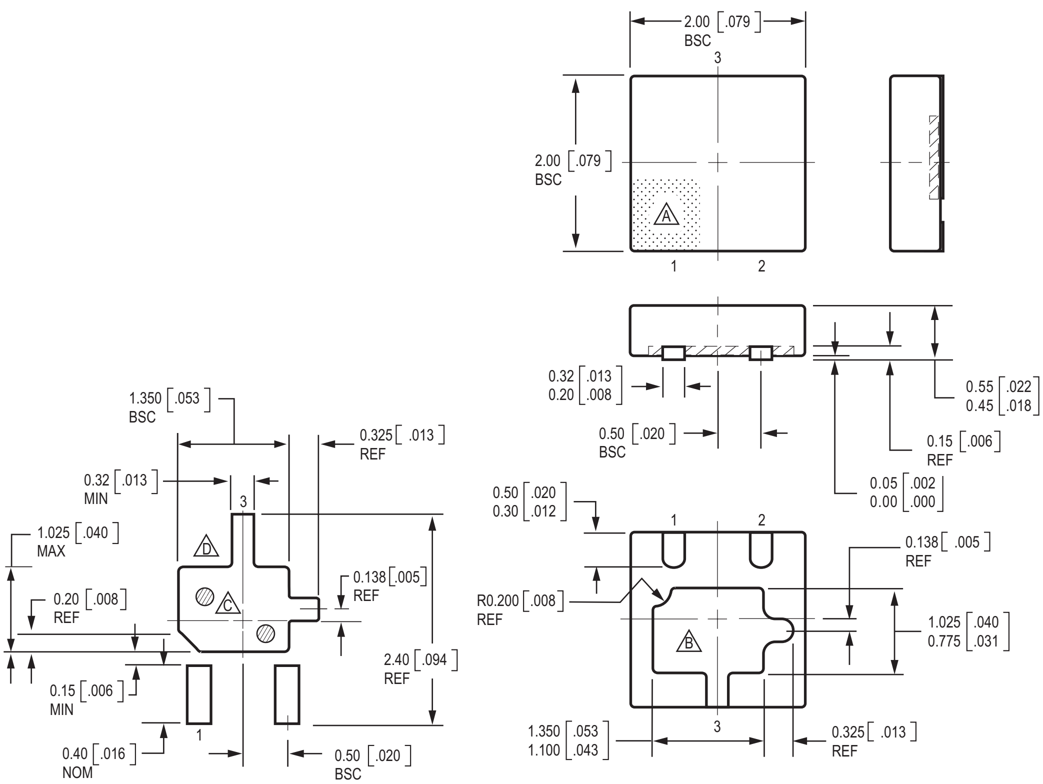
PACKAGE DESIGNATOR 'EH'

(Reference MO-229C WCED-1)



PACKAGE DESIGNATOR ‘EL'

MLPD 3 Contact

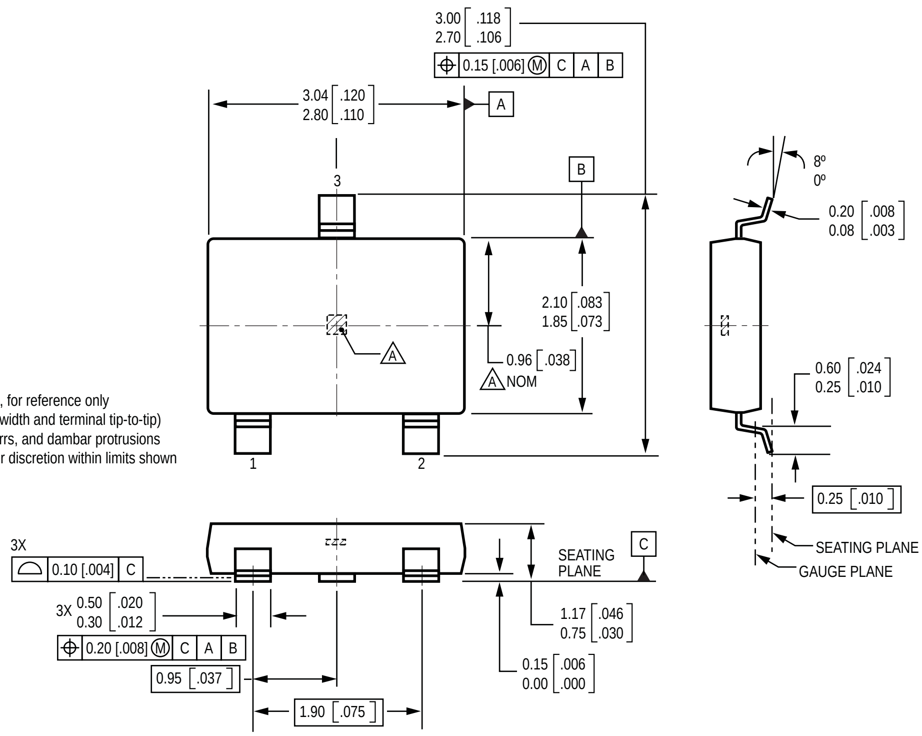


Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only

A: Pin index area
B: Exposed thermal pad
C: Optional thermal vias, ∅0.30 [.012], pitch 1.2 [.047]
D: Typical pad layout; adjust as necessary to meet application process requirements

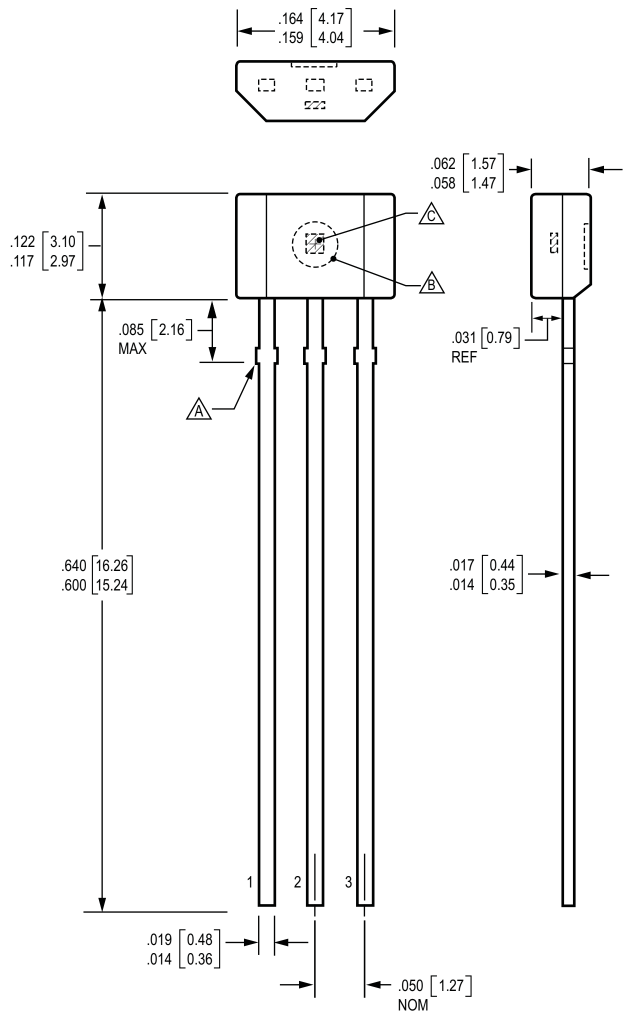
PACKAGE DESIGNATOR 'LH'

(SOT23W, fits SC-59A solder-pad layout)



Preliminary dimensions, for reference only
Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
(reference JEDEC TO-236 AB, except case width and terminal tip-to-tip)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Hall element (not to scale)

PACKAGE DESIGNATOR 'UA'



Dimensions in inches
Metric dimensions (mm) in brackets, for reference only

A Dambar removal protrusion (6X)
B Ejector mark on opposite side
C Hall element (not to scale)

The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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