Am186™CU

High-Performance, 80C186-Compatible 16-Bit Embedded USB Microcontroller

DISTINCTIVE CHARACTERISTICS

- **E86™ family of x86 embedded processors offers improved time-to-market**
  - Software migration (backwards- and upwards-compatible)
  - World-class development tools, applications, and system software
- **Serial Communications Peripherals**
  - Universal Serial Bus (USB) peripheral controller
  - High-Speed UART with autobaud
  - UART
  - Synchronous serial interface (SSI)
  - SmartDMA™ channels (4) to support USB
- **System Peripherals**
  - Three programmable 16-bit timers
  - Hardware watchdog timer
  - General-purpose DMA (4 channels)
  - Programmable I/O (48 PIO signals)
  - Interrupt Controller (36 maskable interrupts)
- **Memory and Peripheral Interface**
  - Integrated DRAM controller
  - Glueless interface to RAM/ROM/Flash memory (55-ns Flash memory required for zero-wait-state operation at 50 MHz)
  - Fourteen chip selects (8 peripherals, 6 memory)
  - External bus mastering support
  - Multiplexed and nonmultiplexed address/data bus
  - Programmable bus sizing
  - 8-bit boot option
- **Available in the following package:**
  - 160-pin plastic quad flat pack (PQFP)
  - 25-, 40-, and 50-MHz operating frequencies
  - Low-voltage operation, V_{CC} = 3.3 V ± 0.3 V
  - Commercial and industrial temperature rating
  - 5-V-tolerant I/O (3.3-V output levels)

GENERAL DESCRIPTION

The Am186™CU USB microcontroller is a member of AMD's Comm86™ family of communications-specific microcontrollers. The microcontroller is a derivative of the Am186CC communications controller and is pin-compatible with that device.

The Am186CU USB microcontroller is a cost-effective, high-performance microcontroller solution for communications applications. This highly integrated microcontroller enables customers to save system costs and increase performance over 8-bit microcontrollers and other 16-bit microcontrollers.

The microcontroller offers the advantages of the x86 development environment's widely available native development tools, applications, and system software. Additionally, the microcontroller uses the industry-standard 186 instruction set that is part of the AMD E86™ family, which continually offers instruction-set-compatible upgrades.

Built into the Am186CU USB microcontroller is a wide range of communications features required in many communications applications, including the Universal Serial Bus (USB) peripheral controller that designers can use to implement a variety of microcontroller-based USB peripheral devices for telephony, audio, or other high-end applications. The USB controller does not support USB host or hub functions, but the Am186CU USB microcontroller can be used to implement USB peripheral functions in a device that also contains separate USB hub circuitry.

Comprehensive development support is available from AMD and its FusionE86^{SM} partners. A customer development platform board is available. AMD and its FusionE86 partners also offer boards, schematics, drivers, protocol stacks, and routing software to enable fast time to market.

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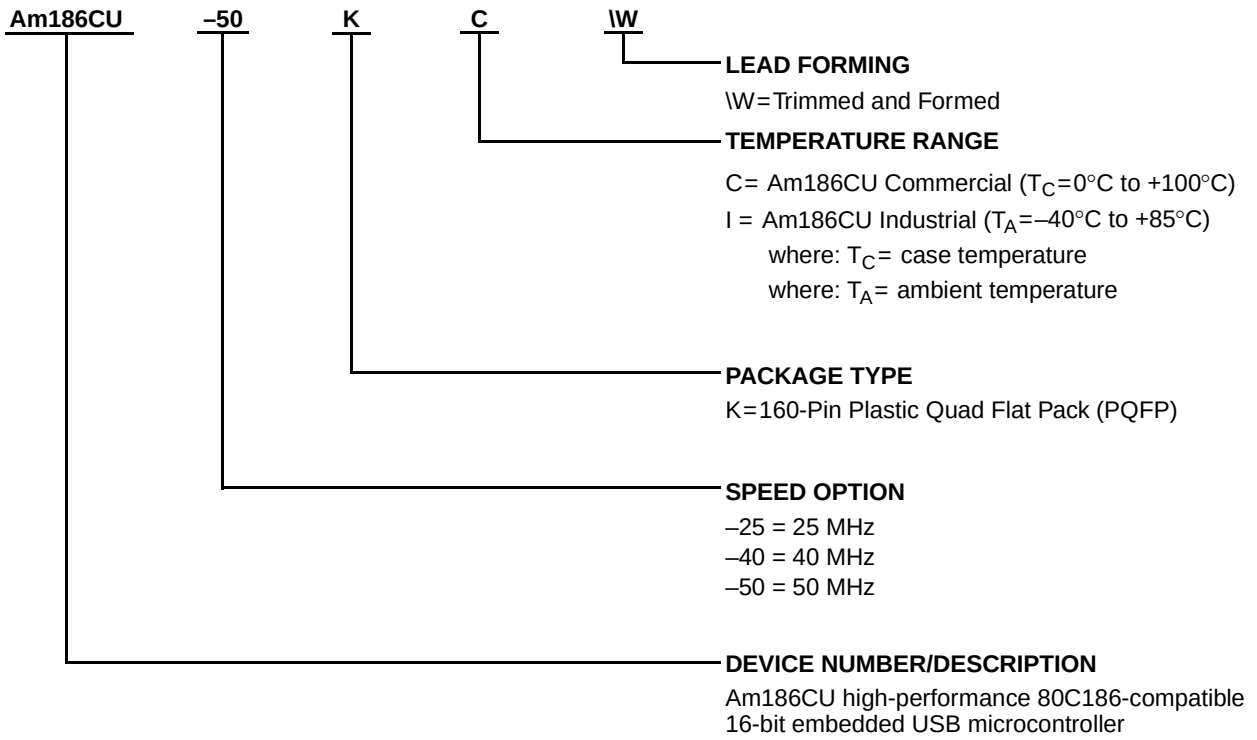
ORDERING INFORMATION



Valid Combinations	
Am186CU–25 Am186CU–40 Am186CU–50	KC\W
Am186CU–25 Am186CU–40	KI\W

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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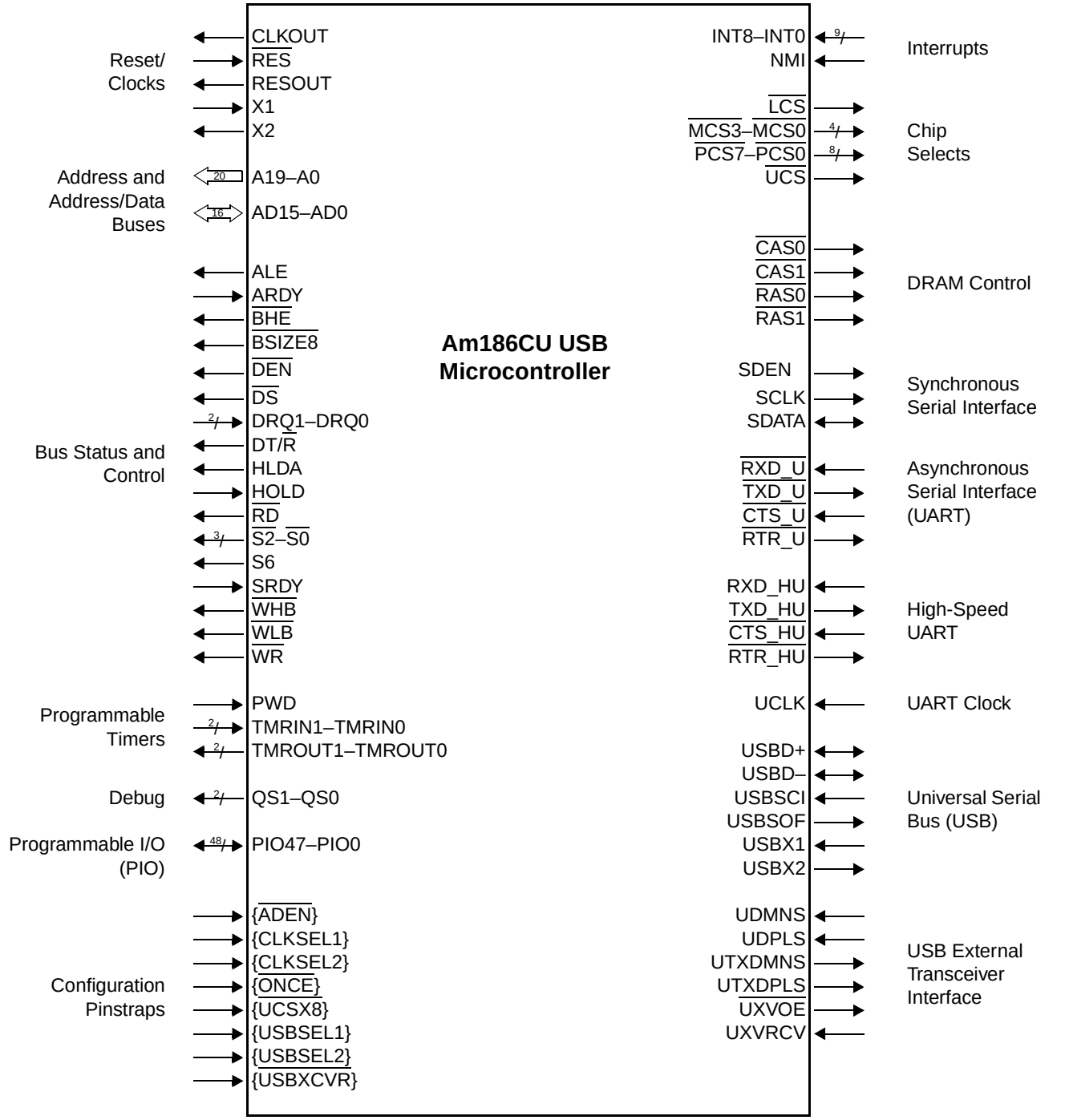
LOGIC DIAGRAM BY INTERFACE[1]



Notes:

1. Because of multiplexing, not all interfaces are available at once. Refer to Table 24, "Multiplexed Signal Trade-Offs," on page A-5.

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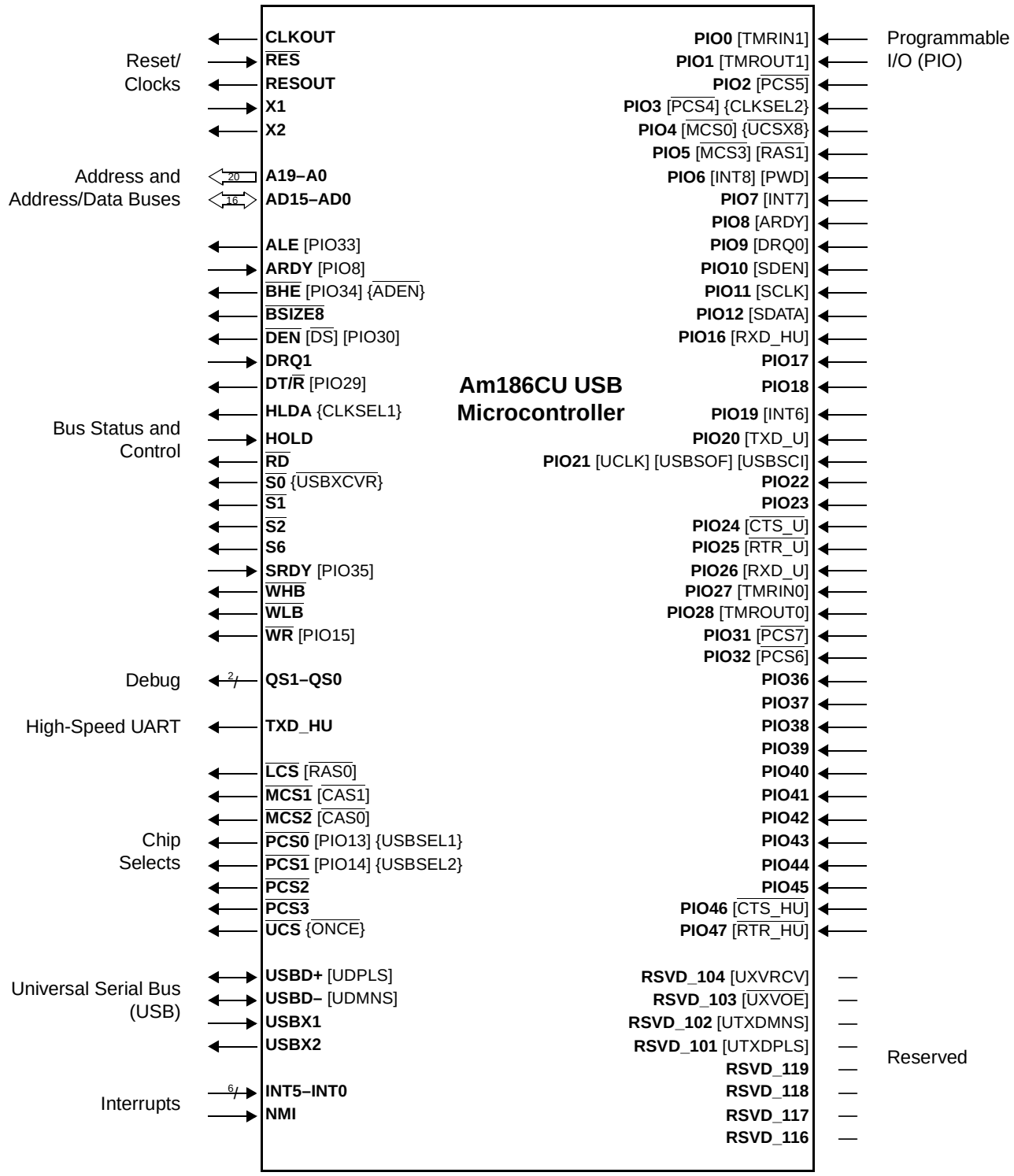
LOGIC DIAGRAM BY DEFAULT PIN FUNCTION[1]



*1. Pin names in **bold** indicate the default pin function. Brackets, [ ], indicate alternate, multiplexed functions. Braces, { }, indicate pinstrap pins.*

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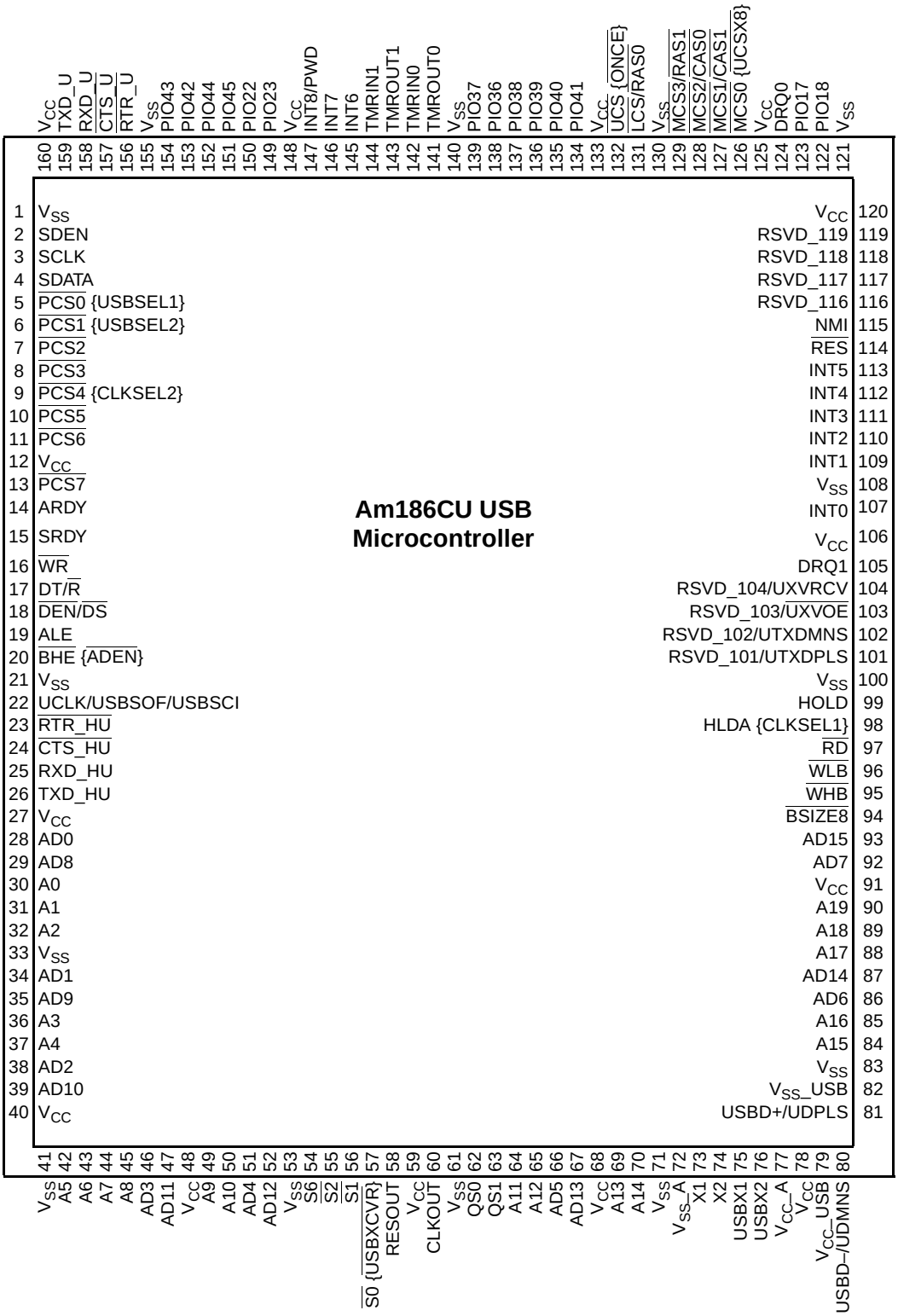
PIN CONNECTION DIAGRAM—160-PIN PQFP PACKAGE



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PIN AND SIGNAL TABLES

Table 1 on page 10 and Table 2 on page 11 show the pins sorted by pin number and signal name, respectively.

Table 4 on page 13 contains the signal descriptions (grouped alphabetically within function). The table includes columns listing the multiplexed functions and I/O type. Table 3 on page 12 defines terms used in Table 4.

Refer to Appendix A, “Pin Tables,” on page A-1 for an additional group of tables with the following information:

- Power-on reset (POR) pin defaults including pin numbers and multiplexed functions—Table 23 on page A-2.
- Multiplexed signal tradeoffs—Table 24 on page A-5.
- Programmable I/O pins ordered by PIO pin number and multiplexed signal name, respectively, including pin numbers, multiplexed functions, and pin configurations following system reset—Table 25 on page A-6 and Table 26 on page A-7.
- Pinstraps and pinstrap options—Table 27 on page A-8.
- Pin and signal summary showing signal name and alternate function, pin number, I/O type, maximum load values, POR default function, reset state, POR default operation, hold state, and voltage—Table 29 on page A-10.

In all tables the brackets, [ ], indicate alternate, multiplexed functions, and braces, { }, indicate reset configuration pins (pinstraps). The line over a pin name indicates an active Low. The word pin refers to the physical wire; the word signal refers to the electrical signal that flows through it.

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Table 1. PQFP Pin Assignments—Sorted by Pin Number[1]

Pin No.	Name—Left Side	Pin No.	Name—Bottom Side	Pin No.	Name—Right Side	Pin No.	Name—Top Side
1	V_{SS}	41	V_{SS}	81	USBD+/UDPLS	121	V_{SS}
2	SDEN/PIO10	42	A5	82	V_{SS}_USB	122	PIO18
3	SCLK/PIO11	43	A6	83	V_{SS}	123	PIO17
4	SDATA/PIO12	44	A7	84	A15	124	DRQ0/PIO9
5	$\overline{PCS0}$/PIO13 {USBSEL1}	45	A8	85	A16	125	V_{CC}
6	$\overline{PCS1}$/PIO14 {USBSEL2}	46	AD3	86	AD6	126	$\overline{MCS0}$/PIO4{$\overline{UCSX8}$}
7	$\overline{PCS2}$	47	AD11	87	AD14	127	$\overline{MCS1}$/$\overline{CAS1}$
8	$\overline{PCS3}$	48	V_{CC}	88	A17	128	$\overline{MCS2}$/$\overline{CAS0}$
9	$\overline{PCS4}$/PIO3{CLKSEL2}	49	A9	89	A18	129	$\overline{MCS3}$/$\overline{RAS1}$/PIO5
10	$\overline{PCS5}$/PIO2	50	A10	90	A19	130	V_{SS}
11	$\overline{PCS6}$/PIO32	51	AD4	91	V_{CC}	131	$\overline{LCS}$/$\overline{RAS0}$
12	V_{CC}	52	AD12	92	AD7	132	$\overline{UCS}${$\overline{ONCE}$}
13	$\overline{PCS7}$/PIO31	53	V_{SS}	93	AD15	133	V_{CC}
14	ARDY/PIO8	54	S6	94	$\overline{BSIZE8}$	134	PIO41
15	SRDY/PIO35	55	$\overline{S2}$	95	$\overline{WHB}$	135	PIO40
16	$\overline{WR}$/PIO15	56	$\overline{S1}$	96	$\overline{WLB}$	136	PIO39
17	DT/$\overline{R}$/PIO29	57	$\overline{S0}${$\overline{USBXCVR}$}	97	$\overline{RD}$	137	PIO38
18	$\overline{DEN}$/$\overline{DS}$/PIO30	58	RESOUT	98	HLDA {CLKSEL1}	138	PIO36
19	ALE/PIO33	59	V_{CC}	99	HOLD	139	PIO37
20	$\overline{BHE}$/PIO34{$\overline{ADEN}$}	60	CLKOUT	100	V_{SS}	140	V_{SS}
21	V_{SS}	61	V_{SS}	101	RSVD_101/UTXDPLS	141	TMROUT0/PIO28
22	UCLK/PIO21/USBSOF/ USBSCI	62	QS0	102	RSVD_102/UTXDMNS	142	TMRIN0/PIO27
23	$\overline{RTR\_HU}$/PIO47	63	QS1	103	RSVD_103/$\overline{UXVOE}$	143	TMROUT1/PIO1
24	$\overline{CTS\_HU}$/PIO46	64	A11	104	RSVD_104/UXVRCV	144	TMRIN1/PIO0
25	RXD_HU/PIO16	65	A12	105	DRQ1	145	INT6/PIO19
26	TXD_HU	66	AD5	106	V_{CC}	146	INT7/PIO7
27	V_{CC}	67	AD13	107	INT0	147	INT8/PWD/PIO6
28	AD0	68	V_{CC}	108	V_{SS}	148	V_{CC}
29	AD8	69	A13	109	INT1	149	PIO23
30	A0	70	A14	110	INT2	150	PIO22
31	A1	71	V_{SS}	111	INT3	151	PIO45
32	A2	72	V_{SS}_A	112	INT4	152	PIO44
33	V_{SS}	73	X1	113	INT5	153	PIO42
34	AD1	74	X2	114	$\overline{RES}$	154	PIO43
35	AD9	75	USBX1	115	NMI	155	V_{SS}
36	A3	76	USBX2	116	RSVD_116	156	$\overline{RTR\_U}$/PIO25
37	A4	77	V_{CC}_A	117	RSVD_117	157	$\overline{CTS\_U}$/PIO24
38	AD2	78	V_{CC}	118	RSVD_118	158	RXD_U/PIO26
39	AD10	79	V_{CC}_USB	119	RSVD_119	159	TXD_U/PIO20
40	V_{CC}	80	USBD–/UDMNS	120	V_{CC}	160	V_{CC}

Notes:

1. See Table 25, "PIOs Sorted by PIO Number," on page A-6 for PIOs sorted by PIO number.

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Table 2. PQFP Pin Assignments—Sorted by Signal Name[1]

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	30	CLKOUT	60	PIO40	135	USBD–/UDMNS	80
A1	31	$\overline{\text{CTS\_HU}}$/PIO46	24	PIO41	134	USBX1	75
A2	32	$\overline{\text{CTS\_U}}$/PIO24	157	PIO42	153	USBX2	76
A3	36	$\overline{\text{DEN}}$/$\overline{\text{DS}}$/PIO30	18	PIO43	154	V_{CC}	12
A4	37	DRQ0/PIO9	124	PIO44	152	V_{CC}	27
A5	42	DRQ1	105	PIO45	151	V_{CC}	40
A6	43	DT/$\overline{\text{R}}$/PIO29	17	QS0	62	V_{CC}	48
A7	44	HLDA {CLKSEL1}	98	QS1	63	V_{CC}	59
A8	45	HOLD	99	$\overline{\text{RD}}$	97	V_{CC}	68
A9	49	INT0	107	$\overline{\text{RES}}$	114	V_{CC}	78
A10	50	INT1	109	RESOUT	58	V_{CC}	91
A11	64	INT2	110	RSVD_101/UTXDPLS	101	V_{CC}	106
A12	65	INT3	111	RSVD_102/UTXDMNS	102	V_{CC}	120
A13	69	INT4	112	RSVD_103/$\overline{\text{UXVOE}}$	103	V_{CC}	125
A14	70	INT5	113	RSVD_104/UXVRCV	104	V_{CC}	133
A15	84	INT6/PIO19	145	RSVD_116	116	V_{CC}	148
A16	85	INT7/PIO7	146	RSVD_117	117	V_{CC}	160
A17	88	INT8/PWD/PIO6	147	RSVD_118	118	V_{CC}_A	77
A18	89	$\overline{\text{LCS}}$/$\overline{\text{RAS0}}$	131	RSVD_119	119	V_{CC}_USB	79
A19	90	$\overline{\text{MCS0}}$/PIO4{$\overline{\text{UCSX8}}$}	126	$\overline{\text{RTR\_HU}}$/PIO47	23	V_{SS}	1
AD0	28	$\overline{\text{MCS1}}$/$\overline{\text{CAS1}}$	127	$\overline{\text{RTR\_U}}$/PIO25	156	V_{SS}	21
AD1	34	$\overline{\text{MCS2}}$/$\overline{\text{CAS0}}$	128	RXD_HU/PIO16	25	V_{SS}	33
AD2	38	$\overline{\text{MCS3}}$/$\overline{\text{RAS1}}$/PIO5	129	RXD_U/PIO26	158	V_{SS}	41
AD3	46	NMI	115	$\overline{\text{S0}}$ {$\overline{\text{USBXCVR}}$}	57	V_{SS}	53
AD4	51	$\overline{\text{PCS0}}$/PIO13{USBSEL1}	5	$\overline{\text{S1}}$	56	V_{SS}	61
AD5	66	$\overline{\text{PCS1}}$/PIO14{USBSEL2}	6	$\overline{\text{S2}}$	55	V_{SS}	71
AD6	86	$\overline{\text{PCS2}}$	7	S6	54	V_{SS}	83
AD7	92	$\overline{\text{PCS3}}$	8	SCLK/PIO11	3	V_{SS}	100
AD8	29	$\overline{\text{PCS4}}$/PIO3{CLKSEL2}	9	SDATA/PIO12	4	V_{SS}	108
AD9	35	$\overline{\text{PCS5}}$/PIO2	10	SDEN/PIO10	2	V_{SS}	121
AD10	39	$\overline{\text{PCS6}}$/PIO32	11	SRDY/PIO35	15	V_{SS}	130
AD11	47	$\overline{\text{PCS7}}$/PIO31	13	TMRIN0/PIO27	142	V_{SS}	140
AD12	52	PIO17	123	TMRIN1/PIO0	144	V_{SS}	155
AD13	67	PIO18	122	TMROUT0/PIO28	141	V_{SS}_A	72
AD14	87	PIO22	150	TMROUT1/PIO1	143	V_{SS}_USB	82
AD15	93	PIO23	149	TXD_HU	26	$\overline{\text{WHB}}$	95
ALE/PIO33	19	PIO36	138	TXD_U/PIO20	159	$\overline{\text{WLB}}$	96
ARDY/PIO8	14	PIO37	139	UCLK/USBSOF/ USBSCI/PIO21	22	$\overline{\text{WR}}$/PIO15	16
$\overline{\text{BHE}}$/PIO34{$\overline{\text{ADEN}}$}	20	PIO38	137	$\overline{\text{UCS}}$ {$\overline{\text{ONCE}}$}	132	X1	73
$\overline{\text{BSIZE8}}$	94	PIO39	136	USBD+/UDPLS	81	X2	74

Notes:

1. See Table 26, "PIOs Sorted by Signal Name," on page A-7 for PIOs sorted by signal name.

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Signal Descriptions

Table 4 on page 13 contains a description of the Am186CU USB microcontroller signals. Table 3 describes the terms used in Table 4. The signals are organized alphabetically within the following functional groups:

- Bus interface/general-purpose DMA request (page 13)
- Clocks/reset/watchdog timer (page 17)
- Reserved (page 18)
- Power and ground (page 18)
- Debug support (page 18)
- Chip selects (page 19)
- DRAM (page 20)
- Interrupts (page 20)
- Programmable I/O (PIOs) (page 21)
- Programmable timers (page 21)
- Asynchronous serial ports (UART and High-Speed UART) (page 22)
- Synchronous serial interface (SSI) (page 23)
- Universal Serial Bus (USB) (page 23)

For pinstraps refer to Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8.

Table 3. Signal Descriptions Table Definitions

Term	Definition
General terms	
[ ]	Indicates the pin alternate function; a pin defaults to the signal named without the brackets.
{ }	Indicates the reset configuration pin (pinstrap).
pin	Refers to the physical wire.
reset	An *external or power-on reset* is caused by asserting $\overline{\text{RES}}$. An *internal reset* is initiated by the watchdog timer. A *system reset* is one that resets the Am186CU USB microcontroller (the CPU plus the internal peripherals) as well as any external peripherals connected to RESOUT. An external reset always causes a system reset; an internal reset can optionally cause a system reset.
signal	Refers to the electrical signal that flows across a pin.
$\overline{\text{SIGNAL}}$	A line over a signal name indicates that the signal is active Low; a signal name without a line is active High.
Signal types	
B	Bidirectional
H	High
LS	Programmable to hold last state of pin
O	Totem pole output
OD	Open drain output
OD-O	Open drain output or totem pole output
PD	Internal pulldown resistor
PU	Internal pullup resistor
STI	Schmitt trigger input
STI-OD	Schmitt trigger input or open drain output
TS	Three-state output

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Table 4. Signal Descriptions

Signal Name	Multiplexed Signal(s)	Type	Description
BUS INTERFACE/GENERAL-PURPOSE DMA REQUEST			
A19–A0	—	O	**Address Bus** supplies nonmultiplexed memory or I/O addresses to the system one half of a CLKOUT period earlier than the multiplexed address and data bus (AD15–AD0). During bus-hold or reset conditions, the address bus is three-stated with pulldowns. When the lower or upper chip-select regions are configured for DRAM mode, the A19–A0 bus provides the row and column addresses at the appropriate times. The upper and lower memory chip-select ranges can be individually configured for DRAM mode.
AD15–AD0	—	B	**Address and Data Bus** time-multiplexed pins supply memory or I/O addresses and data to the system. This bus can supply an address to the system during the first period of a bus cycle (t_1). It transmits (write cycle) or receives (read cycle) data to or from the system during the remaining periods of that cycle (t_2, t_3, and t_4). The address phase of these pins can be disabled—see the {ADEN} pin description in Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8. During a reset condition, the address and data bus is three-stated with pulldowns, and during a bus hold it is three-stated. In addition, during a reset the state of the address and data bus pins (AD15–AD0) is latched into the Reset Configuration (RESCON) register. This feature can be used to provide software with information about the external system at reset time.
ALE	[PIO33]	O	**Address Latch Enable** indicates to the system that an address appears on the address and data bus (AD15–AD0). The address is guaranteed valid on the falling edge of ALE. ALE is three-stated and has a pulldown resistor during bus-hold or reset conditions.
ARDY	[PIO8]	STI	**Asynchronous Ready** is a true asynchronous ready that indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The ARDY pin is asynchronous to CLKOUT and is active High. To guarantee the number of wait states inserted, ARDY or SRDY must be synchronized to CLKOUT. If the falling edge of ARDY is not synchronized to CLKOUT as specified, an additional clock period can be added. To always assert the ready condition to the microcontroller, tie ARDY and SRDY High. If the system does not use ARDY, tie the pin Low to yield control to SRDY.

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Table 4. Signal Descriptions (Continued)

<table>
<tr><th>Signal Name</th><th>Multiplexed Signal(s)</th><th>Type</th><th>Description</th></tr>
<tr><td>$\overline{\text{BHE}}$</td><td>[PIO34]
{ADEN}</td><td>O</td><td>Bus High Enable: During a memory access, $\overline{\text{BHE}}$ and the least-significant address bit (AD0) indicate to the system which bytes of the data bus (upper, lower, or both) participate in a bus cycle. The $\overline{\text{BHE}}$ and AD0 pins are encoded as follows:
Data Byte Encoding
<table>
<tr><th>$\overline{\text{BHE}}$</th><th>AD0</th><th>Type of Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>1</td><td>High byte transfer (bits 15–8)</td></tr>
<tr><td>1</td><td>0</td><td>Low byte transfer (bits 7–0)</td></tr>
<tr><td>1</td><td>1</td><td>Refresh</td></tr>
</table>
$\overline{\text{BHE}}$ is asserted during t_1 and remains asserted through t_3 and t_W. $\overline{\text{BHE}}$ does not require latching. $\overline{\text{BHE}}$ is three-stated with a pullup during bus-hold and reset conditions.

$\overline{\text{WLB}}$ and $\overline{\text{WHB}}$ implement the functionality of $\overline{\text{BHE}}$ and AD0 for high and low byte write enables, and they have timing appropriate for use with the nonmultiplexed bus interface.

$\overline{\text{BHE}}$ also signals DRAM refresh cycles when using the multiplexed address and data (AD) bus. A refresh cycle is indicated when both $\overline{\text{BHE}}$ and AD0 are High. During refresh cycles, the AD bus is driven during the t_1 phase and three-stated during the t_2, t_3, and t_4 phases. The value driven on the A bus is undefined during a refresh cycle. For this reason, the A0 signal cannot be used in place of the AD0 signal to determine refresh cycles.</td></tr>
<tr><td>$\overline{\text{BSIZE8}}$</td><td>—</td><td>O</td><td>Bus Size 8 is asserted during t_1–t_4 to indicate an 8-bit cycle, or is deasserted to indicate a 16-bit cycle.</td></tr>
<tr><td>$\overline{\text{DEN}}$</td><td>[$\overline{\text{DS}}$]
[PIO30]</td><td>O</td><td>Data Enable supplies an output enable to an external data-bus transceiver. $\overline{\text{DEN}}$ is asserted during memory and I/O cycles. $\overline{\text{DEN}}$ is deasserted when DT/$\overline{\text{R}}$ changes state. $\overline{\text{DEN}}$ is three-stated with a pullup during bus-hold or reset conditions.</td></tr>
<tr><td>[DRQ0]

DRQ1</td><td>PIO9

—</td><td>STI

STI</td><td>DMA Requests 0 and 1 indicate to the microcontroller that an external device is ready for a DMA channel to perform a transfer. DRQ1–[DRQ0] are level-triggered and internally synchronized. DRQ1–[DRQ0] are not latched and must remain active until serviced.</td></tr>
<tr><td>[$\overline{\text{DS}}$]</td><td>$\overline{\text{DEN}}$
[PIO30]</td><td>O</td><td>Data Strobe provides a signal where the write cycle timing is identical to the read cycle timing. When used with other control signals, [$\overline{\text{DS}}$] provides an interface for 68K-type peripherals without the need for additional system interface logic.

When [$\overline{\text{DS}}$] is asserted, addresses are valid. When [$\overline{\text{DS}}$] is asserted on writes, data is valid. When [$\overline{\text{DS}}$] is asserted on reads, data can be driven on the AD bus.

Following a reset, this pin is configured as $\overline{\text{DEN}}$. The pin is then configured by software to operate as [$\overline{\text{DS}}$].</td></tr>
<tr><td>DT/$\overline{\text{R}}$</td><td>[PIO29]</td><td>O</td><td>Data Transmit or Receive indicates which direction data should flow through an external data-bus transceiver. When DT/$\overline{\text{R}}$ is asserted High, the microcontroller transmits data. When this pin is deasserted Low, the microcontroller receives data. DT/$\overline{\text{R}}$ is three-stated with a pullup during a bus-hold or reset condition.</td></tr>
</table>

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
HLDA	{CLKSEL1}	O	**Bus-Hold Acknowledge** is asserted to indicate to an external bus master that the microcontroller has relinquished control of the local bus. When an external bus master requests control of the local bus (by asserting HOLD), the microcontroller completes the bus cycle in progress, then relinquishes control of the bus to the external bus master by asserting HLDA and three-stating $\overline{S2}$–$\overline{S0}$, AD15–AD0, S6, and A19–A0. The following are also three-stated and have pullups: $\overline{UCS}$, $\overline{LCS}$, $\overline{MCS3}$–$\overline{MCS0}$, $\overline{PCS7}$–$\overline{PCS0}$, $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{BHE}$, $\overline{WHB}$, $\overline{WLB}$, and DT/$\overline{R}$. ALE is three-stated and has a pulldown. When the external bus master has finished using the local bus, it indicates this to the microcontroller by deasserting HOLD. The microcontroller responds by deasserting HLDA. If the microcontroller requires access to the bus (for example, for refresh), the microcontroller deasserts HLDA before the external bus master deasserts HOLD. The external bus master must be able to deassert HOLD and allow the microcontroller access to the bus. See the timing diagrams for bus hold on page 60.
HOLD	—	STI	**Bus-Hold Request** indicates to the microcontroller that an external bus master needs control of the local bus. The microcontroller HOLD latency time—the time between HOLD request and HOLD acknowledge—is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is second only to DRAM refresh requests in priority of activity requests received by the processor. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency can be as great as four bus cycles. This occurs if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clock cycles or more if wait states are required. In addition, if locked transfers are performed, the HOLD latency time is increased by the length of the locked transfer. HOLD latency is also potentially increased by DRAM refreshes. The board designer is responsible for properly terminating the HOLD input. For more information, see the HLDA pin description above.
$\overline{RD}$	—	O	**Read Strobe** indicates to the system that the microcontroller is performing a memory or I/O read cycle. $\overline{RD}$ is guaranteed not to be asserted before the address and data bus is three-stated during the address-to-data transition. $\overline{RD}$ is three-stated with a pullup during bus-hold or reset conditions.

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Table 4. Signal Descriptions (Continued)

<table>
<tr><th>Signal Name</th><th>Multiplexed Signal(s)</th><th>Type</th><th>Description</th></tr>
<tr><td>$\overline{S0}$

$\overline{S1}$

$\overline{S2}$</td><td>{$\overline{USBXCVR}$}

—

—</td><td>O</td><td>Bus Cycle Status 2–0 indicate to the system the type of bus cycle in progress. $\overline{S2}$ can be used as a logical memory or I/O indicator, and $\overline{S1}$ can be used as a data transmit or receive indicator. $\overline{S2}$–$\overline{S0}$ are three-stated during bus hold and three-stated with a pullup during reset. The $\overline{S2}$–$\overline{S0}$ pins are encoded as follows:

Bus Status Pins
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Bus Cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read data from I/O</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write data to I/O</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Instruction fetch</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read data from memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write data to memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None (passive)</td></tr>
</table></td></tr>
<tr><td>S6</td><td>—</td><td>O</td><td>Bus Cycle Status Bit 6: This signal is asserted during t_1–t_4 to indicate a DMA-initiated bus cycle or a refresh cycle. S6 is three-stated during bus hold and three-stated with a pulldown during reset.</td></tr>
<tr><td>SRDY</td><td>[PIO35]</td><td>STI</td><td>Synchronous Ready indicates to the microcontroller that the addressed memory space or I/O device will complete a data transfer. The SRDY pin accepts an active High input synchronized to CLKOUT.

Using SRDY instead of ARDY allows a relaxed system timing because of the elimination of the one-half clock period required to internally synchronize ARDY. To always assert the ready condition to the microcontroller, tie SRDY High. If the system does not use SRDY, tie the pin Low to yield control to ARDY.</td></tr>
<tr><td>$\overline{WHB}$

$\overline{WLB}$</td><td>—

—</td><td>O

O</td><td>Write High Byte and Write Low Byte indicate to the system which bytes of the data bus (upper, lower, or both) participate in a write cycle. In 80C186 microcontroller designs, this information is provided by $\overline{BHE}$, AD0, and $\overline{WR}$. However, by using $\overline{WHB}$ and $\overline{WLB}$, the standard system interface logic and external address latch that were required are eliminated.

$\overline{WHB}$ is asserted with AD15–AD8. $\overline{WHB}$ is the logical AND of $\overline{BHE}$ and $\overline{WR}$. This pin is three-stated with a pullup during bus-hold or reset conditions.

$\overline{WLB}$ is asserted with AD7–AD0. $\overline{WLB}$ is the logical AND of AD0 and $\overline{WR}$. This pin is three-stated with a pullup during bus-hold or reset conditions.</td></tr>
<tr><td>$\overline{WR}$</td><td>[PIO15]</td><td>O</td><td>Write Strobe indicates to the system that the data on the bus is to be written to a memory or I/O device. $\overline{WR}$ is three-stated with a pullup during bus-hold or reset conditions.</td></tr>
</table>

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
CLOCKS/RESET/WATCHDOG TIMER			
CLKOUT	—	O	**Clock Output** supplies the clock to the system. Depending on the values of the CPU mode select pinstraps, {CLKSEL1} and {CLKSEL2}, CLKOUT operates at either the PLL frequency or the source input frequency during PLL Bypass mode. (See Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8.) CLKOUT remains active during bus-hold or reset conditions. The DISCLK bit in the SYSCON register can be set to disable the CLKOUT signal. Refer to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, order #21916. All synchronous AC timing specifications not associated with SSI, UARTs, and the USB are synchronous to CLKOUT.
$\overline{\text{RES}}$	—	STI	**Reset** requires the microcontroller to perform a reset. When $\overline{\text{RES}}$ is asserted, the microcontroller immediately terminates its present activity, clears its internal logic, and on the deassertion of $\overline{\text{RES}}$, transfers CPU control to the reset address FFFF0h. $\overline{\text{RES}}$ must be asserted for at least 1 ms to allow the internal circuits to stabilize. $\overline{\text{RES}}$ can be asserted asynchronously to CLKOUT because $\overline{\text{RES}}$ is synchronized internally. For proper initialization, V_{CC} must be within specifications, and CLKOUT must be stable for more than four CLKOUT periods during which $\overline{\text{RES}}$ is asserted. If $\overline{\text{RES}}$ is asserted while the watchdog timer is performing a watchdog-timer reset, the external reset takes precedence over the watchdog-timer reset. This means that the RESOUT signal asserts as with any external reset and the WDTCON register will not have the RSTFLAG bit set. In addition, the microcontroller will exit reset based on the external reset timing (i.e., 4.5 clocks after the deassertion of $\overline{\text{RES}}$ rather than 2^{16} clocks after the watchdog timer timeout occurred). The microcontroller begins fetching instructions approximately 6.5 CLKOUT periods after $\overline{\text{RES}}$ is deasserted. This input is provided with a Schmitt trigger to facilitate power-on $\overline{\text{RES}}$ generation via a resistor-capacitor (RC) network.
RESOUT	—	O	**Reset Out** indicates that the microcontroller is being reset (either externally or internally), and the signal can be used as a system reset to reset any external peripherals connected to RESOUT. During an external reset, RESOUT remains active (High) for two clocks after $\overline{\text{RES}}$ is deasserted. The microcontroller exits reset and begins the first valid bus cycle approximately 4.5 clocks after $\overline{\text{RES}}$ is deasserted.
[UCLK]	[USBSOF] [USBSCI] PIO21	STI	**UART Clock** can be used instead of the processor clock as the source clock for either the UART or the High-Speed UART. The source clock for the UART and the High-Speed UART are selected independently and both can use the same source.
USBX1 USBX2	— —	STI O	**USB Controller Crystal Input** (USBX1) and **USB Controller Crystal Output** (USBX2) provide connections for a fundamental mode, parallel-resonant crystal used by the internal USB oscillator circuit. If the CPU crystal is used to generate the USB clock, USBX1 must be pulled down.
X1 X2	— —	STI O	**CPU Crystal Input** (X1) and **CPU Crystal Output** (X2) provide connections for a fundamental mode, parallel-resonant crystal used by the internal oscillator circuit. If an external oscillator is used, inject the signal directly into X1 and leave X2 floating.

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
PINSTRAPS (See Table 27, "Reset Configuration Pins (Pinstraps)," on page A-8.)			
RESERVED			
RSVD_101	UTXDPLS	—	The pins RSVD_104–RSVD_101 are reserved unless pinstrap {$\overline{\text{USBXCVR}}$} is sampled Low on the rising edge of RESET. The pins RSVD_119–RSVD_116 are reserved. All reserved pins should not be connected.
RSVD_102	UTXDMNS	—	
RSVD_103	$\overline{\text{UXVOE}}$	—	
RSVD_104	UXVRCV	—	
RSVD_116	—	—	
RSVD_117	—	—	
RSVD_118	—	—	
RSVD_119	—	—	
POWER AND GROUND			
V_{CC} (15)	—	STI	**Digital Power Supply** pins supply power (+3.3 ± 0.3 V) to the Am186CU USB microcontroller logic.
V_{CC}_A (1)	—	STI	**Analog Power Supply** pin supplies power (+3.3 ± 0.3 V) to the oscillators and PLLs.
V_{CC}_USB (1)	—	STI	**USB Power Supply** pin supplies power (+3.3 ± 0.3 V) to the USB block.
V_{SS} (15)	—	STI	**Digital Ground** pins connect the Am186CU USB microcontroller logic to the system ground.
V_{SS}_A (1)	—	STI	**Analog Ground** pin connects the oscillators and PLLs to the system ground.
V_{SS}_USB (1)	—	STI	**USB Ground** pin connects the USB block to the system ground.
DEBUG SUPPORT			
QS0	—	O	**Queue Status 1–0** values provide information to the system concerning the interaction of the CPU and the instruction queue. The pins have the following meanings:
QS1	—	O	

Queue Status Pins

QS1	QS0	Queue Operation
0	0	None
0	1	First opcode byte fetched from queue
1	0	Queue was initialized
1	1	Subsequent byte fetched from queue

The following signals are also used by emulators: A19–A0, AD15–AD0, {$\overline{\text{ADEN}}$}, ALE, ARDY, $\overline{\text{BHE}}$, $\overline{\text{BSIZE8}}$, $\overline{\text{CAS1}}$–$\overline{\text{CAS0}}$, CLKOUT, {CLKSEL2–CLKSEL1}, HLDA, HOLD, $\overline{\text{LCS}}$, $\overline{\text{MCS3}}$–$\overline{\text{MCS0}}$, NMI, {$\overline{\text{ONCE}}$}, QS1–QS0, $\overline{\text{RAS1}}$–$\overline{\text{RAS0}}$, $\overline{\text{RD}}$, $\overline{\text{RES}}$, RESOUT, $\overline{\text{S2}}$–$\overline{\text{S0}}$, S6, SRDY, $\overline{\text{UCS}}$, {$\overline{\text{UCSX8}}$}, $\overline{\text{WHB}}$, $\overline{\text{WLB}}$, $\overline{\text{WR}}$. See the *Am186CC/CH/CU Microcontrollers User's Manual*, order #21914, for more information.

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
CHIP SELECTS			
LCS	[RAS0]	O	**Lower Memory Chip Select** indicates to the system that a memory access is in progress to the lower memory block. The base address and size of the lower memory block are programmable up to 512 Kbyte. LCS can be configured for 8-bit or 16-bit bus size. LCS is three-stated with a pullup resistor during bus-hold or reset conditions.
[MCS0] MCS1 MCS2 [MCS3]	{UCSX8} PIO4 [CAS1] [CAS0] [RAS1] PIO5	O	**Midrange Memory Chip Selects 3–0** indicate to the system that a memory access is in progress to the corresponding region of the midrange memory block. The base address and size of the midrange memory block are programmable. The midrange chip selects can be configured for 8-bit or 16-bit bus size. The midrange chip selects are three-stated with pullup resistors during bus-hold or reset conditions. [MCS0] can be programmed as the chip select for the entire middle chip select address range. Unlike the UCS and LCS chip selects that operate relative to the earlier timing of the nonmultiplexed A address bus, the MCS outputs assert with the multiplexed AD address and data bus timing.
PCS0 PCS1 PCS2 PCS3 [PCS4] [PCS5] [PCS6] [PCS7]	[PIO13] {USBSEL1} [PIO14] {USBSEL2} — — PIO3 {CLKSEL2} PIO2 PIO32 PIO31	O	**Peripheral Chip Selects 7–0** indicate to the system that an access is in progress to the corresponding region of the peripheral address block (either I/O or memory address space). The base address of the peripheral address block is programmable. PCS7–PCS0 are three-stated with pullup resistors during bus-hold or reset conditions. Unlike the UCS and LCS chip selects that operate relative to the earlier timing of the nonmultiplexed A address bus, the PCS outputs assert with the multiplexed AD address and data bus timing.
UCS	{ONCE}	O	**Upper Memory Chip Select** indicates to the system that a memory access is in progress to the upper memory block. The base address and size of the upper memory block are programmable up to 512 Kbytes. UCS is three-stated with a weak pullup during bus-hold or reset conditions. The UCS can be configured for an 8-bit or 16-bit bus size out of reset. For additional information, see the {UCSX8} pin description in Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8. After reset, UCS is active for the 64-Kbyte memory range from F0000h to FFFFFh, including the reset address of FFFF0h.

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
DRAM			
[CAS0] [CAS1]	MCS2 MCS1	O	**Column Address Strobes 1–0**: When either the upper or lower chip select regions are configured for DRAM, these pins provide the column address strobe signals to the DRAM. The CAS signals can be used to perform byte writes in a manner similar to WLB and WHB, respectively (i.e., [CAS0] corresponds to the low byte (WLB) and [CAS1] corresponds to the high byte (WHB)).
[RAS0]	LCS	O	**Row Address Strobe 0**: When the lower chip select region is configured to DRAM, this pin provides the row address strobe signal to the lower DRAM bank.
[RAS1]	[MCS3] PIO5	O	**Row Address Strobe 1**: When the upper chip select region is configured to DRAM, this pin provides the row address strobe signal to the upper DRAM bank.
INTERRUPTS			
NMI	—	STI	**Nonmaskable Interrupt** indicates to the microcontroller that an interrupt request has occurred. The NMI signal is the highest priority hardware interrupt and cannot be masked. The microcontroller always transfers program execution to the location specified by the nonmaskable interrupt vector in the microcontroller's interrupt vector table when NMI is asserted. Although NMI is the highest priority hardware interrupt source, it does not participate in the priority resolution process of the maskable interrupts. There is no bit associated with NMI in the interrupt in-service or interrupt request registers. This means that a new NMI request can interrupt an executing NMI interrupt service routine. As with all hardware interrupts, the interrupt flag (IF) is cleared when the processor takes the interrupt, disabling the maskable interrupt sources. However, if maskable interrupts are re-enabled by software in the NMI interrupt service routine (for example, via the STI instruction), the fact that an NMI is currently in service does not have any effect on the priority resolution of maskable interrupt requests. For this reason, it is strongly advised that the interrupt service routine for NMI should not enable the maskable interrupts. An NMI transition from Low to High is latched and synchronized internally, and it initiates the interrupt at the next instruction boundary. To guarantee that the interrupt is recognized, the NMI pin must be asserted for at least one CLKOUT period. The board designer is responsible for properly terminating the NMI input.
INT5–INT0 [INT6] [INT7] [INT8]	— PIO19 PIO7 [PWD] PIO6	STI STI STI STI	**Maskable Interrupt Requests 8–0** indicate to the microcontroller microcontroller that an external interrupt request has occurred. If the individual pin is not masked, the microcontroller transfers program execution to the location specified by the associated interrupt vector in the microcontroller's interrupt vector table. Interrupt requests are synchronized internally and can be edge-triggered or level-triggered. The interrupt polarity is programmable.To guarantee interrupt recognition for edge-triggered interrupts, the user should hold the interrupt source for a minimum of five system clocks. A second interrupt from the same source is not recognized until after an acknowledge of the first. The board designer is responsible for properly terminating the INT8–INT0 inputs.
Also configurable as interrupts are PIO5, PIO15, PIO27, PIO29, PIO30, PIO33, PIO34, and PIO35. (See the *Am186CC/CH/CU Microcontrollers User's Manual*, order #21914 for more information.)			

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
PROGRAMMABLE I/O (PIOS)			
PIO47–PIO0	(For multiplexed signals see Table 25, "PIOs Sorted by PIO Number," on page A-6 and Table 26, "PIOs Sorted by Signal Name," on page A-7.)	B	**Shared Programmable I/O** pins can be programmed with the following attributes: PIO function (enabled/disabled), direction (input/output), and weak pullup or pulldown. After a reset, the PIO pins default to various configurations. The column entitled "Pin Configuration Following System Reset" in Table 25 on page A-6 and Table 26 on page A-7 lists the defaults for the PIOs. Most of the PIO pins are configured as PIO inputs with pullup after reset. See Table 29 on page A-10 for detailed termination information for all pins. The system initialization code must reconfigure any PIO pins as required. PIO5, PIO15, PIO27, PIO29, PIO30, and PIO33–PIO35 are capable of generating an interrupt on the shared interrupt channel 14. The multiplexed signals PIO33/ALE, PIO8/ARDY, PIO34/$\overline{\text{BHE}}$, PIO30/$\overline{\text{DEN}}$, PIO29/DT/$\overline{\text{R}}$, PIO14/$\overline{\text{PCS1}}$–PIO13/$\overline{\text{PCS0}}$, PIO35/SRDY, and PIO15/$\overline{\text{WR}}$ default to non-PIO operation at reset. The following PIO signals are multiplexed with alternate signals that can be used by emulators: PIO8, PIO15, PIO33, PIO34, and PIO35. Consider any emulator requirements for the alternate signals before using these pins as PIOs.
PROGRAMMABLE TIMERS			
[PWD]	[INT8] PIO6	STI	**Pulse-Width Demodulator:** If pulse-width demodulation is enabled, [PWD] processes a signal through the Schmitt trigger input. [PWD] is used internally to drive [TMRIN0] and [INT8], and [PWD] is inverted internally to drive [TMRIN1] and an additional internal interrupt. If interrupts are enabled and Timer 0 and Timer 1 are properly configured, the pulse width of the alternating [PWD] signal can be calculated by comparing the values in Timer 0 and Timer 1. In PWD mode, the signals [TMRIN0]/PIO27 and [TMRIN1]/PIO0 can be used as PIOs. If they are not used as PIOs they are ignored internally. The additional internal interrupt used in PWD mode uses the same interrupt channel as [INT7]. If [INT7] is used, it must be assigned to the shared interrupt channel.
[TMRIN0] [TMRIN1]	PIO27 PIO0	STI STI	**Timer Inputs 1–0** supply a clock or control signal to the internal microcontroller timers. After internally synchronizing a Low-to-High transition on [TMRIN1]–[TMRIN0], the microcontroller increments the timer. [TMRIN1]–[TMRIN0] must be tied High if not being used. When PIO is enabled for one or both, the pin is pulled High internally. [TMRIN1]–[TMRIN0] are driven internally by [INT8]/[PWD] when pulse-width demodulation functionality is enabled. The [TMRIN1]–[TMRIN0] pins can be used as PIOs when pulse-width demodulation is enabled.
[TMROUT0] [TMROUT1]	PIO28 PIO1	O O	**Timer Outputs 1–0** supply the system with either a single pulse or a continuous waveform with a programmable duty cycle. [TMROUT1]–[TMROUT0] are three-stated during bus-hold or reset conditions.

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
ASYNCHRONOUS SERIAL PORTS (UART AND HIGH-SPEED UART)			
UART			
[RXD_U]	PIO26	STI	**Receive Data UART** is the asynchronous serial receive data signal that supplies data from the asynchronous serial port to the microcontroller.
[TXD_U]	PIO20	O	**Transmit Data UART** is the asynchronous serial transmit data signal that supplies data to the asynchronous serial port from the microcontroller.
[$\overline{\text{CTS\_U}}$]	PIO24	STI	**Clear-To-Send UART** provides the Clear-to-Send signal from the asynchronous serial port when hardware flow control is enabled for the port. The [$\overline{\text{CTS\_U}}$] signal gates the transmission of data from the serial port transmit shift register. When [$\overline{\text{CTS\_U}}$] is asserted, the transmitter begins transmission of a frame of data, if any is available. If [$\overline{\text{CTS\_U}}$] is deasserted, the transmitter holds the data in the serial port transmit shift register. The value of [$\overline{\text{CTS\_U}}$] is checked only at the beginning of the transmission of the frame. [$\overline{\text{CTS\_U}}$] and [$\overline{\text{RTR\_U}}$] form the hardware handshaking interface for the UART.
[$\overline{\text{RTR\_U}}$]	PIO25	O	**Ready-To-Receive UART** provides the Ready-to-Receive signal for the asynchronous serial port when hardware flow control is enabled for the port. The [$\overline{\text{RTR\_U}}$] signal is asserted when the associated serial port receive data register does not contain valid, unread data. [$\overline{\text{CTS\_U}}$] and [$\overline{\text{RTR\_U}}$] form the hardware handshaking interface for the UART.
HIGH-SPEED UART			
[RXD_HU]	PIO16	STI	**Receive Data High-Speed UART** is the asynchronous serial receive data signal that supplies data from the high-speed serial port to the microcontroller.
TXD_HU	—	O	**Transmit Data High-Speed UART** is the asynchronous serial transmit data signal that supplies data to the high-speed serial port from the microcontroller.
[$\overline{\text{CTS\_HU}}$]	PIO46	STI	**Clear-To-Send High-Speed UART** provides the Clear-to-Send signal from the high-speed asynchronous serial port when hardware flow control is enabled for the port. The [$\overline{\text{CTS\_HU}}$] signal gates the transmission of data from the serial port transmit shift register. When [$\overline{\text{CTS\_HU}}$] is asserted, the transmitter begins transmission of a frame of data, if any is available. If [$\overline{\text{CTS\_HU}}$] is deasserted, the transmitter holds the data in the serial port transmit shift register. The value of [$\overline{\text{CTS\_HU}}$] is checked only at the beginning of the transmission of the frame. [$\overline{\text{CTS\_HU}}$] and [$\overline{\text{RTR\_HU}}$] form the hardware handshaking interface for the High-Speed UART.
[$\overline{\text{RTR\_HU}}$]	PIO47	O	**Ready-To-Receive High-Speed UART** provides the Ready-to-Receive signal to the high-speed asynchronous serial port when hardware flow control is enabled for the port. The [$\overline{\text{RTR\_HU}}$] signal is asserted when the associated serial port receive data register does not contain valid, unread data. [$\overline{\text{CTS\_HU}}$] and [$\overline{\text{RTR\_HU}}$] form the hardware handshaking interface for the High-Speed UART.

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Table 4. Signal Descriptions (Continued)

Signal Name	Multiplexed Signal(s)	Type	Description
SYNCHRONOUS SERIAL INTERFACE (SSI)			
[SCLK]	PIO11	O	**Serial Clock** provides the clock for the synchronous serial interface to allow synchronous transfers between the Am186CU USB microcontroller and a slave device.
[SDATA]	PIO12	B	**Serial Data** is used to transmit and receive data between the Am186CU USB microcontroller and a slave device on the synchronous serial interface.
[SDEN]	PIO10	O	**Serial Data Enable** enables data transfers on the synchronous serial interface.
UNIVERSAL SERIAL BUS (USB)			
[UDMNS] [UDPLS]	USBD– USBD+	STI STI	**USB External Transceiver Gated Differential Plus** and **USB External Transceiver Gated Differential Minus** are inputs from the external USB transceiver used to detect single-ended zero and error conditions. The signals have the following meanings: **USB External Transceiver Signals** UDPLS / UDMNS / Status: 0 / 0 / Single-Ended Zero (SE0) 0 / 1 / Full speed 1 / 0 / Reserved 1 / 1 / Error
USBD+ USBD–	[UDPLS] [UDMNS]	B B	**USB Differential Plus** and **USB Differential Minus** form the bidirectional electrical data interface for the USB port. The pins form a differential pair that can be connected to a physical USB connector without an external transceiver.
[USBSCI]	[UCLK] [USBSOF] PIO21	STI	**USB Sample Clock Input** is used to synchronize an external clock to the internal USB peripheral controller for isochronous transfers.
[USBSOF]	[UCLK] [USBSCI] PIO21	O	**USB Start of Frame** is a 1-kHz frame pulse used to synchronize USB isochronous transfers to an external device on a frame-by-frame basis.
UTXDMNS	RSVD_102	O	**USB External Transceiver Differential Minus** is an output that drives the external transceiver differential driver minus input.
UTXDPLS	RSVD_101	O	**USB External Transceiver Differential Plus** is an output that drives the external transceiver differential driver plus input.
$\overline{\text{UXVOE}}$	RSVD_103	O	**USB External Transceiver Transmit Output Enable** is an output that enables the external transceiver. $\overline{\text{UXVOE}}$ signals the external transceiver that USB data is being output by the Am186CU USB microcontroller. When Low this pin enables the transceiver output, and when High this pin enables the receiver.
UXVRCV	RSVD_104	STI	**USB External Transceiver Differential Receiver** is a data input received from the external transceiver differential receiver.

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ARCHITECTURAL OVERVIEW

The architectural goal of the Am186CU USB microcontroller is to provide comprehensive communications features on a processor running the widely known x86 instruction set. The Am186CU USB microcontroller combines a USB peripheral controller and general communications peripherals with the Am186 microcontroller. This highly integrated microcontroller provides system cost and performance advantages for a wide range of communications applications. Figure 1 is a block diagram of the Am186CU USB microcontroller followed by sections providing an overview of the features.

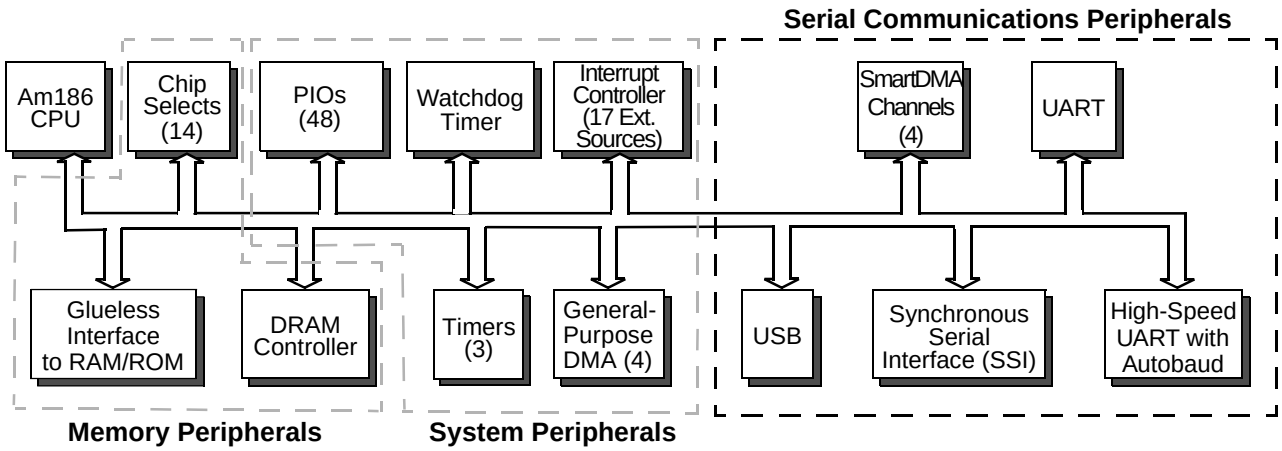

Figure 1. Am186CU USB Microcontroller Block Diagram

Detailed Description

- **Universal Serial Bus (USB) peripheral controller works with a wide variety of USB devices**
  - Implements high-speed 12-Mbit/s device function
  - Allows an unlimited number of device descriptors
  - Supports a total of six endpoints: one control endpoint; one interrupt endpoint; and four data endpoints that can be either bulk or isochronous, IN or OUT
  - Two data endpoints have 16-byte FIFOs; two data endpoints have 64-byte FIFOs
  - Fully integrated differential driver directly supports the USB interface (D+, D–)
  - Specialized hardware supports adaptive isochronous data streams
  - General-purpose DMA and SmartDMA™ channels supported
- **8 Direct Memory Access (DMA) channels**
  - Four buffer descriptor ring SmartDMA channels for the USB bulk and isochronous endpoints
  - Four general-purpose DMAs support the two integrated asynchronous serial ports and/or USB endpoints; two DMA channels have external DMA request inputs
- **High-speed asynchronous serial interface provides enhanced UART functions**
  - Capable of sustained operation at 460 Kbaud
  - 7-, 8-, or 9-bit data transfers
  - FIFOs to support high-speed operation
  - DMA support available
  - Automatic baud-rate detection that allows emulation of a Hayes AT-compatible modem
  - Independent baud generator with clock input source programmable to use CPU or external clock input pin
- **Asynchronous serial interface (UART)**
  - 7-, 8-, or 9-bit data transfers
  - DMA support available
  - Independent baud generator with clock input source programmable to use CPU or external clock input pin
- **Synchronous Serial Interface (SSI) provides half-duplex, bidirectional interface to high-speed peripherals**
  - Useful with many telecommunication interface peripherals such as codecs, line interface units, and transceivers
  - Selectable device-select polarity

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- Selectable bit shift order on transmit and receive
- Glueless connection to AMD Subscriber Line Audio Processing Circuit (SLAC™) devices

■ **Clocking options offer high flexibility**

- Separate crystal oscillator inputs for CPU and USB clock sources
- CPU can run in 1x, 2x, or 4x mode
- USB can run in 2x or 4x mode
- USB can run from system clock if running at 48 MHz, allowing entire system to run from one 12-MHz or 24-MHz crystal

Am186™ Embedded CPU

All members of the Am186 family, including the Am186CU USB microcontroller, are compatible with the original industry-standard 186 parts, and build on the same core set of 186 registers, address generation, I/O space, instruction set, segments, data types, and addressing modes.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address consisting of a 16-bit segment value and a 16-bit offset. The 16-bit segment values are contained in one of four internal segment registers (CS, DS, SS, or ES). The physical address is calculated by shifting the segment value left by 4 bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 2). This allows for a 1-Mbyte physical address size.

All instructions that address operands in memory must specify the segment value and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 5).

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions (IN/INS and OUT/OUTS) address the I/O space with either an 8-bit port address specified in the instruction, or a 16-bit port address in the DX register. Eight-bit port addresses are zero-extended such that A15–A8 are Low.

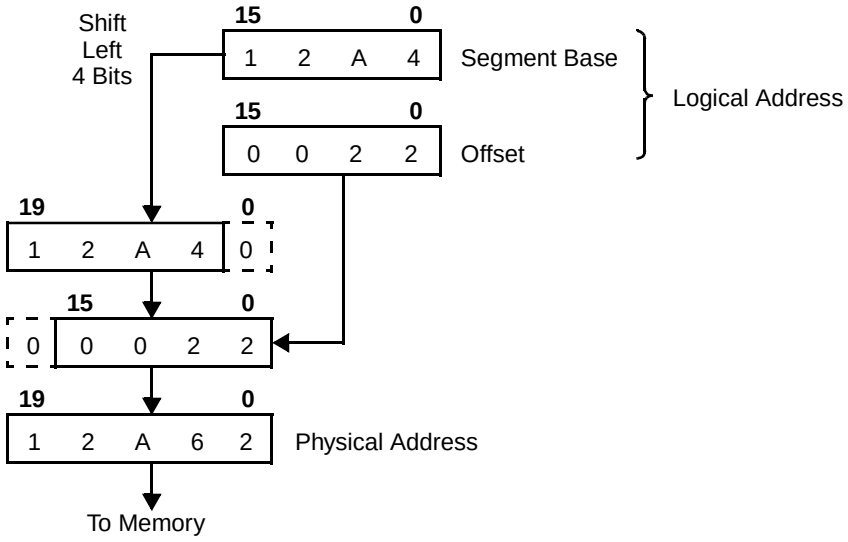

Figure 2. Two-Component Address Example

Table 5. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instructions (including immediate data)
Local Data	Data (DS)	All data references
Stack	Stack (SS)	All stack pushes and pops; any memory references that use the BP register
External Data (Global)	Extra (ES)	All string instruction references that use the DI register as an index

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Serial Communications Support

The Am186CU USB microcontroller supports four serial interfaces. This includes a USB peripheral controller, two UARTs, and a synchronous serial interface.

Universal Serial Bus

The Am186CU USB microcontroller includes a highly flexible integrated USB peripheral controller that designers can use to implement a variety of microcontroller-based USB peripheral devices for telephony, audio, or other high-end applications. This integrated USB peripheral controller can provide a significant system-cost reduction compared to other platforms that require a separate USB controller.

The Am186CU USB microcontroller can be used in self-powered USB peripherals that use the full-speed signalling rate of 12 Mbit/s. The USB low-speed rate (1.5 Mbit/s) is not supported. An integrated USB transceiver is provided to minimize system device count and cost, but an external transceiver can be used instead, if necessary.

The USB controller does not support USB host or hub functions. However, the Am186CU USB microcontroller can be used to implement USB peripheral functions in a device that also contains separate USB hub circuitry.

In addition, the Am186CU USB microcontroller supports the following:

- An unlimited number of device descriptors
- A total of 6 endpoints: 1 control endpoint, 1 interrupt endpoint, and 4 data endpoints that can be configured as control, interrupt, bulk, or isochronous. The interrupt, bulk, and isochronous endpoints can be configured for the IN or OUT direction.
- Two data endpoints have 16-byte FIFOs; two data endpoints have 64-byte FIFOs
- Fully integrated differential driver, which supports the USB interface directly
- Specialized hardware, which supports adaptive isochronous data streams
- General-purpose DMA and SmartDMA channels

Four SmartDMA Channels

The Am186CU USB microcontroller provides four SmartDMA channels, which provide a faster method for moving data between peripherals and memory with lower CPU utilization. SmartDMA transmits and receives data across multiple memory buffers and a sophisticated buffer-chaining mechanism. These channels are always used in pairs: transmitter and receiver. The transmit channels can only transfer data from memory to a peripheral; the receive channels can only transfer data from a peripheral to memory.

The four SmartDMA channels (two pairs) support USB endpoints A, B, C, or D.

In addition to the four SmartDMA channels, the Am186CU USB microcontroller provides four general-purpose DMA channels (see page 27).

Two Asynchronous Serial Ports

The Am186CU USB microcontroller has two asynchronous serial ports (a UART and a High-Speed UART) which provide full-duplex, bidirectional data transfer at speeds of up to 115.2 Kbaud or up to 460 Kbaud, respectively. The High-Speed UART has 16-byte transmit and 32-byte receive FIFOs, special-character matching, and automatic baud-rate detection, suitable for implementation of a Hayes-compatible modem interface to a host PC. There is also a lower speed UART that typically is used for a low baud-rate system configuration port or debug port. Each of these UARTs can derive its baud rate from the system clock or from a separate baud-rate generator clock input. Both UARTs support 7-, 8-, or 9-bit data transfers; address bit generation and detection in 7- or 8-bit frames; one or two stop bits; even, odd, or no parity; break generation and detection; hardware flow control; and DMA to and/or from the serial ports using the general-purpose DMA channels.

Synchronous Serial Port

The Am186CU USB microcontroller includes one SSI port that provides a half-duplex, bidirectional, communications interface between the microcontroller and other system components. This interface is typically used by the microcontroller to monitor the status of other system devices and/or to configure these devices under software control. In a communications application, these devices could be system components such as audio codecs, line interface units, and transceivers. The SSI supports data transfer speeds of up to 25 Mbit/s with a 50-MHz system clock.

The SSI port operates as an interface master, with the other attached devices acting as slave devices. Using this protocol, the Am186CU USB microcontroller sends a command byte to the attached device, and then follows that with either a read or write of a byte of data.

The SSI port consists of three I/O pins: an enable (SDEN), a clock (SCLK), and a bidirectional data pin (SDATA). SDEN can be used directly as an enable for a single attached device. When more than one device requires control via the SSI, PIOs can be used to provide enable pins for those devices.

The Am186CU SSI is, in general, software compatible with software written for the Am186EM SSI. (Additional features have been added to the Am186CU SSI

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implementation.) The Am186CU USB microcontroller features the additional capability of selecting the polarity of the SCLK and SDEN pins, as well as the shift order of bits on the SDATA pin (least-significant-bit first versus most-significant-bit first). The SSI port also offers a programmable clock divisor (dividing the clock from 2 to 256 in power of 2 increments), a bidirectional transmit/receive shift register, and direct connection to AMD SLAC devices.

System Peripherals

Interrupt Controller

The Am186CU USB microcontroller features an interrupt controller that arranges the 36 maskable interrupt requests by priority and presents them one at a time to the CPU. In addition to interrupts managed by the interrupt controller, the Am186CU USB microcontroller supports eight nonmaskable interrupts—an external or internal nonmaskable interrupt (NMI), a trace interrupt, and software interrupts and exceptions.

The interrupt controller supports the 36 maskable interrupt sources through the use of 15 channels. Because of this, most channels support multiple interrupt sources. These channels are programmable to support the external interrupt pins and/or various peripheral devices that can be configured to generate interrupts. The 36 maskable interrupt sources include 19 internal sources and 17 external sources.

Four General-Purpose DMA Channels

The Am186CU USB microcontroller provides four general-purpose DMA channels that can be used for data transfer between memory and I/O spaces (i.e., memory-to-I/O or I/O-to-memory) or within the same space (i.e., memory-to-memory or I/O-to-I/O). In addition, the Am186CU USB microcontroller supports data transfer between peripherals and memory or I/O. Internal peripherals that support general-purpose DMA are the USB peripheral controller, Timer 2, and the two asynchronous serial ports (UART and High-Speed UART). External peripherals support DMA transfers through the external DMA request pins. Each general-purpose channel can accept synchronized DMA requests from one of four sources: the DMA request pins (DRQ1–DRQ0), Timer 2, the UARTs, or the USB controller. In addition, system software can initialize and start unsynchronized DMA transfers.

In addition to the four general-purpose channels, the Am186CU USB microcontroller provides four SmartDMA channels (see page 26).

48 Programmable I/O Signals

The Am186CU USB microcontroller provides 48 user-programmable input/output signals (PIOs). Thirty-four of the 48 signals share a pin with at least one alternate function. If an application does not need the alternate function, the associated PIO can be used by programming the PIO registers.

If a pin is enabled to function as a PIO signal, the alternate function is disabled and does not affect the pin. A PIO signal can be configured to operate as an input or output, with or without internal pullup or pulldown resistors (pullup or pulldown depends on the pin configuration and is not user-configurable), or as an open-drain output. Additionally, eight PIOs can be configured as external interrupt sources.

Three Programmable Timers

There are three 16-bit programmable timers in the Am186CU USB microcontroller. Timers 0 and 1 are highly versatile and are each connected to two external pins (each one has an input and an output). These two timers can be used to count or time external events that drive the timer input pins. Timers 0 and 1 can also be used to generate nonrepetitive or variable-duty-cycle waveforms on the timer output pins.

Timer 2 is not connected to any external pins. It can be used by software to generate interrupts, or it can be polled for real-time coding and time-delay applications. Timer 2 can also be used as a prescaler to Timer 0 and Timer 1, or as a DMA request source.

The source clock for Timer 2 is one-fourth of the system clock frequency. The source clock for Timers 0 and 1 can be configured to be one-fourth of the system clock, or they can be driven from their respective timer input pins. When driven from a timer input pin, the timer is counting the “event” of an input transition.

The Am186CU USB microcontroller also provides a pulse width demodulation (PWD) option so that a toggling input signal’s Low state and High state durations can be measured.

Hardware Watchdog Timer

The Am186CU USB microcontroller provides a full-featured watchdog timer, which includes the ability to generate Non-Maskable Interrupts (NMIs), microcontroller resets, and system resets when the timeout value is reached. The timeout value is programmable and ranges from 2^{10} to 2^{26} processor clocks.

The watchdog timer is used to regain control when a system has failed due to a software error or to failure of an external device to respond in the expected way. Software errors can sometimes be resolved by recapturing control of the execution sequence via a watchdog-timer-generated NMI. When an external device fails to respond, or responds incorrectly, it may be necessary to reset the controller or the entire system, including external devices. The watchdog timer provides the flexibility to support both NMI and reset generation.

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Memory and Peripheral Interface

System Interfaces

The Am186CU USB microcontroller bus interface controls all accesses to the peripheral control block (PCB), memory-mapped and I/O-mapped external peripherals, and memory devices. Internal peripherals are accessed by the bus interface through the PCB.

The bus interface features programmable bus sizing; individually selectable chip selects for the upper ($\overline{UCS}$) memory space, lower ($\overline{LCS}$) memory space, all non-$\overline{UCS}$, non-$\overline{LCS}$ and I/O memory spaces; separate byte-write enables; and, boot option from an 8- or 16-bit device.

The integrated peripherals are controlled by 16-bit read/write registers. The peripheral registers are contained within an internal 1-Kbyte control block. At reset, the base of the PCB is set to FC00h in I/O space. The registers are physically located in the peripheral devices they control, but they are addressed as a single 1-Kbyte block. For details on the PCB registers, refer to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, order #21916.

Accesses to the PCB should be performed by direct processor actions. The use of DMA to write or read from the PCB results in unpredictable behavior, except where explicit exception is made to support a peripheral function, such as the High-Speed UART transmit and receive data registers.

The 80C186 and 80C188 microcontrollers use a multiplexed address and data (AD) bus. The address is present on the AD bus only during the t_1 clock phase. The Am186CU USB microcontroller continues to provide the multiplexed AD bus and, in addition, provide a nonmultiplexed address (A) bus. The A bus provides an address to the system for the complete bus cycle (t_1–t_4). During refresh cycles, the AD bus is driven during the t_1 phase and the values are unknown during the t_2, t_3, and t_4 phases. The value driven on the A bus is undefined during a refresh cycle.

The nonmultiplexed address bus (A19–A0) is valid one-half CLKOUT cycle in advance of the address on the AD bus. When used with the modified $\overline{UCS}$ and $\overline{LCS}$ outputs and the byte write enable signals, the A19–A0 bus provides a seamless interface to SRAM, DRAM, and Flash/EPROM memory systems.

For systems where power consumption is a concern, it is possible to disable the address from being driven on the AD bus on the microcontroller during the normal address portion of the bus cycle for accesses to upper ($\overline{UCS}$) and/or lower ($\overline{LCS}$) address spaces. In this mode, the affected bus is placed in a high-impedance state during the address portion of the bus cycle. This feature is enabled through the DA bits in the Upper Memory Chip Select (UMCS) and Lower Memory Chip Select (LMCS) registers.

When address disable is in effect, the number of signals that assert on the bus during all normal bus cycles to the associated address space is reduced, thus decreasing power consumption, reducing processor switching noise, and preventing bus contention with memory devices and peripherals when operating at high clock rates.

If the $\overline{ADEN}$ pin is asserted during processor reset, the value of the DA bits in the UMCS and LMCS registers is ignored and the address is driven on the AD bus for all accesses, thus preserving the industry-standard 80C186 and 80C188 microcontrollers' multiplexed address bus and providing support for existing emulation tools. For details on these registers, refer to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, order #21916.

Figure 3 on page 29 shows the affected signals during a normal read or write operation. The address and data are multiplexed onto the AD bus.

Figure 4 on page 29 shows a bus cycle when address bus disable is in effect, which causes the AD bus to operate in a nonmultiplexed data-only mode. The A bus has the address during a read or write operation.

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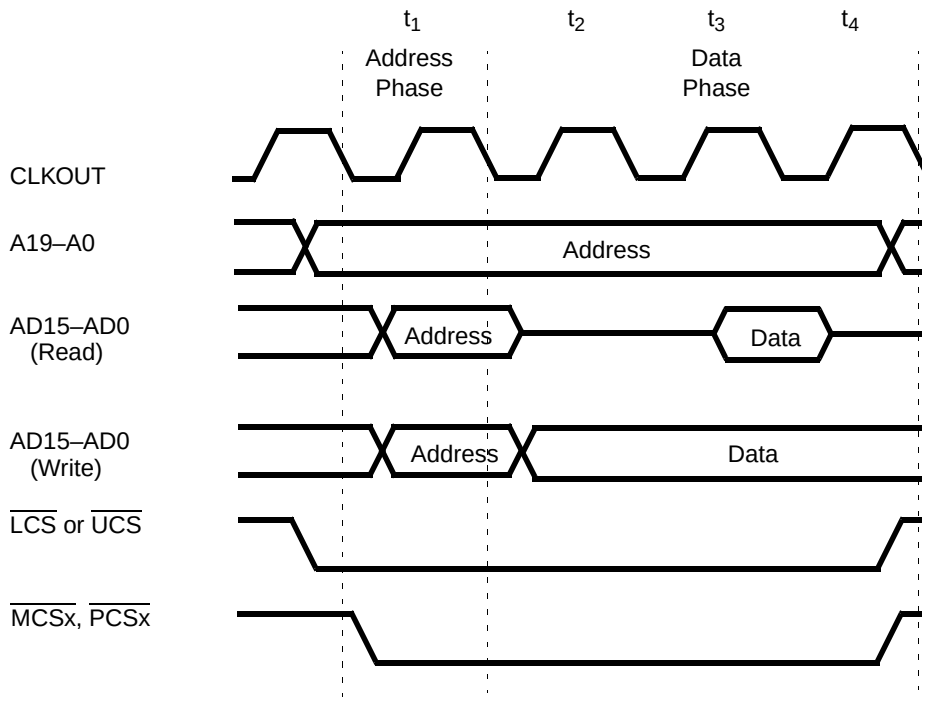

Figure 3. Am186CU Microcontroller Address Bus — Default Operation

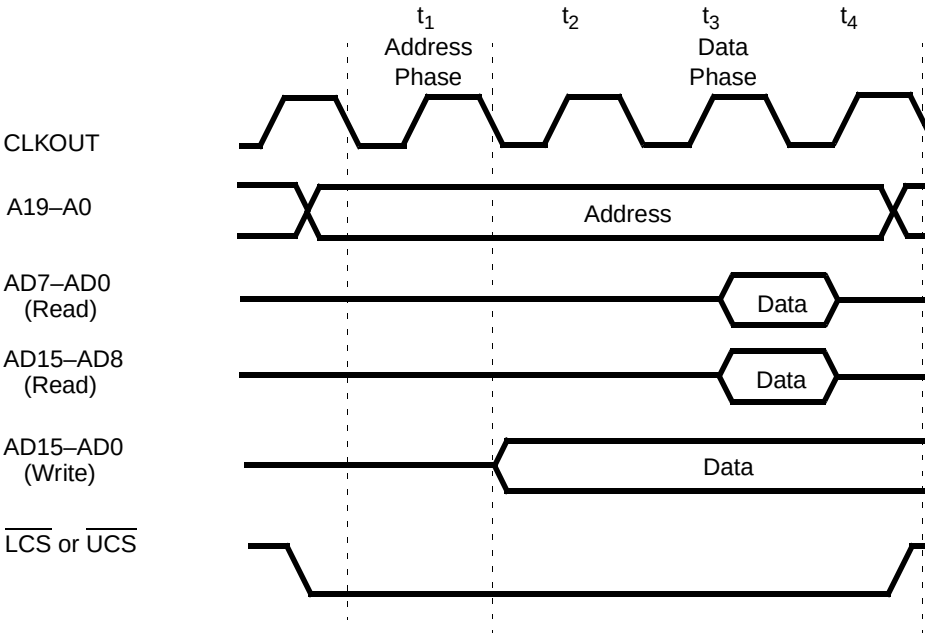

Figure 4. Am186CU Microcontroller—Address Bus Disable In Effect

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Bus Interface

The bus interface controls all accesses to external peripherals and memory devices. External accesses include those to memory devices, as well as those to memory-mapped and I/O-mapped peripherals and the peripheral control block. The Am186CU USB microcontroller provides an enhanced bus interface unit with the following features:

- Nonmultiplexed address bus
- Separate byte write enables for high and low bytes
- Output enable

The standard 80C186/80C188 multiplexed address and data bus requires system interface logic and an external address latch. On the Am186CU USB microcontroller, byte write enables and a nonmultiplexed address bus can reduce design costs by eliminating this external logic.

Nonmultiplexed Address Bus

The nonmultiplexed address bus (A19–A0) is valid one-half CLKOUT cycle in advance of the address on the AD bus. When used with the modified $\overline{UCS}$ and $\overline{LCS}$ outputs and the byte write enable signals, the A19–A0 bus provides a seamless interface to external SRAM, and Flash memory/EPROM systems.

Byte Write Enables

The Am186CU USB microcontroller provides the $\overline{WHB}$ (Write High Byte) and $\overline{WLB}$ (Write Low Byte) signals that act as byte write enables.

$\overline{WHB}$ is the logical OR of $\overline{BHE}$ and $\overline{WR}$. $\overline{WHB}$ is Low when both $\overline{BHE}$ and $\overline{WR}$ are Low. $\overline{WLB}$ is the logical OR of A0 and $\overline{WR}$. $\overline{WLB}$ is Low when A0 and $\overline{WR}$ are both Low.

The byte write enables are driven with the nonmultiplexed address bus as required for the write timing requirements of common SRAMs.

Output Enable

The Am186CU USB microcontroller provides the $\overline{RD}$ (Read) signal that acts as an output enable for memory or peripheral devices. The $\overline{RD}$ signal is Low when a word or byte is read by the microcontroller.

DRAM Support

To support DRAM, the Am186CU USB microcontroller has a fully integrated DRAM controller that provides a glueless interface to 25–70-ns Extended Data Out (EDO) DRAM. (EDO DRAM is sometimes called Hyper-Page Mode DRAM.) Up to two banks of 4-Mbit (256 Kbit x 16 bit) DRAM can be accessed. Page Mode DRAM, Fast Page Mode DRAM, Asymmetrical DRAM, and 8-bit wide DRAM are not supported. The microcontroller provides zero-wait state operation at up to 50 MHz with 40-ns DRAM. This allows designs requiring larger amounts of memory to save system cost over SRAM designs by taking advantage of low DRAM memory costs.

The DRAM interface uses various chip select pins to implement the $\overline{RAS}$/$\overline{CAS}$ interface required by DRAMs. The DRAM controller drives the $\overline{RAS}$/$\overline{CAS}$ interface appropriately during both normal memory accesses and during refresh. All signals required are generated by the microcontroller and no external logic is required.

The DRAM multiplexed address pins are connected to the odd address pins of the Am186CU USB microcontroller, starting with A1 on the Am186CU USB microcontroller connecting to MA0 on the DRAM. The correct row and column addresses are generated on these odd address pins during a DRAM access.

The $\overline{RAS}$ pins are multiplexed with $\overline{LCS}$ and $\overline{MCS3}$, allowing a DRAM bank to be present in either high or low memory space. The $\overline{MCS1}$ and $\overline{MCS2}$ function as the upper and lower $\overline{CAS}$ pins, respectively, and define which byte of data in a 16-bit DRAM is being accessed.

The microcontroller supports the most common DRAM refresh option, CAS-Before-RAS. All refresh cycles contain three wait states to support the DRAMs at various frequencies. The DRAM controller never performs a burst access. All accesses are single accesses to DRAM. If the $\overline{PCS}$ chip selects are decoded to be in the DRAM address range, $\overline{PCS}$ accesses take precedence over the DRAM.

Chip Selects

The Am186CU USB microcontroller provides six chip select outputs for use with memory devices and eight more for use with peripherals in either memory or I/O space. The six memory chip selects can be used to address three memory ranges. Each peripheral chip select addresses a 256-byte block offset from a programmable base address.

The microcontroller can be programmed to sense a ready signal for each of the peripheral or memory chip select lines. A bit in each chip select control register determines whether the external ready signal is required or ignored.

The chip selects can control the number of wait states inserted in the bus cycle. Although most memory and peripheral devices can be accessed with three or less wait states, some slower devices cannot. This feature allows devices to use wait states to slow down the bus.

The chip select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or by the integrated DMA unit.

General enhancements over the original 80C186 include bus mastering (three-state) support for all chip selects and activation only when the associated register is written, not when it is read.

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Clock Control

The processor supports clock rates from 16 to 50 MHz using an integrated crystal oscillator and PLL. Commercial and industrial temperature ratings are available. Separate crystal oscillator inputs are provided for the USB and CPU. Flexibility is provided to run the entire device from a 12- or 24-MHz crystal when the USB is in use. The CPU can run in 1x, 2x, or 4x PLL mode. The USB can run in 2x or 4x PLL mode.

In-Circuit Emulator Support

Because pins are an expensive resource, many play a dual role, and the programmer selects PIO operation or an alternate function. However, a pin configured to be a PIO may also be required for emulation support. Therefore, it is important that before a design is committed to hardware, a user should contact potential emulator suppliers for a list of their emulator's pin requirements. The following PIO signals are multiplexed with alternate signals that may be used by emulators: PIO8, PIO15, PIO33–PIO35.

The Am186CU USB microcontroller was designed to minimize conflicts. In most cases, pin conflict is avoided. For example, if the ALE signal is required for multiplex bus support, then it is not programmed as PIO33. If the multiplexed AD bus is not used, then ALE can be programmed as a PIO pin. And if the multiplexed bus is not in use, then the emulator does not require the ALE signal. However, an emulator is likely to always use the de-multiplexed address, regardless of how the AD bus is programmed.

APPLICATIONS

The Am186CU USB microcontroller with its integrated USB and other communications features provides a highly integrated, cost-effective solution for a wide range of telecommunications and networking applications.

- **xDSL Applications:** Today's xDSL applications, such as high-speed ADSL modems, require data handling of 2 Mbit/s or greater and can take advantage of the USB interface for easy connectivity to the PC.
- **USB Peripheral Devices:** These devices will become more common as the PC market embraces the USB protocol. In addition to implementing communications devices, the USB peripheral controller makes the Am186CU USB microcontroller suitable for certain PC desktop applications such as a USB camera interface, ink-jet printers, and scanners.
- **General Communications Applications:** The Am186CU USB microcontroller will also find a home in general embedded applications, because many devices will incorporate communications capability in the future. The microcontroller is especially attractive for 186 designs adding USB.

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CLOCK GENERATION AND CONTROL

The Am186CU USB microcontroller clocks include the general system clock (CLKOUT), USB clock, and the baud rate generator clock for UART and High-Speed UART.

The SSI and the timers (Timers 0, 1, and 2) derive their clocks from the system clock.

Features

The Am186CU USB microcontroller clocks include the following features and characteristics:

- Two independent crystal-controlled oscillators that use external fundamental mode crystals or oscillators to generate the system input clock and the USB input clock.
- Two independent internal PLLs, one of which generates a system clock (CLKOUT) that is 1x, 2x, or 4x the system input clock, and one that generates the 48-MHz clock required for the USB from either a48-, 24-, or 12-MHz input.
- Single clock source operation possible by sharing the clock source between the system and the USB.
- SSI clock (SCLK) is derived from the system clock, divided by 2, 4, 8, 16, 32, 64, 128, or 256.
- Timers 0 and 1 can be configured to be driven by the timer input pins (TMRIN1, TMRIN0) or at one-fourth of the system clock. Timer 2 is driven at one-fourth of the system clock.
- UART clock can be derived from the internal system clock frequency or from the UART clock (UCLK) input.

See Figure 5 on page 33 for a diagram of the basic clock generation and Figure 6 on page 34 for suggested clock frequencies and modes.

System Clock

The system PLL generates frequencies from 16 to 50 MHz. The reference for the system PLL can vary from 8 to 40 MHz, depending on the PLL mode selected and the desired system frequency (see Figure 6 on page 34).

The system PLL modes are chosen by the state of the {CLKSEL1} and {CLKSEL2} pins during reset. For these pinstrap settings see Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8.

The system clock can be generated in one of two ways:

- Using the internal PLL running at 1x, 2x, or 4x the reference clock. The reference clock can be generated from an external crystal using the integrated oscillator or an external oscillator input.
- Bypassing the internal PLL. The external reference generated from either a crystal or an external oscillator input is used to generate the system clock. For more information about bypassing the internal PLL, refer to “PLL Bypass Mode” on page 35.

USB Clock

The USB PLL provides the 48-MHz clock that is required for USB full-speed operation. This clock is divided down to provide a 12-MHz clock that supports the full-speed USB rate (12 Mbit/s). The low-speed rate of 1.5 Mbit/s is not supported. The USB PLL modes are chosen by the state of the {USBSEL1} and {USBSEL2} pins during reset. For these pinstrap settings see Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8.

The USB clock can be generated in one of two ways:

- Using the system clock. In this mode, the system PLL is restricted to 48-MHz operation only.

Note: *When using the system clock for the USB clock source, the designer must externally pull down the USBX1 input.*

- Using its own internal 48-MHz PLL. This PLL can run in 2x or 4x mode and requires a 12- or 24-MHz reference that can be generated by either the integrated crystal-controlled oscillator or an external oscillator input.

Note: *The system clock must be a minimum of 24 MHz when using the USB peripheral controller and its internal 48-MHz PLL.*

The USB specification requires a frequency tolerance of less than 2500 ppm, which must be met whether using an external clock source, a crystal on USBX1–USBX2, or clock sharing by system and USB. When using a crystal, some frequency tolerance margin must be allowed to account for the differences in external loading capacitances, etc. The usual rule of thumb is to specify a crystal with a frequency tolerance of one half the required frequency tolerance.

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Clock Sharing by System and USB

The CPU and USB clocks can be generated from a single source in one of two ways:

- The system can run at 48 MHz by using the system clock for the USB clock.

Note: *When using the system clock for the USB clock source, the designer must externally pull down the USBX1 input.*

- The system can be run at 24 MHz by sharing an external clock reference (X1) with the USB (USBX1). A 12-MHz source can be used with the system PLL in 2x mode and the USB PLL in 4x mode, or a 24-MHz source can be used with the system in 1x mode and the USB in 2x mode.

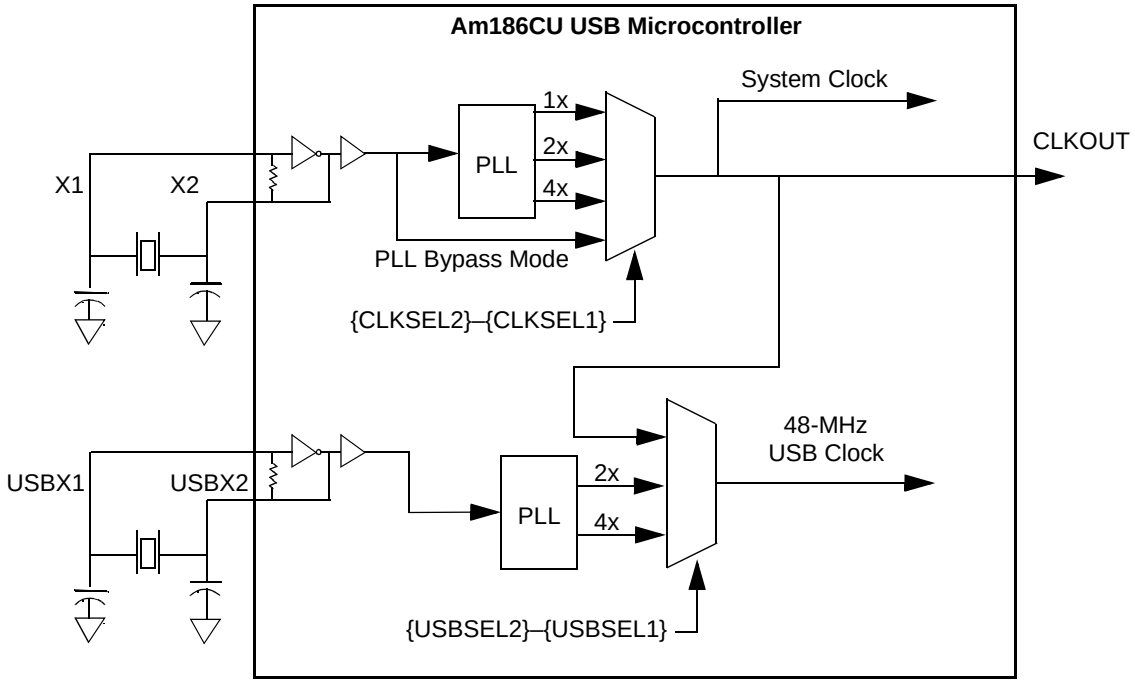

Figure 5. System and USB Clock Generation

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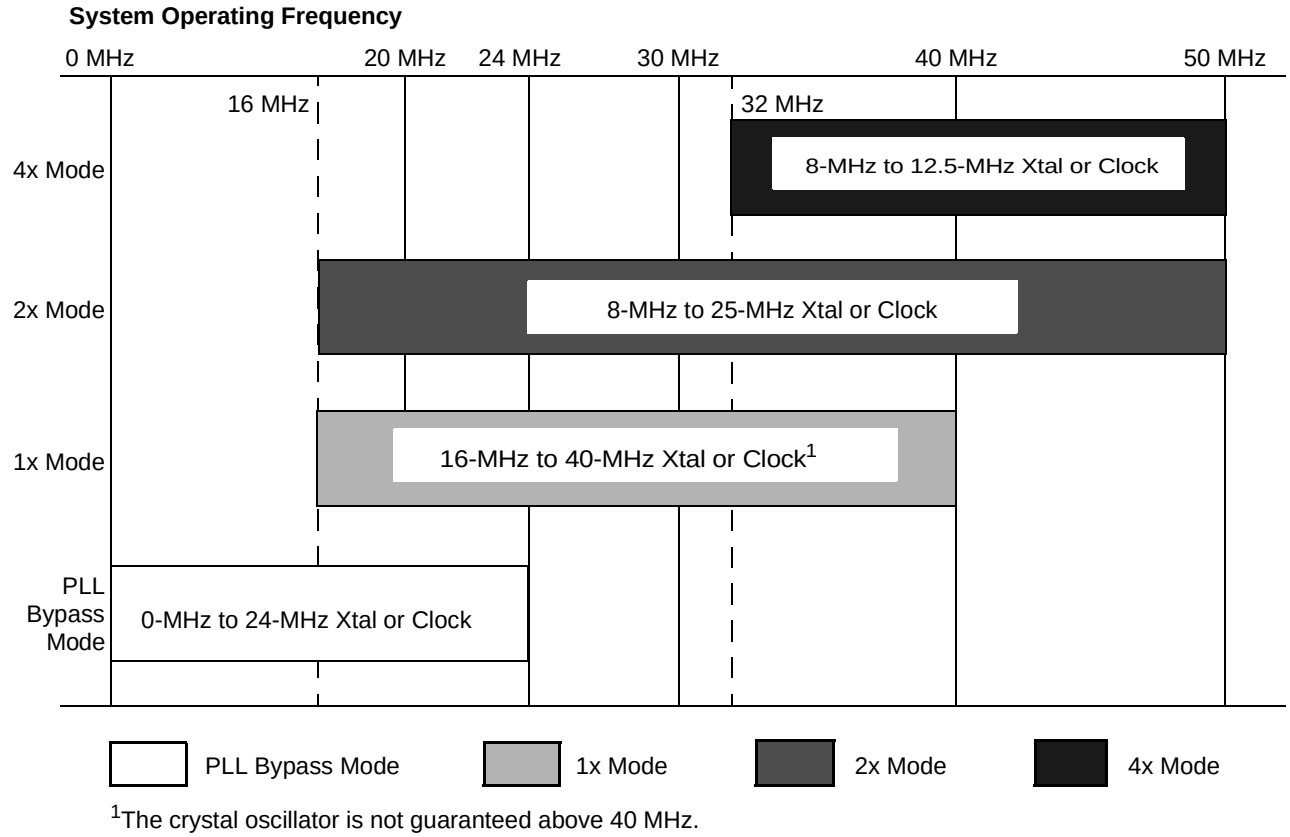

Figure 6. Suggested System Clock Frequencies, Clock Modes, and Crystal Frequencies

Crystal-Driven Clock Source

The internal oscillator circuit is designed to function with an external parallel-resonant fundamental mode crystal. The crystal frequency can vary from 8 to 40 MHz, depending on the PLL mode selected and desired system frequency.

When selecting a crystal, the load capacitance should always be specified (C_L). This value can cause variance in the oscillation frequency from the desired specified value (resonance). The load capacitance and the loading of the feedback network have the following relationship:

$$C_L = \frac{(C_1 \cdot C_2)}{(C_1 + C_2)} + C_S$$

where C_S is the stray capacitance of the circuit.

Table 6 shows crystal parameter values. Figure 7 shows the system clocks using an external crystal and the integrated oscillator. The specific values for C_1 and C_2 must be determined by the designer and are dependent on the characteristics of the chosen crystal and board design.

Table 6. Crystal Parameters[1]

Parameter	Min. Value	Max. Value	Units
Frequency	8	40	MHz
ESR			
8–24 MHz	20	90	ohms
24–50 MHz	20	60	ohms
Load capacitance	10	—	pF

Notes:

1. If the crystal is used for a USB clock source, there is an additional clock jitter tolerance.

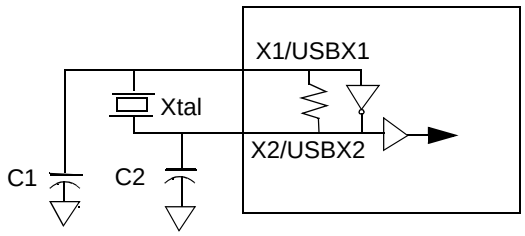

Figure 7. External Interface to Support Clocks—Fundamental Mode Crystal

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External Clock Source

The internal oscillator also can be driven by an external clock source. The external clock source should be connected to the input of the inverting amplifier (X1 or USBX1) with the output (X2 or USBX2) left unconnected. Figure 8 shows the system clocks using an external clock source (oscillator bypass).

Note: *X1, X2, USBX1, and USBX2 are not 5-V tolerant and have a maximum input equal to V_{CC}.*

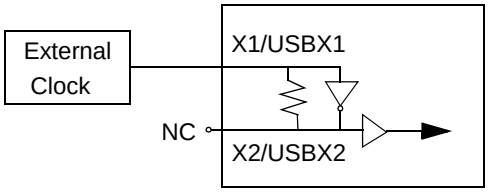

Figure 8. External Interface to Support Clocks—External Clock Source

Static Operation

The Am186CU USB microcontroller is a fully static design and can be placed in static mode by stopping the input clock. See the PLL Bypass Mode discussion below.

Note: *It is the responsibility of the system designer to ensure that no short clock phases are generated when starting or stopping the clock.*

PLL Bypass Mode

The Am186CU USB microcontroller provides a PLL Bypass mode that allows the X1 input frequency to be anywhere from 0 to 24 MHz. When the microcontroller is in PLL Bypass mode, the CLKOUT frequency equals the X1 input frequency. This mode must be used with an external clock source. For PLL Bypass mode enabling, see Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8.

When changing frequency in PLL Bypass mode, the X1 input must not have any short or “runt” pulses. At 24 MHz, the nominal High/Low time is 21 ns. The actual High times and Low times must not fall below 16 ns. These values allow a 60%/40% duty cycle at X1.

In the Am186CU microcontroller, the USB PLL and USBX1 determine the USB clock. USB requires the system clock to be 24 MHz or greater. Therefore, disable the USB peripheral controller before slowing the system clock to less than 24 MHz. If USB is not used, the USBX1 can be pulled down.

UART Baud Clock

The UART and High-Speed UART have two possible clock sources: the system clock or the UCLK input pin. If UCLK is used for the UART clock, the system clock must be at least the same frequency as UCLK. The clock configurations are shown graphically in Figure 9.

The baud clock is generated by dividing the clock source by the value of the baud rate divisor register. The serial port logic can select its baud rate clock from either an external pin (UCLK) or from the system clock.

The system or UCLK clock is selected independent of any other settings.

The formula for determining the baud rate divisor register value is:

BAUDDIV = (clock frequency/(16 • baud rate))

Note: *UCLK cannot be clocked at a frequency higher than the system clock frequency.*

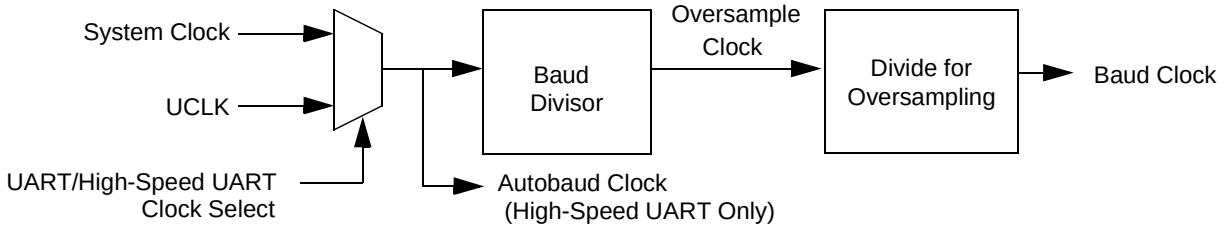

Figure 9. UART and High-Speed UART Clocks

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POWER SUPPLY OPERATION

CMOS dynamic power consumption is proportional to the square of the operating voltage multiplied by capacitance and operating frequency. Static CPU operation can reduce power consumption by enabling the system designer to reduce operating frequency when possible. However, operating voltage is always the dominant factor in power consumption. By reducing the operating voltage from 5 V to 3.3 V for any device, the power consumed is reduced by 56%.

Reduction of CPU and system logic operating voltage dramatically reduces overall system power consumption. Additional power savings can be realized as low-voltage mass storage and peripheral devices become available.

Two basic strategies exist in designing systems containing the Am186CU USB microcontroller. The first strategy is to design a homogenous system in which all logic components operate at 3.3 V. This provides the lowest overall power consumption. However, system designers may need to include devices for which 3.3-V versions are not available.

In the second strategy, the system designer must then design a mixed 5-V/3.3-V system. This compromise enables the system designer to minimize the system logic power consumption while still including the functionality of the 5-V features. The choice of a mixed voltage system design also involves balancing design complexity with the need for the additional features.

Power Supply Connections

Connect all V_{CC} pins together to the 3.3-V power supply and all ground pins to a common system ground.

Input/Output Circuitry

To accommodate current 5-V systems, the Am186CU USB microcontroller has 5-V tolerant I/O drivers. The drivers produce TTL-compatible drive output (minimum 2.4-V logic High) and receive TTL and CMOS levels (up to V_{CC} + 2.6 V). The following are some design issues that should be considered with mixed 3.3-V/5-V designs:

- During power-up, if the 3.3-V supply has a significant delay in achieving stable operation relative to 5-V supply, then the 5-V circuitry in the system may start driving the processor's inputs above the maximum levels (V_{CC} + 2.6 V). The system design should ensure that the 5-V supply does not exceed 2.6 V above the 3.3-V supply during a power-on sequence.
- Preferably, all inputs are driven by sources that can be three-stated during a system reset condition. The system reset condition should persist until stable V_{CC} conditions are met. This should help ensure that the maximum input levels are not exceeded during power-up conditions.
- Preferably, all pullup resistors are tied to the 3.3-V supply, which ensures that inputs requiring pullups are not over stressed during power-up.

PIO Supply Current Limit

Each programmable I/O output is able to sink or source a sustained 16-mA drive current. However, only 40 mA of sustained PIO current is allowed for each supply pin (V_{CC}), and only 60 mA is allowed for each ground pin (V_{SS}).

To calculate the PIO current for each supply or ground pin, sum the applicable current (source or sink) of all PIO pins on either side of the pin (to the adjacent corresponding pins), and divide the sum by two. The resulting value should not exceed 40 mA for V_{CC} or 60 mA for V_{SS}.

Exclude the following pins from this calculation: 72 (V_{SS}_A), 82 (V_{SS}_USB), 77 (V_{CC}_A), and 79 (V_{CC}_USB).

For example, to calculate the PIO current for pin 83 (V_{SS}), total the sustained sinking current for all PIO pins between pin 71 (V_{SS}) and pin 100 (V_{SS}), and divide the sum by two.

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ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Minimum	Maximum	Unit
Temperature under bias: Commercial	T_C[2]	0	100	°C
Industrial	T_A[3]	–40	+85	°C
Storage temperature	—	–65	+150	°C
Voltage on 5-V-tolerant pins[4] with respect to ground	—	–0.5	V_{CC} + 2.6	V
Voltage on other pins with respect to ground	—	–0.5	V_{CC} + 0.5	V
Sustained PIO current on any supply (V_{CC}) pin[5]	—	40	—	mA
Sustained PIO current on any ground (V_{SS}) pin[5]	—	60	—	mA

Notes:

1. Stresses above those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2. T_C = case temperature.

3. T_A = ambient temperature.

4. 5 V-tolerant pins are indicated in Table 29, "Pin List Summary," on page A-10.

5. See "Power Supply Current" on page 39.

OPERATING RANGES[1]

Parameter	Symbol	Minimum	Maximum	Unit
Commercial	T_C[2]	0	100	°C
Industrial	T_A[3]	–40	+ 85	°C
Supply voltage with respect to ground	V_{CC}	3.0	3.6	V

Notes:

1. Operating Ranges define those limits between which the functionality of the device is guaranteed.

2. T_C = case temperature.

3. T_A = ambient temperature.

DRIVER CHARACTERISTICS—UNIVERSAL SERIAL BUS

Each USBD+ and USBD– pin connects through a series resistor directly to the USB. The series resistor value should be selected to achieve a total driver impedance between 29 and 44 ohms, as required by the USB version 1.0 specification. A 36-Ω ±1% series resistor is recommended for each pin.

Characteristics of these two pins are defined in the USB version 1.0 specification. Consult this specification for details about overall USB system design. (At the time of this writing, the current USB specification and related information can be obtained on the Web at **www.usb.org**.)

The Am186CU USB microcontroller is guaranteed to meet all USB specifications. Required analog transceivers are integrated into the Am186CU USB microcontroller.

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DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES[1]

Symbol	Parameter	Preliminary		Unit
		Minimum	Maximum	
V_{OH}	Output High voltage (I_{OH} = –2.4 mA)	2.4	—	V
V_{OH}	Output High voltage (I_{OH} = –0.1 mA)[2]	V_{CC} – 0.2	—	V
V_{OL}	Output Low voltage (I_{OL} = 4.0 mA)	—	0.45	V
V_{IH5}	5-V tolerant Input High voltage	2.0	V_{CC} + 2.6	V
V_{IH}	Input High voltage, except 5-V tolerant	2.0	V_{CC}+0.3	V
V_{IL}	Input Low voltage	–0.3	0.8	V
I_{LI}	Input leakage current (0.1 V ≤ V_{OUT} ≤ V_{CC}) (all pins except those with internal pullup/pulldown resistors)	—	±10	µA
I_{LO}	Output leakage current[3] (0.1 V ≤ V_{OUT} ≤ V_{CC})	—	±15	µA
P_{CC}	Power consumption	—	1.2	W

Notes:

1. Current out of pin is stated as a negative value.

2. Characterized but not tested.

3. This parameter is for three-state outputs where V_{OUT} is driven on the three-state output.

CAPACITANCE

Symbol	Parameter	Preliminary		Unit
		Minimum	Maximum	
C_{IN}	Input capacitance	—	15	pF
C_{CLK}	Clock capacitance	—	15	pF
C_{OUT}	Output capacitance	—	20	pF
$C_{I/O}$	I/O pin capacitance	—	20	pF

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MAXIMUM LOAD DERATING

All maximum delay numbers should be increased by 0.035 ns for every pF of load over the maximum load (up to a maximum of 150 pF) specified in Table 29, “Pin List Summary,” on page A-10.

POWER SUPPLY CURRENT

For the following typical system specification shown in Figure 10, I_{CC} has been measured at 6 mA per MHz of system clock. The typical system is measured while the system is executing code in a typical application with nominal voltage and maximum case temperature. Actual power supply current is dependent on system design and may be greater or less than the typical I_{CC} figure presented here.

Typical current in Figure 10 is given by:

$$I_{CC} = 6\ mA \cdot freq(MHz)$$

Please note that dynamic I_{CC} measurements are dependent upon chip activity, operating frequency, output buffer logic, and capacitive/resistive loading of the outputs. For these I_{CC} measurements, the devices were set to the following modes:

- No DC loads on the output buffers
- Output capacitive load set to 30 pF
- AD bus set to data only
- PIOs are disabled
- Timer, serial port, refresh, and DMA are enabled

Table 7 shows the values that are used to calculate the typical power consumption value for the Am186CU USB microcontroller.

Table 7. Typical Power Consumption Calculation

MHz · I_{CC} · Volts / 1000 = P			Typical Power in Watts
MHz	Typical I_{CC}	Volts	
25	6	3.3	0.495
40	6	3.3	0.792
50	6	3.3	0.99

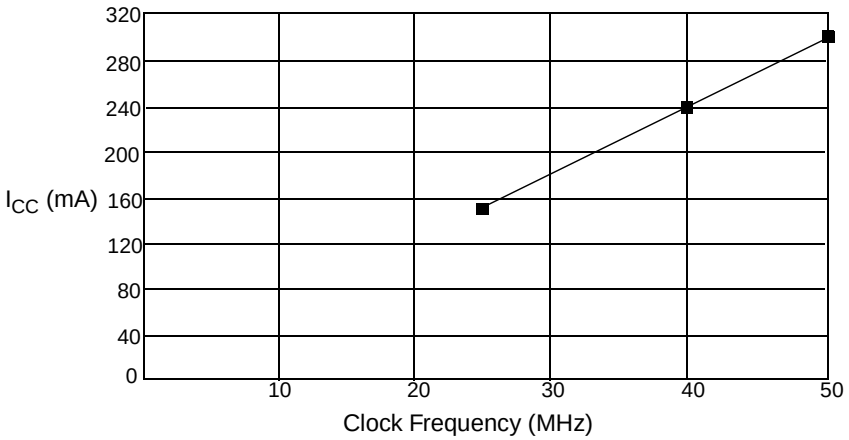

Figure 10. Typical I_{cc} Versus Frequency

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THERMAL CHARACTERISTICS—PQFP PACKAGE

The Am186CU USB microcontroller is specified for operation with case temperature ranges from 0°C to +100°C for 3.3 V ± 0.3 V (commercial). Case temperature is measured at the top center of the package as shown in Figure 11. The various temperatures and thermal resistances can be determined using the equations in Figure 12 with information given in Table 8.

The total thermal resistance is θ_{JA}; θ_{JA} is the sum of θ_{JC}, the internal thermal resistance of the assembly, and θ_{CA}, the case-to-ambient thermal resistance.

The variable P is power in watts. Power supply current (I_{CC}) is in mA per MHz of clock frequency.

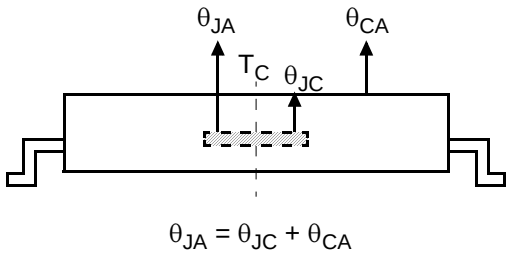

Figure 11. Thermal Resistance (°C/Watt)

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$
$$P = I_{CC} \cdot \text{freq (MHz)} \cdot V_{CC}$$

$$T_J = T_C + (P \cdot \theta_{JC})$$
$$T_J = T_A + (P \cdot \theta_{JA})$$

$$T_C = T_J - (P \cdot \theta_{JC})$$
$$T_C = T_A + (P \cdot \theta_{CA})$$

$$T_A = T_J - (P \cdot \theta_{JA})$$
$$T_A = T_C - (P \cdot \theta_{CA})$$

Figure 12. Thermal Characteristics Equations

Table 8. Thermal Characteristics (°C/Watt)

Package/Board	Airflow (Linear Feet per Minute)	θ_{JC}	θ_{CA}	θ_{JA}
PQFP/2-Layer	0 fpm	7	38	45
	200 fpm	7	32	39
	400 fpm	7	28	35
	600 fpm	7	26	33
PQFP/4-Layer to 6-Layer	0 fpm	5	18	23
	200 fpm	5	16	21
	400 fpm	5	14	19
	600 fpm	5	12	17

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COMMERCIAL AND INDUSTRIAL SWITCHING CHARACTERISTICS AND WAVEFORMS

In the switching waveforms that follow, several abbreviations are used to indicate the specific periods of a bus cycle. These periods are referred to as time states. A typical bus cycle is composed of four consecutive time states: t_1, t_2, t_3, and t_4. Wait states, which represent multiple t_3 states, are referred to as t_w states. When no bus cycle is pending, an idle (t_i) state occurs.

In the switching parameter descriptions, the *multiplexed* address is referred to as the AD address bus; the *demultiplexed* address is referred to as the A address bus. Figure 13 defines symbols used in the switching waveform diagrams.

Table 9 on page 42 contains an alphabetical listing of the switching parameter symbols (grouped by function), and Table 10 on page 45 contains a numerical listing of the switching parameter symbols (grouped by function).

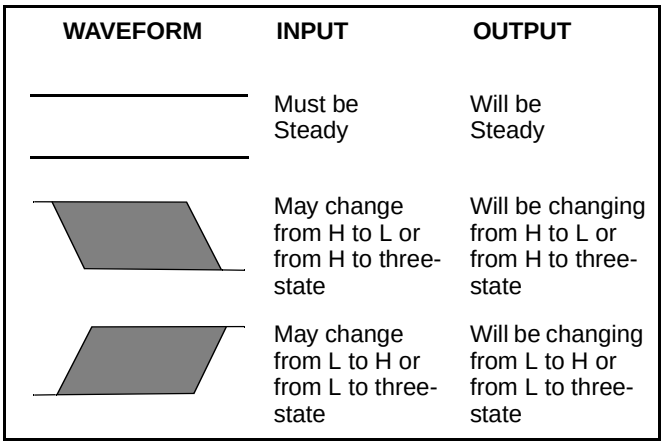

Figure 13. Key to Switching Waveforms

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Table 9. Alphabetical Key to Switching Parameter Symbols

Parameter Symbol	No.	Description
t_{ARYCH}	49	ARDY resolution transition setup time
t_{ARYCHL}	51	ARDY inactive holding time
$t_{ARYHDSH}$	95[1]	ARDY High to $\overline{DS}$ High
t_{ARYHDV}	89[1]	ARDY assert to data valid
t_{ARYLCL}	52	ARDY setup time
$t_{ARYLDSH}$	96[1]	ARDY Low to $\overline{DS}$ High
t_{AVBL}	87	A address valid to $\overline{WHB}$, $\overline{WLB}$ Low
t_{AVCH}	14	AD address valid to clock High
t_{AVLL}	12	AD address valid to ALE Low
t_{AVRL}	66	A address valid to $\overline{RD}$ Low
t_{AVWL}	65	A address valid to $\overline{WR}$ Low
t_{AZRL}	24	AD address float to $\overline{RD}$ active
t_{CH1CH2}	45	CLKOUT rise time
t_{CHAV}	68	CLKOUT High to A address valid
t_{CHCAS}	404	Change in $\overline{CAS}$ delay
t_{CHCK}	38	X1 High time
t_{CHCL}	44	CLKOUT High time
t_{CHCSV}	67	CLKOUT High to $\overline{LCS}$/$\overline{UCS}$ valid
t_{CHCSX}	18	$\overline{MCSx}$/$\overline{PCSx}$ inactive delay
t_{CHCTV}	22	Control active delay 2
t_{CHCV}	64	Command lines valid delay (after float)
t_{CHCZ}	63	Command lines float delay
t_{CHDX}	8	Status hold time
t_{CHLH}	9	ALE active delay
t_{CHLL}	11	ALE inactive delay
t_{CHQS0V}	55	Queue status 0 output delay
t_{CHQS1V}	56	Queue status 1 output delay
t_{CHRAS}	403	Change in $\overline{RAS}$ delay
t_{CHRFD}	79[1]	CLKOUT High to $\overline{RFSH}$ valid
t_{CHSV}	3	Status active delay
t_{CICO}	69	X1 to CLKOUT skew
t_{CKHL}	39	X1 fall time
t_{CKIN}	36	X1 period
t_{CKLH}	40	X1 rise time
t_{CL2CL1}	46	CLKOUT fall time
t_{CLARX}	50	ARDY active hold time
t_{CLAV}	5	AD address and $\overline{BHE}$ valid delay
t_{CLAX}	6	Address hold
t_{CLAZ}	15	AD address float delay
t_{CLCH}	43	CLKOUT Low time
t_{CLCK}	37	X1 Low time
t_{CLCL}	42	CLKOUT period
t_{CLCLX}	80[1]	$\overline{LCS}$ inactive delay

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Table 9. Alphabetical Key to Switching Parameter Symbols (Continued)

Parameter Symbol	No.	Description
t_{CLCSL}	81[1]	$\overline{LCS}$ active delay
t_{CLCSV}	16	$\overline{MCSx}$/$\overline{PCSx}$ active delay
t_{CLDOX}	30	Data hold time
t_{CLDV}	7	Data valid delay
t_{CLDX}	2	Data in hold
t_{CLHAV}	62	HLDA valid delay
t_{CLRF}	82[1]	CLKOUT High to $\overline{RFSH}$ invalid
t_{CLRH}	27	$\overline{RD}$ inactive delay
t_{CLRL}	25	$\overline{RD}$ active delay
t_{CLRO}	61	Reset delay
t_{CLSH}	4	Status and $\overline{BHE}$ inactive delay
t_{CLSRY}	48	SRDY transition hold time
t_{CLTMV}	54	Timer output delay
t_{COLV}	402	Column address valid delay
$t_{CSHARYL}$	88[1]	Chip select to ARDY Low
t_{CVCTV}	20	Control active delay 1
t_{CVCTX}	31	Control inactive delay
t_{CVDEX}	21	$\overline{DEN}$/$\overline{DS}$ inactive delay
t_{CXCSX}	17	$\overline{MCSx}$/$\overline{PCSx}$ hold from command inactive
t_{DSHDIR}	92[1]	$\overline{DS}$ High to data invalid—read
t_{DSHDIW}	98[1]	$\overline{DS}$ High to data invalid—write
t_{DSHDX}	93[1]	$\overline{DS}$ High to data bus turn-off time
t_{DSHLH}	41	$\overline{DS}$ inactive to ALE inactive
t_{DSLDD}	90[1]	$\overline{DS}$ Low to data driven
t_{DSLDV}	91[1]	$\overline{DS}$ Low to data valid
t_{DVCL}	1	Data in setup
t_{DVDSL}	97[1]	Data valid to $\overline{DS}$ Low
t_{DXDL}	19	$\overline{DEN}$/$\overline{DS}$ inactive to DT/$\overline{R}$ Low
t_{HVCL}	58	HOLD setup
t_{INVCH}	53	Peripheral setup time
t_{LCRF}	86[1]	$\overline{LCS}$ inactive to $\overline{RFSH}$ active delay
t_{LHAV}	23	ALE High to address valid
t_{LHLL}	10	ALE width
t_{LLAX}	13	AD address hold from ALE inactive
t_{LRLL}	84[1]	$\overline{LCS}$ precharge pulse width
t_{RESIN}	57	$\overline{RES}$ setup time
t_{RFCY}	85[1]	$\overline{RFSH}$ cycle time
t_{RHAV}	29	$\overline{RD}$ inactive to AD address active
t_{RHDX}	59	$\overline{RD}$ High to data hold on AD bus
t_{RHDZ}	94[1]	$\overline{RD}$ High to data bus turn-off time
t_{RHLH}	28	$\overline{RD}$ inactive to ALE High
t_{RLRH}	26	$\overline{RD}$ pulse width
t_{SRYCL}	47	SRDY transition setup time

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Table 9. Alphabetical Key to Switching Parameter Symbols (Continued)

Parameter Symbol	No.	Description
t_{WHDEX}	35	$\overline{WR}$ inactive to $\overline{DEN}$ inactive
t_{WHDX}	34	Data hold after $\overline{WR}$
t_{WHLH}	33	$\overline{WR}$ inactive to ALE High
t_{WLWH}	32	$\overline{WR}$ pulse width
USB Timing (Clocks)		
t_{UCHCK}	3	USBX1 High time
t_{UCKHL}	4	USBX1 fall time
t_{UCKIN}	1	USBX1 period
t_{UCKLH}	5	USBX1 rise time
t_{UCLCK}	2	USBX1 Low time
USB Timing (Data/Jitter)		
t_F	2	Fall time
t_{JR1}	3	Consecutive transition jitter
t_{JR2}	4	Paired transition jitter
t_R	1	Rise time
SSI		
t_{CLEV}	1	CLKOUT Low to SDEN valid
t_{CLSL}	2	CLKOUT Low to SCLK Low
t_{DVSH}	3	Data valid to SCLK High
t_{SHDX}	4	SCLK High to data invalid
t_{SLDV}	5	SCLK Low to data valid

Notes:

1. Specification defined but not in use at this time.

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Table 10. Numerical Key to Switching Parameter Symbols

No.	Parameter Symbol	Description
1	t_{DVCL}	Data in setup
2	t_{CLDX}	Data in hold
3	t_{CHSV}	Status active delay
4	t_{CLSH}	Status and $\overline{BHE}$ inactive delay
5	t_{CLAV}	AD address and $\overline{BHE}$ valid delay
6	t_{CLAX}	Address hold
7	t_{CLDV}	Data valid delay
8	t_{CHDX}	Status hold time
9	t_{CHLH}	ALE active delay
10	t_{LHLL}	ALE width
11	t_{CHLL}	ALE inactive delay
12	t_{AVLL}	AD address valid to ALE Low
13	t_{LLAX}	AD address hold from ALE inactive
14	t_{AVCH}	AD address valid to clock High
15	t_{CLAZ}	AD address float delay
16	t_{CLCSV}	$\overline{MCSx}$/$\overline{PCSx}$ active delay
17	t_{CXCSX}	$\overline{MCSx}$/$\overline{PCSx}$ hold from command inactive
18	t_{CHCSX}	$\overline{MCSx}$/$\overline{PCSx}$ inactive delay
19	t_{DXDL}	$\overline{DEN}$/$\overline{DS}$ inactive to DT/$\overline{R}$ Low
20	t_{CVCTV}	Control active delay 1
21	t_{CVDEX}	$\overline{DEN}$/$\overline{DS}$ inactive delay
22	t_{CHCTV}	Control active delay 2
23	t_{LHAV}	ALE High to address valid
24	t_{AZRL}	AD address float to $\overline{RD}$ active
25	t_{CLRL}	$\overline{RD}$ active delay
26	t_{RLRH}	$\overline{RD}$ pulse width
27	t_{CLRH}	$\overline{RD}$ inactive delay
28	t_{RHLH}	$\overline{RD}$ inactive to ALE High
29	t_{RHAV}	$\overline{RD}$ inactive to AD address active
30	t_{CLDOX}	Data hold time
31	t_{CVCTX}	Control inactive delay
32	t_{WLWH}	$\overline{WR}$ pulse width
33	t_{WHLH}	$\overline{WR}$ inactive to ALE High
34	t_{WHDX}	Data hold after $\overline{WR}$
35	t_{WHDEX}	$\overline{WR}$ inactive to $\overline{DEN}$ inactive
36	t_{CKIN}	X1 period
37	t_{CLCK}	X1 Low time
38	t_{CHCK}	X1 High time
39	t_{CKHL}	X1 fall time
40	t_{CKLH}	X1 rise time
41	t_{DSHLH}	$\overline{DS}$ inactive to ALE inactive
42	t_{CLCL}	CLKOUT period
43	t_{CLCH}	CLKOUT Low time

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Table 10. Numerical Key to Switching Parameter Symbols (Continued)

No.	Parameter Symbol	Description
44	t_{CHCL}	CLKOUT High time
45	t_{CH1CH2}	CLKOUT rise time
46	t_{CL2CL1}	CLKOUT fall time
47	t_{SRYCL}	SRDY transition setup time
48	t_{CLSRY}	SRDY transition hold time
49	t_{ARYCH}	ARDY resolution transition setup time
50	t_{CLARX}	ARDY active hold time
51	t_{ARYCHL}	ARDY inactive holding time
52	t_{ARYLCL}	ARDY setup time
53	t_{INVCH}	Peripheral setup time
54	t_{CLTMV}	Timer output delay
55	t_{CHQS0V}	Queue status 0 output delay
56	t_{CHQS1V}	Queue status 1 output delay
57	t_{RESIN}	$\overline{RES}$ setup time
58	t_{HVCL}	HOLD setup
59	t_{RHDX}	$\overline{RD}$ High to data hold on AD bus
61	t_{CLRO}	Reset delay
62	t_{CLHAV}	HLDA valid delay
63	t_{CHCZ}	Command lines float delay
64	t_{CHCV}	Command lines valid delay (after float)
65	t_{AVWL}	A address valid to $\overline{WR}$ Low
66	t_{AVRL}	A address valid to $\overline{RD}$ Low
67	t_{CHCSV}	CLKOUT High to $\overline{LCS}$/$\overline{UCS}$ valid
68	t_{CHAV}	CLKOUT High to A address valid
69	t_{CICO}	X1 to CLKOUT skew
79[1]	t_{CHRFD}	CLKOUT High to $\overline{RFSH}$ valid
80[1]	t_{CLCLX}	$\overline{LCS}$ inactive delay
81[1]	t_{CLCSL}	$\overline{LCS}$ active delay
82[1]	t_{CLRF}	CLKOUT High to $\overline{RFSH}$ invalid
84[1]	t_{LRLL}	$\overline{LCS}$ precharge pulse width
85[1]	t_{RFCY}	$\overline{RFSH}$ cycle time
86[1]	t_{LCRF}	$\overline{LCS}$ inactive to $\overline{RFSH}$ active delay
87[1]	t_{AVBL}	A address valid to $\overline{WHB}$, $\overline{WLB}$ Low
88[1]	$t_{CSHARYL}$	Chip select to ARDY Low
89[1]	t_{ARYHDV}	ARDY assert to data valid
90[1]	t_{DSLDD}	$\overline{DS}$ Low to data driven
91[1]	t_{DSLDV}	$\overline{DS}$ Low to data valid
92[1]	t_{DSHDIR}	$\overline{DS}$ High to data invalid—read
93[1]	t_{DSHDX}	$\overline{DS}$ High to data bus turn-off time
94[1]	t_{RHDZ}	$\overline{RD}$ High to data bus turn-off time
95[1]	$t_{ARYHDSH}$	ARDY High to $\overline{DS}$ High
96[1]	$t_{ARYLDSH}$	ARDY Low to $\overline{DS}$ High
97[1]	t_{DVDSL}	Data valid to $\overline{DS}$ Low

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Table 10. Numerical Key to Switching Parameter Symbols (Continued)

No.	Parameter Symbol	Description
98[1]	t_{DSHDIW}	$\overline{DS}$ High to data invalid—write
402	t_{COLV}	Column address valid delay
403	t_{CHRAS}	Change in $\overline{RAS}$ delay
404	t_{CHCAS}	Change in $\overline{CAS}$ delay
USB Timing (Clocks)		
1	t_{UCKIN}	USBX1 period
2	t_{UCLCK}	USBX1 Low time
3	t_{UCHCK}	USBX1 High time
4	t_{UCKHL}	USBX1 fall time
5	t_{UCKLH}	USBX1 rise time
USB Timing (Data/Jitter)		
1	t_R	Rise time
2	t_F	Fall time
3	t_{JR1}	Consecutive transition jitter
4	t_{JR2}	Paired transition jitter
SSI		
1	t_{CLEV}	CLKOUT Low to SDEN valid
2	t_{CLSL}	CLKOUT Low to SCLK Low
3	t_{DVSH}	Data valid to SCLK High
4	t_{SHDX}	SCLK High to data invalid
5	t_{SLDV}	SCLK Low to data valid

Notes:

1. Specification defined but not in use at this time.

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Switching Characteristics over Commercial and Industrial Operating Ranges

In this section, the following timings and timing waveforms are shown:

Table 11. Read Cycle Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
General Timing Requirements									
1	t_{DVCL}	Data in setup	10	—	5	—	5	—	ns
2	t_{CLDX}	Data in hold[2]	3	—	2	—	2	—	ns
General Timing Responses									
3	t_{CHSV}	Status active delay	0	20	0	12	0	10	ns
4	t_{CLSH}	Status and $\overline{BHE}$ inactive delay	0	20	0	12	0	10	ns
5	t_{CLAV}	AD address and $\overline{BHE}$ valid delay	0	20	0	12	0	10	ns
6	t_{CLAX}	Address hold	0	—	0	—	0	—	ns
8	t_{CHDX}	Status hold time	0	—	0	—	0	—	ns
9	t_{CHLH}	ALE active delay	—	20	—	12	—	10	ns
10	t_{LHLL}	ALE width	t_{CLCL}–10=30	—	t_{CLCL}–5=20	—	t_{CLCL}–5=15	—	ns
11	t_{CHLL}	ALE inactive delay	—	20	—	12	—	10	ns
12	t_{AVLL}	AD address valid to ALE Low[3]	0.5 • t_{CLCH}	—	0.5 • t_{CLCH}	—	0.5 • t_{CLCH}	—	ns
13	t_{LLAX}	AD address hold from ALE inactive[3]	t_{CHCL}	—	t_{CHCL}	—	t_{CHCL}	—	ns
14	t_{AVCH}	AD address valid to clock High	0	—	0	—	0	—	ns
15	t_{CLAZ}	AD address float delay	t_{CLAX}=0	20	t_{CLAX}=0	12	t_{CLAX}=0	10	ns
16	t_{CLCSV}	$\overline{MCSx}$/$\overline{PCSx}$ active delay	0	20	0	12	0	10	ns
17	t_{CXCSX}	$\overline{MCSx}$/$\overline{PCSx}$ hold from command inactive	t_{CLCH}	—	t_{CLCH}	—	t_{CLCH}	—	ns
18	t_{CHCSX}	$\overline{MCSx}$/$\overline{PCSx}$ inactive delay	0	20	0	12	0	10	ns
19	t_{DXDL}	$\overline{DEN}$/$\overline{DS}$ inactive to DT/$\overline{R}$ Low[3, 4]	–1	—	–1	—	–1	—	ns
20	t_{CVCTV}	Control active delay 1	0	20	0	12	0	10	ns

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Table 11. Read Cycle Timing[1] (Continued)

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
21	t_{CVDEX}	$\overline{DEN}$/$\overline{DS}$ inactive delay[4]	0	20	0	12	0	10	ns
22	t_{CHCTV}	Control active delay 2	0	20	0	12	0	10	ns
23	t_{LHAV}	ALE High to address valid	15	—	7.5	—	5	—	ns
Read Cycle Timing Responses									
24	t_{AZRL}	AD address float to $\overline{RD}$ active	0	—	0	—	0	—	ns
25	t_{CLRL}	$\overline{RD}$ active delay	0	20	0	10	0	10	ns
26	t_{RLRH}	$\overline{RD}$ pulse width	$2t_{CLCL}$–15=65	—	$2t_{CLCL}$–10=40	—	$2t_{CLCL}$–10=30	—	ns
27	t_{CLRH}	$\overline{RD}$ inactive delay	0	20	0	12	0	10	ns
28	t_{RHLH}	$\overline{RD}$ inactive to ALE High[3]	t_{CLCH}–3	—	t_{CLCH}–2	—	t_{CLCH}–2	—	ns
29	t_{RHAV}	$\overline{RD}$ inactive to AD address active [3]	t_{CLCL}–10=30	—	t_{CLCL}–5=20	—	t_{CLCL}–5=15	—	ns
59	t_{RHDX}	$\overline{RD}$ High to data hold on AD Bus[2]	3	—	2	—	0	—	ns
66	t_{AVRL}	A address valid to $\overline{RD}$ Low	$1.5t_{CLCL}$–15=45	—	$1.5t_{CLCL}$–10= 27.5	—	$1.5t_{CLCL}$–10=20	—	ns
67	t_{CHCSV}	CLKOUT High to $\overline{LCS}$/$\overline{UCS}$ valid	0	20	0	10	0	10	ns
68	t_{CHAV}	CLKOUT High to A address valid	0	20	0	10	0	10	ns

Notes:

1. All timing parameters are measured at V_{CC}/2 with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

2. If either specification 2 or specification 59 is met with respect to data hold time, then the device functions correctly.

3. Testing is performed with equal loading on referenced pins.

4. The timing of this signal is the same for a read cycle, whether it is configured to be $\overline{DEN}$ or $\overline{DS}$.

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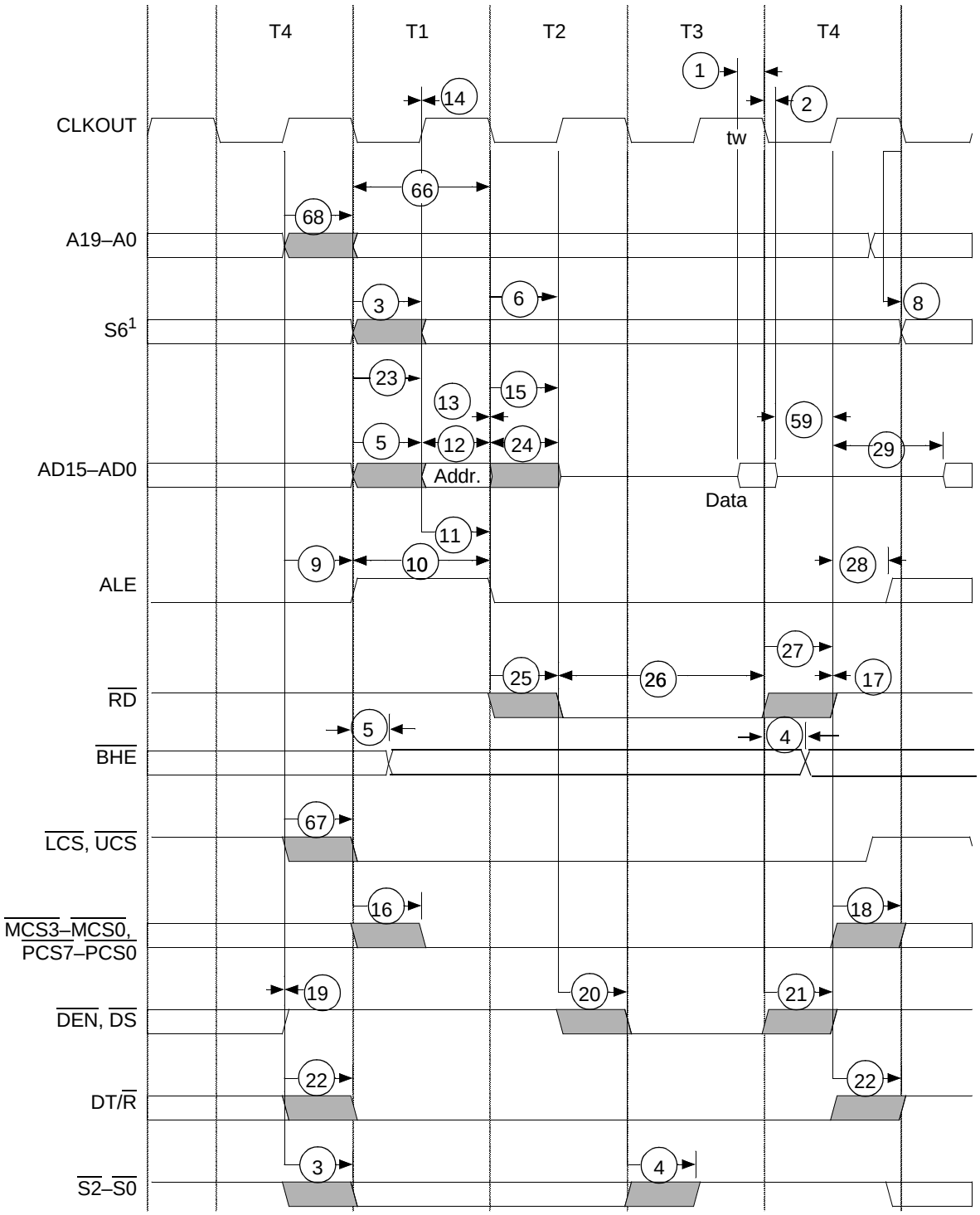

Notes:

1. S6 is not valid for the first fetch until the timing for parameter 3 (status active delay (t_{CHSV})) is met.

Figure 14. Read Cycle Waveforms

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Table 12. Write Cycle Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
General Timing Responses									
3	t_{CHSV}	Status active delay	0	20	0	12	0	10	ns
4	t_{CLSH}	Status and $\overline{BHE}$ inactive delay	0	20	0	12	0	10	ns
5	t_{CLAV}	AD address and $\overline{BHE}$ valid delay	0	20	0	12	0	10	ns
6	t_{CLAX}	Address hold	0	—	0	—	0	—	ns
7	t_{CLDV}	Data valid delay	0	20	0	12	0	10	ns
8	t_{CHDX}	Status hold time	0	—	0	—	0		ns
9	t_{CHLH}	ALE active delay	—	20	—	12	—	10	ns
10	t_{LHLL}	ALE width	t_{CLCL} – 10 = 30	—	t_{CLCL} – 5 = 20	—	t_{CLCL} – 5 = 15	—	ns
11	t_{CHLL}	ALE inactive delay	—	20	—	12	—	10	ns
12	t_{AVLL}	AD address valid to ALE Low[2]	0.5 • t_{CLCH}	—	0.5 • t_{CLCH}	—	0.5 • t_{CLCH}	—	ns
13	t_{LLAX}	AD address hold from ALE inactive	t_{CHCL}	—	t_{CHCL}	—	t_{CHCL}	—	ns
14	t_{AVCH}	AD address valid to clock High	0	—	0	—	0	—	ns
16	t_{CLCSV}	$\overline{MCSx}$/$\overline{PCSx}$ active delay	0	20	0	12	0	10	ns
17	t_{CXCSX}	$\overline{MCSx}$/$\overline{PCSx}$ hold from command inactive	t_{CLCH}	—	t_{CLCH}	—	t_{CLCH}	—	ns
18	t_{CHCSX}	$\overline{MCSx}$/$\overline{PCSx}$ inactive delay	0	20	0	12	0	10	ns
19	t_{DXDL}	$\overline{DEN}$ inactive to DT/$\overline{R}$[2, 3]	–1	—	–1	—	–1	—	ns
20	t_{CVCTV}	Control active delay 1[3,4]	0	20	0	12	0	10	ns
21	t_{CVDEX}	DS inactive delay[3,4]	0	20	0	12	0	10	ns
23	t_{LHAV}	ALE High to address valid	15	—	7.5	—	5	—	ns

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Table 12. Write Cycle Timing[1] (Continued)

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
Write Cycle Timing Responses									
30	t_{CLDOX}	Data hold time	0	—	0	—	0	—	ns
31	t_{CVCTX}	Control inactive delay[3,4]	0	20	0	12	0	10	ns
32	t_{WLWH}	$\overline{WR}$ pulse width	$2t_{CLCL} - 10 = 70$	—	$2t_{CLCL} - 10 = 40$	—	$2t_{CLCL} - 10 = 30$	—	ns
33	t_{WHLH}	$\overline{WR}$ inactive to ALE High[2]	$t_{CLCH} - 2$	—	$t_{CLCH} - 2$	—	$t_{CLCH} - 2$	—	ns
34	t_{WHDX}	Data hold after $\overline{WR}$[2]	$t_{CLCL} - 10 = 30$	—	$t_{CLCL} - 10 = 15$	—	$t_{CLCL} - 10 = 10$	—	ns
35	t_{WHDEX}	$\overline{WR}$ inactive to $\overline{DEN}$ inactive[2,3]	$t_{CLCH} - 3$	—	t_{CLCH}	—	t_{CLCH}	—	ns
65	t_{AVWL}	A address valid to $\overline{WR}$ Low	$t_{CLCL} + t_{CHCL} - 3$	—	$t_{CLCL} + t_{CHCL} - 1.25$	—	$t_{CLCL} + t_{CHCL} - 1.25$	—	ns
67	t_{CHCSV}	CLKOUT High to $\overline{LCS}$/$\overline{UCS}$ valid	0	20	0	10	0	10	ns
68	t_{CHAV}	CLKOUT High to A address valid	0	20	0	10	0	10	ns
87	t_{AVBL}	A address valid to $\overline{WHB}$, $\overline{WLB}$ Low	$t_{CHCL} - 3$	20	$t_{CHCL} - 1.25$	12	$t_{CHCL} - 1.25$	10	ns

Notes:

1. All timing parameters are measured at $V_{CC}/2$ with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

2. Testing is performed with equal loading on referenced pins.

3. The timing of this signal is different during a write cycle depending on whether it is configured to be $\overline{DEN}$ or $\overline{DS}$.

4. This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.

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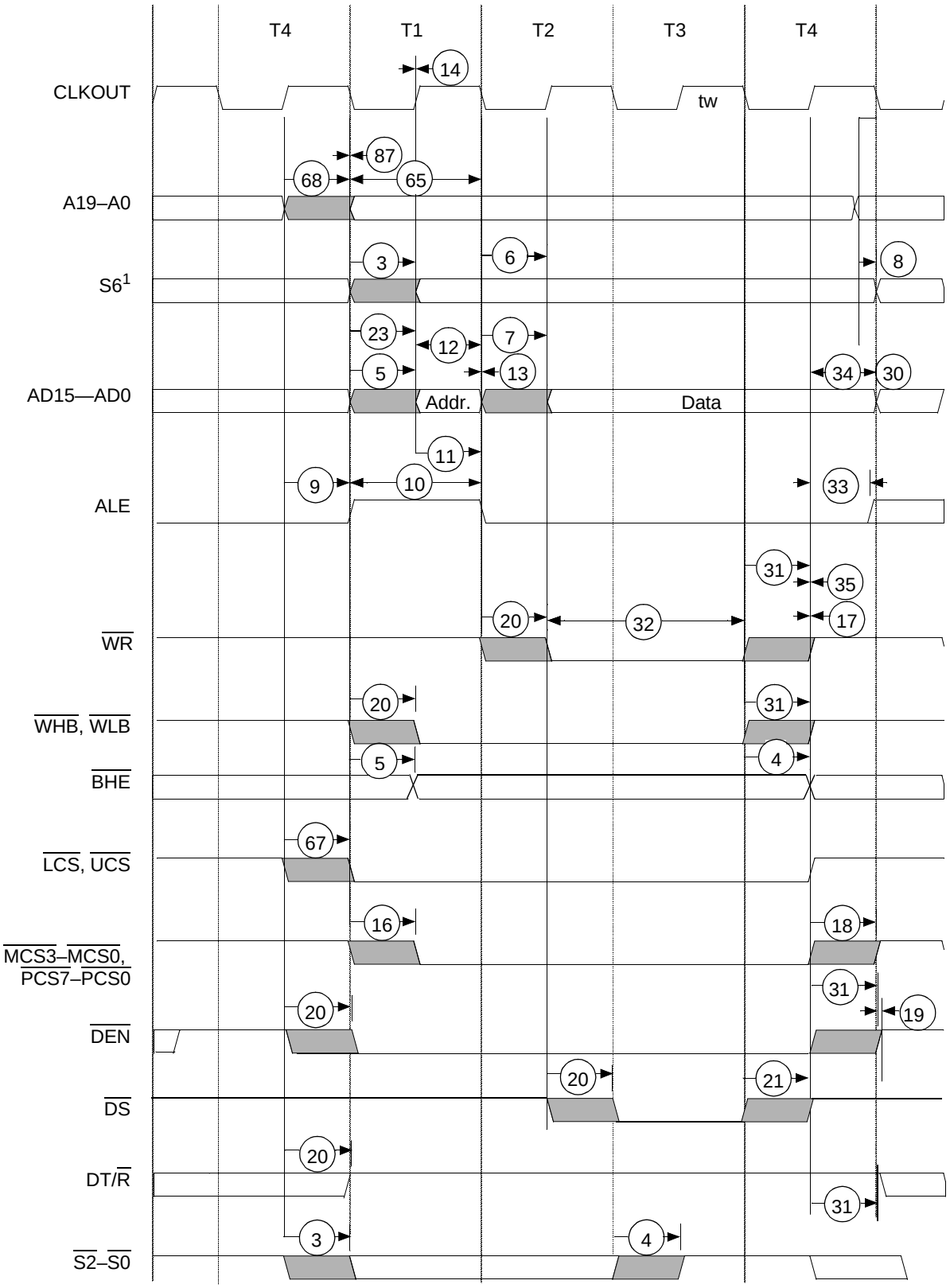

Notes:

1. S6 is not valid for the first fetch until the timing for parameter 3 (status active delay (t_{CHSV})) is met.

Figure 15. Write Cycle Waveforms

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Table 13. Software Halt Cycle Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
3	t_{CHSV}	Status active delay	0	20	0	12	0	10	ns
4	t_{CLSH}	Status inactive delay	0	20	0	12	0	10	ns
5	t_{CLAV}	AD address invalid delay	0	20	0	12	0	10	ns
9	t_{CHLH}	ALE active delay	—	20	—	12	—	10	ns
10	t_{LHLL}	ALE width	t_{CLCL} – 10 = 30	—	t_{CLCL} – 5 = 20	—	t_{CLCL} – 5 = 15	—	ns
11	t_{CHLL}	ALE inactive delay	—	20	—	12	—	10	ns
19	t_{DXDL}	$\overline{DEN}$ inactive to DT/$\overline{R}$ Low[2]	–1	—	–1	—	–1		ns
22	t_{CHCTV}	Control active delay 2[3]	0	20	0	12	0	10	ns
68	t_{CHAV}	CLKOUT High to A address invalid	0	20	0	12	0	10	ns

Notes:

1. All timing parameters are measured at V_{CC}/2 with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

2. Testing is performed with equal loading on referenced pins.

3. This parameter applies to the $\overline{DEN}$/$\overline{DS}$ signal.

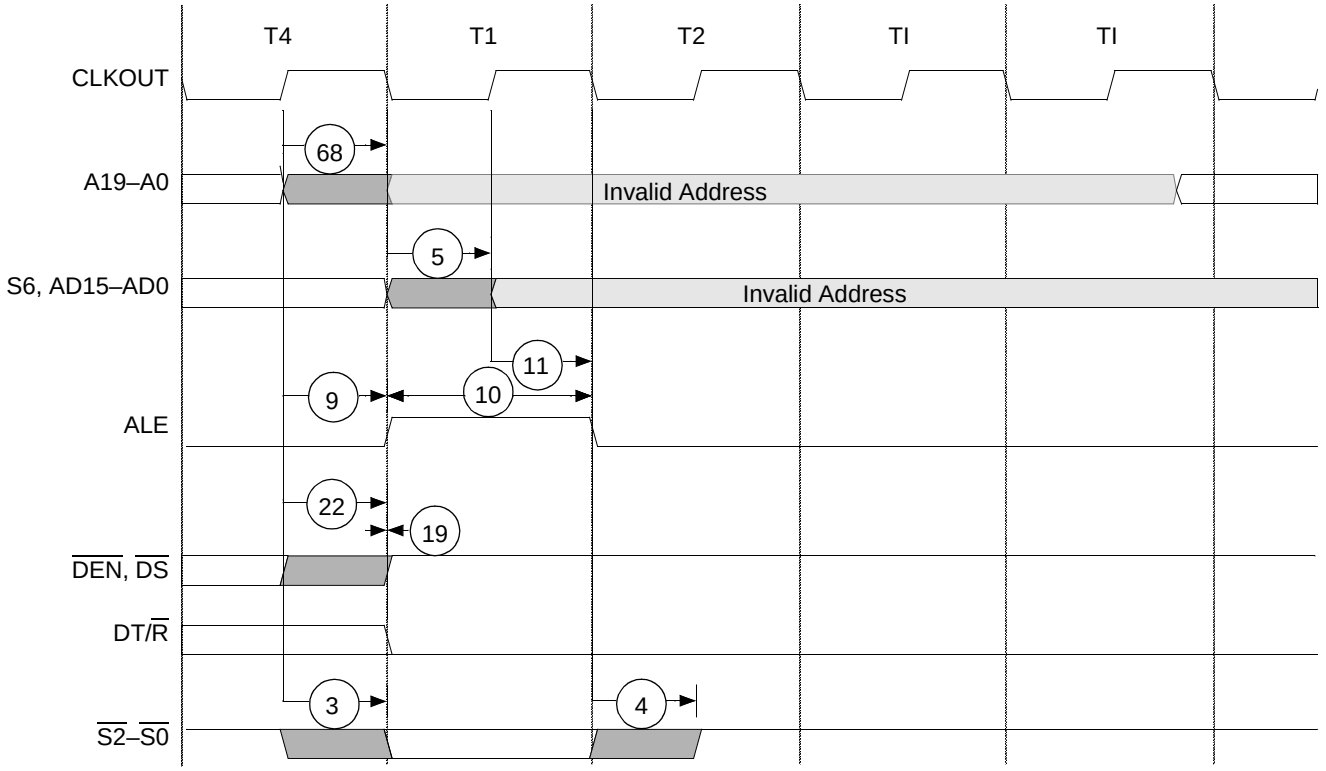

Figure 16. Software Halt Cycle Waveforms

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Table 14. Peripheral Timing[1, 2]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
53	t_{INVCH}	Peripheral setup time	10	—	5	—	5	—	ns
54	t_{CLTMV}	Timer output delay	—	25	—	15	—	12	ns
55	t_{CHQS0V}	Queue status 0 output delay	—	25	—	15	—	12	ns
56	t_{CHQS1V}	Queue status 1 output delay	—	25	—	15	—	12	ns

Notes:

1. All timing parameters are measured at $V_{CC}/2$ with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

2. PIO outputs change anywhere from the beginning of T3 to the first half of T4 of the bus cycle in which the PIO data register is written.

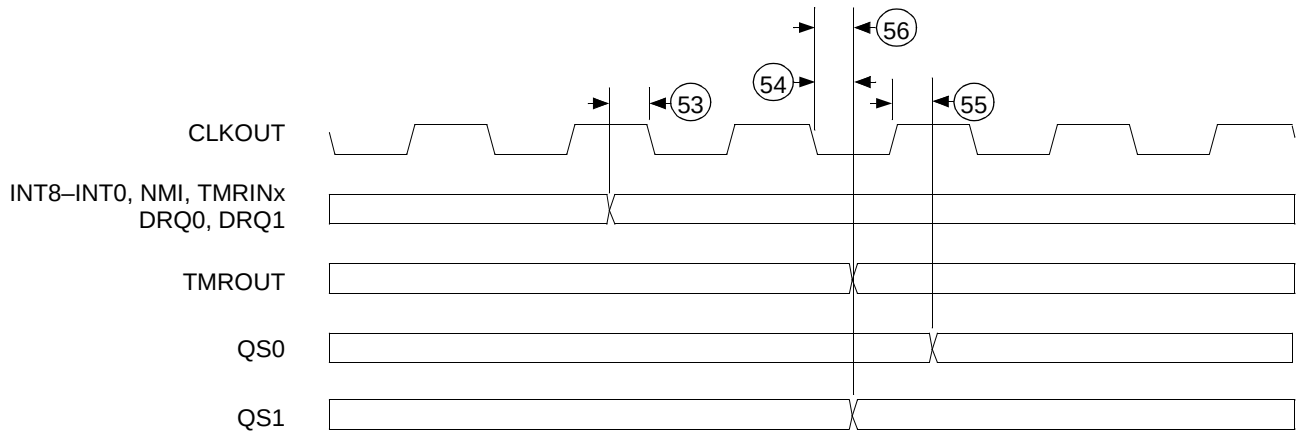

Figure 17. Peripheral Waveforms

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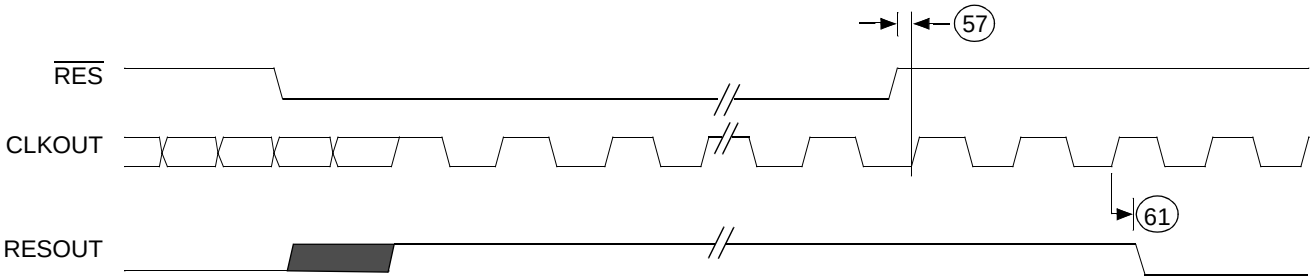
Table 15. Reset Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
57	t_{RESIN}	$\overline{RES}$ setup time	10	—	5	—	5	—	ns
61	t_{CLRO}	Reset delay	—	18	—	15	—	12	ns

Notes:

1. All timing parameters are measured at $V_{CC}/2$ with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.



Notes:

1. *$\overline{RES}$ must be held Low for 1 ms during power-up to ensure proper device initialization.*
2. *Diagram is shown for the system PLL in its 2x mode of operation.*
3. *Diagram assumes that V_{CC} is stable (i.e., 3.3 V ± 0.3 V) during the 1-ms $\overline{RES}$ active time.*

Figure 18. Reset Waveforms

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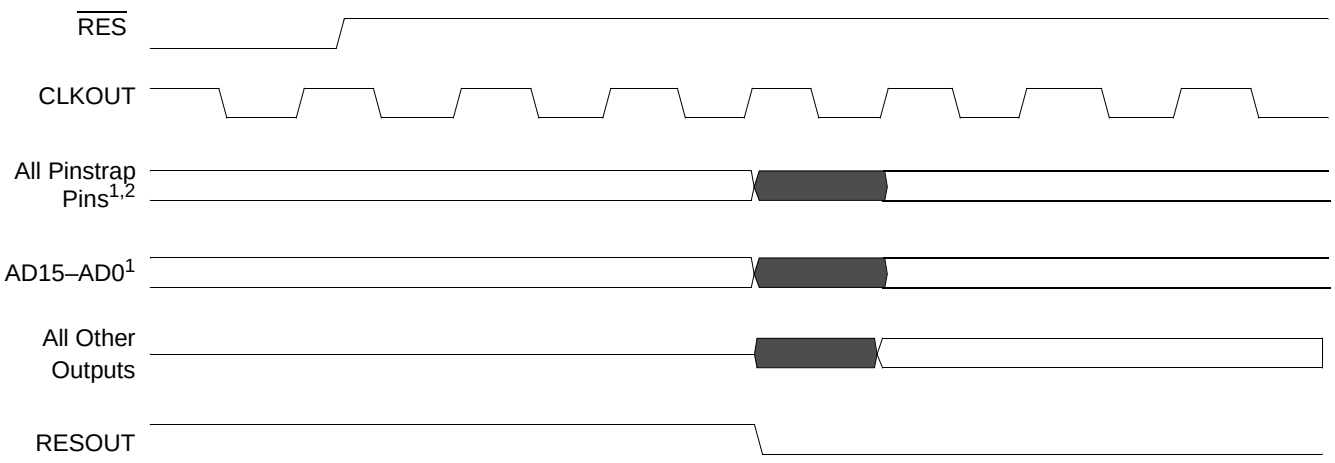
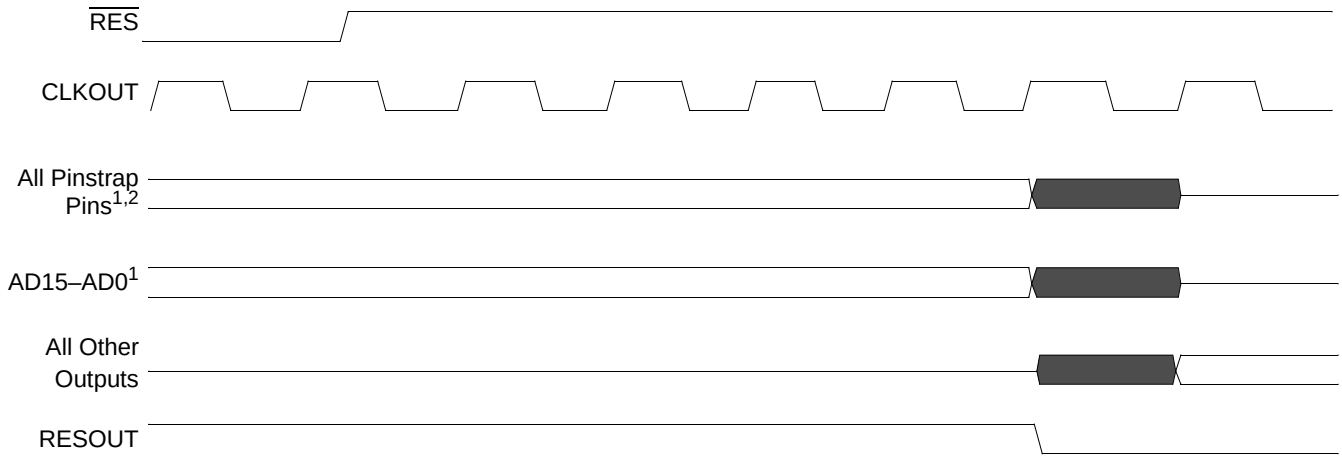


Notes:

1. *The pinstraps and AD bus are sampled during the assertion of RESOUT for system configuration purposes.*
2. *See Appendix A, "Reset Configuration Pins (Pinstraps)," on page A-8 for a list of all the pinstraps.*

Figure 19. Signals Related to Reset (System PLL in 1x or 2x Mode)



Notes:

1. *The pinstraps and AD bus are sampled during the assertion of RESOUT for system configuration purposes.*
2. *See Appendix A, "Reset Configuration Pins (Pinstraps)," on page A-8 for a list of all the pinstraps.*

Figure 20. Signals Related to Reset (System PLL in 4x Mode)

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Table 16. External Ready Cycle Timing[1]

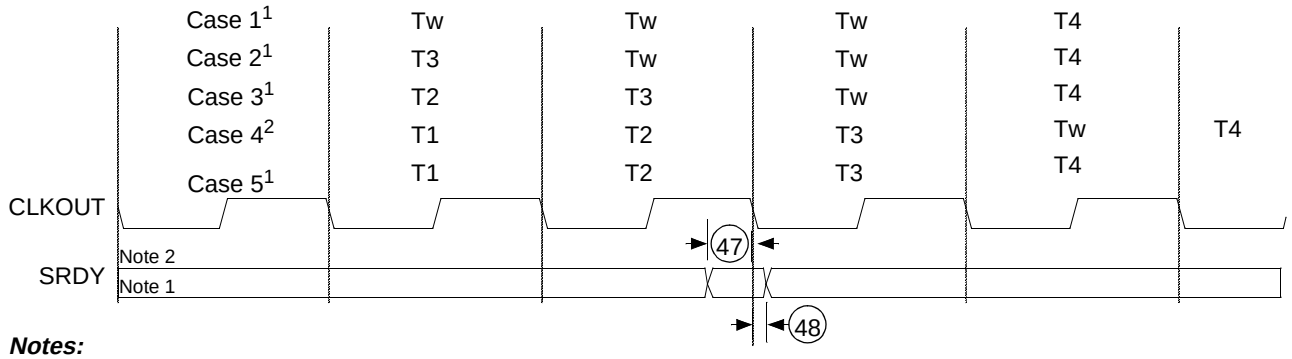
Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
Ready Timing Requirements									
47	t_{SRYCL}	SRDY transition setup time[2]	10	—	5	—	5	—	ns
48	t_{CLSRY}	SRDY transition hold time[2]	3	—	2	—	2	—	ns
49	t_{ARYCH}	ARDY resolution transition setup time[3]	10	—	5	—	5	—	ns
50	t_{CLARX}	ARDY active hold time[2]	4	—	3	—	3	—	ns
51	t_{ARYCHL}	ARDY inactive holding time	10	—	5	—	5	—	ns
52	t_{ARYLCL}	ARDY setup time[2]	15	—	5	—	5	—	ns

Notes:

1. All timing parameters are measured at V_{CC}/2 with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

2. This timing must be met to guarantee proper operation.

3. This timing must be met to guarantee recognition at the clock edge.



Notes:

1. Normally not ready system

2. Normally ready system

Figure 21. Synchronous Ready Waveforms

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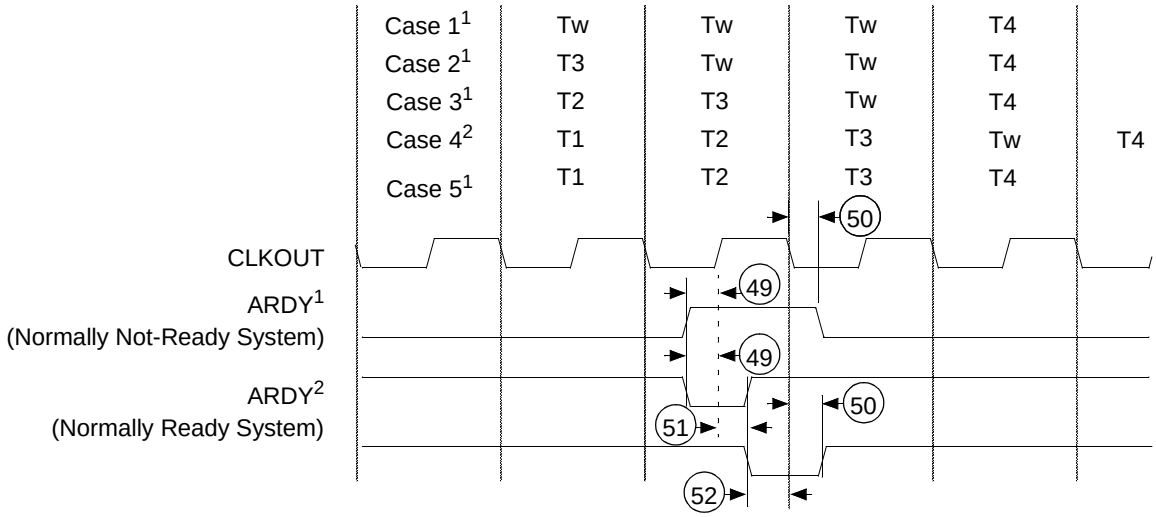

Notes:

1. *In a normally not ready system, wait states are added after T3 until t_{ARYCH} (49) and t_{CLARX} (50) are met.*
2. *In a normally ready system, a wait state is added if t_{ARYCH} (49) and t_{ARYCHL} (51) during T2 or t_{ARYLCL} (52) and t_{CLARX} (50) during T3 are met.*

Figure 22. Asynchronous Ready Waveforms

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Table 17. Bus Hold Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
5	t_{CLAV}	AD address valid delay	0	20	0	12	0	10	ns
15	t_{CLAZ}	AD address float delay	0	20	0	12	0	10	ns
18	t_{CHCSX}	$\overline{MCSx}$/$\overline{PCSx}$ inactive delay	0	20	0	12	0	10	ns
58	t_{HVCL}	HOLD setup[2]	10	—	5	—	5	—	ns
62	t_{CLHAV}	HLDA valid delay	0	20	0	12	0	10	ns
63	t_{CHCZ}	Command lines float delay	—	20	—	12	—	10	ns
64	t_{CHCV}	Command lines valid delay (after float)	—	25	—	12	—	10	ns

Notes:

1. All timing parameters are measured at V_{CC}/2 with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

2. This timing must be met to guarantee recognition at the next clock.

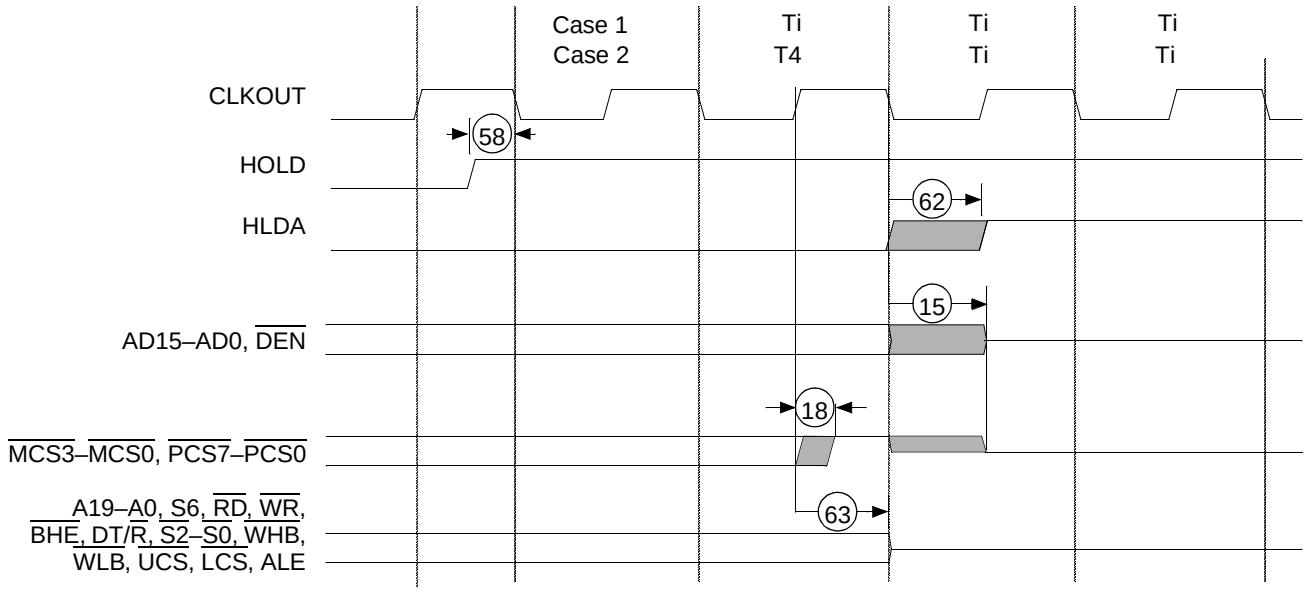

Figure 23. Entering Bus Hold Waveforms

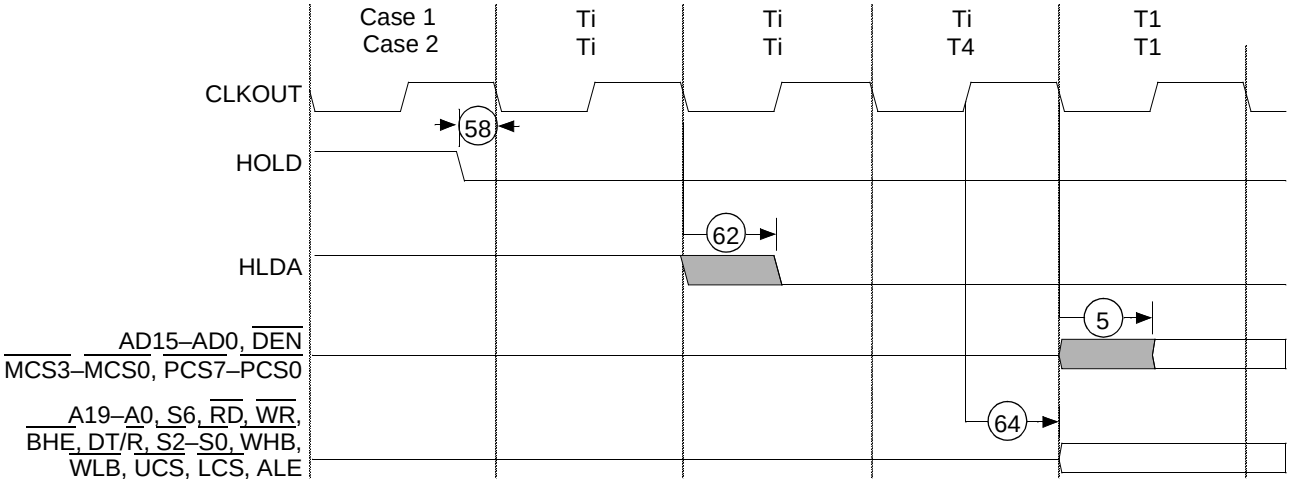

Figure 24. Exiting Bus Hold Waveforms

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Table 18. System Clocks Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
CLKIN Requirements for 4x PLL Mode									
36	t_{CKIN}	X1 period[2]	Not Supported		100	125	80	125	ns
37	t_{CLCK}	X1 Low time (1.5 V)			45	—	35	—	ns
38	t_{CHCK}	X1 High time (1.5 V)			45	—	35	—	ns
39	t_{CKHL}	X1 fall time (3.5 to 1.0 V)			—	5	—	5	ns
40	t_{CKLH}	X1 rise time (1.0 to 3.5 V)			—	5	—	5	ns
CLKIN Requirements for 2x PLL Mode									
36	t_{CKIN}	X1 period[2]	80	125	50	125	40	125	ns
37	t_{CLCK}	X1 Low time (1.5 V)	35	—	20	—	15	—	ns
38	t_{CHCK}	X1 High time (1.5 V)	35	—	20	—	15	—	ns
39	t_{CKHL}	X1 fall time (3.5 to 1.0 V)	—	5	—	5	—	5	ns
40	t_{CKLH}	X1 rise time (1.0 to 3.5 V)	—	5	—	5	—	5	ns
CLKIN Requirements for 1x PLL Mode									
36	t_{CKIN}	X1 period[2]	40	60	25	60	Not Supported		ns
37	t_{CLCK}	X1 Low time (1.5 V)	15	—	7.5	—			ns
38	t_{CHCK}	X1 High time (1.5 V)	15	—	7.5	—			ns
39	t_{CKHL}	X1 fall time (3.5 to 1.0 V)	—	5	—	5			ns
40	t_{CKLH}	X1 rise time (1.0 to 3.5 V)	—	5	—	5			ns
CLKOUT Timing[3]									
42	t_{CLCL}	CLKOUT period	40	—	25	—	20	—	ns
43	t_{CLCH}	CLKOUT Low time (C_L = 50 pF)	$0.5t_{CLCL}-2$ =18	—	$0.5t_{CLCL}-1.25$ =11.25	—	$0.5t_{CLCL}-1$ = 9	—	ns
44	t_{CHCL}	CLKOUT High time (C_L = 50 pF)	$0.5t_{CLCL}-2$ =18	—	$0.5t_{CLCL}-1.25$ =11.25	—	$0.5t_{CLCL}-1$ = 9	—	ns
45	t_{CH1CH2}	CLKOUT rise time (1.0 to 3.5 V)	—	3	—	3	—	3	ns
46	t_{CL2CL1}	CLKOUT fall time (3.5 to 1.0 V)	—	3	—	3	—	3	ns
69	t_{CICO}	X1 to CLKOUT skew	—	10	—	10	—	10	ns

Notes:

1. *All timing parameters are measured at $V_{CC}/2$ with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.*
2. *Testing is performed with equal loading on referenced pins.*
3. *The PLL requires a maximum of 1 ms to achieve lock after all other operating conditions (V_{CC}) are stable, which is normally achieved by holding $\overline{RES}$ active for at least 1 ms.*

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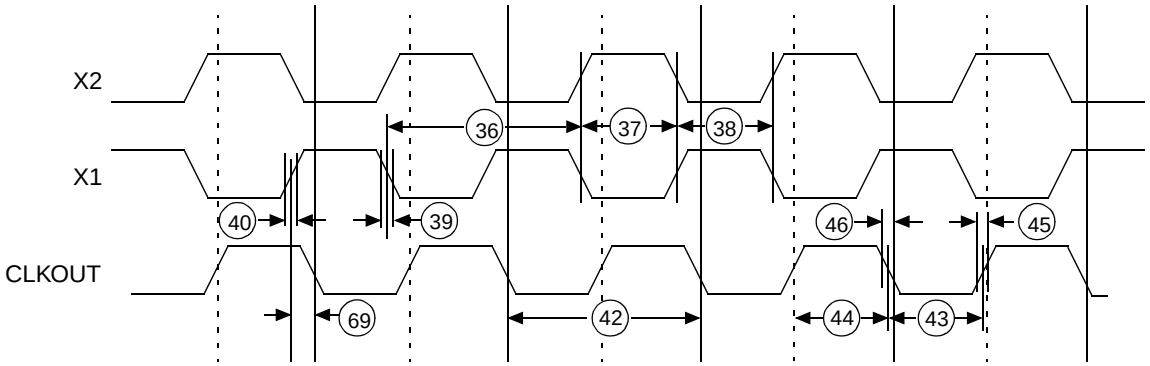

Figure 25. System Clocks Waveforms—Active Mode (PLL 1x Mode)

Table 19. USB Clocks Timing[1]

Parameter			Preliminary 48 MHz		Unit
No.	Symbol	Description	Min	Max	
CLKIN Requirements for 4x PLL Mode					
1	t_{UCKIN}	USBX1 period	80	85	ns
2	t_{UCLCK}	USBX1 Low time (1.5 V)	35	—	ns
3	t_{UCHCK}	USBX1 High time (1.5 V)	35	—	ns
4	t_{UCKHL}	USBX1 fall time (3.5 to 1.0 V)	—	5	ns
5	t_{UCKLH}	USBX1 rise time (1.0 to 3.5 V)	—	5	ns
CLKIN Requirements for 2x PLL Mode					
1	t_{UCKIN}	USBX1 period	40	42	ns
2	t_{UCLCK}	USBX1 Low time (1.5 V)	15	—	ns
3	t_{UCHCK}	USBX1 High time (1.5 V)	15	—	ns
4	t_{UCKHL}	USBX1 fall time (3.5 to 1.0 V)	—	5	ns
5	t_{UCKLH}	USBX1 rise time (1.0 to 3.5 V)	—	5	ns

Notes:

1. All timing parameters are measured at V_{CC}/2 with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

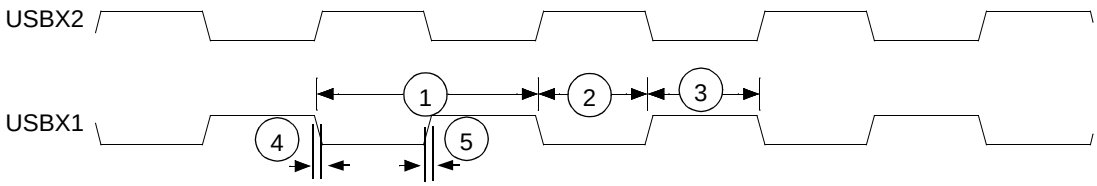

Figure 26. USB Clocks Waveforms

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Table 20. USB Timing[1, 2]

Parameter			Preliminary 48 MHz		Unit
No.	Symbol	Description	Min	Max	
1	t_R	Rise time (Cl = 50 pF)	4 ns	20 ns	ns
2	t_F	Fall time (Cl = 50 pF)	4 ns	20 ns	ns
3	t_{JR1}	Consecutive transition jitter (measured at crossover point)	–18.5 ns	18.5 ns	ns
4	t_{JR2}	Paired transition jitter (measured at crossover point)	–9 ns	9 ns	ns

Notes:

1. All timing parameters are measured at V_{CC}/2 with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

2. Parameters 3 (t_{JR1}) and 4 (t_{JR2}) show jitter for the receiver, not the transmitter, See the USB version 1.0 specification for more details.

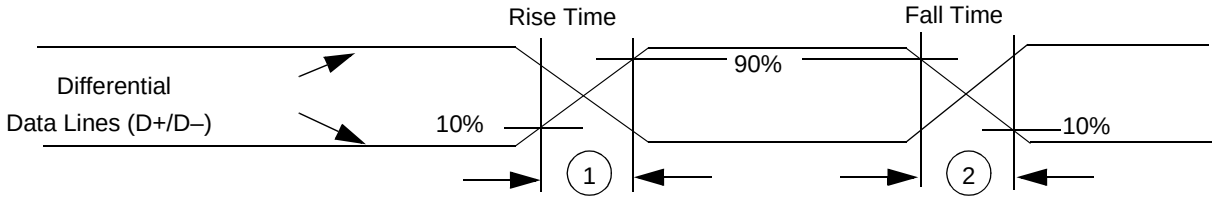

Figure 27. USB Data Signal Rise and Fall Times

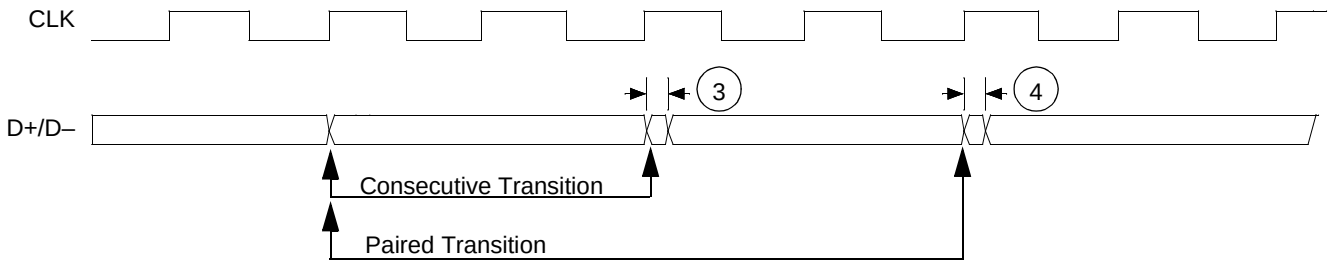

Figure 28. USB Receiver Jitter Tolerance

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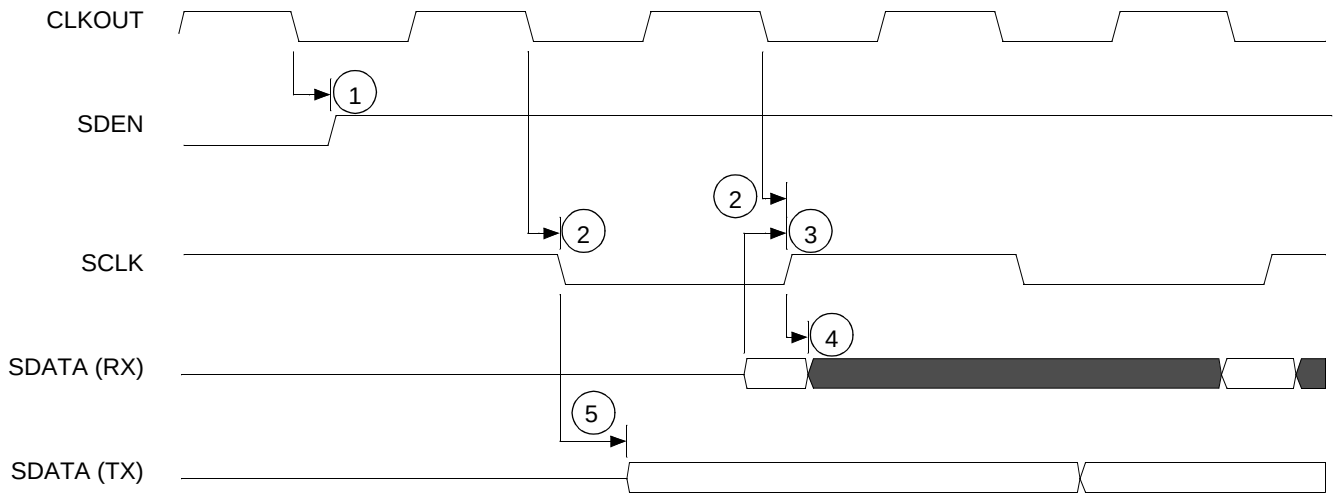
Table 21. SSI Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
1	t_{CLEV}	CLKOUT Low to SDEN valid	0	20	0	12	0	10	ns
2	t_{CLSL}	CLKOUT Low to SCLK Low	0	20	0	15	0	12	ns
3	t_{DVSH}	Data valid to SCLK High	10	—	5	—	5	—	ns
4	t_{SHDX}	SCLK High to data invalid	3	—	2	—	2	—	ns
5	t_{SLDV}	SCLK Low to data valid	—	20	—	12	—	10	ns

Notes:

1. All timing parameters are measured at V_{CC}/2 with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.



Notes:

1. SDEN is configured to be active High.
2. SCLK is configured to be CLKOUT/2.
3. Waveforms are shown for "normal" clock mode (i.e., transmit on negative edge of SCLK and receive on positive edge of SCLK).

Figure 29. SSI Waveforms

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Table 22. DRAM Timing[1]

Parameter			Preliminary						Unit
			25 MHz		40 MHz		50 MHz (Commercial Only)		
No.	Symbol	Description	Min	Max	Min	Max	Min	Max	
1	t_{DVCL}	Data in setup	10	—	5	—	5	—	ns
2	t_{CLDX}	Data in hold	3	—	2	—	2	—	ns
5	t_{CLAV}	AD address valid delay	0	20	0	12	0	10	ns
7	t_{CLDV}	Data valid delay	0	20	0	12	0	10	ns
15	t_{CLAZ}	AD address float delay	0	20	0	12	0	10	ns
20	t_{CVCTV}	Control active delay 1	0	20	0	12	0	10	ns
25	t_{CLRL}	$\overline{RD}$ active delay	0	20	0	12	0	10	ns
27	t_{CLRH}	$\overline{RD}$ inactive delay	0	20	0	12	0	10	ns
30	t_{CLDOX}	Data hold time	0	—	0	—	0	—	ns
31	t_{CVCTX}	Control inactive delay	0	20	0	12	0	10	ns
68	t_{CHAV}	CLKOUT High to A address valid	0	20	0	12	0	10	ns
402	t_{COLV}	Column address valid delay	0	20	0	12	0	10	ns
403	t_{CHRAS}	Change in $\overline{RAS}$ delay	3	20	3	12	3	10	ns
404	t_{CHCAS}	Change in $\overline{CAS}$ delay	3	20	3	12	3	10	ns

Notes:

1. All timing parameters are measured at $V_{CC}/2$ with 50-pF loading on CLKOUT unless otherwise noted. All output test conditions are with the load values shown in Table 29, "Pin List Summary," on page A-10.

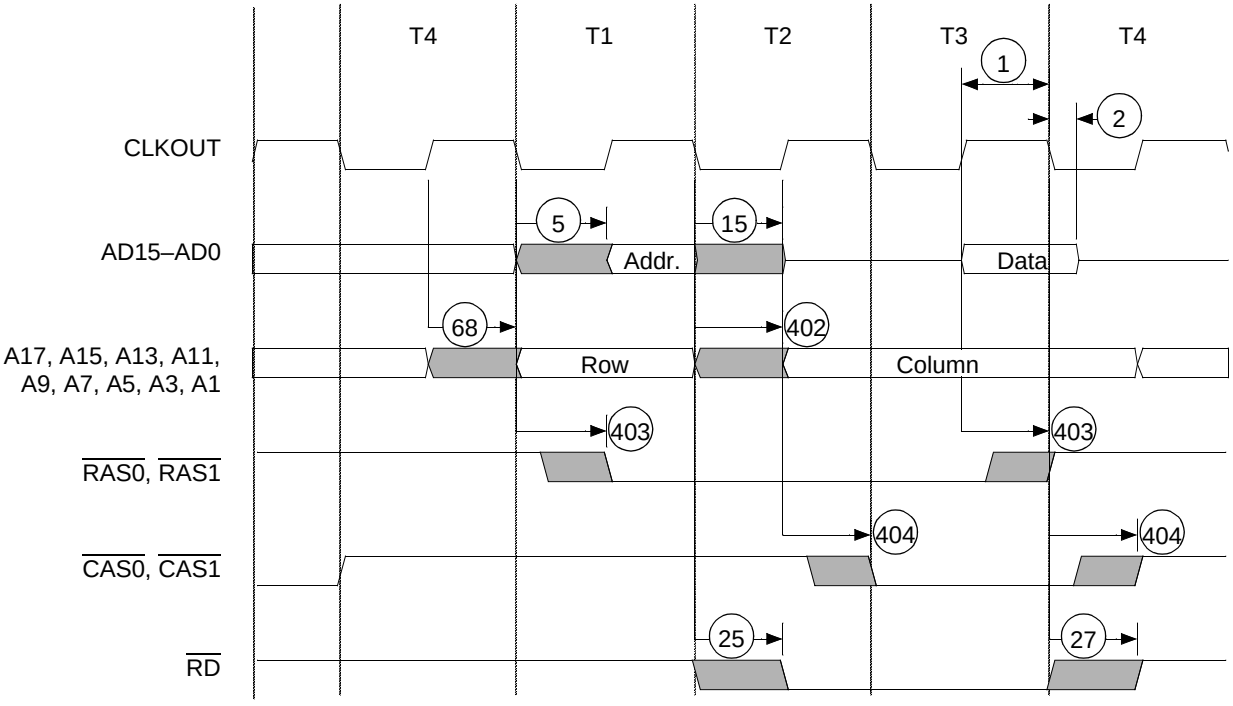

Figure 30. DRAM Read Cycle without Wait States Waveform

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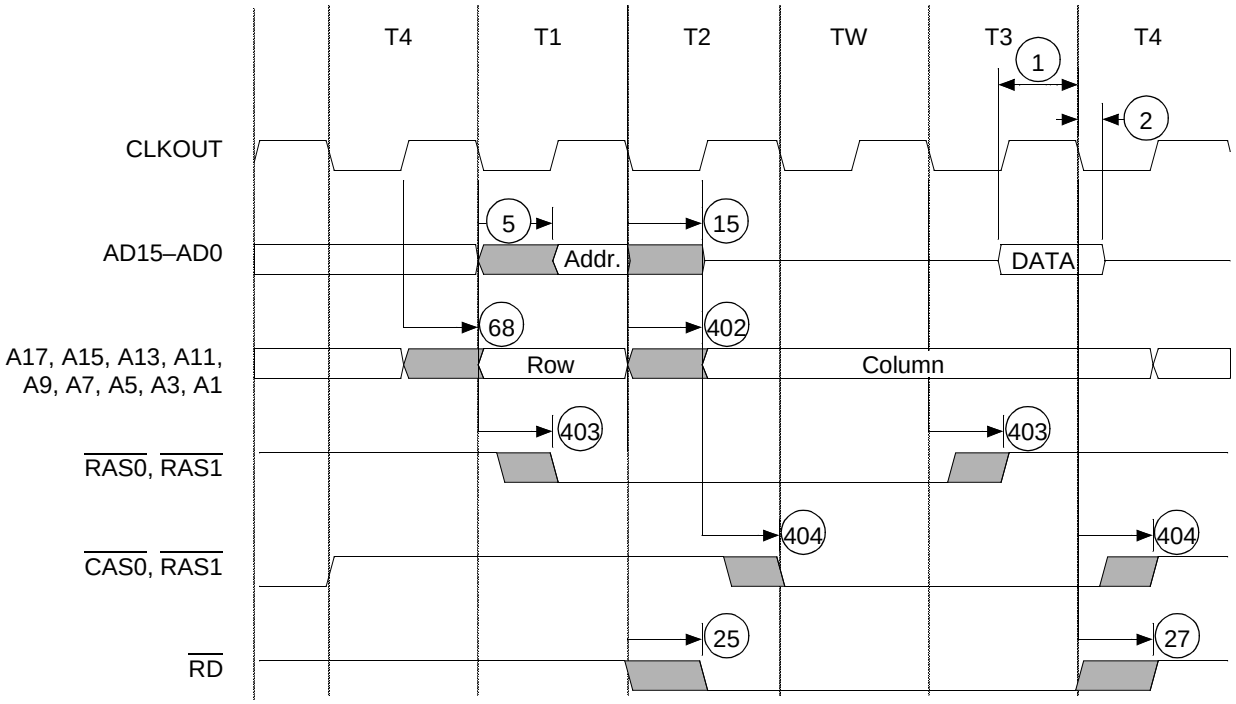

Figure 31. DRAM Read Cycle with Wait States Waveform

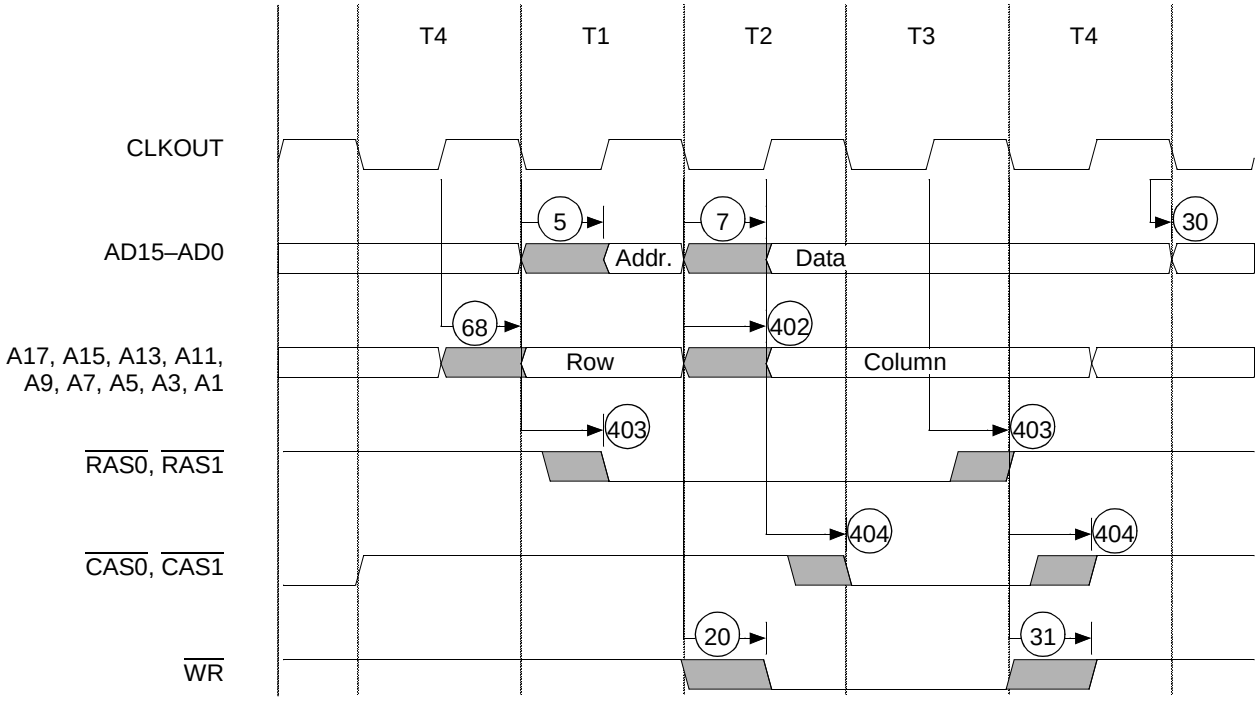

Figure 32. DRAM Write Cycle without Wait States Waveform

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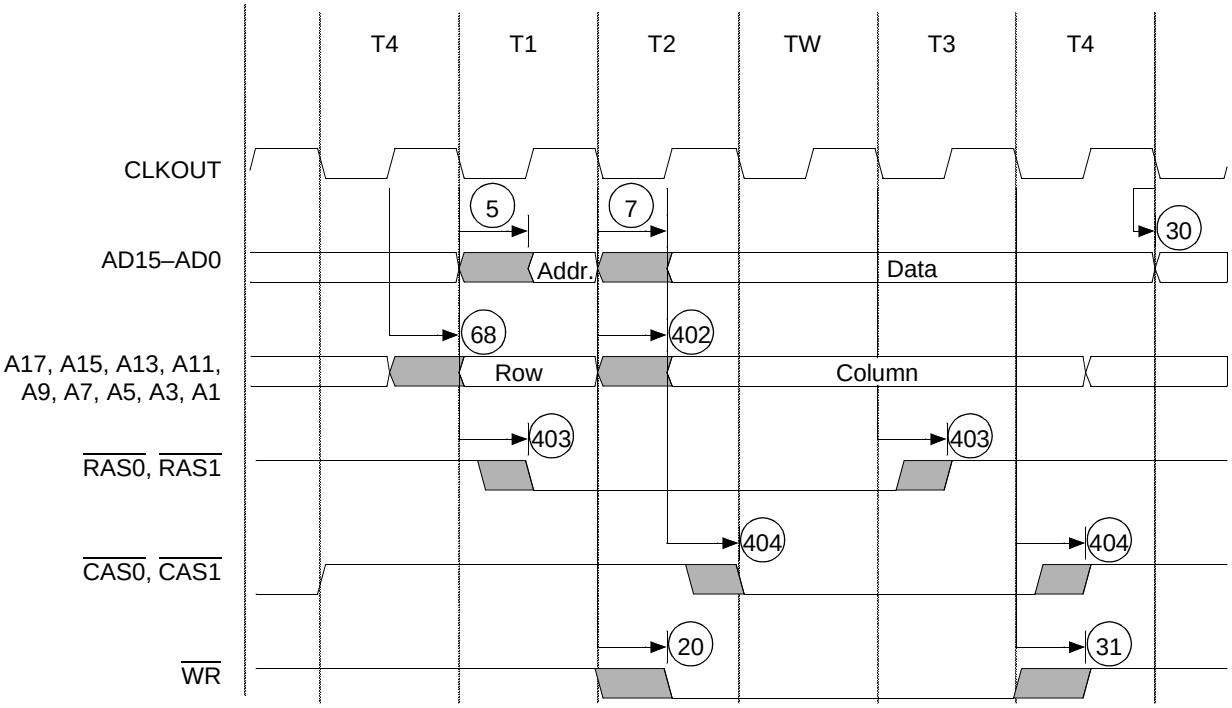

Figure 33. DRAM Write Cycle with Wait States Waveform

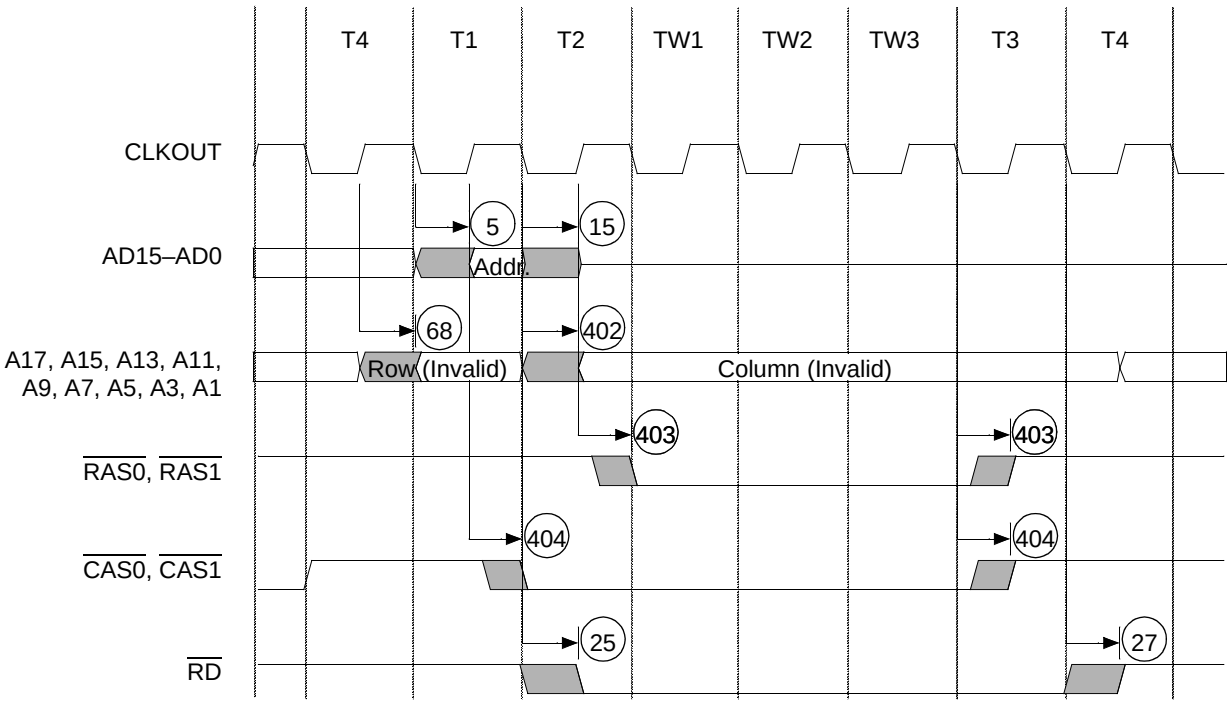

Figure 34. DRAM Refresh Cycle Waveform

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APPENDIX A—PIN TABLES

This appendix contains pin tables for the Am186CU USB microcontroller. Several different tables are included with the following characteristics:

- Power-on reset (POR) pin defaults including pin numbers and multiplexed functions—Table 23 on page A-2.
- Multiplexed signal tradeoffs—Table 24 on page A-5.
- Programmable I/O pins ordered by PIO pin number and multiplexed signal name, respectively, including pin numbers, multiplexed functions, and pin configurations following system reset—Table 25 on page A-6 and Table 26 on page A-7.
- Pinstraps and pinstrap options—Table 27 on page A-8.
- Pin and signal summary showing signal name and alternate function, pin number, I/O type, maximum load values, POR default function, reset state, POR default operation, hold state, and voltage column—Table 29 on page A-10.

For pin tables showing pins sorted by pin number and signal name, respectively, see Table 1, “PQFP Pin Assignments—Sorted by Pin Number” on page 10 and Table 2, “PQFP Pin Assignments—Sorted by Signal Name” on page 11.

For signal descriptions, see Table 4, “Signal Descriptions” on page 13.

In all tables the brackets, [ ], indicate alternate, multiplexed functions, and braces, { }, indicate reset configuration pins (pinstraps). The line over a pin name indicates an active Low. The word pin refers to the physical wire; the word signal refers to the electrical signal that flows through it.

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Table 23. Power-On Reset (POR) Pin Defaults[1]

POR Default	Pin Number	Multiplexed Signal	Multiplexed Signal	Multiplexed Signal	PIO	Pinstrap
Bus Interface Unit						
A0	30	—	—	—	—	—
A1	31	—	—	—	—	—
A2	32	—	—	—	—	—
A3	36	—	—	—	—	—
A4	37	—	—	—	—	—
A5	42	—	—	—	—	—
A6	43	—	—	—	—	—
A7	44	—	—	—	—	—
A8	45	—	—	—	—	—
A9	49	—	—	—	—	—
A10	50	—	—	—	—	—
A11	64	—	—	—	—	—
A12	65	—	—	—	—	—
A13	69	—	—	—	—	—
A14	70	—	—	—	—	—
A15	84	—	—	—	—	—
A16	85	—	—	—	—	—
A17	88	—	—	—	—	—
A18	89	—	—	—	—	—
A19	90	—	—	—	—	—
AD0	28	—	—	—	—	—
AD1	34	—	—	—	—	—
AD2	38	—	—	—	—	—
AD3	46	—	—	—	—	—
AD4	51	—	—	—	—	—
AD5	66	—	—	—	—	—
AD6	86	—	—	—	—	—
AD7	92	—	—	—	—	—
AD8	29	—	—	—	—	—
AD9	35	—	—	—	—	—
AD10	39	—	—	—	—	—
AD11	47	—	—	—	—	—
AD12	52	—	—	—	—	—
AD13	67	—	—	—	—	—
AD14	87	—	—	—	—	—
AD15	93	—	—	—	—	—
ALE	19	—	—	—	PIO33	—
ARDY	14	—	—	—	PIO8	—
$\overline{\text{BHE}}$	20	—	—	—	PIO34	{$\overline{\text{ADEN}}$}
$\overline{\text{BSIZE8}}$	94	—	—	—	—	—
$\overline{\text{DEN}}$	18	$\overline{\text{DS}}$	—	—	PIO30	—
DRQ1	105	—	—	—	—	—
DT/$\overline{\text{R}}$	17	—	—	—	PIO29	—
HLDA	98	—	—	—	—	—
HOLD	99	—	—	—	—	{CLKSEL1}
$\overline{\text{RD}}$	97	—	—	—	—	—
$\overline{\text{S0}}$	57	—	—	—	—	{$\overline{\text{USBXCVR}}$}
$\overline{\text{S1}}$	56	—	—	—	—	—
$\overline{\text{S2}}$	55	—	—	—	—	—

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Table 23. Power-On Reset (POR) Pin Defaults[1] (Continued)

POR Default	Pin Number	Multiplexed Signal	Multiplexed Signal	Multiplexed Signal	PIO	Pinstrap
S6	54	—	—	—	—	—
SRDY	15	—	—	—	PIO35	—
$\overline{WHB}$	95	—	—	—	—	—
$\overline{WLB}$	96	—	—	—	—	—
$\overline{WR}$	16	—	—	—	PIO15	—
Chip Selects						—
$\overline{LCS}$	131	$\overline{RAS0}$	—	—	—	—
$\overline{MCS1}$	127	$\overline{CAS1}$	—	—	—	—
$\overline{MCS2}$	128	$\overline{CAS0}$	—	—	—	—
$\overline{PCS0}$	5	—	—	—	PIO13	{USBSEL1}
$\overline{PCS1}$	6	—	—	—	PIO14	{USBSEL2}
$\overline{PCS2}$	7	—	—	—	—	—
$\overline{PCS3}$	8	—	—	—	—	—
$\overline{UCS}$	132	—	—	—	—	{$\overline{ONCE}$}
Reset/Clocks						
CLKOUT	60	—	—	—	—	—
$\overline{RES}$	114	—	—	—	—	—
RESOUT	58	—	—	—	—	—
USBX1	75	—	—	—	—	—
USBX2	76	—	—	—	—	—
X1	73	—	—	—	—	—
X2	74	—	—	—	—	—
Interrupts						
INT0	107	—	—	—	—	—
INT1	109	—	—	—	—	—
INT2	110	—	—	—	—	—
INT3	111	—	—	—	—	—
INT4	112	—	—	—	—	—
INT5	113	—	—	—	—	—
NMI	115	—	—	—	—	—
High-Speed UART						
TXD_HU	26	—	—	—	—	—
Debug Support						
QS0	62	—	—	—	—	—
QS1	63	—	—	—	—	—
Universal Serial Bus						
USBD+	81	UDPLS	—	—	—	—
USBD-	80	UDMNS	—	—	—	—
PIOs						
PIO0	144	TMRIN1	—	—		—
PIO1	143	TMROUT1	—	—		—
PIO2	10	$\overline{PCS5}$	—	—		—
PIO3	9	$\overline{PCS4}$	—	—		{CLKSEL2}
PIO4	126	$\overline{MCS0}$	—	—		{$\overline{UCSX8}$}
PIO5	129	$\overline{MCS3}$	$\overline{RAS1}$	—		—
PIO6	147	INT8	PWD	—		—
PIO7	146	INT7	—	—		—
PIO9	124	DRQ0	—	—		—
PIO10	2	SDEN	—	—		—
PIO11	3	SCLK	—	—		—

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Table 23. Power-On Reset (POR) Pin Defaults[1] (Continued)

POR Default	Pin Number	Multiplexed Signal	Multiplexed Signal	Multiplexed Signal	PIO	Pinstrap
PIO12	4	SDATA	—	—		—
PIO16	25	RXD_HU	—	—		—
PIO17	123	—	—	—		—
PIO18	122	—	—	—		—
PIO19	145	INT6	—	—		—
PIO20	159	TXD_U	—	—		—
PIO21	22	UCLK	USBSOF	USBSCI		—
PIO22	150	—	—	—		—
PIO23	149	—	—	—		—
PIO24	157	$\overline{\text{CTS\_U}}$	—	—		—
PIO25	156	$\overline{\text{RTR\_U}}$	—	—		—
PIO26	158	RXD_U	—	—		—
PIO27	142	TMRIN0	—	—		—
PIO28	141	TMROUT0	—	—		—
PIO31	13	$\overline{\text{PCS7}}$	—	—		—
PIO32	11	$\overline{\text{PCS6}}$	—	—		—
PIO36	138	—	—	—		—
PIO37	139	—	—	—		—
PIO38	137	—	—	—		—
PIO39	136	—	—	—		—
PIO40	135	—	—	—		—
PIO41	134	—	—	—		—
PIO42	153	—	—	—		—
PIO43	154	—	—	—		—
PIO44	152	—	—	—		—
PIO45	151	—	—	—		—
PIO46	24	$\overline{\text{CTS\_HU}}$	—	—		—
PIO47	23	$\overline{\text{RTR\_HU}}$	—	—		—
Reserved						
RSVD_104	104	UXVRCV	—	—	—	—
RSVD_103	103	$\overline{\text{UXVOE}}$	—	—	—	—
RSVD_102	102	UTXDMNS	—	—	—	—
RSVD_101	101	UTXDPLS	—	—	—	—
RSVD_119	119	—	—	—	—	—
RSVD_118	118	—	—	—	—	—
RSVD_117	117	—	—	—	—	—
RSVD_116	116	—	—	—	—	—

Notes:

1. For default reset functions and pin states refer to Table 29, "Pin List Summary," on page A-10.

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Table 24. Multiplexed Signal Trade-Offs

DESIRED FUNCTION			LOST FUNCTION							
Interface	**Name**	**Pin**	**Interface**	**Name**	**Interface**	**Name**	**Interface**	**Name**	**Interface**	**Name**
Memory										
SRAM	$\overline{LCS}$	131	DRAM	$\overline{RAS0}$	—	—	—	—	PIO	—
	$\overline{MCS1}$	127		$\overline{CAS1}$	—	—	—	—		—
	$\overline{MCS2}$	128		$\overline{CAS0}$	—	—	—	—		—
	MCS3	129		$\overline{RAS1}$	—	—	—	—		PIO5
DRAM	$\overline{CAS0}$	128	SRAM	$\overline{MCS2}$	—	—	—	—	—	—
	$\overline{CAS1}$	127		$\overline{MCS1}$	—	—	—	—	—	—
	$\overline{RAS0}$	131		$\overline{LCS}$	—	—	—	—	—	—
	$\overline{RAS1}$	129		$\overline{MCS3}$	—	—	—	—	—	PIO5
Miscellaneous										
Bus Interface	$\overline{DEN}$	18	Bus Interface	$\overline{DS}$	—	—	—	—	—	PIO30
	$\overline{DS}$	18		$\overline{DEN}$	—	—	—	—	—	PIO30
Clocks	UCLK	22	Clocks	USBSOF	Clocks	USBSCI	—	—	PIO	PIO21
	USBSOF	22		UCLK		USBSCI	—	—		PIO21
	USBSCI	22		UCLK		USBSOF	—	—		PIO21
PIOs										
	PIO0	144		TMRIN1		—		—		
	PIO1	143		TMROUT1		—		—		
	PIO2	10		PCS5		—		—		
	PIO3	9		PCS4		—		—		
	PIO4	126		MCS0		—		—		
	PIO5	129		MCS3		RAS1		—		
	PIO6	147		INT8		PWD		—		
	PIO7	146		INT7		—		—		
	PIO8	14		ARDY		—		—		
	PIO9	124		DRQ0		—		—		
	PIO10	2		SDEN		—		—		
	PIO11	3		SCLK		—		—		
	PIO12	4		SDATA		—		—		
	PIO13	5		PCS0		—		—		
	PIO14	6		PCS1		—		—		
	PIO15	16		WR		—		—		
	PIO16	25		RXD_HU		—		—		
	PIO19	145		INT6		—		—		
	PIO20	159		TXD_U		—		—		
	PIO21	22		UCLK		USBSOF		USBSCI		
	PIO24	157		CTS_U		—		—		
	PIO25	156		RTR_U		—		—		
	PIO26	158		RXD_U		—		—		
	PIO27	142		TMRIN0		—		—		
	PIO28	141		TMROUT0		—		—		
	PIO29	17		$DT/\overline{R}$		—		—		
	PIO30	18		DEN		DS		—		
	PIO31	13		PCS7		—		—		
	PIO32	11		PCS6		—		—		
	PIO33	19		ALE		—		—		
	PIO34	20		BHE		—		—		
	PIO35	15		SRDY		—		—		
	PIO46	24		CTS_HU		—		—		
	PIO47	23		RTR_HU		—		—		

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Table 25. PIOs Sorted by PIO Number

PIO No.	Pin No.	Multiplexed Signal	Multiplexed Signal	Multiplexed Signal	Pin Configuration Following System Reset[1]
PIO0	144	TMRIN1	—	—	Input with pullup
PIO1	143	TMROUT1	—	—	Input with pulldown
PIO2	10	PCS5	—	—	Input with pullup
PIO3	9	PCS4	—	—	Input with pullup
PIO4	126	MCS0	—	—	Input with pullup
PIO5	129	MCS3	RAS1	—	Input with pullup
PIO6	147	INT8	PWD	—	Input with pullup
PIO7	146	INT7	—	—	Input with pullup
PIO8	14	ARDY	—	—	Alternate operation[2]
PIO9	124	DRQ0	—	—	Input with pulldown
PIO10	2	SDEN	—	—	Input with pulldown
PIO11	3	SCLK	—	—	Input with pullup
PIO12	4	SDATA	—	—	Input with pullup
PIO13	5	PCS0	—	—	Alternate operation[2]
PIO14	6	PCS1	—	—	Alternate operation[2]
PIO15	16	WR	—	—	Alternate operation[2]
PIO16	25	RXD_HU	—	—	Input with pullup
PIO17	123	—	—	—	Input with pullup
PIO18	122	—	—	—	Input with pullup
PIO19	145	INT6	—	—	Input with pullup
PIO20	159	TXD_U	—	—	Input with pullup
PIO21	22	UCLK	USBSOF	USBSCI	Input with pullup
PIO22	150	—	—	—	Input with pulldown
PIO23	149	—	—	—	Input with pulldown
PIO24	157	CTS_U	—	—	Input with pullup
PIO25	156	RTR_U	—	—	Input with pullup
PIO26	158	RXD_U	—	—	Input with pullup
PIO27	142	TMRIN0	—	—	Input with pullup
PIO28	141	TMROUT0	—	—	Input with pulldown
PIO29	17	DT/$\overline{R}$	—	—	Alternate operation[2]
PIO30	18	DEN	DS	—	Alternate operation[2]
PIO31	13	PCS7	—	—	Input with pullup
PIO32	11	PCS6	—	—	Input with pullup
PIO33	19	ALE	—	—	Alternate operation[3]
PIO34	20	BHE	—	—	Alternate operation[2]
PIO35	15	SRDY	—	—	Alternate operation[2]
PIO36	138	—	—	—	Input with pullup
PIO37	139	—	—	—	Input with pullup
PIO38	137	—	—	—	Input with pullup
PIO39	136	—	—	—	Input with pullup
PIO40	135	—	—	—	Input with pullup
PIO41	134	—	—	—	Input with pullup
PIO42	153	—	—	—	Input with pulldown
PIO43	154	—	—	—	Input with pulldown
PIO44	152	—	—	—	Input with pullup
PIO45	151	—	—	—	Input with pullup
PIO46	24	CTS_HU	—	—	Input with pullup
PIO47	23	RTR_HU	—	—	Input with pullup

Notes:

1. *System reset is defined as a power-on reset (i.e., the* $\overline{\text{RES}}$ *input pin transitioning from its Low to High state) or a reset due to a watchdog timer timeout.*
2. *When used as a PIO, input with pullup option available.*
3. *When used as a PIO, input with a pulldown option available.*

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Table 26. PIOs Sorted by Signal Name

Signal	PIO No.	Pin No.	Multiplexed Signal	Multiplexed Signal	Pin Configuration Following System Reset[1]
ALE	PIO33	19	—	—	Alternate operation[2]
ARDY	PIO8	14	—	—	Alternate operation[3]
BHE	PIO34	20	—	—	Alternate operation[3]
CTS_HU	PIO46	24	—	—	Input with pullup
CTS_U	PIO24	157	—	—	Input with pullup
DEN	PIO30	18	DS	—	Alternate operation[3]
DRQ0	PIO9	124	—	—	Input with pulldown
DT/$\overline{R}$	PIO29	17	—	—	Alternate operation[3]
INT6	PIO19	145	—	—	Input with pullup
INT7	PIO7	146	—	—	Input with pullup
INT8	PIO6	147	PWD	—	Input with pullup
MCS0	PIO4	126	—	—	Input with pullup
MCS3	PIO5	129	RAS1	—	Input with pullup
PCS0	PIO13	5	—	—	Alternate operation[3]
PCS1	PIO14	6	—	—	Alternate operation[3]
PCS4	PIO3	9	—	—	Input with pullup
PCS5	PIO2	10	—	—	Input with pullup
PCS6	PIO32	11	—	—	Input with pullup
PCS7	PIO31	13	—	—	Input with pullup
PIO17	—	123	—	—	Input with pullup
PIO18	—	122	—	—	Input with pullup
PIO22	—	150	—	—	Input with pulldown
PIO23	—	149	—	—	Input with pulldown
PIO36	—	138	—	—	Input with pullup
PIO37	—	139	—	—	Input with pullup
PIO38	—	137	—	—	Input with pullup
PIO39	—	136	—	—	Input with pullup
PIO40	—	135	—	—	Input with pullup
PIO41	—	134	—	—	Input with pullup
PIO42	—	153	—	—	Input with pulldown
PIO43	—	154	—	—	Input with pulldown
PIO44	—	152	—	—	Input with pullup
PIO45	—	151	—	—	Input with pullup
RTR_HU	PIO47	23	—	—	Input with pullup
RTR_U	PIO25	156	—	—	Input with pullup
RXD_HU	PIO16	25	—	—	Input with pullup
RXD_U	PIO26	158	—	—	Input with pullup
SCLK	PIO11	3	—	—	Input with pullup
SDATA	PIO12	4	—	—	Input with pullup
SDEN	PIO10	2	—	—	Input with pulldown
SRDY	PIO35	15	—	—	Alternate operation[3]
TMRIN0	PIO27	142	—	—	Input with pullup
TMRIN1	PIO0	144			Input with pullup
TMROUT0	PIO28	141	—	—	Input with pulldown
TMROUT1	PIO1	143	—	—	Input with pulldown
TXD_U	PIO20	159	—	—	Input with pullup
UCLK	PIO21	22	USBSOF	USBSCI	Input with pullup
WR	PIO15	16	—	—	Alternate operation[3]

Notes:

1. *System reset is defined as a power-on reset (i.e., the $\overline{RES}$ input pin transitioning from its Low to High state) or a reset due to a watchdog timer timeout.*
2. *When used as a PIO, input with a pulldown option available.*
3. *When used as a PIO, input with a pullup option available.*

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Table 27. Reset Configuration Pins (Pinstraps)[1]

Signal Name	Multiplexed Signal(s)	Description
{ADEN}	BHE PIO34	**Address Enable**: If {ADEN} is held High or left floating during power-on reset, the address portion of the AD bus (AD15–AD0) is enabled or disabled during LCS, UCS, or other memory bus cycles based on how the software configures the DA bit setting. In this case, the memory address is accessed on the A19–A0 pins. There is a weak internal pullup resistor on {ADEN} so no external pullup is required. This mode of operation reduces power consumption. If {ADEN} is held Low on power-on reset, the AD bus drives both addresses and data, regardless of how software configures the DA bit setting.
{CLKSEL1} {CLKSEL2}	HLDA [PCS4] PIO3	**CPU PLL Mode Select 1** determines the PLL mode for the system clock source. **CPU PLL Mode Select 2** is sampled on the rising edge of reset and determines the PLL mode for the system clock source. This pin has an internal pullup resistor that is active only during reset. There are four CPU PLL modes that are selected by the values of {CLKSEL1} and {CLKSEL2} as shown below. (For details on clocks see “Clock Generation and Control” on page 32.) **CPU PLL Modes** {CLKSEL1} / {CLKSEL2} / CPU PLL Mode: 1 / 1 / 2X, CPU PLL enabled (default) 1 / 0 / 4X, CPU PLL enabled 0 / 1 / 1X, CPU PLL enabled 0 / 0 / PLL Bypass
{ONCE}	UCS	**ONCE Mode Request** asserted Low places the Am186CU USB microcontroller into ONCE mode. Otherwise, the controller operates normally. In ONCE mode, all pins are three-stated and remain in that state until a subsequent reset occurs. To guarantee that the controller does not inadvertently enter ONCE mode, {ONCE} has a weak internal pullup resistor that is active only during a reset. A reset ending ONCE mode should be as long as a power-on reset so that the PLL will stabilize.
{UCSX8}	[MCS0] PIO4	**Upper Memory Chip Select, 8-Bit Bus** asserted Low configures the upper chip select region for an 8-bit bus size. This pin has a pullup resistor that is active only during reset, so no external pullup is required to set the bus to 16-bit mode.
{USBSEL1} {USBSEL2}	PCS0 PIO13 PCS1 PIO14	**USB Clock Mode Selects 1–2** select the USB PLL operating mode. The pins have internal pullups that are active only during reset. The USB PLL can operate in one of three modes. With a crystal and the internal USB oscillator or an external oscillator, the USB PLL can output 4x or 2x the input frequency. The USB PLL can also be disabled and the USB peripheral controller can receive its clock from the CPU PLL, which is the default mode. The pins are encoded as shown below. (For details on clocks see “Clock Generation and Control” on page 32.) **USB PLL Modes** {USBSEL1} / {USBSEL2} / USB PLL Mode: 1 / 1 / Use system clock (after CPU PLL mode select), USB PLL disabled (default) 1 / 0 / 4x, USB PLL enabled 0 / 1 / 2x, USB PLL enabled 0 / 0 / Reserved
{USBXCVR}	S0	**USB External Transceiver Enable** asserted Low disables the internal USB transceiver and enables the pins needed to hook up an external transceiver. This pin has a pullup resistor that is active only during reset, so no external pullup is required as long as the user ensures that this input is not driven Low during a power-on reset.

Notes:

1. A pinstrap is used to enable or disable features based on the state of the pin during an external reset. The pinstrap must be held in its desired state for at least 4.5 clock cycles after the deassertion of RES. The pinstraps are sampled in an external reset only (when RES is asserted), not during an internal watchdog timer-generated reset.

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Pin List Table Column Definitions

The following paragraphs describe the individual columns of information in Table 29, “Pin List Summary,” on page A-10. The pins are grouped alphabetically by function.

Note: All maximum delay numbers should be increased by 0.035 ns for every pF of load (up to a maximum of 150 pF) over the maximum load specified in Table 29.

Column #1—Signal Name, [Alternate Function], {Pinstrap}

This column denotes the primary and alternate functions of the pins. Most of the pins that have alternate functions are configured for these functions via firmware modifying values in the Peripheral Control Block. Refer to the *Am186™CC/CH/CU Microcontrollers Register Set Manual*, order #21916, for full documentation of this process.

Brackets, [ ], are used to indicate the alternate, multiplexed function of a pin (i.e., not power-on reset default).

Braces, { }, are used to indicate the functionality of a pin only during a processor reset. These signals are called pinstraps. To select the desired configuration, the pinstraps are terminated internally with pullup resistors or externally with pulldown resistors. Their state is sampled during a processor reset and latched on the rising edge of reset. The signals must be held in the desired state for 4.5 system clock cycles after the deassertion of reset. Based on the pinstrap’s state at the time they are latched, certain features of the Am186CU USB microcontroller are enabled or disabled. All external termination should be implemented with 10-Kohm resistors on these signals.

The pinstraps are listed in Table 27, “Reset Configuration Pins (Pinstraps),” on page A-8.

Column #2—Pin No.

The pin number column identifies the pin number of the individual I/O signal on the package.

Column #3—Type

Definitions of the abbreviations in the Type column are shown in Table 28.

Table 28. Pin List Table Definitions

Type	Definition
[ ]	Pin alternate function
{ }	Pinstrap pin
B	Bidirectional
H	High
LS	Programmable to hold last state of pin
O	Totem pole output
OD	Open drain output
OD-O	Open drain output or totem pole output
PD	Internal pulldown resistor
PU	Internal pullup resistor
STI	Schmitt trigger Input
STI-OD	Schmitt trigger input or open drain output
TS	Three-state output

Column #4—Max Load (pF)

The Max Load column designates the capacitive load at which the I/O timing for that pin is guaranteed.

Column #5—POR Default Function

The POR Default Function column shows the status of these pins after a power-on reset. In some cases the pin is the function outlined in the “Signal Name” column of the table. The signal name is listed in the POR Default Function column if the signal is the default function and not a PIO after a processor reset. In other cases the pin is a PIO configured as an input.

Column #6—Reset State

The Reset State column indicates the termination present on the signal at reset (pullup or pulldown) and indicates whether the signal is a three-stated output or a Schmitt trigger input. Refer to Table 28 for abbreviations used in this column.

Column #7—POR Default Operation

The POR Default Operation column describes the type of input and/or output that is default pin operation. Refer to Table 28 for abbreviations used in this column.

Column #8—Hold State

The Hold State column shows the state of the pin in hold state. Refer to Table 28 for abbreviations used in this column.

Column #9—5 V

A "5 V" in the 5-V column indicates 5-V tolerant inputs. These inputs are not damaged and do not draw excess power when driven with levels up to V_{CC} + 2.6 volts. These pins only drive to V_{CC}.

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Table 29. Pin List Summary

Signal Name [Alternate Function] {Pinstrap}	Pin No.	Type	Max Load (pF)	POR Default Function	Reset State	POR Default Operation	Hold State	5 V
BUS INTERFACE/GENERAL-PURPOSE DMA REQUEST								
A0	30	O	70	A0	TS-PD	O	TS-PD	5 V
A1	31	O	70	A1	TS-PD	O	TS-PD	5 V
A2	32	O	70	A2	TS-PD	O	TS-PD	5 V
A3	36	O	70	A3	TS-PD	O	TS-PD	5 V
A4	37	O	70	A4	TS-PD	O	TS-PD	5 V
A5	42	O	70	A5	TS-PD	O	TS-PD	5 V
A6	43	O	70	A6	TS-PD	O	TS-PD	5 V
A7	44	O	70	A7	TS-PD	O	TS-PD	5 V
A8	45	O	70	A8	TS-PD	O	TS-PD	5 V
A9	49	O	70	A9	TS-PD	O	TS-PD	5 V
A10	50	O	70	A10	TS-PD	O	TS-PD	5 V
A11	64	O	70	A11	TS-PD	O	TS-PD	5 V
A12	65	O	70	A12	TS-PD	O	TS-PD	5 V
A13	69	O	70	A13	TS-PD	O	TS-PD	5 V
A14	70	O	70	A14	TS-PD	O	TS-PD	5 V
A15	84	O	70	A15	TS-PD	O	TS-PD	5 V
A16	85	O	70	A16	TS-PD	O	TS-PD	5 V
A17	88	O	70	A17	TS-PD	O	TS-PD	5 V
A18	89	O	70	A18	TS-PD	O	TS-PD	5 V
A19	90	O	70	A19	TS-PD	O	TS-PD	5 V
AD0	28	B	70	AD0	TS-PD	B	TS	5 V
AD1	34	B	70	AD1	TS-PD	B	TS	5 V
AD2	38	B	70	AD2	TS-PD	B	TS	5 V
AD3	46	B	70	AD3	TS-PD	B	TS	5 V
AD4	51	B	70	AD4	TS-PD	B	TS	5 V
AD5	66	B	70	AD5	TS-PD	B	TS	5 V
AD6	86	B	70	AD6	TS-PD	B	TS	5 V
AD7	92	B	70	AD7	TS-PD	B	TS	5 V
AD8	29	B	70	AD8	TS-PD	B	TS	5 V
AD9	35	B	70	AD9	TS-PD	B	TS	5 V
AD10	39	B	70	AD10	TS-PD	B	TS	5 V
AD11	47	B	70	AD11	TS-PD	B	TS	5 V
AD12	52	B	70	AD12	TS-PD	B	TS	5 V
AD13	67	B	70	AD13	TS-PD	B	TS	5 V
AD14	87	B	70	AD14	TS-PD	B	TS	5 V
AD15	93	B	70	AD15	TS-PD	B	TS	5 V
ALE [PIO33]	19	O STI-PD [STI] [O]	50	ALE	TS-PD	O	TS-PD	5 V
ARDY [PIO8]	14	STI-PU STI-PU [STI] [O]	50	ARDY	STI-PU	STI-PU	STI	5 V

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Table 29. Pin List Summary (Continued)

Signal Name [Alternate Function] {Pinstrap}	Pin No.	Type	Max Load (pF)	POR Default Function	Reset State	POR Default Operation	Hold State	5 V
$\overline{\text{BHE}}$ [PIO34] {ADEN}	20	O STI-PU [STI] [O] STI	50	$\overline{\text{BHE}}$	STI-PU	O	TS-PU	5 V
$\overline{\text{BSIZE8}}$	94	O	50	$\overline{\text{BSIZE8}}$	TS-PU	O	—	—
$\overline{\text{DEN}}$ [DS] [PIO30]	18	O O STI-PU [STI] [O]	50	$\overline{\text{DEN}}$	TS-PU	O	TS-PU	5 V
[DRQ0] PIO9	124	STI-PD STI-PD [STI] [O]	50	PIO9	STI-PD	STI-PD [STI] [O]	—	5 V
DRQ1	105	STI-PD	—	DRQ1	STI-PD	STI-PD	—	5 V
DT/$\overline{\text{R}}$ [PIO29]	17	O STI-PU [STI] [O]	50	DT/$\overline{\text{R}}$	TS-PU	O	TS-PU	5 V
HLDA {CLKSEL1}	98	O STI	50	HLDA	STI-PU	O	H	5 V
HOLD	99	STI	—	HOLD	STI-PD	STI	H	5 V
$\overline{\text{RD}}$	97	O	70	$\overline{\text{RD}}$	TS-PU	O	TS-PU	5 V
$\overline{\text{S0}}$ {USBXCVR}	57	O STI	50	$\overline{\text{S0}}$	STI-PU	O	TS	5 V
$\overline{\text{S1}}$	56	O	50	$\overline{\text{S1}}$	TS-PU	O	TS	5 V
$\overline{\text{S2}}$	55	O	50	$\overline{\text{S2}}$	TS-PU	O	TS	5 V
S6	54	O	50	S6	TS-PD	O	TS	5 V
SRDY [PIO35]	15	STI-PU STI-PU [STI] [O]	50	SRDY	STI-PU	STI-PU	—	5 V
$\overline{\text{WHB}}$	95	O	70	$\overline{\text{WHB}}$	TS-PU	O	TS-PU	5 V
$\overline{\text{WLB}}$	96	O	70	$\overline{\text{WLB}}$	TS-PU	O	TS-PU	5 V
$\overline{\text{WR}}$ [PIO15]	16	O STI-PU [STI] [O]	50	$\overline{\text{WR}}$	STI-PU	O	TS-PU	5 V
CHIP SELECTS								
$\overline{\text{LCS}}$ [RAS0]	131	O O	50	$\overline{\text{LCS}}$	TS-PU	O	TS-PU	5 V
[$\overline{\text{MCS0}}$] PIO4 {UCSX8}	126	O STI-PU [STI] [O] STI	50	PIO4	STI-PU	STI-PU [STI] [O]	TS-PU	5 V
$\overline{\text{MCS1}}$ [CAS1]	127	O O	50	$\overline{\text{MCS1}}$	TS-PU	O	TS-PU	5 V
$\overline{\text{MCS2}}$ [CAS0]	128	O O	50	$\overline{\text{MCS2}}$	TS-PU	O	TS-PU	5 V
[$\overline{\text{MCS3}}$] [RAS1] PIO5	129	O O STI-PU [STI] [O]	50	PIO5	STI-PU	STI-PU [STI] [O]	TS-PU	5 V
$\overline{\text{PCS0}}$ [PIO13] {USBSEL1}	5	O STI-PU [STI] [O] STI	50	$\overline{\text{PCS0}}$	STI-PU	O	TS-PU	5 V
$\overline{\text{PCS1}}$ [PIO14] {USBSEL2}	6	O STI-PU [STI] [O] STI	50	$\overline{\text{PCS1}}$	STI-PU	O	TS-PU	5 V
$\overline{\text{PCS2}}$	7	O	50	$\overline{\text{PCS2}}$	TS-PU	O	TS-PU	5 V

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Table 29. Pin List Summary (Continued)

Signal Name [Alternate Function] {Pinstrap}	Pin No.	Type	Max Load (pF)	POR Default Function	Reset State	POR Default Operation	Hold State	5 V
PCS3	8	O	50	PCS3	TS-PU	O	TS-PU	5 V
[PCS4] PIO3 {CLKSEL2}	9	O STI-PU [STI] [O] STI	50	PIO3	STI-PU	STI-PU [STI] [O]	TS-PU	5 V
[PCS5] PIO2	10	O STI-PU [STI] [O]	50	PIO2	STI-PU	O	TS-PU	5 V
[PCS6] PIO32	11	O STI-PU [STI] [O]	50	PIO32	STI-PU	STI-PU [STI] [O]	TS-PU	5 V
[PCS7] PIO31	13	O STI-PU [STI] [O]	50	PIO31	STI-PU	STI-PU [STI] [O]	TS-PU	5 V
UCS {ONCE}	132	O STI	50	UCS	STI-PU	O	TS-PU	5 V
CLOCKS/RESET/WATCHDOG TIMER								
CLKOUT	60	O	70	CLKOUT	—	O	—	—
RES	114	ST	—	RES	STI	STI	—	5 V
RESOUT	58	O	50	RESOUT	H	O	—	5 V
[UCLK] [USBSOF] [USBSCI] PIO21	22	STI O STI STI-PU [STI] [O]	50	PIO21	STI-PU	STI-PU [STI] [O]	—	5 V
USBX1	75	STI	—	USBX1	—	STI	—	—
USBX2	76	O	—	USBX2	—	O	—	—
X1	73	STI	—	X1	—	STI	—	—
X2	74	O	—	X2	—	O	—	—
PROGRAMMABLE TIMERS								
[PWD] [INT8] PIO6	147	STI STI STI-PU [STI] [O]	50	PIO6	STI-PU	STI-PU [STI] [O]	—	5 V
[TMRIN0] PIO27	142	STI-PU STI-PU [STI] [O]	50	PIO27	STI-PU	STI-PU [STI] [O]	—	5 V
[TMRIN1] PIO0	144	STI-PU STI-PU [STI] [O]	50	PIO0	STI-PU	STI-PU [STI] [O]	—	5 V
[TMROUT0] PIO28	141	O STI-PD [STI] [O]	50	PIO28	STI-PD	STI-PD [STI] [O]	TS	5 V
[TMROUT1] PIO1	143	O STI-PD [STI] [O]	50	PIO1	STI-PD	STI-PD [STI] [O]	TS	5 V
INTERRUPTS								
INT0	107	STI	—	INT0	STI-PU	STI	—	5 V
INT1	109	STI	—	INT1	STI-PU	STI	—	5 V
INT2	110	STI	—	INT2	STI-PU	STI	—	5 V
INT3	111	STI	—	INT3	STI-PU	STI	—	5 V
INT4	112	STI	—	INT4	STI-PU	STI	—	5 V
INT5	113	STI	—	INT5	STI-PU	STI	—	5 V
[INT6] PIO19	145	STI STI-PU [STI] [O]	50	PIO19	STI-PU	STI-PU [STI] [O]	—	5 V

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Table 29. Pin List Summary (Continued)

Signal Name [Alternate Function] {Pinstrap}	Pin No.	Type	Max Load (pF)	POR Default Function	Reset State	POR Default Operation	Hold State	5 V
[INT7] PIO7	146	STI STI-PU [STI] [O]	50	PIO7	STI-PU	STI-PU [STI] [O]	—	5 V
[INT8] [PWD] PIO6	147	STI STI STI-PU [STI] [O]	50	PIO6	STI-PU	STI-PU [STI] [O]	—	5 V
NMI	115	STI	—	NMI	STI-PU	STI	—	5 V
ASYNCHRONOUS SERIAL PORTS (UART AND HIGH-SPEED UART)								
UART								
[RXD_U] PIO26	158	STI STI-PU [STI] [O]	50	PIO26	STI-PU	STI-PU [STI] [O]	—	5 V
[TXD_U] PIO20	159	O STI-PU [STI] [O]	50	PIO20	STI-PU	STI-PU [STI] [O]	—	5 V
[$\overline{\text{CTS\_U}}$] PIO24	157	STI STI-PU [STI] [O]	50	PIO24	STI-PU	STI-PU [STI] [O]	—	5 V
[$\overline{\text{RTR\_U}}$] PIO25	156	O STI-PU [STI] [O]	30	PIO25	STI-PU	STI-PU [STI] [O]	—	5 V
HIGH-SPEED UART								
[RXD_HU] PIO16	25	STI STI-PU [STI] [O]	50	PIO16	STI-PU	STI-PU [STI] [O]	—	5 V
TXD_HU	26	O	30	TXD_HU	TS-PU	O	—	5 V
[$\overline{\text{CTS\_HU}}$] PIO46	24	STI STI-PU [STI] [O]	50	PIO46	STI-PU	STI-PU [STI] [O]	—	5 V
[$\overline{\text{RTR\_HU}}$] PIO47	23	O STI-PU [STI] [O]	30	PIO47	STI-PU	STI-PU [STI] [O]	—	5 V
DEBUG SUPPORT								
QS0	62	O	30	QS0	TS-PD	O	—	5 V
QS1	63	O	30	QS1	TS-PD	O	—	5 V
UNIVERSAL SERIAL BUS								
USBD+ [UDPLS]	81	B STI	—	USBD+	TS	B	—	—
USBD– [UDMNS]	80	B STI	—	USBD–	TS	B	—	—
SYNCHRONOUS SERIAL INTERFACE (SSI)								
[SCLK] PIO11	3	O STI-PU [STI] [O]	50	PIO11	STI-PU	STI-PU [STI] [O]	—	5 V
[SDATA] PIO12	4	O STI-PU [STI] [O]	50	PIO12	STI-PU	STI-PU [STI] [O]	—	5 V
[SDEN] PIO10	2	O STI-PD [STI] [O]	50	PIO10	STI-PD	STI-PD [STI] [O]	—	5 V

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Table 29. Pin List Summary (Continued)

Signal Name [Alternate Function] {Pinstrap}	Pin No.	Type	Max Load (pF)	POR Default Function	Reset State	POR Default Operation	Hold State	5 V
RESERVED PINS								
RSVD_104 [UXVRCV]	104	— STI	—	—	STI-PU	—	—	—
RSVD_103 [UXVOE]	103	— O	50	—	TS-PU	—	—	—
RSVD_102 [UTXDMNS]	102	— O	50	—	PU	—	—	—
RSVD_101 [UTXDPLS]	101	— O	50	—	PU	—	—	—
RSVD_119	119	—	—	—	—	—	—	—
RSVD_118	118	—	—	—	—	—	—	—
RSVD_117	117	—	—	—	—	—	—	—
RSVD_116	116	—	—	—	—	—	—	—
POWER AND GROUND								
V_{CC}	12	—	—	—	—	—	—	—
V_{CC}	27	—	—	—	—	—	—	—
V_{CC}	40	—	—	—	—	—	—	—
V_{CC}	48	—	—	—	—	—	—	—
V_{CC}	59	—	—	—	—	—	—	—
V_{CC}	68	—	—	—	—	—	—	—
V_{CC}	78	—	—	—	—	—	—	—
V_{CC}	91	—	—	—	—	—	—	—
V_{CC}	106	—	—	—	—	—	—	—
V_{CC}	120	—	—	—	—	—	—	—
V_{CC}	125	—	—	—	—	—	—	—
V_{CC}	133	—	—	—	—	—	—	—
V_{CC}	148	—	—	—	—	—	—	—
V_{CC}	160	—	—	—	—	—	—	—
V_{CC}_A	77	—	—	—	—	—	—	—
V_{CC}_USB	79	—	—	—	—	—	—	—
V_{SS}	1	—	—	—	—	—	—	—
V_{SS}	21	—	—	—	—	—	—	—
V_{SS}	33	—	—	—	—	—	—	—
V_{SS}	41	—	—	—	—	—	—	—
V_{SS}	53	—	—	—	—	—	—	—
V_{SS}	61	—	—	—	—	—	—	—
V_{SS}	71	—	—	—	—	—	—	—
V_{SS}	83	—	—	—	—	—	—	—
V_{SS}	100	—	—	—	—	—	—	—
V_{SS}	108	—	—	—	—	—	—	—
V_{SS}	121	—	—	—	—	—	—	—
V_{SS}	130	—	—	—	—	—	—	—
V_{SS}	140	—	—	—	—	—	—	—
V_{SS}	155	—	—	—	—	—	—	—

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Table 29. Pin List Summary (Continued)

Signal Name [Alternate Function] {Pinstrap}	Pin No.	Type	Max Load (pF)	POR Default Function	Reset State	POR Default Operation	Hold State	5 V
V_{SS}_A	72	—	—	—	—	—	—	—
V_{SS}_USB	82	—	—	—	—	—	—	—

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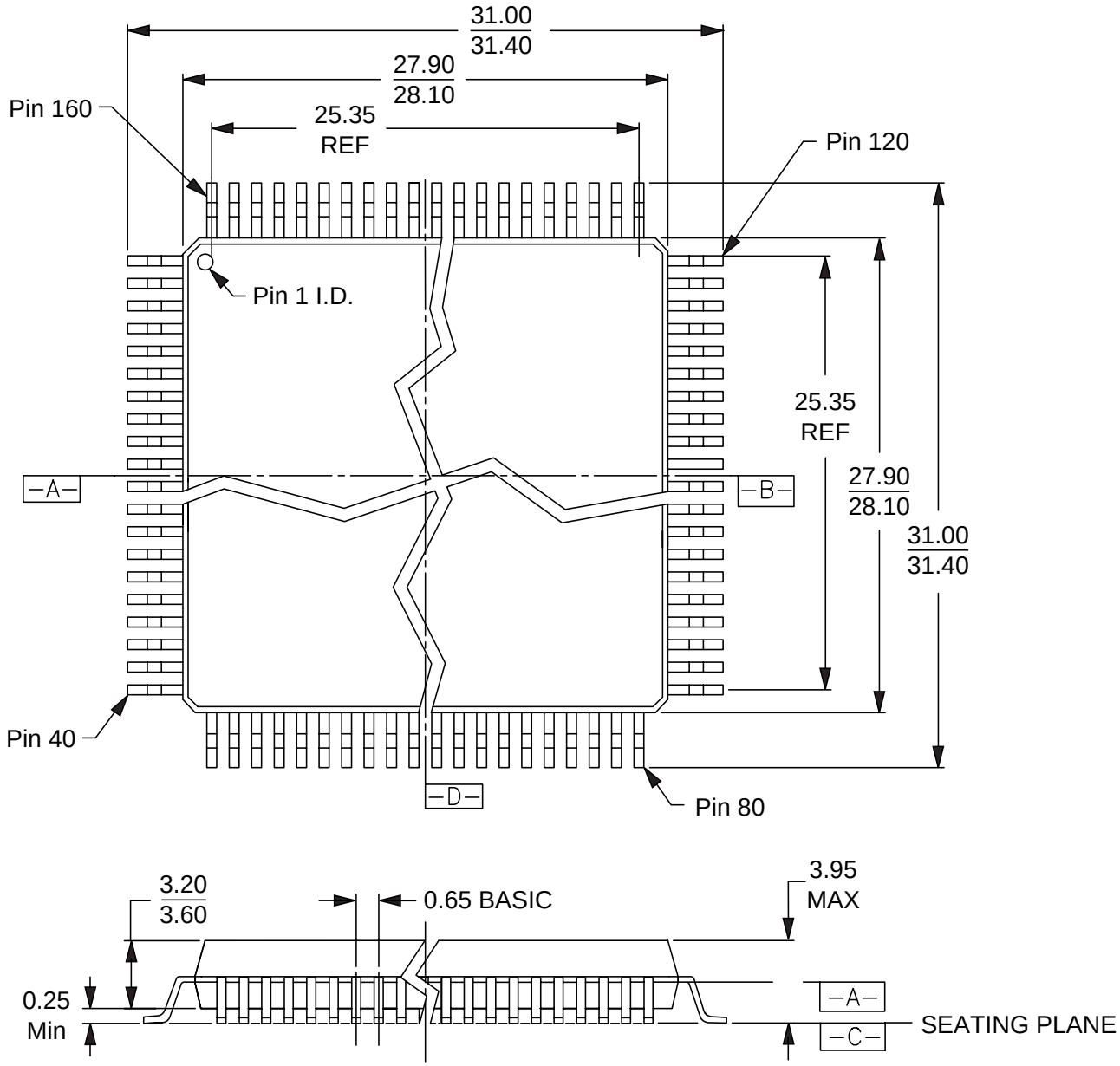
APPENDIX B—PHYSICAL DIMENSIONS: PQR160, PLASTIC QUAD FLAT PACK (PQFP)



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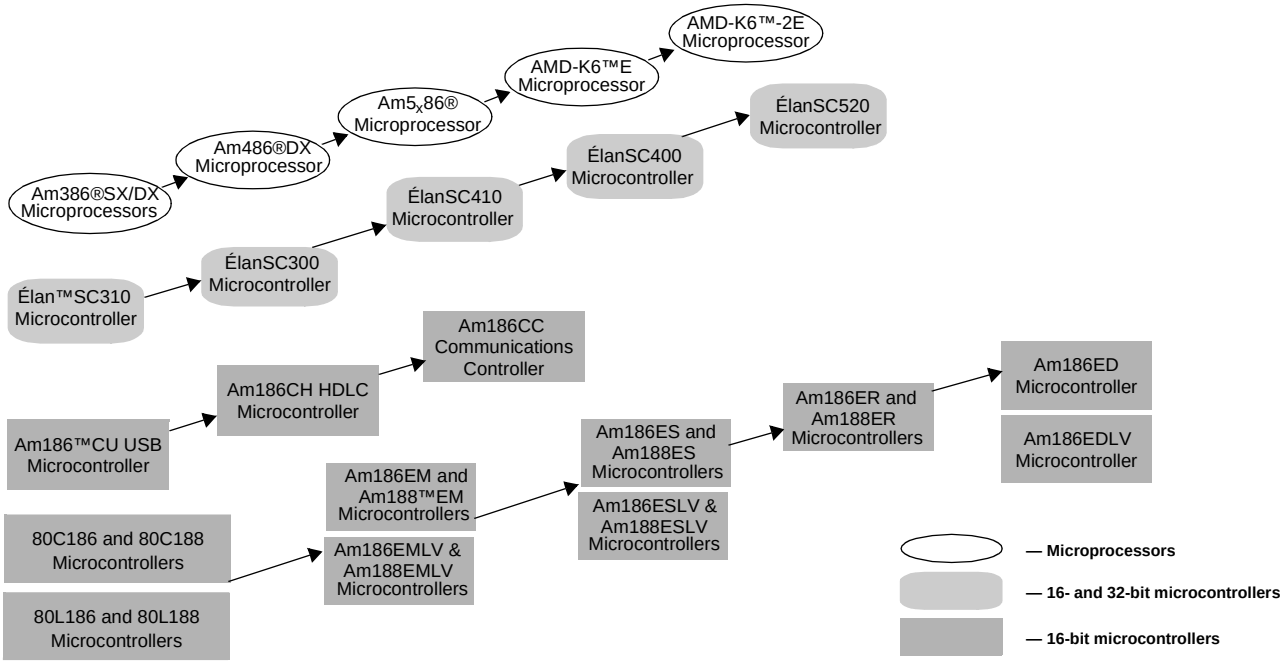
APPENDIX C—CUSTOMER SUPPORT



E86™ Family of Embedded Microprocessors and Microcontrollers

Related AMD Products—E86™ Family Devices

Device	Description
80C186/80C188	16-bit microcontroller
80L186/80L188	Low-voltage, 16-bit microcontroller
Am186™EM/Am188™EM	High-performance, 16-bit embedded microcontroller
Am186EMLV/Am188EMLV	High-performance, 16-bit embedded microcontroller
Am186ES/Am188ES	High-performance, 16-bit embedded microcontroller
Am186ESLV/Am188ESLV	High-performance, 16-bit embedded microcontroller
Am186ED	High-performance, 80C186- and 80C188-compatible, 16-bit embedded microcontroller with 8- or 16-bit external data bus
Am186EDLV	High-performance, 80C186- and 80C188-compatible, low-voltage, 16-bit embedded microcontroller with 8- or 16-bit external data bus
Am186ER/Am188ER	High-performance, low-voltage, 16-bit embedded microcontroller with 32 Kbyte of internal RAM
Am186CC	High-performance, 16-bit embedded communications controller
Am186CH	High-performance, 16-bit embedded HDLC microcontroller
Am186CU	High-performance, 16-bit embedded USB microcontroller
Élan™SC300	High-performance, highly integrated, low-voltage, 32-bit embedded microcontroller
ÉlanSC310	High-performance, single-chip, 32-bit embedded PC/AT microcontroller
ÉlanSC400	Single-chip, low-power, PC/AT-compatible microcontroller
ÉlanSC410	Single-chip, PC/AT-compatible microcontroller
ÉlanSC520	High-performance, 32-bit embedded microcontroller
Am386®DX	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
Am386®SX	High-performance, 32-bit embedded microprocessor with 16-bit external data bus
Am486®DX	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
$Am5_x86$	High-performance, 32-bit embedded microprocessor with 32-bit external data bus
AMD-K6™E	High-performance, 32-bit embedded microprocessor with 64-bit external data bus
AMD-K6™-2E	High-performance, 32-bit embedded microprocessor with 64-bit external data bus and 3DNow!™ technology

Notes:

1. 186 = 16-bit microcontroller and 80C186-compatible (except where noted otherwise); 188 = 16-bit microcontroller with 8-bit external data bus and 80C188-compatible (except where noted otherwise); LV = low voltage

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Related Documents

The following documents provide additional information regarding the Am186CU USB microcontroller.

- *Am186™CC/CH/CU Microcontrollers User's Manual*, order #21914
- *Am186™CC/CH/CU Microcontrollers Register Set Manual*, order #21916
- *Am186™ and Am188™ Family Instruction Set Manual*, order #21267
- *Interfacing an Am186™CC Communications Controller to an AMD SLAC™ Device Using the Enhanced SSI Application Note*, order #21921

Other information of interest includes:

- *E86™ Family Products and Development Tools CD,* order #21058

Am186CC/CH/CU Microcontroller Customer Development Platform

The Am186CC/CH/CU customer development platform (CDP) is provided as a test and development platform for the Am186CC/CH/CU microcontrollers Am186CU USB microcontroller. The Am186CC/CH/CU CDP ships with the Am186CC microcontroller. Because this device supports a superset of the features of the Am186CU USB microcontroller, the development platform can be used to evaluate the Am186CU device.

The CDP is divided into two major sections: a main board and a development module. The main board serves as the primary platform for silicon evaluation and software development. The board provides connectors for accessing the major communications peripherals, switches to easily configure the microcontroller, logic analyzer, and debug headers. The development module, which attaches to the top of the main board, provides ready-to-run hardware for three of the most common communications requirements:

- A 10 Mbit/s Ethernet connection
- An ISDN connection (with both an S/T and a U interface)
- Two POTS interfaces

The CDP provides a good starting point for hardware designers, and software development can begin immediately without the normal delay that occurs while waiting for prototypes.

The CDP also comes with AMD's CodeKit software that provides customers with pre-written driver software for the major communications peripherals associated with a typical Am186Cx design. Included are drivers for the HDLC channels, USB peripheral controller (for the Am186CU USB microcontroller), UARTs, PCnet-ISA II (AMD's single-chip Ethernet solution), and several other common peripherals. The CodeKit software comes complete with instructions, royalty-free distribution rights, and software in both binary and source code formats.

Third-Party Development Support Products

The FusionE86℠ Program of Partnerships for Application Solutions provides the customer with an array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD FusionE86 partners include protocol stacks, emulators, hardware and software debuggers, board-level products, and software development tools, among others.

In addition, mature development tools and applications for the x86 platform are widely available in the general marketplace.

Customer Service

The AMD customer service network includes U.S. offices, international offices, and a customer training center. Expert technical assistance is available from the AMD worldwide staff of field application engineers and factory support staff to answer E86™ and Comm86™ family hardware and software development questions.

Note: *The support telephone numbers listed below are subject to change. For current telephone numbers, refer to* ***www.amd.com/support/literature****.*

Hotline and World Wide Web Support

For answers to technical questions, AMD provides e-mail support as well as a toll-free number for direct access to our corporate applications hotline.

The AMD World Wide Web home page provides the latest product information, including technical information and data on upcoming product releases. In addition, EPD CodeKit software on the Web site provides tested source code example applications.

Corporate Applications Hotline

(800) 222-9323	Toll-free for U.S. and Canada
44-(0) 1276-803-299	U.K. and Europe hotline

Additional contact information is listed on the back of this datasheet. For technical support questions on all E86 and Comm86 products, send e-mail to **epd.support@amd.com**.

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World Wide Web Home Page

To access the AMD home page go to: **www.amd.com**. Then follow the **Embedded Processors** link for information about E86 and Comm86 products.

Questions, requests, and input concerning AMD's WWW pages can be sent via e-mail to **webmaster@amd.com**.

Documentation and Literature

Free information such as data books, user's manuals, data sheets, application notes, the *E86™ Family Products and Development Tools CD*, order #21058, and other literature is available with a simple phone call. Internationally, contact your local AMD sales office for product literature. Additional contact information is listed on the back of this data sheet.

Literature Ordering

(800) 222-9323	Toll-free for U.S. and Canada

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