BLF644P

Broadband power LDMOS transistor

Rev. 3 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 70 W LDMOS RF power transistor for broadcast transmitter, communications and industrial applications. The transistor is suitable for the frequency range HF to 1300 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital applications.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source test circuit.

Test signal	f	V_{DS}	P_L	G_p	η_D	IMD
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
CW, class-A	860	32	100	23	65	-
CW pulsed, class-AB	860	32	100	23.5	66	-
2-tone, class-AB	860	32	45	23	50	−25
	860	32	30	24	40	−35

1.2 Features and benefits

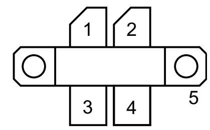
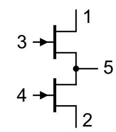
- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Communication transmitter applications in the HF to 1300 MHz frequency range
- Industrial applications in the HF to 1300 MHz frequency range
- Broadcast transmitters

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		 aaa-005775
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF644P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1228A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 90 W [1]	0.75	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 32 V; I_D = 50 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_{Dq} = 250 mA	1.5	2.0	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	9.0	-	A
I_{GSS}	gate leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.5 A	-	3.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.75 A	-	300	-	mΩ

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	39	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	15	-	pF
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 32 V; f = 1 MHz	-	0.84	-	pF

Table 8. RF characteristics

Test signal: CW pulsed, class-AB; f = 860 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 200 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

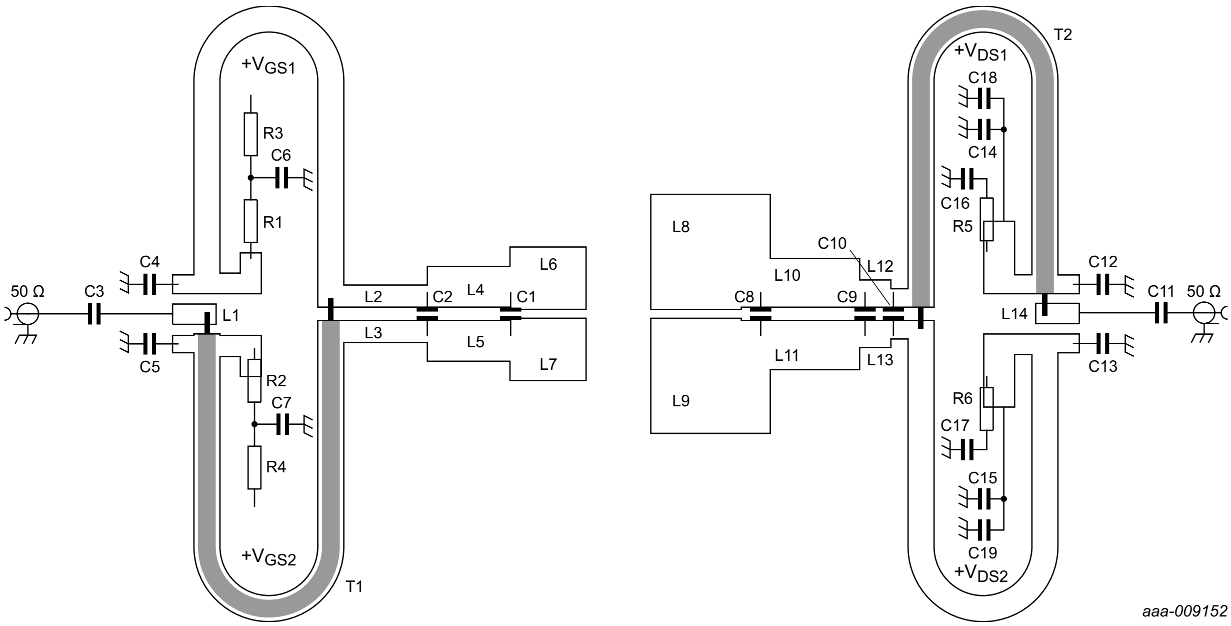
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 100 W	22.8	23.5	-	dB
η_D	drain efficiency	P_L = 100 W	62	66	-	%
RL_{in}	input return loss	P_L = 100 W	-	−15	−7	dBc

7. Test information

7.1 Ruggedness in class-AB operation

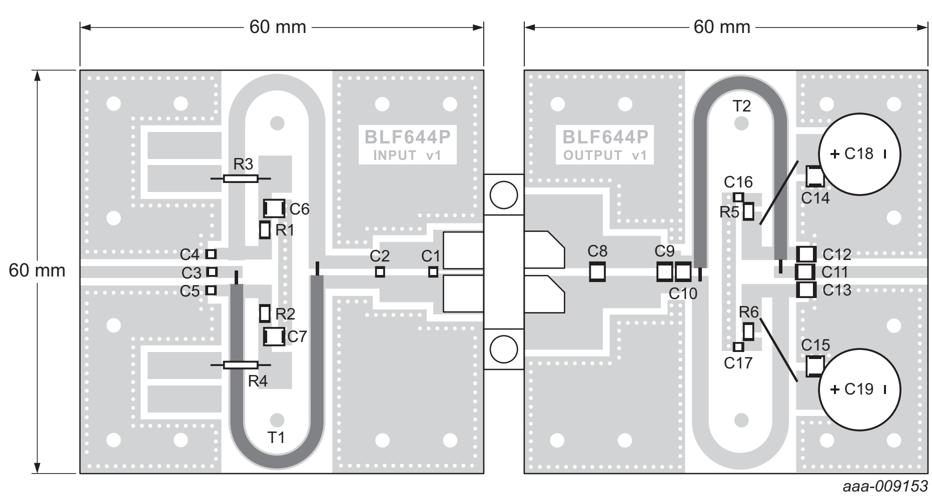
The BLF644P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; f = 860 MHz at rated load power.

7.2 Test circuit information



See Table 9 for list of components.

Fig 1. Schematic for class-AB production test circuit



Printed-Circuit Board (PCB): RF 35; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm.

See Table 9 for list of components.

Fig 2. Component layout for class-AB production test circuit

Table 9. List of components

See Figure 1 and Figure 2.

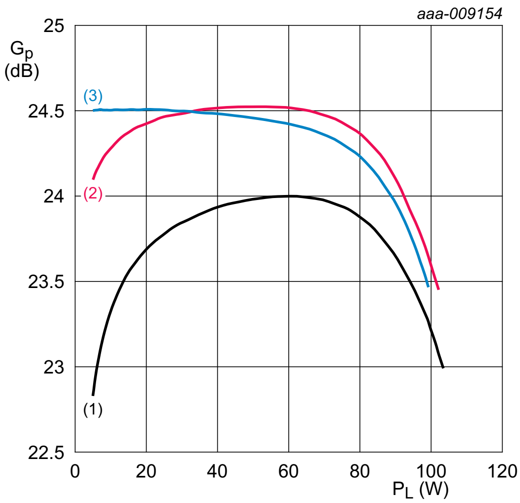
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	22 pF [1]	
C2	multilayer ceramic chip capacitor	8.2 pF [1]	
C3	multilayer ceramic chip capacitor	62 pF [1]	
C4, C5	multilayer ceramic chip capacitor	51 pF [1]	
C6, C7, C14, C15	multilayer ceramic chip capacitor	4.7 μF, 50 V	
C8	multilayer ceramic chip capacitor	12 pF [2]	
C9	multilayer ceramic chip capacitor	5.1 pF [2]	
C10	multilayer ceramic chip capacitor	9.1 pF [2]	
C11	multilayer ceramic chip capacitor	75 pF [2]	
C12, C13	multilayer ceramic chip capacitor	62 pF [2]	
C16, C17	multilayer ceramic chip capacitor	100 pF [1]	
C18, C19	electrolytic capacitor	470 μF, 63 V	
L1	microstrip	-	(L × W) 4 mm × 1.7 mm
L2, L3	microstrip	-	(L × W) 8 mm × 2 mm
L4, L5	microstrip	-	(L × W) 8 mm × 4 mm
L6, L7	microstrip	-	(L × W) 7.4 mm × 6 mm
L8, L9	microstrip	-	(L × W) 11.1 mm × 11.6 mm
L10, L11	microstrip	-	(L × W) 8.6 mm × 4.9 mm
L12, L13	microstrip	-	(L × W) 3 mm × 2.7 mm
L14	microstrip	-	(L × W) 4 mm × 1.7 mm
R1, R2	multilayer ceramic chip capacitor	5.6 Ω	SMD 1206
R3, R4	multilayer ceramic chip capacitor	100 Ω	
R5, R6	multilayer ceramic chip capacitor	30 Ω	SMD 1206
T1, T2	Semi-rigid coaxial cable	25 Ω, 61 mm	UT-90C-25

[1] American Technical Ceramics type 800A or capacitor of same quality.

[2] American Technical Ceramics type 800B or capacitor of same quality.

7.3 Graphical data

7.3.1 1-Tone CW



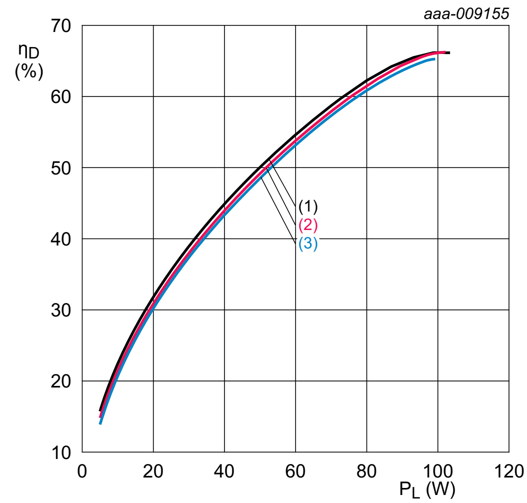
V_{DS} = 32 V; f = 860 MHz.

(1) I_{Dq} = 2 × 100 mA

(2) I_{Dq} = 2 × 200 mA

(3) I_{Dq} = 2 × 300 mA

Fig 3. Power gain as a function of output power; typical values



V_{DS} = 32 V; f = 860 MHz.

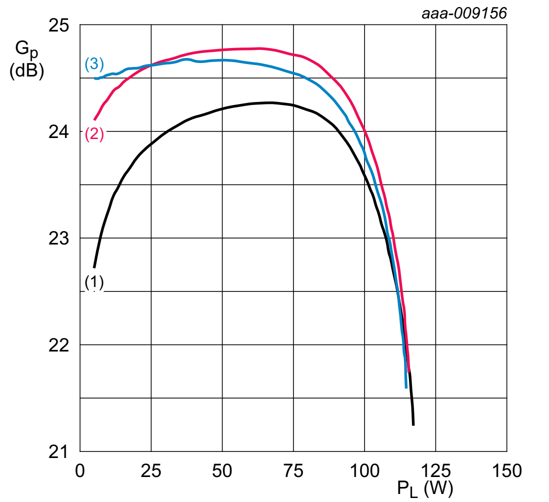
(1) I_{Dq} = 2 × 100 mA

(2) I_{Dq} = 2 × 200 mA

(3) I_{Dq} = 2 × 300 mA

Fig 4. Drain efficiency as a function of output power; typical values

7.3.2 1-Tone pulsed



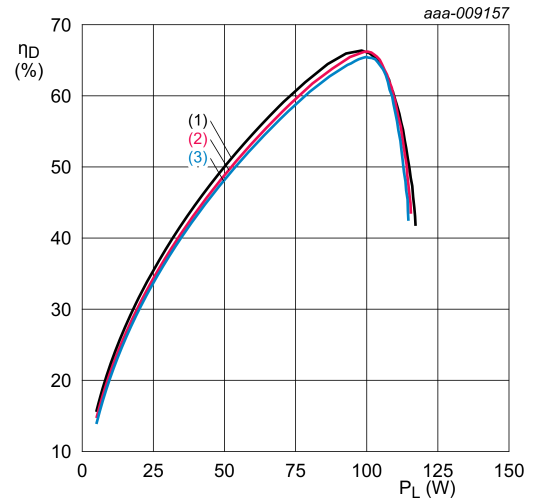
V_{DS} = 32 V; f = 860 MHz; δ = 20 %; t_p = 100 μs.

(1) I_{Dq} = 2 × 100 mA

(2) I_{Dq} = 2 × 200 mA

(3) I_{Dq} = 2 × 300 mA

Fig 5. Power gain as a function of output power; typical values



V_{DS} = 32 V; f = 860 MHz; δ = 20 %; t_p = 100 μs.

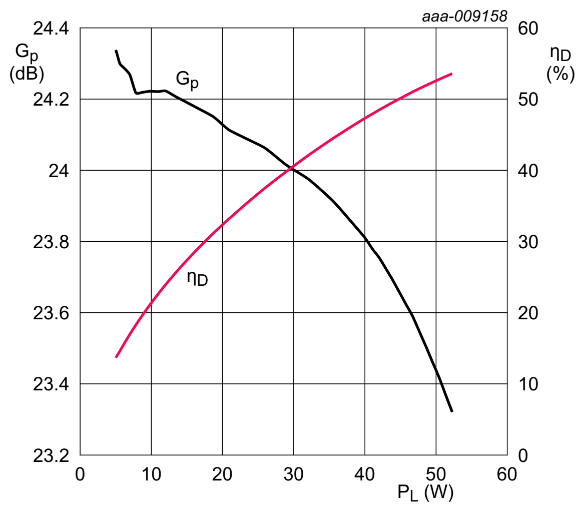
(1) I_{Dq} = 2 × 100 mA

(2) I_{Dq} = 2 × 200 mA

(3) I_{Dq} = 2 × 300 mA

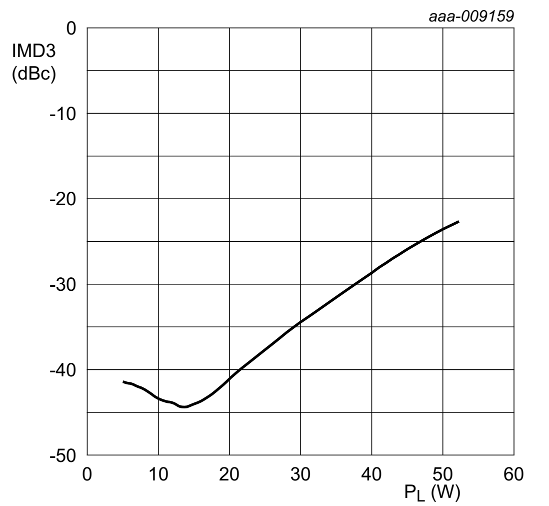
Fig 6. Drain efficiency as a function of output power; typical values

7.3.3 2-Tone CW



V_{DS} = 32 V; I_{Dq} = 2 × 350 mA; f_1 = 889.95 MHz; f_2 = 890.05 MHz.

Fig 7. Power gain and drain efficiency as function of output power; typical values

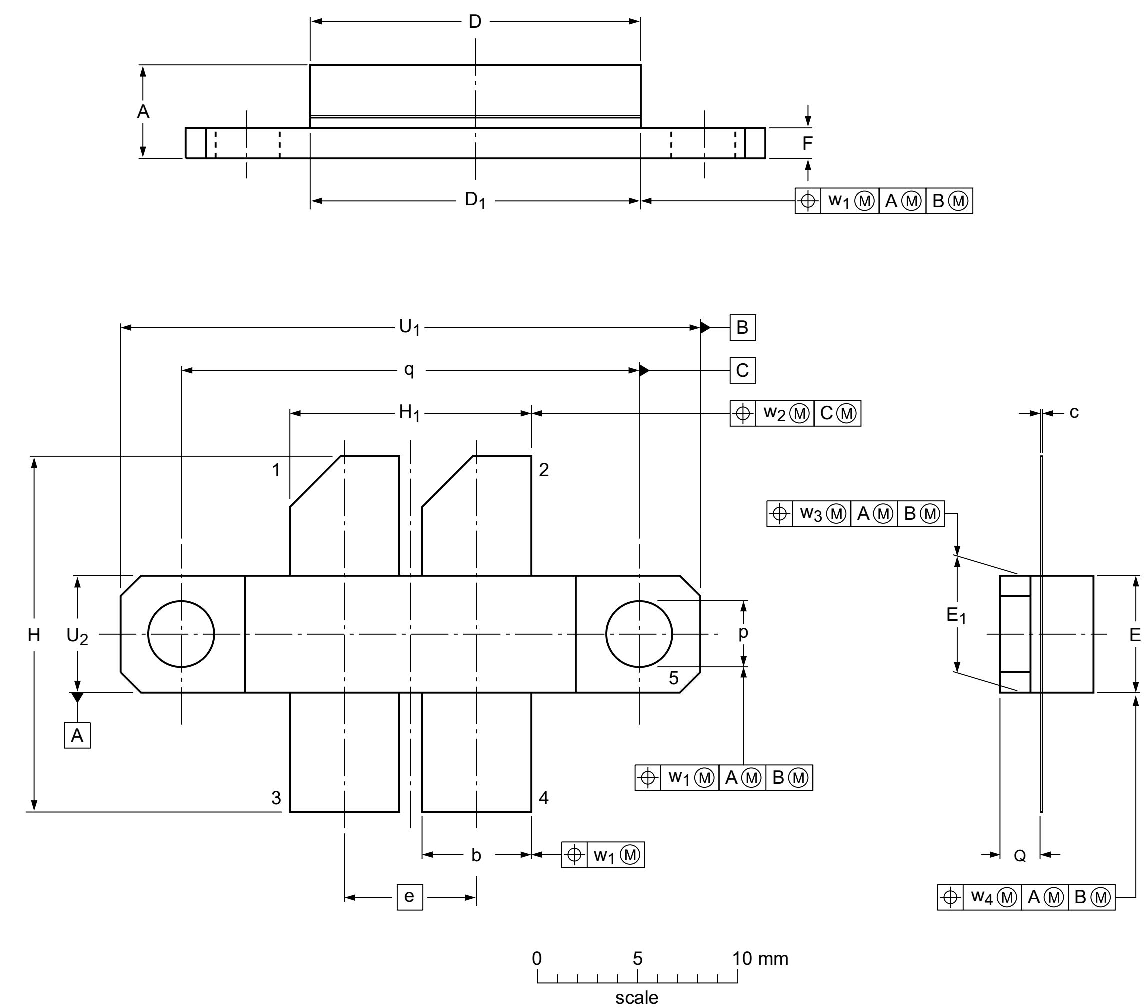


V_{DS} = 32 V; I_{Dq} = 2 × 350 mA; f_1 = 889.95 MHz; f_2 = 890.05 MHz.

Fig 8. Third order modulation distortion as a function of output power; typical values

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads SOT1228A



Dimensions

Unit(1)		A	b	c	D	D1	e	E	E1	F	H	H1	p	Q(2)	q	U1	U2	w1	w2	w3	w4
mm	max	5.2	5.59	0.15	16.66	16.69		5.92	5.97	1.65	18.29	12.19	3.43	2.21		29.08	5.97				
	nom						6.60								22.86			0.25	0.51	0.125	0.380
	min	4.5	5.33	0.08	16.36	16.33		5.77	5.72	1.40	17.27	11.94	3.18	1.96		28.83	5.72				
inches	max	0.205	0.220	0.006	0.656	0.657		0.233	0.235	0.065	0.720	0.480	0.135	0.087		1.145	0.235				
	nom						0.26								0.900			0.01	0.02	0.005	0.015
	min	0.177	0.210	0.003	0.644	0.643		0.227	0.225	0.055	0.680	0.470	0.125	0.077		1.135	0.225				

Note

1. Millimeter dimensions are derived from the original inch dimensions.
2. Dimension is measured 0.030 inch (0.76 mm) from body.

sot1228a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1228A						~~12-06-11~~ 13-05-16

Fig 9. Package outline SOT1228A

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF644P#3	20150901	Product data sheet	-	BLF644P v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF644P v.2	20140627	Product data sheet	-	BLF644P v.1
BLF644P v.1	20130611	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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