

BLP27M810

Power LDMOS transistor

Rev. 1 — 11 February 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

10 W LDMOS power transistor for broadcast and Industrial, Scientific and Medical (ISM) applications at frequencies from HF to 2700 MHz.

The BLP27M810 driver is designed for high power CW applications and is assembled in a high performance thermally enhanced plastic package.

Table 1. Typical performance

RF performance at $V_{DS} = 32\text{ V}$; $I_{DQ} = 100\text{ mA}$; $T_{case} = 25\text{ °C}$ in a class-AB application circuit.

Test signal	f	I_{DQ}	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(mA)	(V)	(W)	(dB)	(%)
CW	2450	100	32	10	18.4	50.6
Pulsed CW	2700	110	28	2	17	19

1.2 Features and benefits

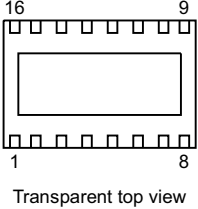
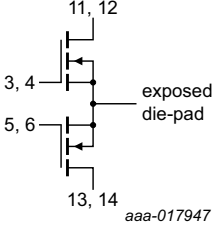
- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (HF to 2700 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Broadcast and Industrial, Scientific and Medical applications in the frequency range from HF to 2700 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol [1]
1, 2, 7, 8, 9, 10, 15, 16	n.c.	 Transparent top view	 aaa-017947
3, 4, 5, 6	gate		
11, 12, 13, 14	drain		
exposed die-pad	source [2]		

[1] To be used in single ended applications only.

[2] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP27M810	HVSON16	plastic thermal enhanced very thin small outline package; no leads; 16 terminals; body 4 × 6 × 0.85 mm	SOT1371-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 2\text{ W}$	3.2	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.18\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 18\text{ mA}$	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-1.4	-	+1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$	-	3.2	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 18\text{ mA}$	-	160	-	mS
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$; $I_D = 630\text{ mA}$	-	1000	-	$\text{m}\Omega$

Table 7. RF characteristics

A derivative functional RF test is performed in production. The performance as mentioned below is verified by design and characterization in an Ampleon class-AB application board.

Test signal: pulsed CW; $\delta = 10\%$; $t_p = 100\text{ }\mu\text{s}$; $V_{DS} = 28\text{ V}$; $I_{Dq} = 110\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; $f = 2140\text{ MHz}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 2\text{ W}$	16	17	-	dB
η_D	drain efficiency	$P_{L(AV)} = 2\text{ W}$	17	19	-	%
$P_{L(1dB)}$	output power at 1 dB gain compression		10	-	-	W

7. Application information

7.1 Application circuit

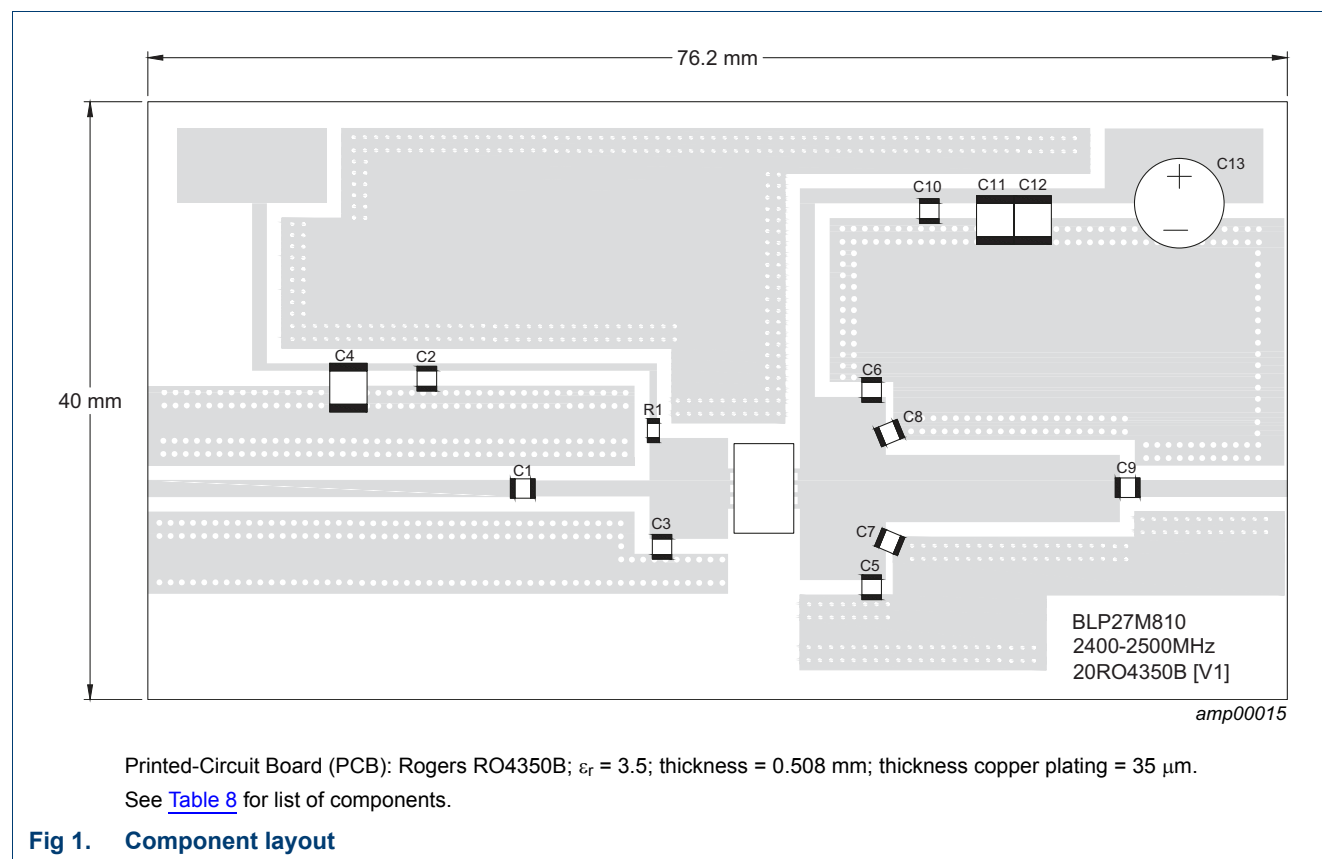
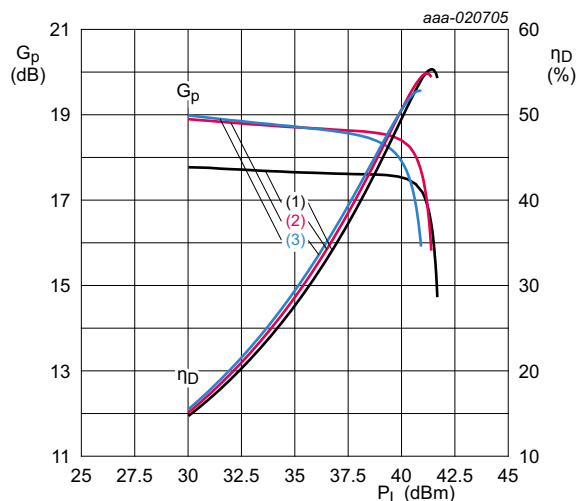


Table 8. List of components

See [Figure 1](#) for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	0.5 pF	ATC 100A
C2, C10	multilayer ceramic chip capacitor	15 pF	ATC 100A
C3	multilayer ceramic chip capacitor	2.2 pF	ATC 100A
C4, C11, C12	multilayer ceramic chip capacitor	1 μF , 50 V	Murata: GRM32RR71H105KA01L
C5, C6	multilayer ceramic chip capacitor	2.4 pF	ATC 100A
C7, C8	multilayer ceramic chip capacitor	1.5 pF	ATC 100A
C9	multilayer ceramic chip capacitor	15 pF	ATC 100A
C13	electrolytic capacitor	10 μF , 63 V	
R1	chip resistor	5.1 Ω	SMD 0805

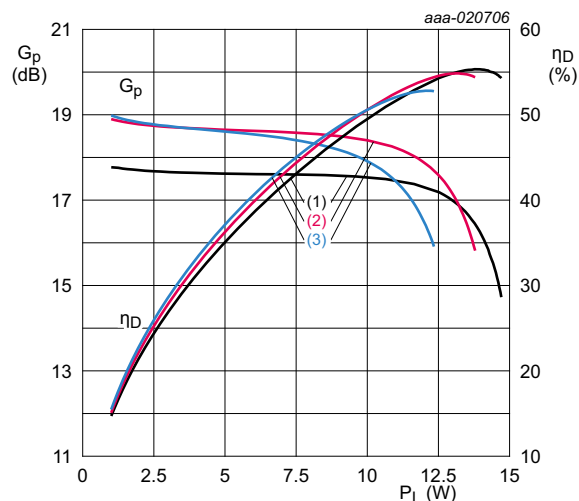
7.2 Graphical data



$V_{DS} = 32 \text{ V}$; $I_{DQ} = 100 \text{ mA}$.

- (1) $f = 2400 \text{ MHz}$
- (2) $f = 2450 \text{ MHz}$
- (3) $f = 2500 \text{ MHz}$

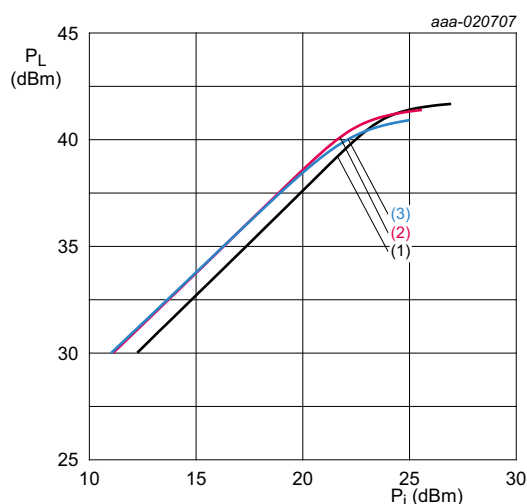
Fig 2. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 32 \text{ V}$; $I_{DQ} = 100 \text{ mA}$.

- (1) $f = 2400 \text{ MHz}$
- (2) $f = 2450 \text{ MHz}$
- (3) $f = 2500 \text{ MHz}$

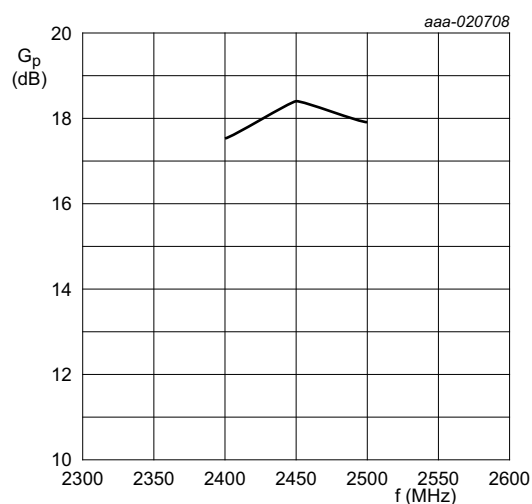
Fig 3. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 32 \text{ V}$; $I_{DQ} = 100 \text{ mA}$.

- (1) $f = 2400 \text{ MHz}$
- (2) $f = 2450 \text{ MHz}$
- (3) $f = 2500 \text{ MHz}$

Fig 4. Output power as a function of input power; typical values



$V_{DS} = 32 \text{ V}$; $I_{DQ} = 100 \text{ mA}$; $P_L = 10 \text{ W}$.

Fig 5. Power gain as a function of frequency; typical values

8. Test information

8.1 Ruggedness in class-AB operation

The BLP27M810 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 32\text{ V}$; $I_{Dq} = 100\text{ mA}$; $P_L = 10\text{ W}$.

Table 9. Typical impedance
Measured load-pull data. Typical values unless otherwise specified. $I_{Dq} = 120\text{ mA}$; $V_{DS} = 28\text{ V}$.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)
2400	$0.6 - j3.0$	$2.2 + j0.2$
2450	$0.6 - j3.3$	$2.4 - j0.1$
2500	$0.6 - j3.5$	$2.5 - j0.3$

[1] Z_S and Z_L defined in [Figure 6](#).

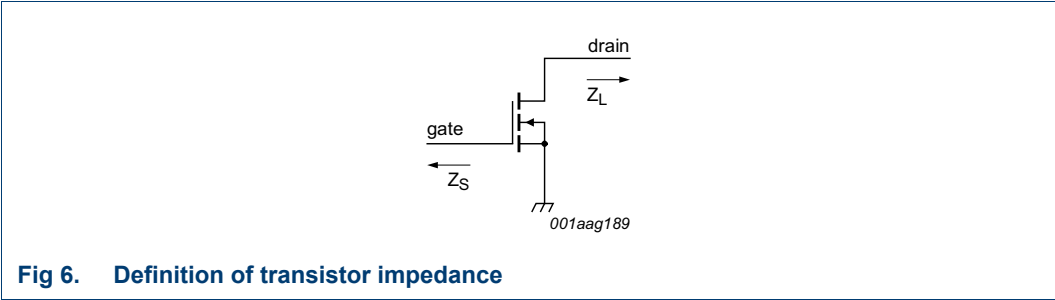


Fig 6. Definition of transistor impedance

9. Package outline

HVSON16: plastic thermal enhanced very thin small outline package; no leads;
16 terminals; body 4 x 6 x 0.85 mm

SOT1371-1

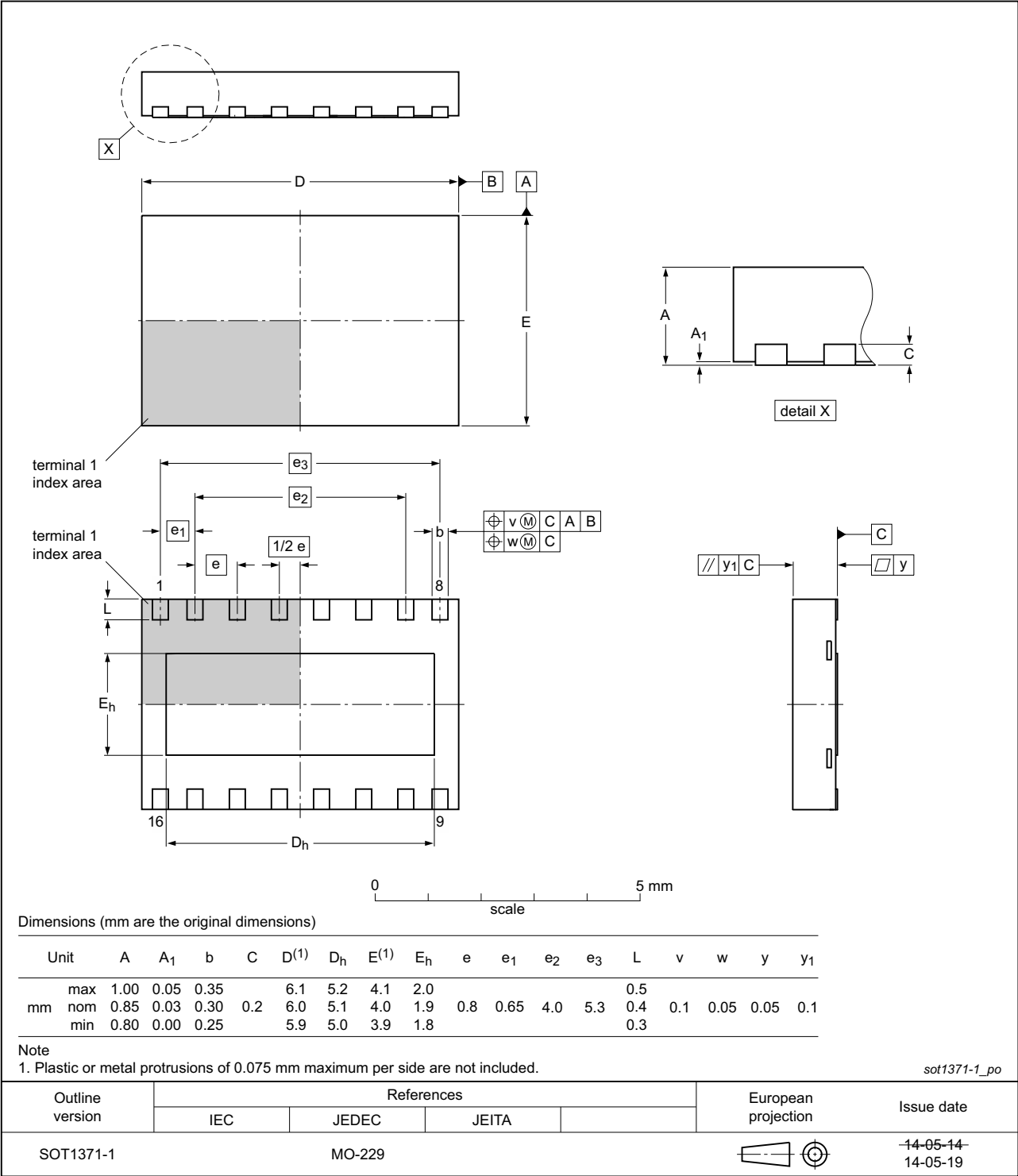


Fig 7. Package outline SOT1371-1 (HVSON16)

10. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP27M810 v.1	20160211	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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15. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	2
6	Characteristics	3
7	Application information	4
7.1	Application circuit	4
7.2	Graphical data	5
8	Test information	6
8.1	Ruggedness in class-AB operation	6
9	Package outline	7
10	Handling information	8
11	Abbreviations	8
12	Revision history	8
13	Legal information	9
13.1	Data sheet status	9
13.2	Definitions	9
13.3	Disclaimers	9
13.4	Trademarks	10
14	Contact information	10
15	Contents	11

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Date of release: 11 February 2016

Document identifier: BLP27M810