TEXAS
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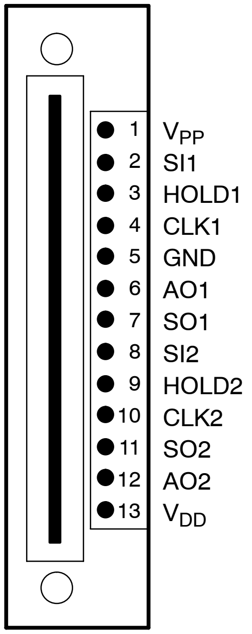
TSL1406R, TSL1406RS
768 × 1 LINEAR SENSOR ARRAY WITH HOLD

TAOS042C − FEBRUARY 2007

- **768 × 1 Sensor-Element Organization**
- **400 Dot-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity**
- **Wide Dynamic Range . . . 4000:1 (72 dB)**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 8 MHz**
- **Single 3-V to 5-V Supply**
- **Rail-to-Rail Output Swing (AO)**
- **No External Load Resistor Required**
- **Replacement for TSL1406**

TSL1406R
(TOP VIEW)



Description

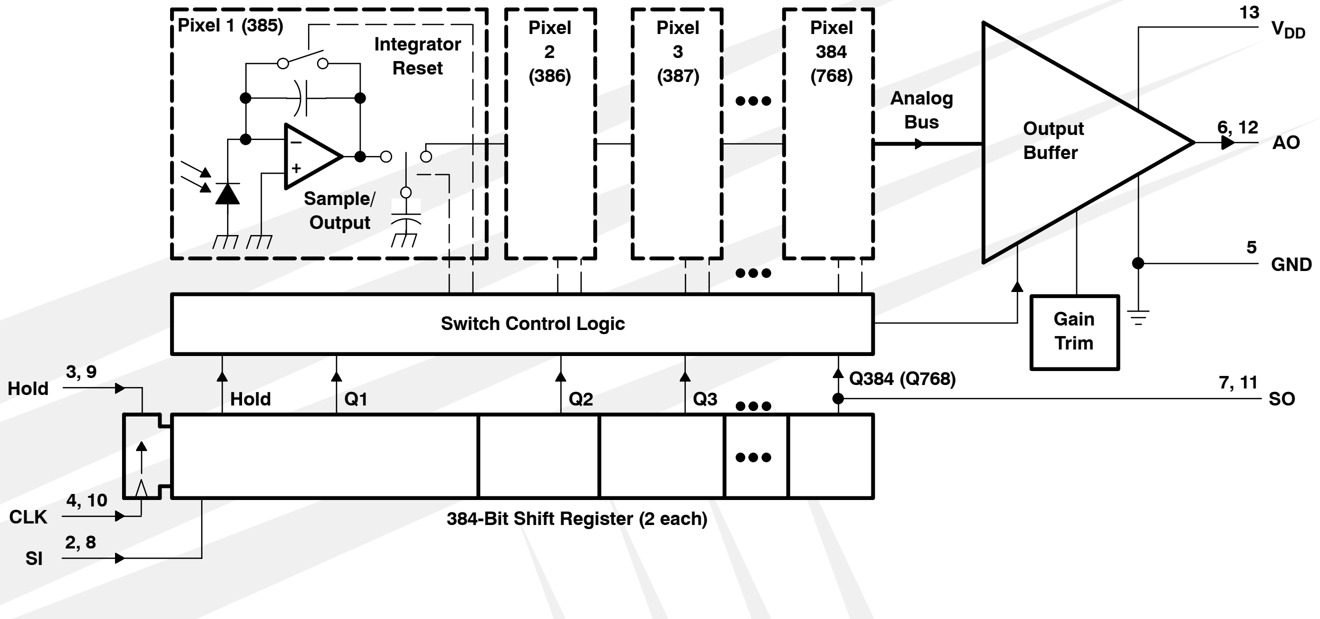
The TSL1406R is a 400 dots-per-inch (DPI) linear sensor array consisting of two 384-pixel sections, each with its own output. The sections are aligned to form a contiguous 768 × 1 pixel array. The device incorporates a pixel data-hold function that provides simultaneous integration-start and integration-stop times for all pixels.

Pixels measure 63.5 μm by 55.5 μm, with 63.5-μm center-to-center spacing and 8-μm spacing between pixels. Operation is simplified by internal logic that requires only a serial-input (SI) pulse and a clock.

The device operates from a single 5-V power source. The two sections of 384 pixels each can be read out separately or can be cascaded to provide a single output for all 768 pixels (see Figure 9).

The TSL1406RS is the same device mounted in a shorter package. These devices are intended for use in a wide variety of applications including mark and code reading, OCR and contact imaging, edge detection and positioning, and optical encoding.

Functional Block Diagram (each section)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AO1	6	O	Analog output, section 1.
AO2	12	O	Analog output, section 2.
CLK1	4	I	Clock, section 1. CLK1 controls charge transfer, pixel output, and reset.
CLK2	10	I	Clock, section 2. CLK2 controls charge transfer, pixel output, and reset.
GND	5		Ground (substrate). All voltages are referenced to GND.
HOLD1	3	I	Hold signal. HOLD1 shifts pixel data to parallel buffer. HOLD1 is normally connected to SI1 and HOLD2 in serial mode, SI1 in parallel mode.
HOLD2	9	I	Hold signal. HOLD2 shifts pixel data to parallel buffer. HOLD2 is normally connected to SI2 in parallel mode.
SI1	2	I	Serial input (section 1). SI1 defines the start of the data-out sequence.
SI2	8	I	Serial input (section 2). SI2 defines the start of the data-out sequence.
SO1	7	O	Serial output (section 1). SO1 provides a signal to drive the SI2 input in serial mode.
SO2	11	O	Serial output (section 2). SO2 provides a signal to drive the SI input of another device for cascading or as an *end-of-data* indication.
V_{DD}	13		Supply voltage for both analog and digital circuitry.
V_{PP}	1		Normally grounded.

Detailed Description

The sensor consists of 768 photodiodes, called pixels, arranged in a linear array. Light energy impinging on a pixel generates photocurrent that is then integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity on that pixel and the integration time.

The output and reset of the integrators are controlled by a 384-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. Another signal, called HOLD, is generated from the rising edge of SI1 when SI1 and HOLD1 are connected together. This causes all 384 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO. The integrator reset period ends 18 clock cycles after the SI pulse is clocked in. Then the next integration period begins. On the 384th clock rising edge, the SI pulse is clocked out on the SO1 pin (section 1) and becomes the SI pulse for section 2 (when SO1 is connected to SI2). The rising edge of the 385th clock cycle terminates the SO1 pulse, and returns the analog output AO of section 1 to high-impedance state. Similarly, SO2 is clocked out on the 768th clock pulse. Note that a 769th clock pulse is needed to terminate the SO2 pulse and return AO of Section 2 to the high-impedance state. If a minimum integration time is desired, the next SI pulse may be presented after a minimum delay of t_{qt} (pixel charge transfer time) after the 769th clock pulse. Sections 1 and 2 may be operated in parallel or in serial fashion.

AO is an op amp-type output that does not require an external pull-down resistor. This design allows a rail-to-rail output voltage swing. With V_{DD} = 5 V, the output is nominally 0 V for no light input, 2 V for normal white level, and 4.8 V for saturation light level. When the device is not in the output phase, AO is in a high-impedance state.

The voltage developed at analog output (AO) is given by:

$$V_{out} = V_{drk} + (R_e)\,(E_e)(t_{int})$$

where:

V_{out}	is the analog output voltage for white condition
V_{drk}	is the analog output voltage for dark condition
R_e	is the device responsivity for a given wavelength of light given in V/(μJ/cm^2)
E_e	is the incident irradiance in μW/cm^2
t_{int}	is integration time in seconds

A 0.1 μF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

Absolute Maximum Ratings†

Supply voltage range, V_{DD} . . . . −0.3 V to 6 V
Input voltage range, V_I . . . . −0.3 V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$) or ($V_I > V_{DD}$) . . . . −20 mA to 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . −25 mA to 25 mA
Voltage range applied to any output in the high impedance or power-off state, V_O . . . −0.3 V to V_{DD} + 0.3 V
Continuous output current, I_O ($V_O = 0$ to V_{DD}) . . . . −25 mA to 25 mA
Continuous current through V_{DD} or GND . . . . −40 mA to 40 mA
Analog output current range, I_O . . . . −25 mA to 25 mA
Maximum light exposure at 638 nm . . . . 5 mJ/cm^2
Operating free-air temperature range, T_A . . . . −25°C to 85°C
Storage temperature range, T_{stg} . . . . −25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		8000	kHz
Sensor integration time, Serial, t_{int} (see Note 1)	0.11375		100	ms
Sensor integration time, Parallel, t_{int} (see Note 1)	0.06575		100	ms
Setup time, serial input, $t_{su(SI)}$	20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 2)	0			ns
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Integration time is calculated as follows:

$$\mathbf{t_{int} = (768 - 18) \times clock\ period + 20\ \mu s}$$

where *768* is the number of pixels in series, *18* is the required logic setup clocks, and *20 μs* is the pixel charge transfer time (t_{qt})

2. SI must go low before the rising edge of the next clock pulse.

Electrical Characteristics at f_{clock} = 1 MHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 640 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 12.5 μW/cm^2 (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{out}	Analog output voltage (white, average over 768 pixels)	See Note 4	1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 256 pixels)	$E_e = 0$	0	0.1	0.3	V
PRNU	Pixel response nonuniformity	See Note 5			±15%	
	Nonlinearity of analog output voltage	See Note 6		0.4%		FS
	Output noise voltage	See Note 7		1		mVrms
R_e	Responsivity	See Note 8	20	30	38	V/ (μJ/cm^2)
V_{sat}	Analog output saturation voltage	V_{DD} = 5 V, R_L = 330 Ω	4.5	4.8		V
		V_{DD} = 3 V, R_L = 330 Ω	2.5	2.8		
SE	Saturation exposure	V_{DD} = 5 V, See Note 9		155		nJ/cm^2
		V_{DD} = 3 V, See Note 9		90		
DSNU	Dark signal nonuniformity	All pixels, $E_e = 0$, See Note 10		0.05	0.15	V
IL	Image lag	See Note 11		0.5%		
I_{DD}	Supply current	V_{DD} = 5 V, E_e = 0, R_L = 330 Ω		18	27	mA
		V_{DD} = 3 V, E_e = 0, R_L = 330 Ω		16	25	
I_{IH}	High-level input current	$V_I = V_{DD}$			10	μA
I_{IL}	Low-level input current	$V_I = 0$			10	μA
C_i	Input capacitance, SI			15		pF
C_i	Input capacitance, CLK			30		pF

NOTES:
3. All measurements made with a 0.1 μF capacitor connected between V_{DD} and ground.
4. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640 nm.
5. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
6. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
7. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
8. $R_{e(min)} = [V_{out(min)} - V_{drk(max)}] \div (E_e \times t_{int})$
9. $SE(min) = [V_{sat(min)} - V_{drk(min)}] \times \langle E_e \times t_{int}\rangle \div [V_{out(max)} - V_{drk(min)}]$
10. DSNU is the difference between the maximum and minimum output voltage for all pixels in the absence of illumination.
11. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out\ (IL)} - V_{drk}}{V_{out\ (white)} - V_{drk}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{su(SI)}$	Setup time, serial input (see Note 12)	20			ns
$t_{h(SI)}$	Hold time, serial input (see Note 12 and Note 13)	0			ns
$t_{pd(SO)}$	Propagation delay time, SO		50		ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns
t_{qt}	Pixel charge transfer time	20			μs

NOTES:
12. Input pulses have the following characteristics: t_r = 6 ns, t_f = 6 ns.
13. SI must go low before the rising edge of the next clock pulse.

Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 7 and 8)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 50 pF		120		ns
$t_{pd(SO)}$	Propagation delay time, SO1, SO2			50		ns

TYPICAL CHARACTERISTICS

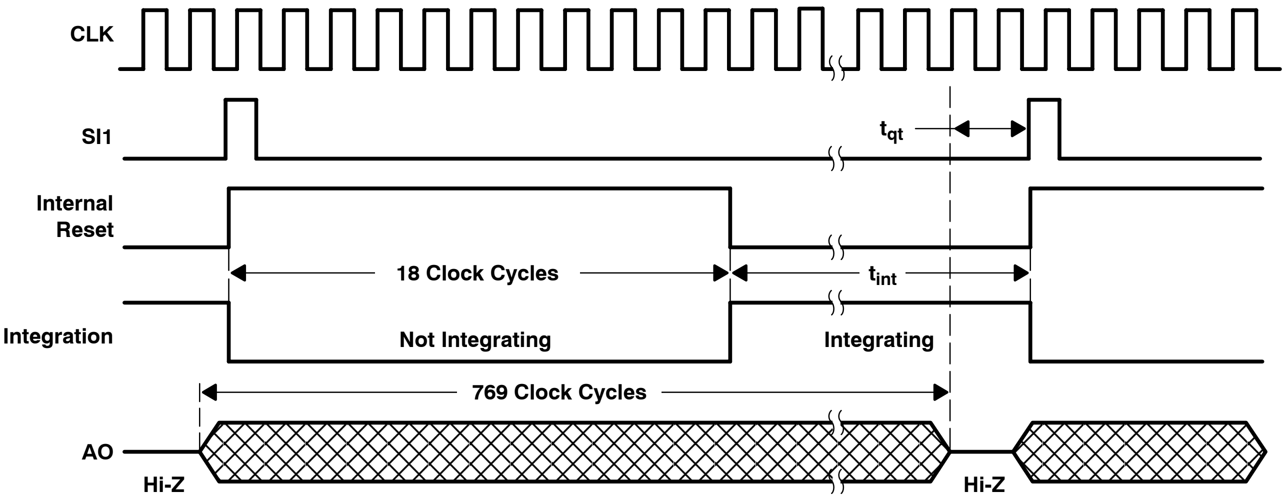


Figure 1. Timing Waveforms (serial connection)

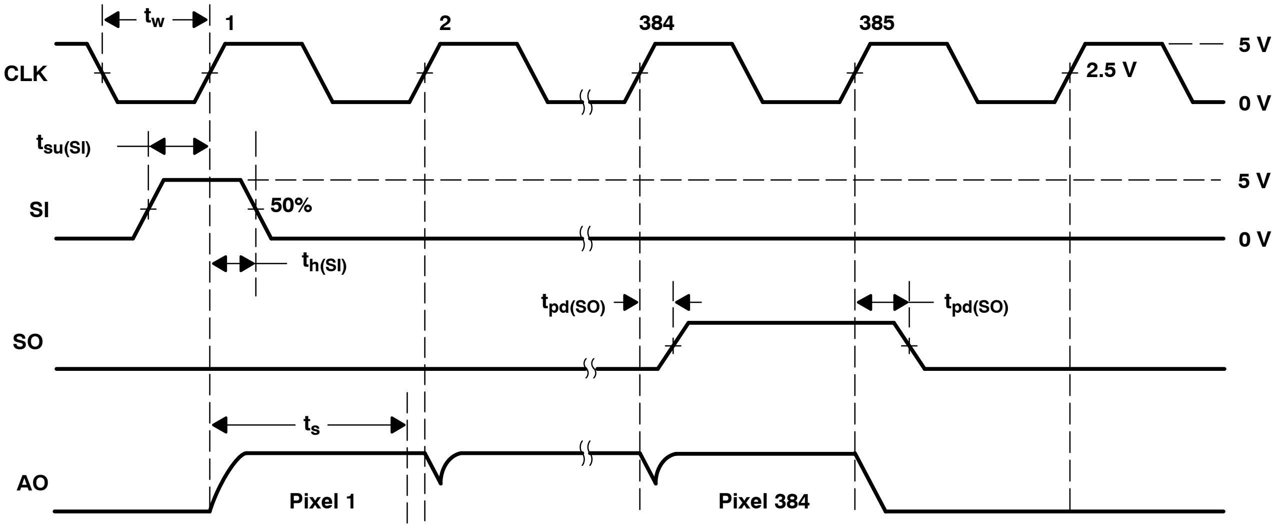


Figure 2. Operational Waveforms (each section)

TYPICAL CHARACTERISTICS

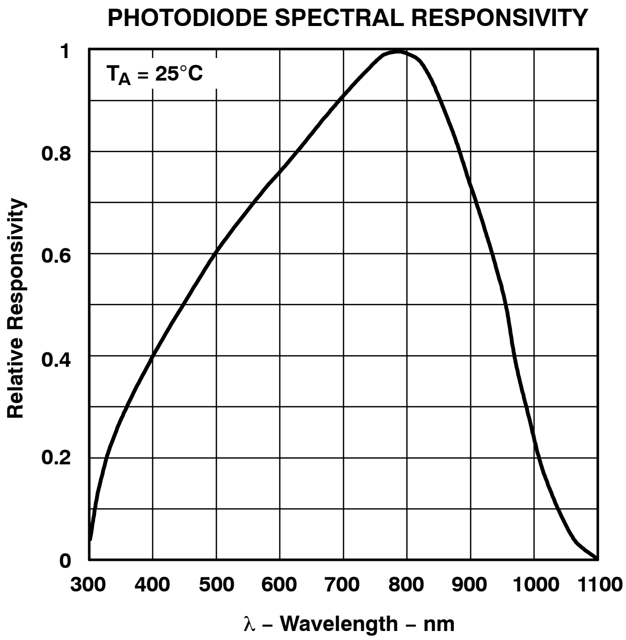

PHOTODIODE SPECTRAL RESPONSIVITY

Figure 3

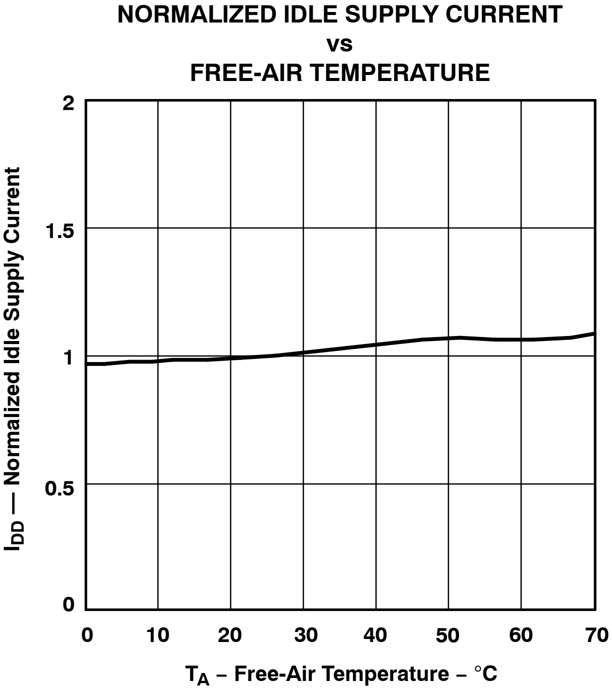

NORMALIZED IDLE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 4

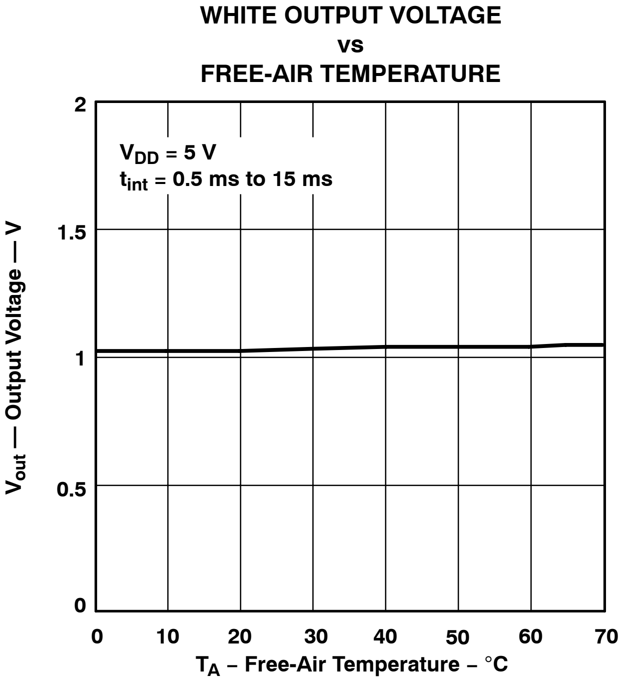

WHITE OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 5

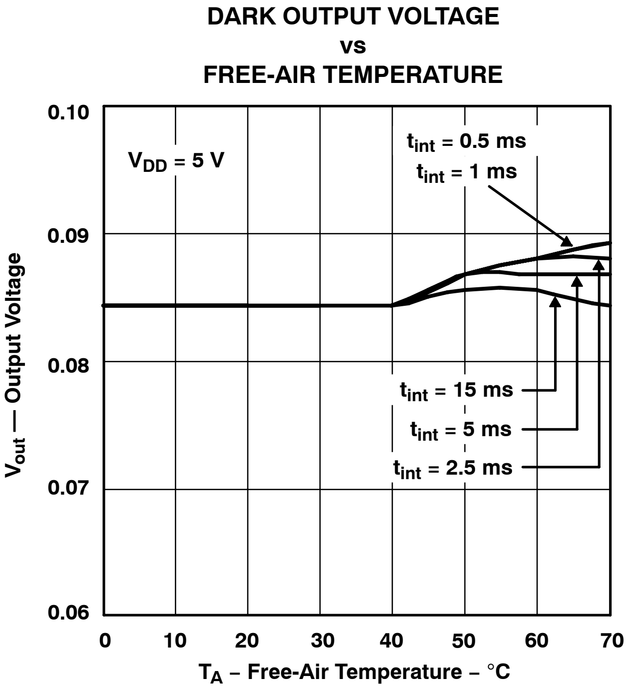

DARK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 6

TYPICAL CHARACTERISTICS

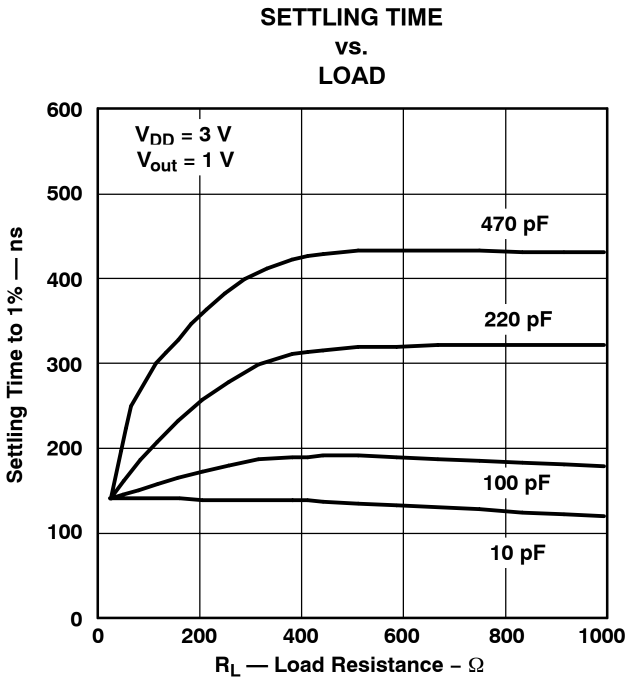


Figure 7

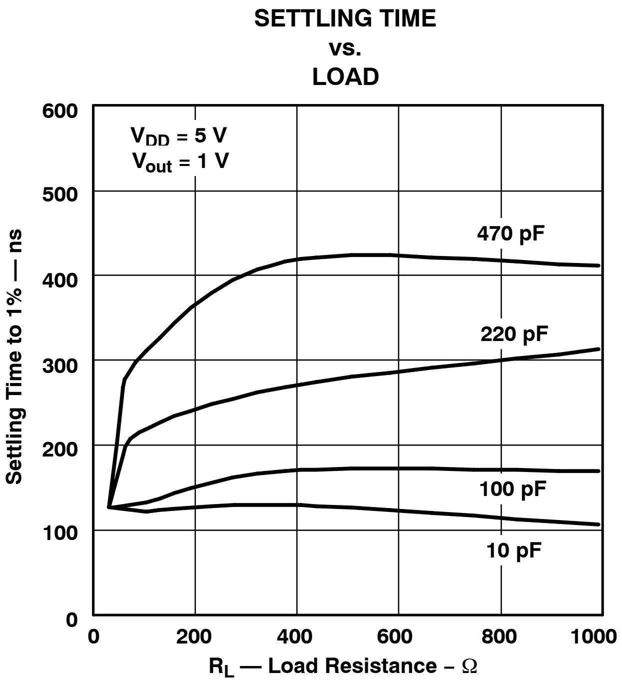


Figure 8

APPLICATION INFORMATION

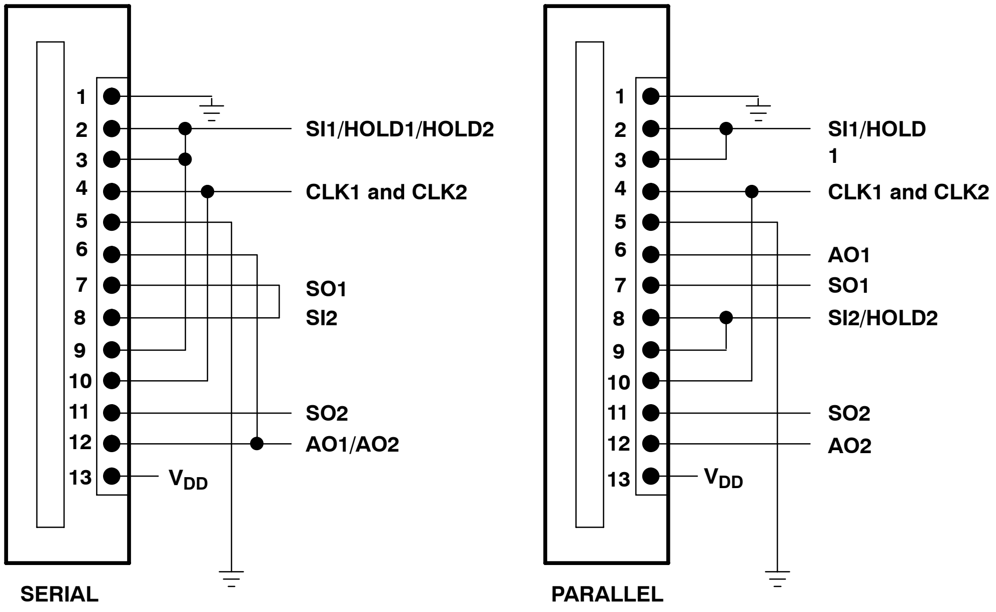


Figure 9. Operational Connections

APPLICATION INFORMATION

Integration Time

The integration time of the linear array is the period during which light is being sampled and charge is being accumulated in the integrating capacitors. The flexibility to adjust the integration period to obtain a desirable output voltage while avoiding saturation for a wide range of light levels is a powerful and useful feature of the TAOS TSL14xx linear array family.

The integration time is the time between two consecutive serial input (SI) high pulses minus 18 clock periods as long as that value falls in the range between the minimum and maximum limits for integration time. Sending a high pulse to SI (observing timing rules for setup and hold to clock edge) starts a new cycle of pixel output and integration setup. However, a minimum of 769 clocks must occur before the next high pulse is applied to SI. It is not necessary to send SI immediately on/after the 769 clocks. A wait of up to 100 ms can be added to increase the integration time to obtain a higher output voltage in low light situations.

It is a good practice on initial power up to run the clock a few times before the first SI pulse. After that, the SI pulse is valid between the time required to get 769 clock edges and at a maximum of 100 ms.

It is not necessary to continue clocking the device after the 769th clock. The output will go into a Hi-Z state after the 769th high clock edge. It is good practice to leave the clock in a low state when inactive, because the SI high pulse is in relation to a low to high transition on the clock.

If the amount of light incident on the array during a given integration period produces a saturated output (Max Voltage output), then the data is not accurate. In this case, the integration period should be reduced until the analog output voltage for each pixel falls below the saturation level. The goal of reducing the period of time the light sampling window is active is to lower the output voltage level to prevent saturation. However, the integration time must be greater than or equal to the minimum integration period. The minimum integration time shown in this datasheet is based on the maximum clock frequency of 8 MHz.

The minimum integration period for any given array is determined by the time required to clock out all the pixels in the array and the time to discharge the pixels between frames. Therefore, the minimum integration period is a function of the clock frequency and the number of pixels in the array. A slower clock speed increases the minimum integration time, which will reduce the maximum light level for saturation on the output.

The minimum integration time $t_{(int)}$ is defined by the following formula:

$$T_{int(min)} = (\text{number of pixels} - \text{setup clocks}) \times \text{clock period} + \text{charge transfer time}$$

In the case of the TSL1406R operating in serial mode with the maximum clock frequency of 8 MHz, the minimum integration time would be:

$$T_{int(min)} = (768 - 18) \times 0.125\ \mu s + 20\ \mu s$$

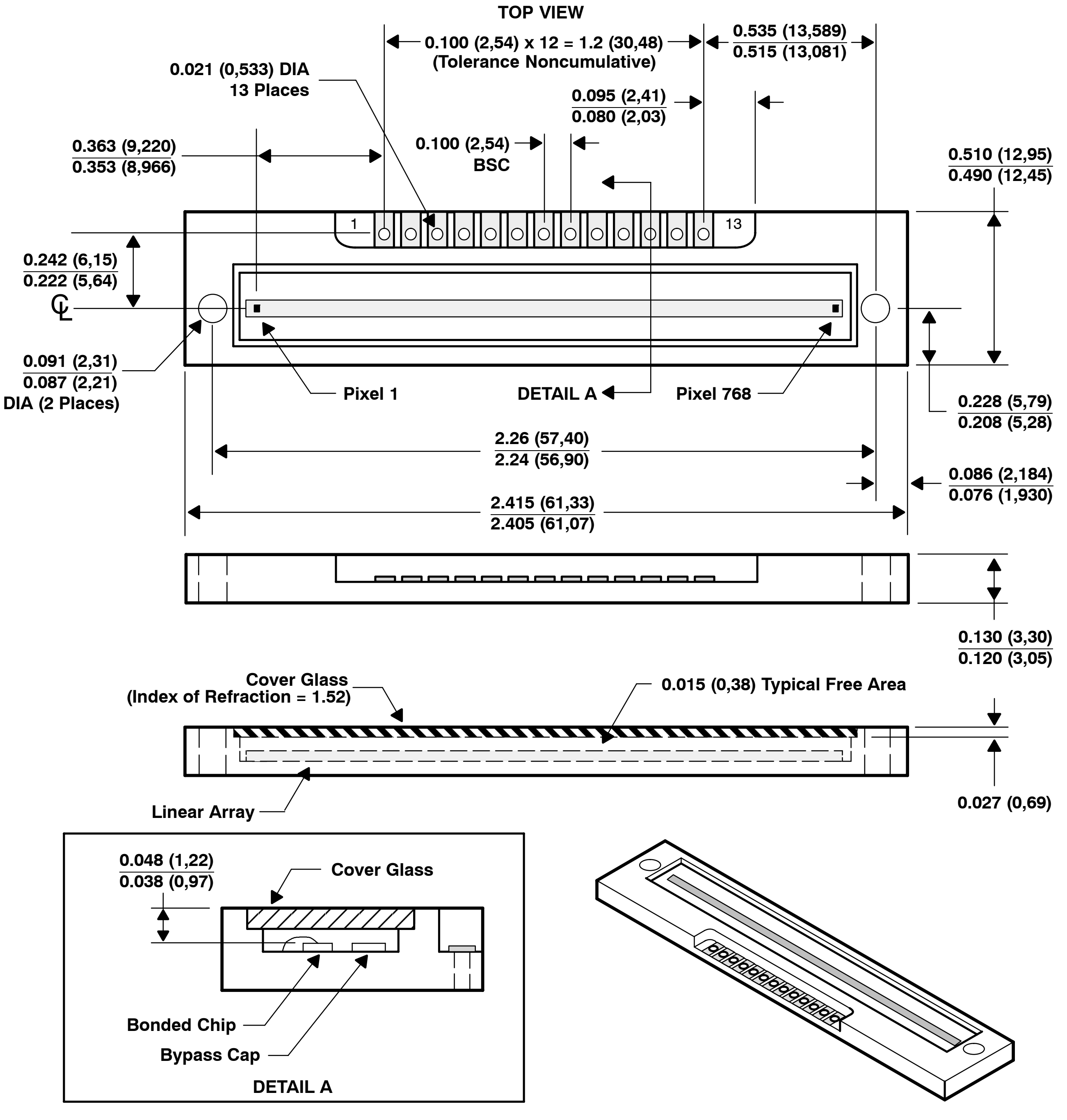
If the light intensity produces an output below desired signal levels, the output voltage level can be increased by increasing the integration period, provided that the maximum integration time is not exceeded. The maximum integration time is limited by the length of time the pixels integrating capacitors can hold their accumulated charge. This value is typically 100 ms.

It should be noted that the light that is sampled during one integration period is made available on the analog output during the next integration period and is clocked out sequentially at a rate of one pixel per clock period.

In other words, at any given time, two frames of data are being handled by the linear array: one stored frame is clocked out as the next frame is being integrated.

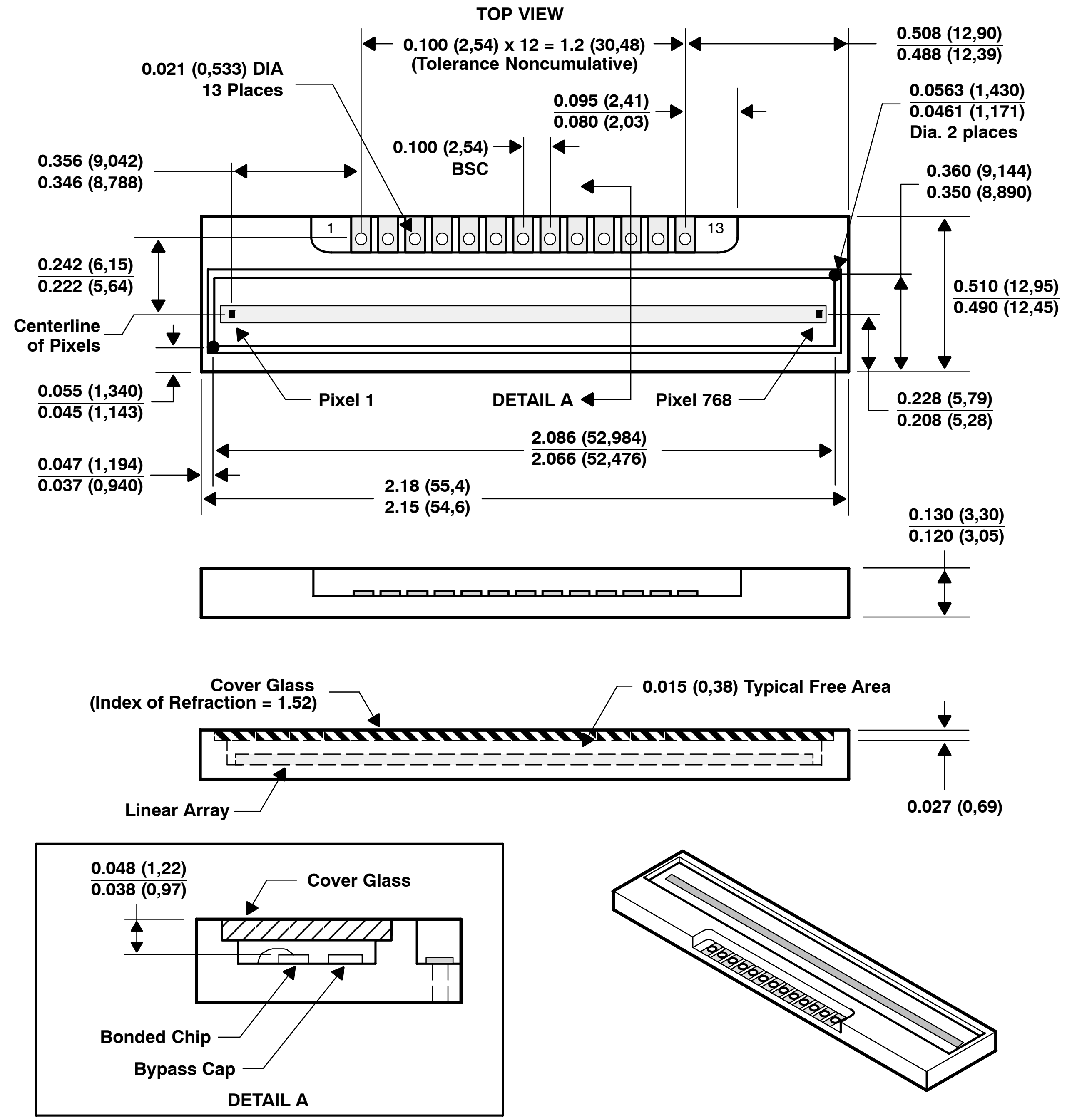
The A/D conversion is likely to be the speed bottleneck. The voltage output is available for the whole period of the clock. So the setup and hold time required for the A/D process must be compared to the clock period.

MECHANICAL DATA



NOTES: A. All linear dimensions are in inches (millimeters).
B. Pixel centers are located along the centerline of the mounting holes.
C. This drawing is subject to change without notice.

Figure 10. TSL1406R Mechanical Specifications



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Figure 11. TSL1406RS Mechanical Specifications

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