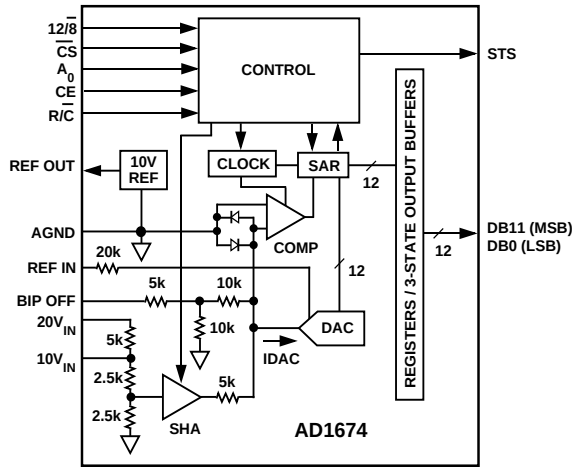
12-Bit 100 kSPS A/D Converter

AD1674*

FEATURES
Complete Monolithic 12-Bit 10 μs Sampling ADC
On-Board Sample-and-Hold Amplifier
Industry Standard Pinout
8- and 16-Bit Microprocessor Interface
AC and DC Specified and Tested
Unipolar and Bipolar Inputs
±5 V, ±10 V, 0 V–10 V, 0 V–20 V Input Ranges
Commercial, Industrial and Military Temperature Range Grades
MIL-STD-883 and SMD Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1674 is a complete, multipurpose, 12-bit analog-to-digital converter, consisting of a user-transparent onboard sample-and-hold amplifier (SHA), 10 volt reference, clock and three-state output buffers for microprocessor interface.

The AD1674 is pin compatible with the industry standard AD574A and AD674A, but includes a sampling function while delivering a faster conversion rate. The on-chip SHA has a wide input bandwidth supporting 12-bit accuracy over the full Nyquist bandwidth of the converter.

The AD1674 is fully specified for ac parameters (such as S/(N+D) ratio, THD, and IMD) and dc parameters (offset, full-scale error, etc.). With both ac and dc specifications, the AD1674 is ideal for use in signal processing and traditional dc measurement applications.

The AD1674 design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic.

Five different temperature grades are available. The AD1674J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from –40°C to +85°C; the AD1674T grade is specified from –55°C to +125°C. The J and K grades are available in both 28-lead plastic DIP and SOIC. The A and B grade devices are available in 28-lead hermetically sealed ceramic DIP and 28-lead SOIC. The T grade is available in 28-lead hermetically sealed ceramic DIP.

***Protected by U. S. Patent Nos. 4,962,325; 4,250,445; 4,808,908; RE30586**.

PRODUCT HIGHLIGHTS

1. Industry Standard Pinout: The AD1674 utilizes the pinout established by the industry standard AD574A and AD674A.
2. Integrated SHA: The AD1674 has an integrated SHA which supports the full Nyquist bandwidth of the converter. The SHA function is transparent to the user; no wait-states are needed for SHA acquisition.
3. DC and AC Specified: In addition to traditional dc specifications, the AD1674 is also fully specified for frequency domain ac parameters such as total harmonic distortion, signal-to-noise ratio and input bandwidth. These parameters can be tested and guaranteed as a result of the onboard SHA.
4. Analog Operation: The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 V to +10 V and 0 V to +20 V unipolar, –5 V to +5 V and –10 V to +10 V bipolar. The AD1674 operates on +5 V and ±12 V or ±15 V power supplies.
5. Flexible Digital Interface: On-chip multiple-mode three-state output buffers and interface logic allow direct connection to most microprocessors.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD1674–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5% unless otherwise noted)

Parameter	AD1674J Min	AD1674J Typ	AD1674J Max	AD1674K Min	AD1674K Typ	AD1674K Max	Unit
RESOLUTION	12			12			Bits
INTEGRAL NONLINEARITY (INL)			±1			±1/2	LSB
DIFFERENTIAL NONLINEARITY (DNL) (No Missing Codes)	12			12			Bits
UNIPOLAR OFFSET[1] @ +25°C			±3			±2	LSB
BIPOLAR OFFSET[1] @ +25°C			±6			±4	LSB
FULL-SCALE ERROR[1, 2] @ +25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.25	% of FSR
TEMPERATURE RANGE	0		+70	0		+70	°C
TEMPERATURE DRIFT[3]							
Unipolar Offset[2]			±2			±1	LSB
Bipolar Offset[2]			±2			±1	LSB
Full-Scale Error[2]			±6			±3	LSB
POWER SUPPLY REJECTION							
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2	LSB
V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2			±1	LSB
ANALOG INPUT							
Input Ranges							
Bipolar	–5		+5	–5		+5	Volts
	–10		+10	–10		+10	Volts
Unipolar	0		+10	0		+10	Volts
	0		+20	0		+20	Volts
Input Impedance							
10 Volt Span	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	kΩ
POWER SUPPLIES							
Operating Voltages							
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	–16.5		–11.4	–16.5		–11.4	Volts
Operating Current							
I_{LOGIC}		5	8		5	8	mA
I_{CC}		10	14		10	14	mA
I_{EE}		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads)[4] (External Load Should Not Change During Conversion			2.0			2.0	mA

NOTES
[1]Adjustable to zero.
[2]Includes internal voltage reference error.
[3]Maximum change from 25°C value to the value at T_{MIN} or T_{MAX}.
[4]Reference should be buffered for ±12 V operation.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

Parameter	AD1674A Min	AD1674A Typ	AD1674A Max	AD1674B Min	AD1674B Typ	AD1674B Max	AD1674T Min	AD1674T Typ	AD1674T Max	Unit
RESOLUTION	12			12			12			Bits
INTEGRAL NONLINEARITY (INL)			±1			±1/2			±1/2	LSB
			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY (DNL) (No Missing Codes)	12			12			12			Bits
UNIPOLAR OFFSET[1] @ +25°C			±2			±2			±2	LSB
BIPOLAR OFFSET[1] @ +25°C			±6			±3			±3	LSB
FULL-SCALE ERROR[1, 2] @ +25°C (with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.125		0.1	0.125	% of FSR
TEMPERATURE RANGE	–40		+85	–40		+85	–55		+125	°C
TEMPERATURE DRIFT[3]										
Unipolar Offset[2]			±2			±1			±1	LSB
Bipolar Offset[2]			±2			±1			±2	LSB
Full-Scale Error[2]			±8			±5			±7	LSB
POWER SUPPLY REJECTION										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	–5		+5	–5		+5	–5		+5	Volts
	–10		+10	–10		+10	–10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20		0	+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Voltages										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	–16.5		–11.4	–16.5		–11.4	–16.5		–11.4	Volts
Operating Current										
I_{LOGIC}		5	8		5	8		5	8	mA
I_{CC}		10	14		10	14		10	14	mA
I_{EE}		14	18		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads)[4] (External Load Should Not Change During Conversion			2.0			2.0			2.0	mA

AD1674–SPECIFICATIONS

AC SPECIFICATIONS

(T_{MIN} to T_{MAX}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ±10% or –12 V ± 5%, f_{SAMPLE} = 100 kSPS, f_{IN} = 10 kHz, stand-alone mode unless otherwise noted)[1]

Parameter	AD1674J/A Min	AD1674J/A Typ	AD1674J/A Max	AD1674K/B/T Min	AD1674K/B/T Typ	AD1674K/B/T Max	Units
Signal to Noise and Distortion (S/N+D) Ratio[2, 3]	69	70		70	71		dB
Total Harmonic Distortion (THD)[4]		–90	–82 0.008		–90	–82 0.008	dB %
Peak Spurious or Peak Harmonic Component		–92	–82		–92	–82	dB
Full Power Bandwidth Full Linear Bandwidth		1 500		1 500			MHz kHz
Intermodulation Distortion (IMD)[5] Second Order Products Third Order Products		 –90 –90	 –80 –80		 –90 –90	 –80 –80	 dB dB
SHA (Specifications are Included in Overall Timing Specifications) Aperture Delay Aperture Jitter Acquisition Time		 50 250 1			 50 250 1		 ns ps µs

DIGITAL SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		+2.0	V_{LOGIC} +0.5 V	V
V_{IL}	Low Level Input Voltage		–0.5	+0.8	V
I_{IH}	High Level Input Current (V_{IN} = 5 V)	$V_{IN} = V_{LOGIC}$	–10	+10	µA
I_{IL}	Low Level Input Current (V_{IN} = 0 V)	V_{IN} = 0 V	–10	+10	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.5 mA	+2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		+0.4	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 to V_{LOGIC}	–10	+10	µA
C_{OZ}	High-Z Output Capacitance			10	pF

NOTES

[1]f_{IN} amplitude = –0.5 dB (9.44 V p-p) 10 V bipolar mode unless otherwise noted. All measurements referred to –0 dB (9.997 V p-p) input signal unless otherwise noted.

[2]Specified at worst case temperatures and supplies after one minute warm-up.

[3]See Figures 12 and 13 for other input frequencies and amplitudes.

[4]See Figure 11.

[5]fa = 9.08 kHz, fb = 9.58 kHz with f_{SAMPLE} = 100 kHz. See *Definition of Specifications* section and Figure 15.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ±10%, V_{EE} = –15 V ± 10% or –12 V ± 5%; V_{IL} = 0.4 V, V_{IH} = 2.4 V unless otherwise noted)

CONVERTER START TIMING (Figure 1)

Parameter	Symbol	J, K, A, B, Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Conversion Time								
8-Bit Cycle	t_C		7	8		7	8	µs
12-Bit Cycle	t_C		9	10		9	10	µs
STS Delay from CE	t_{DSC}			200			225	ns
CE Pulse Width	t_{HEC}	50			50			ns
$\overline{CS}$ to CE Setup	t_{SSC}	50			50			ns
$\overline{CS}$ Low During CE High	t_{HSC}	50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRC}	50			50			ns
R/$\overline{C}$ Low During CE High	t_{HRC}	50			50			ns
A_0 to CE Setup	t_{SAC}	0			0			ns
A_0 Valid During CE High	t_{HAC}	50			50			ns

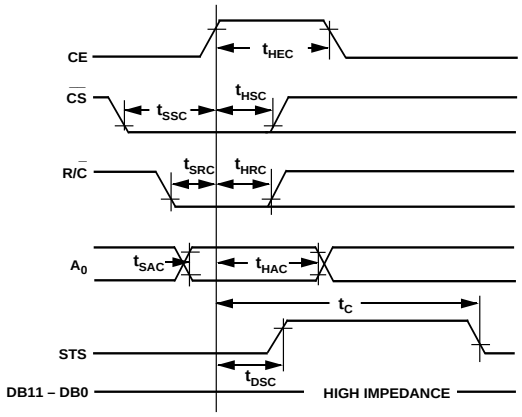


Figure 1. Converter Start Timing

READ TIMING—FULL CONTROL MODE (Figure 2)

Parameter	Symbol	J, K, A, B, Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Access Time	t_{DD}[1]		75	150		75	150	ns
Data Valid After CE Low	t_{HD}	25[2]			25[2]			ns
		20[3]			15[4]			ns
Output Float Delay	t_{HL}[5]			150			150	ns
$\overline{CS}$ to CE Setup	t_{SSR}	50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRR}	0			0			ns
A_0 to CE Setup	t_{SAR}	50			50			ns
$\overline{CS}$ Valid After CE Low	t_{HSR}	0			0			ns
R/$\overline{C}$ High After CE Low	t_{HRR}	0			0			ns
A_0 Valid After CE Low	t_{HAR}	50			50			ns

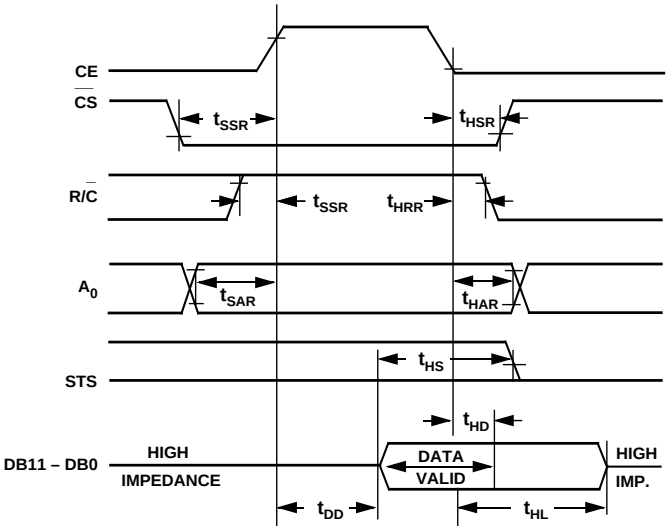


Figure 2. Read Timing

NOTES
[1]t_{DD} is measured with the load circuit of Figure 3 and is defined as the time required for an output to cross 0.4 V or 2.4 V.
[2]0°C to T_{MAX}.
[3]At –40°C.
[4]At –55°C.
[5]t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 3.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

Test	V_{CP}	C_{OUT}
Access Time High Z to Logic Low	5 V	100 pF
Float Time Logic High to High Z	0 V	10 pF
Access Time High Z to Logic High	0 V	100 pF
Float Time Logic Low to High Z	5 V	10 pF

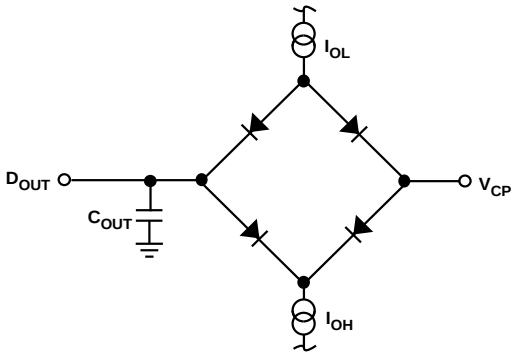


Figure 3. Load Circuit for Bus Timing Specifications

TIMING—STAND-ALONE MODE (Figures 4a and 4b)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Data Access Time	t_{DDR}			150			150	ns
Low R/$\overline{C}$ Pulse Width	t_{HRL}	50			50			ns
STS Delay from R/$\overline{C}$	t_{DS}			200			225	ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}	25			25			ns
STS Delay After Data Valid	t_{HS}	0.6	0.8	1.2	0.6	0.8	1.2	µs
High R/$\overline{C}$ Pulse Width	t_{HRH}	150			150			ns

NOTE
All min and max specifications are guaranteed.
Specifications subject to change without notice.

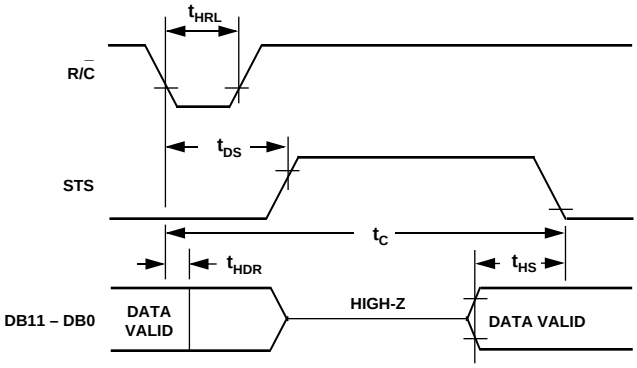


Figure 4a. Stand-Alone Mode Timing Low Pulse for R/$\overline{C}$

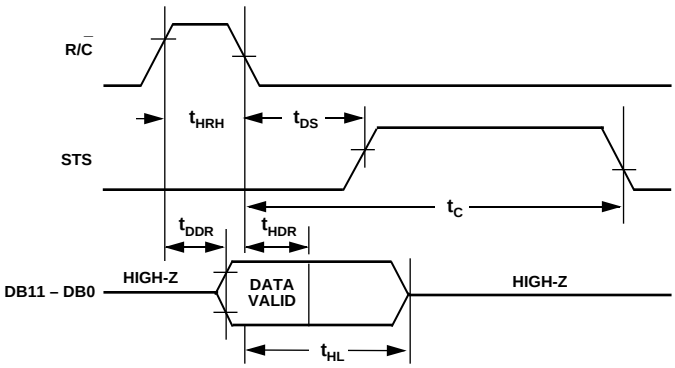


Figure 4b. Stand-Alone Mode Timing High Pulse for R/$\overline{C}$

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . . 0 to + 16.5 V
V_{EE} to Digital Common . . . . . 0 to –16.5 V
V_{LOGIC} to Digital Common . . . . . 0 V to +7 V
Analog Common to Digital Common . . . . . ±1 V
Digital Inputs to Digital Common . . . –0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . . V_{EE} to +24 V
REF OUT . . . . . Indefinite Short to Common
. . . . . Momentary Short to V_{CC}
Junction Temperature . . . . . +175°C
Power Dissipation . . . . . 825 mW
Lead Temperature, Soldering (10 sec) . . . . . +300°C, 10 sec
Storage Temperature . . . . . –65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1674 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model[1]	Temperature Range	INL (T_{MIN} to T_{MAX})	S/(N+D) (T_{MIN} to T_{MAX})	Package Description	Package Option[2]
AD1674JN	0°C to +70°C	±1 LSB	69 dB	Plastic DIP	N-28
AD1674KN	0°C to +70°C	±1/2 LSB	70 dB	Plastic DIP	N-28
AD1674JR	0°C to +70°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674KR	0°C to +70°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AR	–40°C to +85°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674BR	–40°C to +85°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AD	–40°C to +85°C	±1 LSB	69 dB	Ceramic DIP	D-28
AD1674BD	–40°C to +85°C	±1/2 LSB	70 dB	Ceramic DIP	D-28
AD1674TD	–55°C to +125°C	±1 LSB	70 dB	Ceramic DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD1674/883B data sheet. SMD is also available.
[2]N = Plastic DIP; D = Hermetic Ceramic DIP; R = Plastic SOIC.