

FEATURES

High common-mode input voltage range

± 120 V at $V_S = \pm 15$ V

Gain range 0.1 to 100

Operating temperature range: -40°C to $\pm 85^\circ\text{C}$

Supply voltage range

Dual supply: ± 2.25 V to ± 18 V

Single supply: 4.5 V to 36 V

Excellent ac and dc performance

Offset temperature stability RTI: $10 \mu\text{V}/^\circ\text{C}$ max

Offset: ± 1.5 V mV max

CMRR RTI: 75 dB min, dc to 500 Hz, $G = +1$

APPLICATIONS

High voltage current shunt sensing

Programmable logic controllers

Analog input front end signal conditioning

$+5$ V, $+10$ V, ± 5 V, ± 10 V, and 4 to 20 mA

Isolation

Sensor signal conditioning

Power supply monitoring

Electrohydraulic control

Motor control

GENERAL DESCRIPTION

The AD628 is a precision difference amplifier that combines excellent dc performance with high common-mode rejection over a wide range of frequencies. When used to scale high voltages, it allows simple conversion of standard control voltages or currents for use with single-supply ADCs. A wideband feedback loop minimizes distortion effects due to capacitor charging of Σ - Δ ADCs.

A reference pin (V_{REF}) provides a dc offset for converting bipolar to single-sided signals. The AD628 converts $+5$ V, $+10$ V, ± 5 V, ± 10 V, and 4 to 20 mA input signals to a single-ended output within the input range of single-supply ADCs.

The AD628 has an input common-mode and differential mode operating range of ± 120 V. The high common-mode input impedance makes the device well-suited for high voltage measurements across a shunt resistor. The buffer amplifier's inverting input is available for making a remote Kelvin connection.

FUNCTIONAL BLOCK DIAGRAM

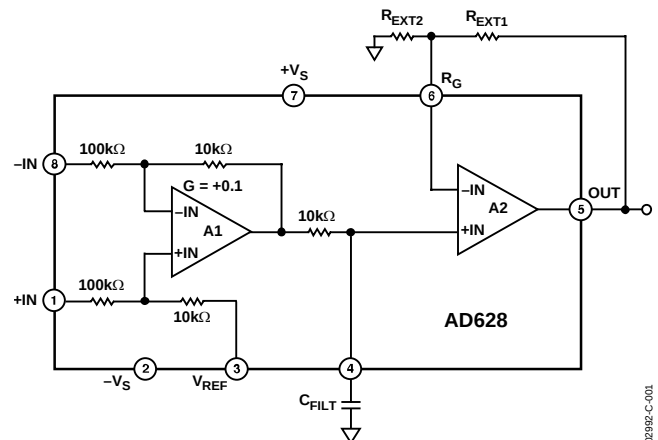


Figure 1.

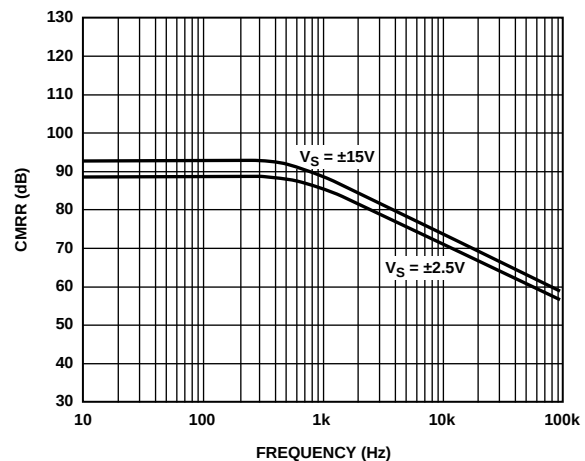


Figure 2. CMRR vs. Frequency of the AD628

A precision 10 k Ω resistor connected to an external pin is provided for either a low-pass filter or to attenuate large differential input signals. A single capacitor implements a low-pass filter. The AD628 operates from single and dual supplies and is available in an 8-lead SOIC or 8-lead MSOP package. It operates over the standard industrial temperature range of -40°C to $+85^\circ\text{C}$.

Rev. E

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3/05—Rev. C to Rev. D

Updated Format.....	Universal
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4/04—Rev. B to Rev. C

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11/02—Rev. 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $R_{EXT1} = 10\text{ k}\Omega$, $R_{EXT2} = \infty$, $V_{REF} = 0$, unless otherwise noted.

Table 1.

Parameter	Conditions	AD628AR			AD628ARM			Unit
		Min	Typ	Max	Min	Typ	Max	
DIFFERENTIAL AMP + OUTPUT AMP								
Gain Equation	$G = +0.1(1 + R_{EXT1}/R_{EXT2})$							V/V
Gain Range	See Figure 29	0.1 ¹		100	0.1 ¹		100	V/V
Offset Voltage	$V_{CM} = 0\text{ V}$; RTI of input pins ² ; Output amp $G = +1$	−1.5		+1.5	−1.5		+1.5	mV
vs. Temperature			4	8		4	8	μV/°C
CMRR ³	RTI of input pins; $G = +0.1$ to +100	75			75			dB
	500 Hz	75			75			dB
Minimum CMRR Over Temperature	−40°C to +85°C	70			70			dB
vs. Temperature			1	4		1	4	(μV/V)/°C
PSRR (RTI)	$V_S = \pm 10\text{ V}$ to $\pm 18\text{ V}$	77	94		77	94		dB
Input Voltage Range								
Common Mode		−120		+120	−120		+120	V
Differential		−120		+120	−120		+120	V
Dynamic Response								
Small Signal BW −3 dB	$G = +0.1$		600			600		kHz
Full Power Bandwidth			5			5		kHz
Settling Time	$G = +0.1$, to 0.01%, 100 V step			40			40	μs
Slew Rate			0.3			0.3		V/μs
Noise (RTI)								
Spectral Density	1 kHz		300			300		nV/√Hz
	0.1 Hz to 10 Hz		15			15		μV p-p
DIFFERENTIAL AMP								
Gain			0.1			0.1		V/V
Error		−0.1	+0.01	+0.1	−0.1	+0.01	+0.1	%
vs. Temperature				5			5	ppm/°C
Nonlinearity				5			5	ppm
vs. Temperature			3	10		3	10	ppm
Offset Voltage	RTI of input pins	−1.5		+1.5	−1.5		+1.5	mV
vs. Temperature				8			8	μV/°C
Input Impedance								
Differential			220			220		kΩ
Common Mode			55			55		kΩ
CMRR ⁴	RTI of input pins; $G = +0.1$ to +100	75			75			dB
	500 Hz	75			75			dB
Minimum CMRR Over Temperature	−40°C to +85°C	70			70			dB
vs. Temperature			1	4		1	4	(μV/V)/°C
Output Resistance			10			10		kΩ
Error		−0.1		+0.1	−0.1		+0.1	%

AD628

Parameter	Conditions	AD628AR			AD628ARM			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT AMPLIFIER								
Gain Equation	$G = (1 + R_{EXT1}/R_{EXT2})$							V/V
Nonlinearity	$G = +1, V_{OUT} = \pm 10\text{ V}$			0.5			0.5	ppm
Offset Voltage	RTI of output amp	−0.15		+0.15	−0.15		+0.15	mV
vs. Temperature				0.6			0.6	μV/°C
Output Voltage Swing	$R_L = 10\text{ k}\Omega$	−14.2		+14.1	−14.2		+14.1	V
	$R_L = 2\text{ k}\Omega$	−13.8		+13.6	−13.8		+13.6	V
Bias Current			1.5	3		1.5	3	nA
Offset Current			0.2	0.5		0.2	0.5	nA
CMRR	$V_{CM} = \pm 13\text{ V}$	130			130			dB
Open-Loop Gain	$V_{OUT} = \pm 13\text{ V}$	130			130			dB
POWER SUPPLY								
Operating Range		±2.25		±18	±2.25		±18	V
Quiescent Current				1.6			1.6	mA
TEMPERATURE RANGE								
		−40		+85	−40		+85	°C

¹ To use a lower gain, see the Gain Adjustment section.

² The addition of the difference amp's and output amp's offset voltage does not exceed this specification.

³ Error due to common mode as seen at the output: $V_{OUT} = \left[\frac{(0.1)(V_{CM})}{\frac{75}{10^{20}}} \right] \times [\text{Output Amplifier Gain}]$

⁴ Error due to common mode as seen at the output of A1: $V_{OUT A1} = \left[\frac{(0.1)(V_{CM})}{\frac{75}{10^{20}}} \right]$

$T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $R_L = 2\text{ k}\Omega$, $R_{EXT1} = 10\text{ k}\Omega$, $R_{EXT2} = \infty$, $V_{REF} = 2.5$, unless otherwise noted.

Table 2.

Parameter	Conditions	AD628AR			AD628ARM			Unit
		Min	Typ	Max	Min	Typ	Max	
DIFFERENTIAL AMP + OUTPUT AMP								
Gain Equation	$G = +0.1(1 + R_{EXT1}/R_{EXT2})$							V/V
Gain Range	See Figure 29	0.1 ¹		100	0.1 ¹		100	V/V
Offset Voltage	$V_{CM} = 2.25\text{ V}$; RTI of input pins ² ; Output Amp $G = +1$	-3.0		+3.0	-3.0		+3.0	mV
vs. Temperature			6	15		6	15	$\mu\text{V}/^{\circ}\text{C}$
CMRR ³	RTI of input pins; $G = +0.1$ to +100 500 Hz	75			75			dB
		75			75			dB
Minimum CMRR Over Temperature	-40°C to +85°C	70			70			dB
vs. Temperature			1	4		1	4	$(\mu\text{V}/\text{V})/^{\circ}\text{C}$
PSRR (RTI)	$V_S = 4.5\text{ V}$ to 10 V	77	94		77	94		dB
Input Voltage Range								
Common Mode ⁴		-12		+17	-12		+17	V
Differential		-15		+15	-15		+15	V
Dynamic Response								
Small Signal BW -3 dB	$G = +0.1$		440			440		kHz
Full Power Bandwidth			30			30		kHz
Settling Time	$G = +0.1$, to 0.01%, 30 V step		15			15		μs
Slew Rate			0.3			0.3		V/ μs
Noise (RTI)								
Spectral Density	1 kHz		350			350		nV/ $\sqrt{\text{Hz}}$
	0.1 Hz to 10 Hz		15			15		$\mu\text{V p-p}$
DIFFERENTIAL AMP								
Gain			0.1			0.1		V/V
Error		-0.1	+0.01	+0.1	-0.1	+0.01	+0.1	%
Nonlinearity				3			3	ppm
vs. Temperature			3	10		3	10	ppm
Offset Voltage	RTI of input pins	-2.5		+2.5	-2.5		+2.5	mV
vs. Temperature				10			10	$\mu\text{V}/^{\circ}\text{C}$
Input Impedance								
Differential			220			220		k Ω
Common Mode			55			55		k Ω
CMRR ⁵	RTI of input pins; $G = +0.1$ to +100 500 Hz	75			75			dB
		75			75			dB
Minimum CMRR Over Temperature	-40°C to +85°C	70			70			dB
vs. Temperature			1	4		1	4	$(\mu\text{V}/\text{V})/^{\circ}\text{C}$
Output Resistance			10			10		k Ω
Error		-0.1		+0.1	-0.1		+0.1	%
OUTPUT AMPLIFIER								
Gain Equation	$G = (1 + R_{EXT1}/R_{EXT2})$							V/V
Nonlinearity	$G = +1$, $V_{OUT} = 1\text{ V}$ to 4 V			0.5			0.5	ppm
Output Offset Voltage	RTI of output amp	-0.15		0.15	-0.15		0.15	mV
vs. Temperature				0.6			0.6	$\mu\text{V}/^{\circ}\text{C}$
Output Voltage Swing	$R_L = 10\text{ k}\Omega$	0.9		4.1	0.9		4.1	V
	$R_L = 2\text{ k}\Omega$	1		4	1		4	V
Bias Current			1.5	3		1.5	3	nA
Offset Current			0.2	0.5		0.2	0.5	nA
CMRR	$V_{CM} = 1\text{ V}$ to 4 V	130			130			dB
Open-Loop Gain	$V_{OUT} = 1\text{ V}$ to 4 V	130			130			dB

AD628

Parameter	Conditions	AD628AR			AD628ARM			Unit
		Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY								
Operating Range		±2.25		+36	±2.25		+36	V
Quiescent Current				1.6			1.6	mA
TEMPERATURE RANGE		−40		+85	−40		+85	°C

¹ To use a lower gain, see the Gain Adjustment section.

² The addition of the difference amp's and output amp's offset voltage does not exceed this specification.

³ Error due to common mode as seen at the output: $V_{OUT} = \left[\frac{(0.1)(V_{CM})}{\frac{75}{10^{20}}} \right] \times [Output\ Amplifier\ Gain]$

⁴ Greater values of voltage are possible with greater or lesser values of V_{REF} .

⁵ Error due to common mode as seen at the output of A1: $V_{OUT\ A1} = \left[\frac{(0.1)(V_{CM})}{\frac{75}{10^{20}}} \right]$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation	See Figure 3
Input Voltage (Common Mode)	$\pm 120\text{ V}^1$
Differential Input Voltage	$\pm 120\text{ V}^1$
Output Short-Circuit Duration	Indefinite
Storage Temperature	-65°C to $+125^\circ\text{C}$
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Lead Temperature Range (10 sec Soldering)	300°C

¹ When using $\pm 12\text{ V}$ supplies or higher (see the Input Voltage Range section).

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

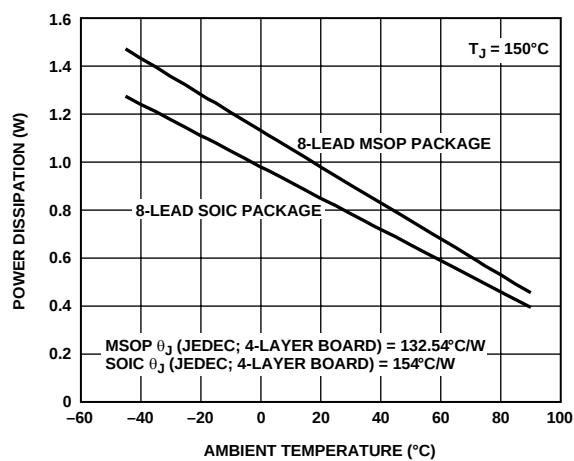


Figure 3. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

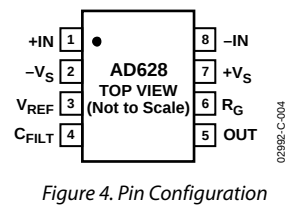


Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Descriptions
1	+IN	Noninverting Input
2	−VS	Negative Supply Voltage
3	VREF	Reference Voltage Input
4	CFILT	Filter Capacitor Connection
5	OUT	Amplifier Output
6	RG	Output Amplifier Inverting Input
7	+VS	Positive Supply Voltage
8	−IN	Inverting Input

TYPICAL PERFORMANCE CHARACTERISTICS

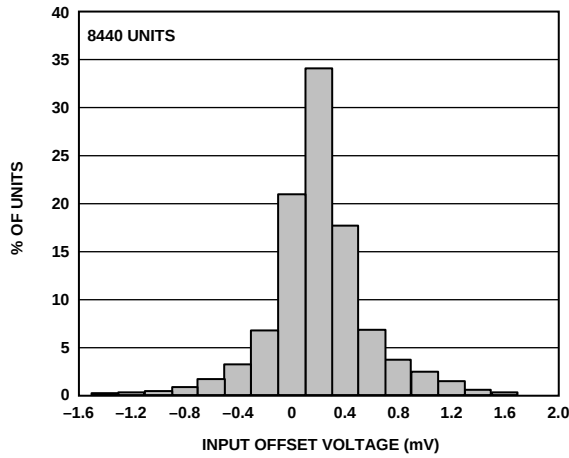


Figure 5. Typical Distribution of Input Offset Voltage, $V_S = \pm 15\text{ V}$, SOIC Package

02992-C-005

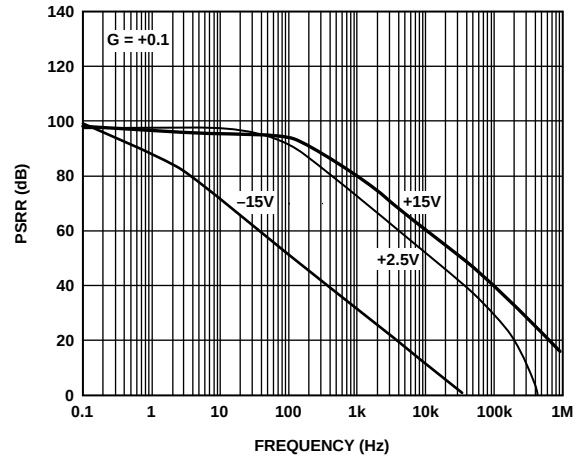


Figure 8. PSRR vs. Frequency, Single and Dual Supplies

02992-C-008

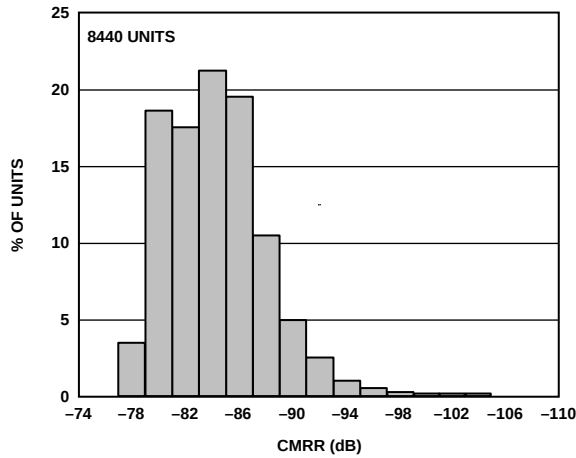


Figure 6. Typical Distribution of Common-Mode Rejection, SOIC Package

02992-C-006

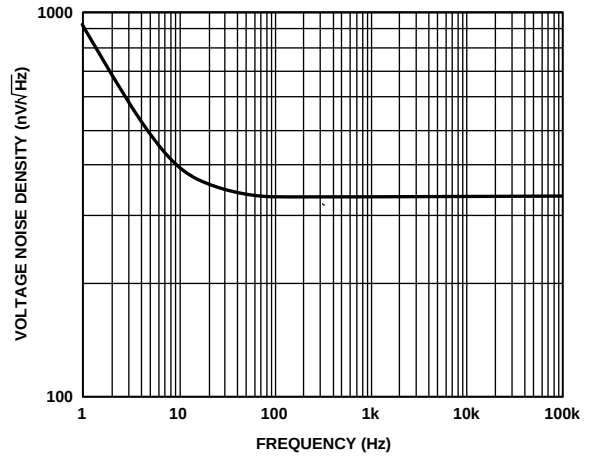


Figure 9. Voltage Noise Spectral Density, RTI, $V_S = \pm 15\text{ V}$

02992-C-009

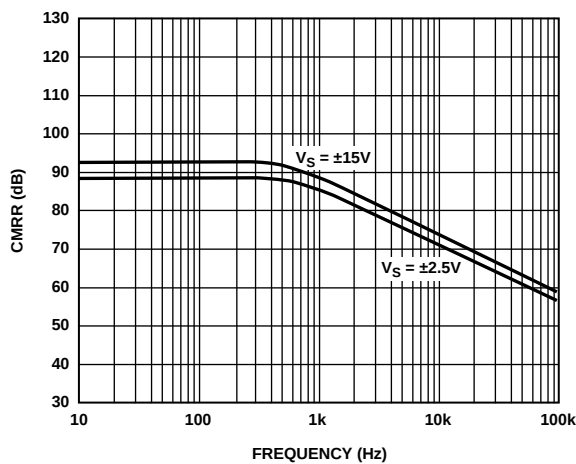


Figure 7. CMRR vs. Frequency

02992-C-007

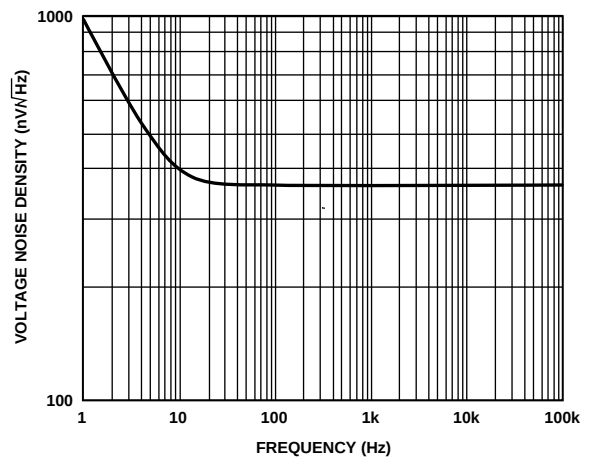


Figure 10. Voltage Noise Spectral Density, RTI, $V_S = \pm 2.5\text{ V}$

02992-C-010

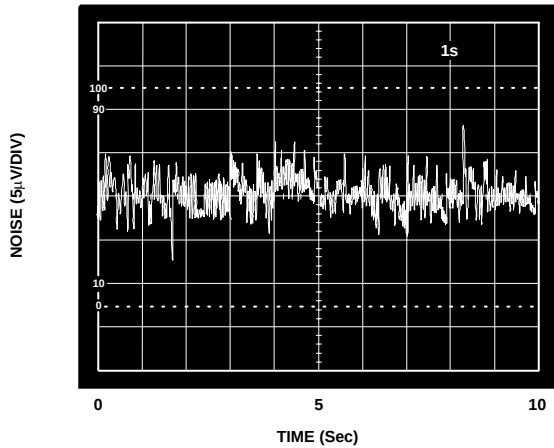


Figure 11. 0.1 Hz to 10 Hz Voltage Noise, RTI

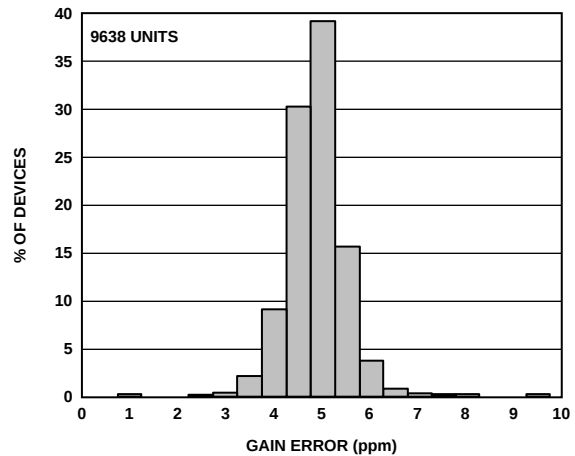


Figure 14. Typical Distribution of +1 Gain Error

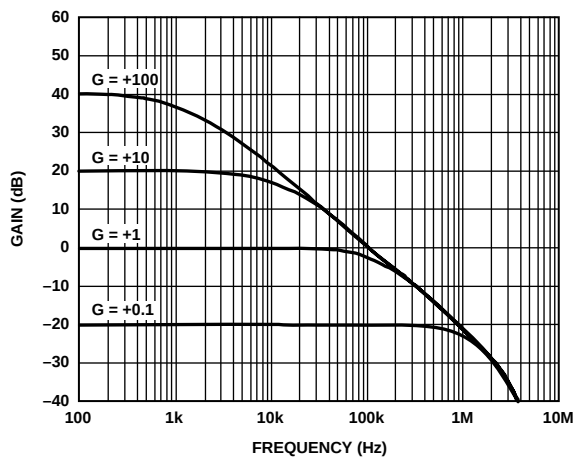


Figure 12. Small Signal Frequency Response, $V_{OUT} = 200 \text{ mV p-p}$, $G = +0.1, +1, +10, \text{ and } +100$

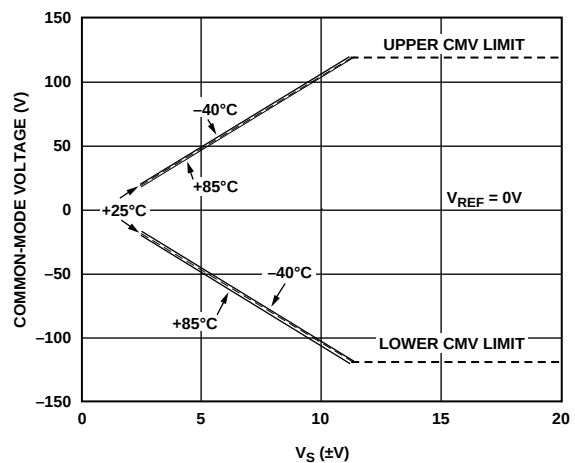


Figure 15. Common-Mode Operating Range vs. Power Supply Voltage for Three Temperatures

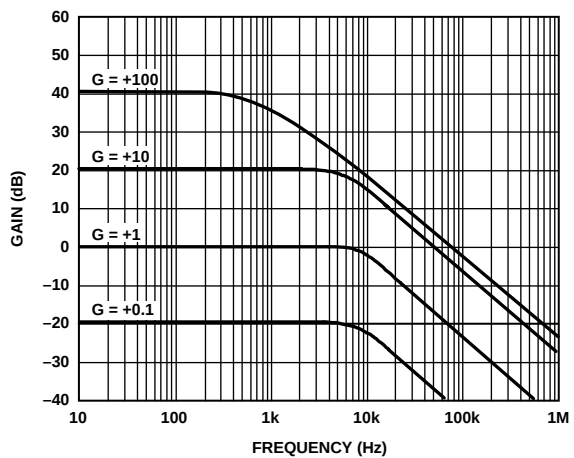


Figure 13. Large Signal Frequency Response, $V_{OUT} = 20 \text{ V p-p}$, $G = +0.1, +1, +10, \text{ and } +100$

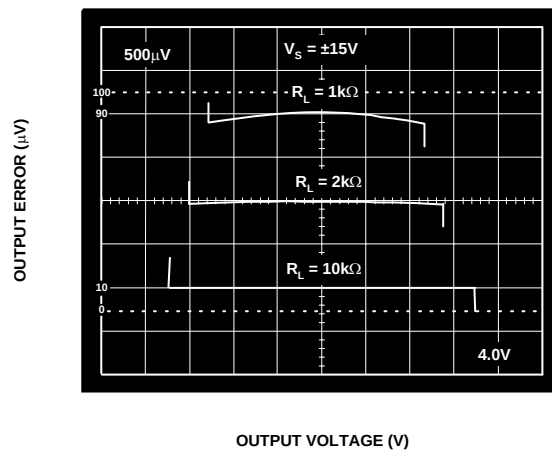


Figure 16. Normalized Gain Error vs. V_{OUT} , $V_S = \pm 15 \text{ V}$

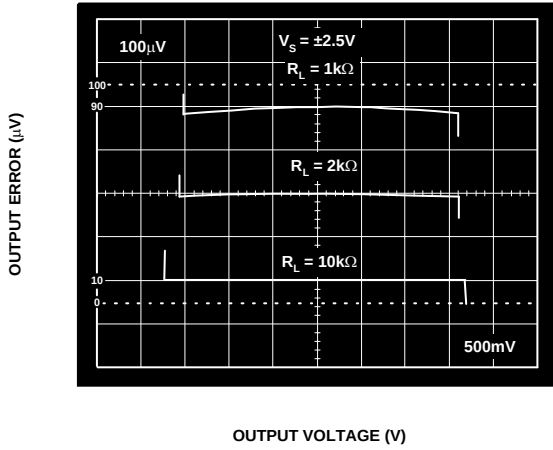


Figure 17. Normalized Gain Error vs. V_{OUT} , $V_S = \pm 2.5$ V

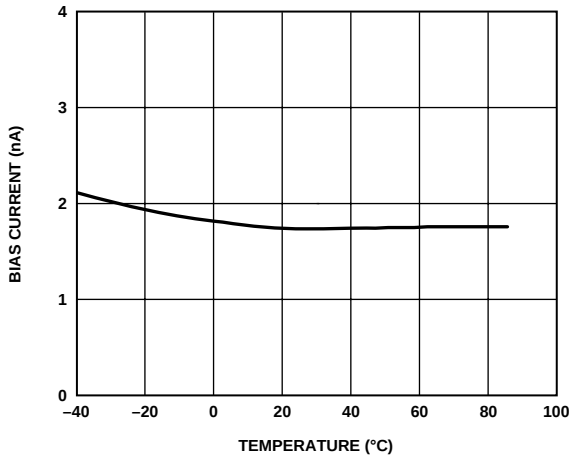


Figure 18. Bias Current vs. Temperature Buffer

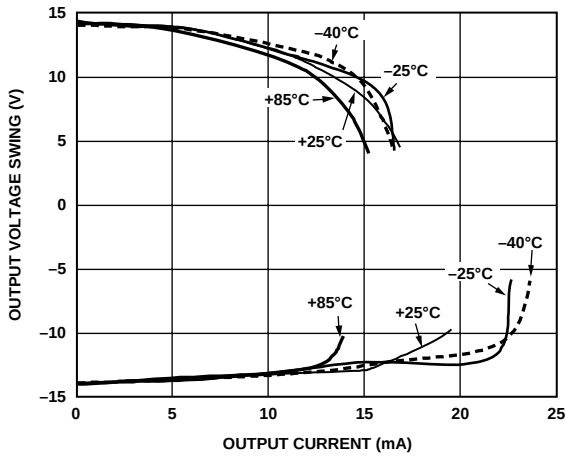


Figure 19. Output Voltage Operating Range vs. Output Current

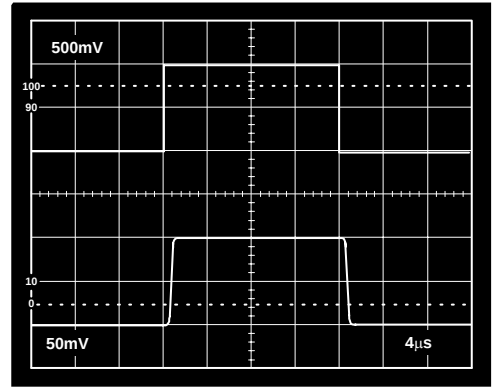


Figure 20. Small Signal Pulse Response, $R_L = 2$ k Ω , $C_L = 0$ pF, Top: Input, Bottom: Output

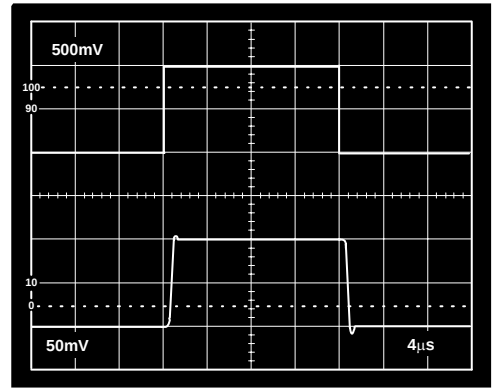


Figure 21. Small Signal Pulse Response, $R_L = 2$ k Ω , $C_L = 1000$ pF, Top: Input, Bottom: Output

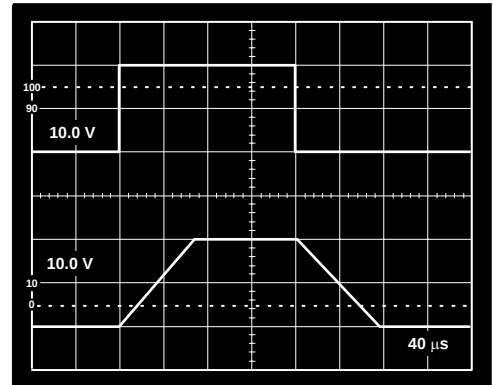


Figure 22. Large Signal Pulse Response, $R_L = 2$ k Ω , $C_L = 1000$ pF, Top: Input, Bottom: Output

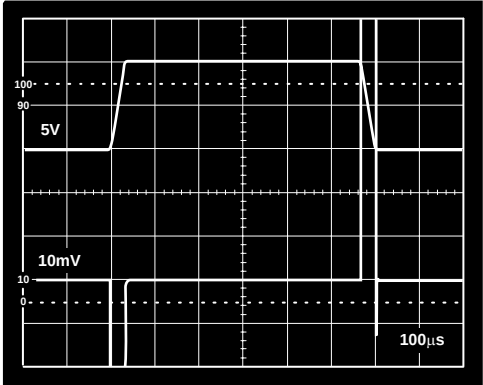


Figure 23. Settling Time to 0.01%, 0 V to 10 V Step

02992-C-023

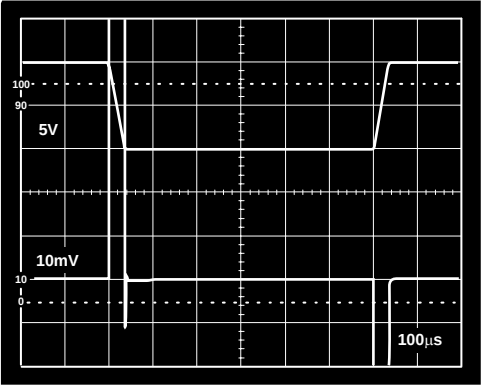


Figure 24. Settling Time to 0.01% 0 V to -10 V Step

02992-C-024

TEST CIRCUITS

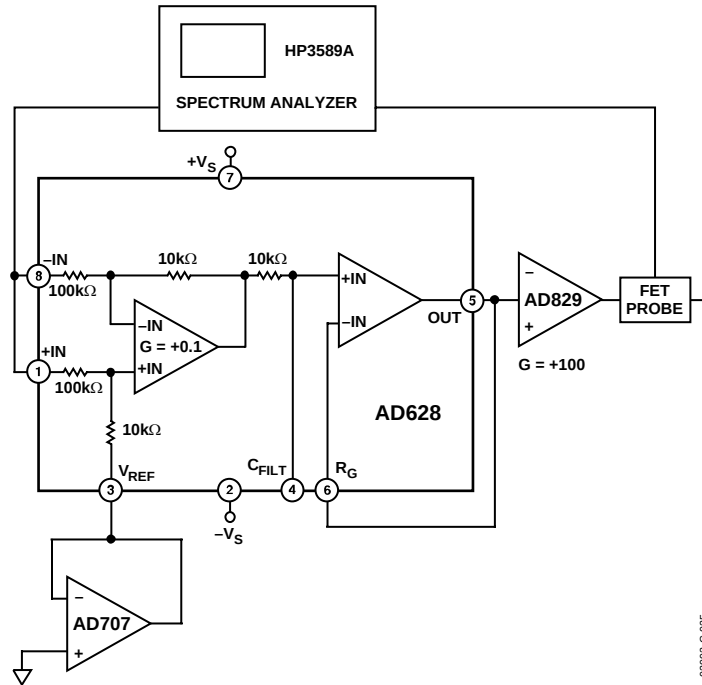


Figure 25. CMRR vs. Frequency

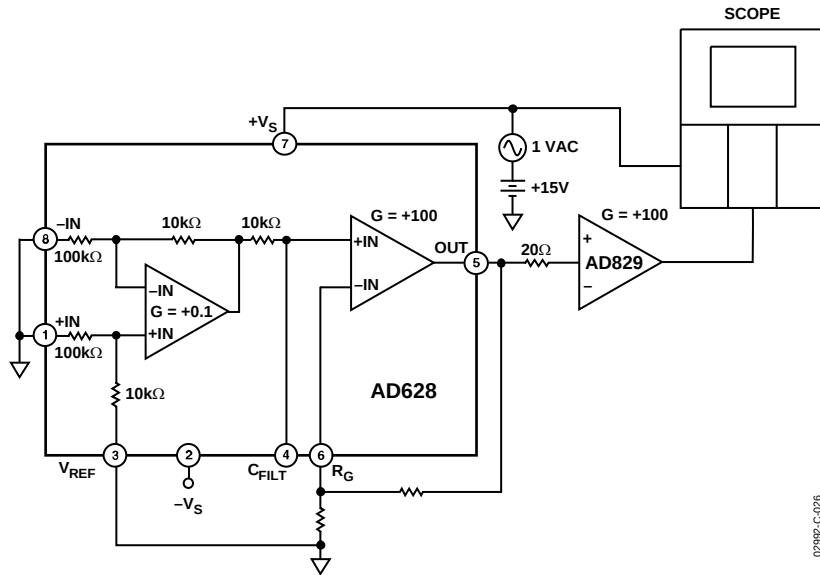


Figure 26. PSRR vs. Frequency

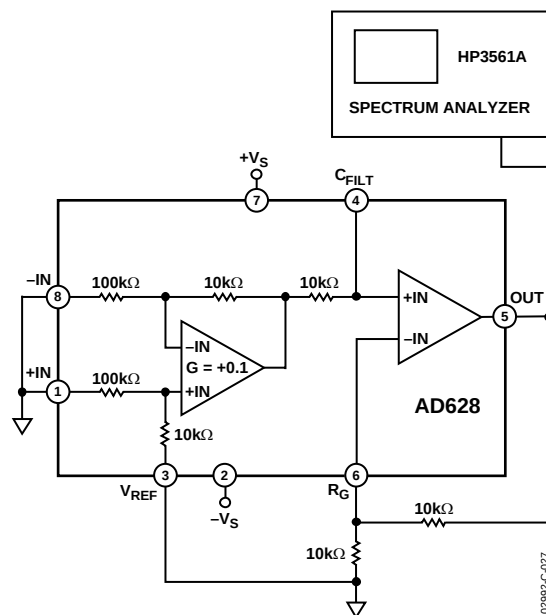


Figure 27. Noise Tests

THEORY OF OPERATION

The AD628 is a high common-mode voltage difference amplifier, combined with a user-configurable output amplifier (see Figure 28 and Figure 29). Differential mode voltages in excess of 120 V are accurately scaled by a precision 11:1 voltage divider at the input. A reference voltage input is available to the user at Pin 3 (V_{REF}). The output common-mode voltage of the difference amplifier is the same as the voltage applied to the reference pin. If the uncommitted amplifier is configured for gain, connecting Pin 3 to one end of the external gain resistor establishes the output common-mode voltage at Pin 5 (OUT).

The output of the difference amplifier is internally connected to a 10 k Ω resistor trimmed to better than $\pm 0.1\%$ absolute accuracy. The resistor is connected to the noninverting input of the output amplifier and is accessible to the user at Pin 4 (C_{FILT}). A capacitor may be connected to implement a low-pass filter, a resistor may be connected to further reduce the output voltage, or a clamp circuit may be connected to limit the output swing.

The uncommitted amplifier is a high open-loop gain, low offset, low drift op amp, with its noninverting input connected to the internal 10 k Ω resistor. Both inputs are accessible to the user.

Careful layout design has resulted in exceptional common-mode rejection at higher frequencies. The inputs are connected to Pin 1 (+IN) and Pin 8 (–IN), which are adjacent to the power pins, Pin 2 ($-V_S$) and Pin 7 ($+V_S$). Because the power pins are at ac ground, input impedance balance and, therefore, common-mode rejection, are preserved at higher frequencies.

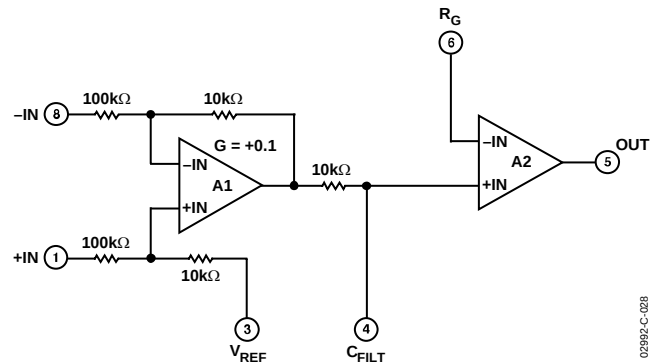


Figure 28. Simplified Schematic

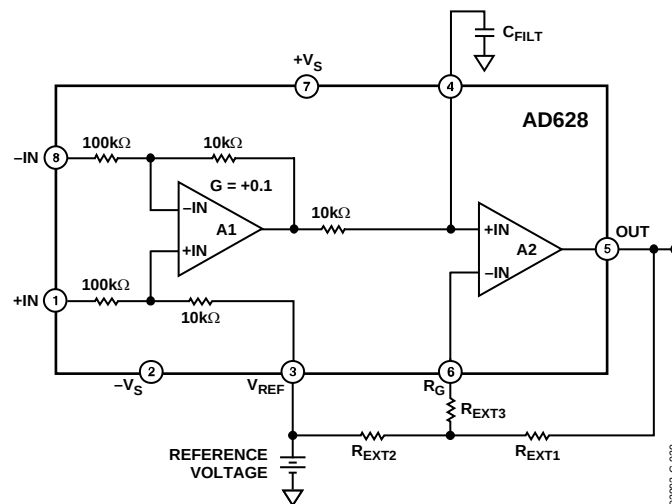


Figure 29. Circuit Connections

APPLICATIONS

GAIN ADJUSTMENT

The AD628 system gain is provided by an architecture consisting of two amplifiers. The gain of the input stage is fixed at 0.1; the output buffer is user-adjustable as $G_{A2} = 1 + R_{EXT1}/R_{EXT2}$. The system gain is then

$$G_{TOTAL} = 0.1 \times \left(1 + \frac{R_{EXT1}}{R_{EXT2}} \right) \quad (1)$$

At a 2 nA maximum, the input bias current of the buffer amplifier is very low and any offset voltage induced at the buffer amplifier by its bias current may be neglected ($2 \text{ nA} \times 10 \text{ k}\Omega = 20 \text{ }\mu\text{V}$). However, to absolutely minimize bias current effects, R_{EXT1} and R_{EXT2} can be selected so that their parallel combination is $10 \text{ k}\Omega$. If practical resistor values force the parallel combination of R_{EXT1} and R_{EXT2} below $10 \text{ k}\Omega$, a series resistor (R_{EXT3}) can be added to make up for the difference. Table 5 lists several values of gain and corresponding resistor values.

Table 5. Nearest Standard 1% Resistor Values for Various Gains (See Figure 29)

Total Gain (V/V)	A2 Gain (V/V)	R_{EXT1} (Ω)	R_{EXT2} (Ω)	R_{EXT3} (Ω)
0.1	1	10 k	∞	0
0.2	2	20 k	20 k	0
0.25	2.5	25.9 k	18.7 k	0
0.5	5	49.9 k	12.4 k	0
1	10	100 k	11 k	0
2	20	200 k	10.5 k	0
5	50	499 k	10.2 k	0
10	100	1 M	10.2 k	0

To set the system gain to less than 0.1, an attenuator can be created by placing a resistor, R_{EXT4} , from Pin 4 (C_{FILT}) to the reference voltage. A divider would be formed by the $10 \text{ k}\Omega$ resistor which is in series with the positive input of A2 and R_{EXT4} . A2 would be configured for unity gain.

Using a divider and setting A2 to unity gain yields

$$G_{W/DIVIDER} = 0.1 \times \left(\frac{R_{EXT4}}{10 \text{ k}\Omega + R_{EXT4}} \right) \times 1$$

INPUT VOLTAGE RANGE

The common-mode input voltage range is determined by V_{REF} and the supply voltage. The relation is expressed by

$$V_{CM_UPPER} \leq 11(V_{S+} - 1.2 \text{ V}) - 10 V_{REF} \quad (2)$$

$$V_{CM_LOWER} \geq 11(V_{S-} + 1.2 \text{ V}) - 10 V_{REF}$$

where V_{S+} is the positive supply, V_{S-} is the negative supply, and 1.2 V is the headroom needed for suitable performance. Equation 2 provides a general formula for calculating the common-mode input voltage range. However, the AD628 should be kept within the maximum limits listed in the Specifications (see Table 1) to maintain optimal performance. This is illustrated in Figure 30 where the maximum common-mode input voltage is limited to $\pm 120 \text{ V}$. Figure 31 shows the common-mode input voltage bounds for single-supply voltages.

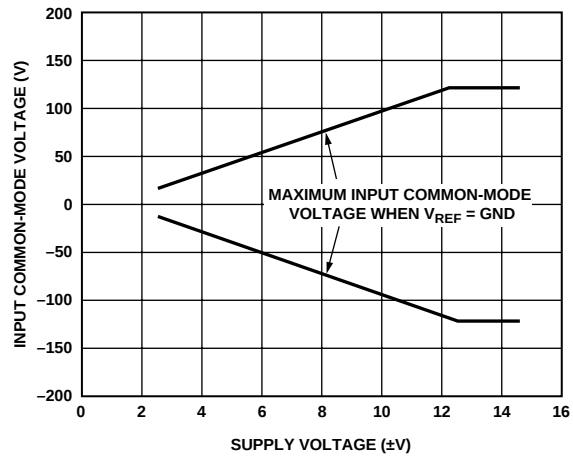


Figure 30. Input Common-Mode Voltage vs. Supply Voltage for Dual Supplies

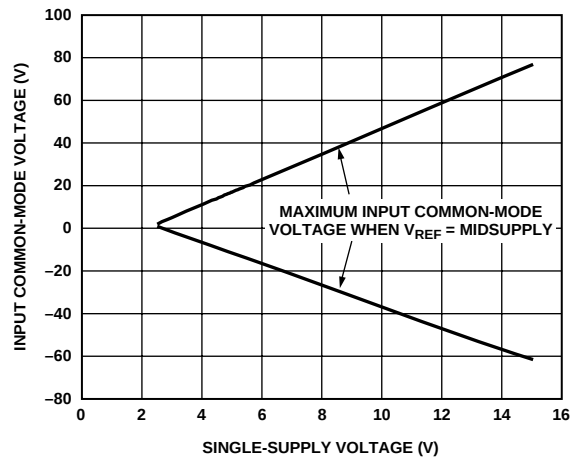


Figure 31. Input Common-Mode Voltage vs. Supply Voltage for Single Supplies

The differential input voltage range is constrained to the linear operation of the internal amplifiers A1 and A2. The voltage applied to the inputs of A1 and A2 should be between $V_{S-} + 1.2 \text{ V}$ and $V_{S+} - 1.2 \text{ V}$. Similarly, the outputs of A1 and A2 should be kept between $V_{S-} + 0.9 \text{ V}$ and $V_{S+} - 0.9 \text{ V}$.

VOLTAGE LEVEL CONVERSION

Industrial signal conditioning and control applications typically require connections between remote sensors or amplifiers and centrally located control modules. Signal conditioners provide output voltages up to $\pm 10 \text{ V}$ full scale; however, ADCs or microprocessors operating on single 3.3 V to 5 V logic supplies are becoming the norm. Thus, the controller voltages require further reduction in amplitude and reference.

Furthermore, voltage potentials between locations are seldom compatible, and power line peaks and surges can generate destructive energy between utility grids. The AD628 is an ideal solution to both problems. It attenuates otherwise destructive signal voltage peaks and surges by a factor of 10 and shifts the differential input signal to the desired output voltage.

Conversion from voltage-driven or current-loop systems is easily accommodated using the circuit in Figure 32. This shows a circuit for converting inputs of various polarities and amplitudes to the input of a single-supply ADC.

Note that the common-mode output voltage can be adjusted by connecting Pin 3 (V_{REF}) and the lower end of the 10 k Ω resistor to the desired voltage. The output common-mode voltage will be the same as the reference voltage.

The design of such an application may be done in a few simple steps, which include the following:

- Determine the required gain. For example, if the input voltage must be transformed from $\pm 10 \text{ V}$ to 0 V to $+5 \text{ V}$, the gain is $+5/+20$ or $+0.25$.
- Determine if the circuit common-mode voltage must be changed. An AD7715-5 ADC is illustrated for this example. When operating from a 5 V supply, the common-mode voltage of the AD7715 is half the supply or 2.5 V. If the AD628 reference pin and the lower terminal of the 10 k Ω resistor are connected to a 2.5 V voltage source, the output common-mode voltage will be 2.5 V.

Table 6 shows resistor and reference values for commonly used single-supply converter voltages. R_{EXT3} is included as an option. It is used to balance the source impedance into A2, which is described in more detail in the Gain Adjustment section.

Table 6. Nearest 1% Resistor Values for Voltage Level Conversion Applications

Input Voltage (V)	ADC Supply Voltage (V)	Desired Output Voltage (V)	V_{REF} (V)	R_{EXT1} (k Ω)	R_{EXT3} (k Ω)
± 10	5	2.5	2.5	15.0	4.02
± 5	5	2.5	2.5	39.7	2.00
+10	5	2.5	2.5	39.7	2.00
+5	5	2.5	2.5	89.8	1.00
± 10	3	1.25	1.25	2.49	7.96
± 5	3	1.25	1.25	15.0	4.02
+10	3	1.25	1.25	15.0	4.02
+5	3	1.25	1.25	39.7	2.00

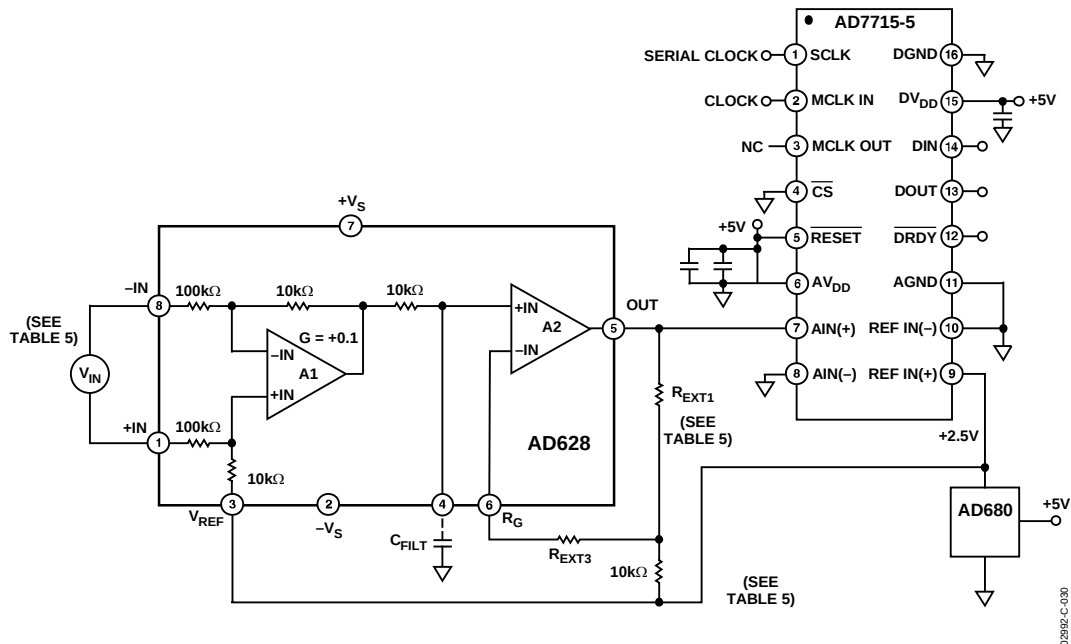


Figure 32. Level Shifter

CURRENT LOOP RECEIVER

Analog data transmitted on a 4 to 20 mA current loop can be detected with the receiver shown in Figure 33. The AD628 is an ideal choice for such a function because the current loop must be driven with a compliance voltage sufficient to stabilize the loop, and the resultant common-mode voltage often exceeds commonly used supply voltages. Note that with large shunt values a resistance of equal value must be inserted in series with the inverting input to compensate for an error at the noninverting input.

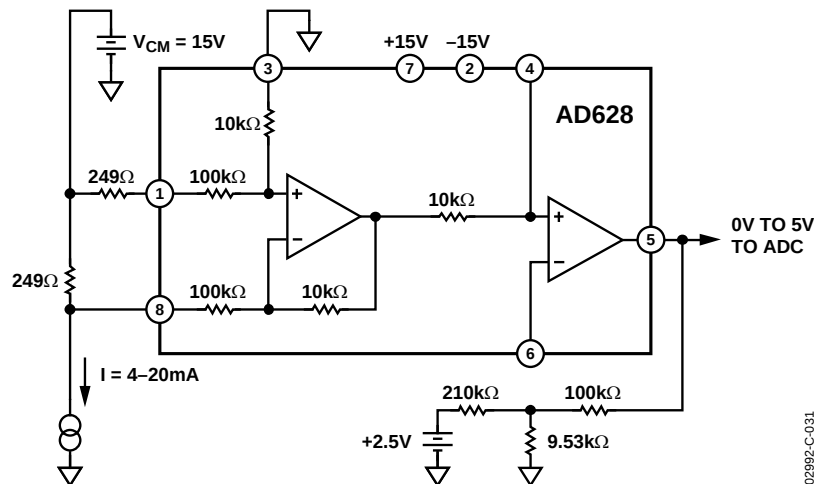


Figure 33. Level Shifter for 4 to 20 mA Current Loop

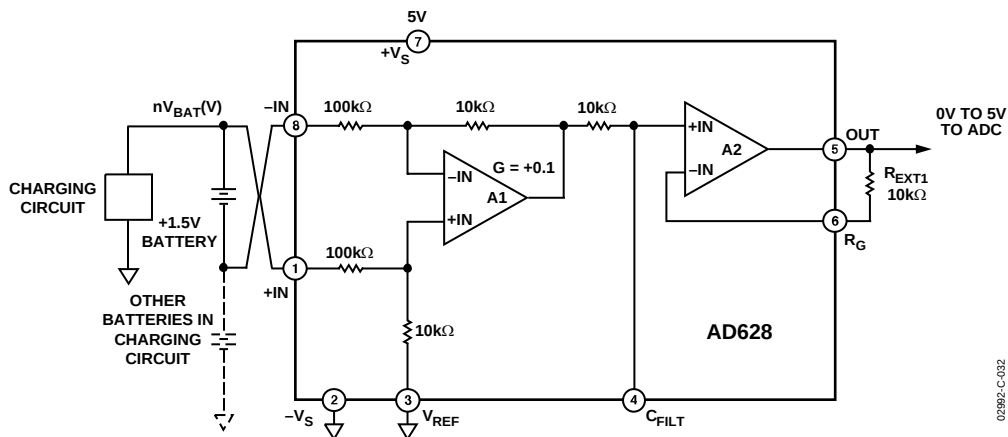


Figure 34. Battery Voltage Monitor

FILTER CAPACITOR VALUES

A capacitor can be connected to Pin 4 (C_{FILT}) to implement a low-pass filter. The capacitor value is

$$C = 15.9/f_i (\mu\text{F})$$

where f_i is the desired 3 dB filter frequency.

Table 7 shows several frequencies and their closest standard capacitor values.

Table 7. Capacitor Values for Various Filter Frequencies

Frequency (Hz)	Capacitor Value (μF)
10	1.5
50	0.33
60	0.27
100	0.15
400	0.039
1 k	0.015
5 k	0.0033
10 k	0.0015

KELVIN CONNECTION

In certain applications, it may be desirable to connect the inverting input of an amplifier to a remote reference point. This eliminates errors resulting in circuit losses in interconnecting wiring. The AD628 is particularly suited for this type of connection. In Figure 35, a 10 k Ω resistor is added in the feedback to match the source impedance of A2, which is described in more detail in the Gain Adjustment section.

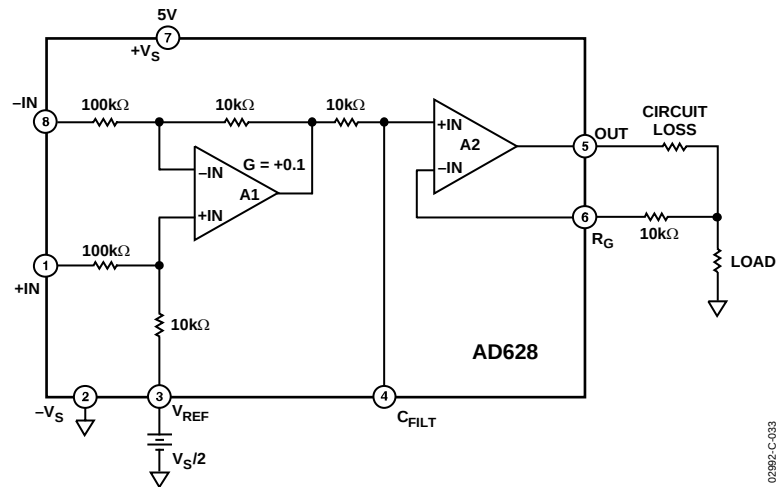


Figure 35. Kelvin Connection

02992-C-033

OUTLINE DIMENSIONS

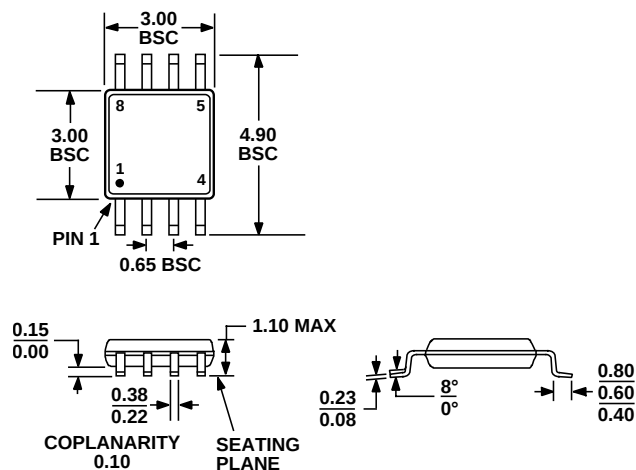


Figure 36. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

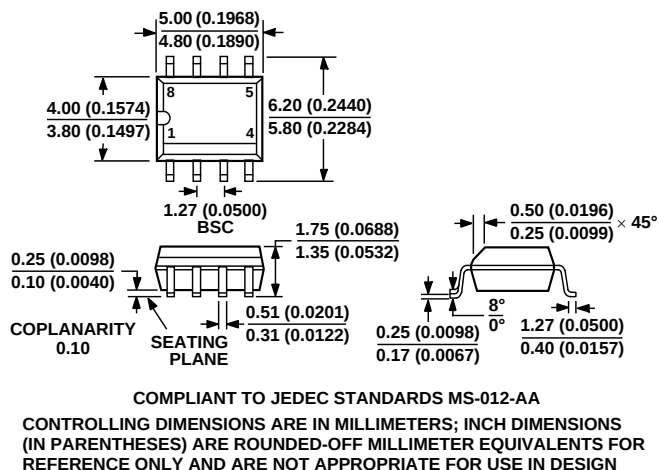


Figure 37. 8-Lead Standard Small Outline Package [SOIC] Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Description	Package Option	Branding
AD628AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD628AR-REEL	−40°C to +85°C	8-Lead SOIC 13" Reel	R-8	
AD628AR-REEL7	−40°C to +85°C	8-Lead SOIC 7" Reel	R-8	
AD628ARZ ¹	−40°C to +85°C	8-Lead SOIC	R-8	
AD628ARZ-RL ¹	−40°C to +85°C	8-Lead SOIC 13" Reel	R-8	
AD628ARZ-R7 ¹	−40°C to +85°C	8-Lead SOIC 7" Reel	R-8	
AD628ARM	−40°C to +85°C	8-Lead MSOP	RM-8	JGA
AD628ARM-REEL	−40°C to +85°C	8-Lead MSOP 13" Reel	RM-8	JGA
AD628ARM-REEL7	−40°C to +85°C	8-Lead MSOP 7" Reel	RM-8	JGA
AD628ARMZ ¹	−40°C to +85°C	8-Lead MSOP	RM-8	JGZ
AD628ARMZ-RL ¹	−40°C to +85°C	8-Lead MSOP 13" Reel	RM-8	JGZ
AD628ARMZ-R7 ¹	−40°C to +85°C	8-Lead MSOP 7" Reel	RM-8	JGZ
AD628-EVAL		Evaluation Board		

¹ Z = Pb-free part.