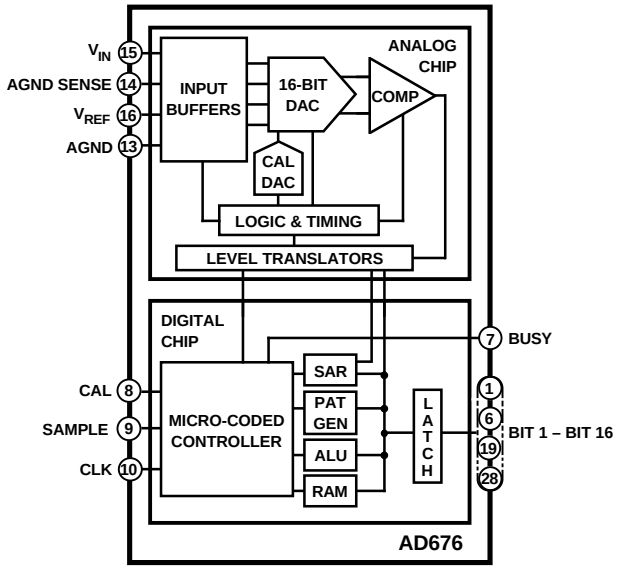
16-Bit 100 kSPS Sampling ADC

AD676

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Parallel Output Format
16 Bits No Missing Codes
±1 LSB INL
–97 dB THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD676 is a multipurpose 16-bit parallel output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 μs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD676 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD676 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD676 operates from +5 V and ±12 V supplies and typically consumes 360 mW during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided for the analog input. Separate analog and digital grounds are also provided.

The AD676 is available in a 28-pin plastic DIP or 28-pin side-brazed ceramic package. A serial-output version, the AD677, is available in a 16-pin 300 mil wide ceramic or plastic package.

REV. A

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AD676–SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD676J/A Min	AD676J/A Typ	AD676J/A Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
Total Harmonic Distortion (THD)[2]							
@ 83 kSPS, T_{MIN} to T_{MAX}		–96	–88		–97	–90	dB
		0.0016	0.004		0.0014	0.003	%
@ 100 kSPS, +25°C		–96			–97		dB
		0.0016			0.0014		%
@ 100 kSPS, T_{MIN} to T_{MAX}		–92			–92		dB
		0.0025			0.0025		%
Signal-to-Noise and Distortion Ratio (S/(N+D))[2, 3]							
@ 83 kSPS, T_{MIN} to T_{MAX}	85	89		87	90		dB
@ 100 kSPS, +25°C		89			90		dB
@ 100 kSPS, T_{MIN} to T_{MAX}		86			86		dB
Peak Spurious or Peak Harmonic Component		–98			–98		dB
Intermodulation Distortion (IMD)[4]							
2nd Order Products		–102			–102		dB
3rd Order Products		–98			–98		dB
Full Power Bandwidth		1			1		MHz
Noise		160			160		μV rms

DIGITAL SPECIFICATIONS (for all grades T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage		–0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	–10		+10	μA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	–10		+10	μA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} –1 V			V
		I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

NOTES

[1]V_{REF} = 10.0 V, (Conversion Rate (fs) = 83 kSPS, f_{IN} = 1.0 kHz, V_{IN} = –0.05 dB, Bandwidth = fs/2 unless otherwise indicated. All measurements referred to a 0 dB (20 V p-p) input signal. Values are post-calibration.

[2]For other input amplitudes, refer to Figure 13.

[3]For other input ranges/voltages reference values see Figure 12.

[4]fa = 1008 Hz. fb = 1055 Hz. See Definition of Specifications section and Figure 15.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD676J/A Min	AD676J/A Typ	AD676J/A Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	–40		+85	–40		+85	°C
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)							
@ 83 kSPS, T_{MIN} to T_{MAX}		±1			±1	±1.5	LSB
@ 100 kSPS, +25°C		±1			±1		LSB
@ 100 kSPS, T_{MIN} to T_{MAX}		±2			±2		LSB
Differential Nonlinearity (DNL)–No Missing Codes		16		16			Bits
Bipolar Zero Error[2] (at Nominal Supplies)		0.005			0.005		% FSR
Gain Error (at Nominal Supplies)							
@ 83 kSPS[2]		0.005			0.005		% FSR
@ 100 kSPS, +25°C		0.005			0.005		% FSR
@ 100 kSPS[2]		0.01			0.01		% FSR
Temperature Drift, Bipolar Zero[3]							% FSR
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
Temperature Drift, Gain[3]							
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
VOLTAGE REFERENCE INPUT RANGE[4] (V_{REF})	5		10	5		10	V
ANALOG INPUT[5]							
Input Range (V_{IN})			±V_{REF}			±V_{REF}	V
Input Impedance		⋆			⋆		
Input Settling Time		2			2		µs
Input Capacitance During Sample			50⋆			50⋆	pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±1			±1		LSB
V_{EE} = –12 V ± 5%		±1			±1		LSB
V_{DD} = +5 V ± 10%		±1			±1		LSB
Operating Current							
I_{CC}		14.5	18		14.5	18	mA
I_{EE}		14.5	18		14.5	18	mA
I_{DD}		2	5		2	5	mA
Power Consumption		360	480		360	480	mW

NOTES
[1]V_{REF} = 5.0 V, Conversion Rate = 83 kSPS unless otherwise noted. Values are post-calibration.
[2]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature.
[3]Values shown are based upon calibration at +25°C with no additional calibration at temperature. Values shown are the worst case variation from the value at +25 °C.
[4]See "APPLICATIONS" section for recommended voltage reference circuit, and Figure 12 for dynamic performance with other reference voltage values.
[5]See "APPLICATIONS" section for recommended input buffer circuit.
⋆For explanation of input characteristics, see "ANALOG INPUT" section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX} V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%, V_{REF} = 10.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Units
Conversion Time[2]	t_C	10		1000	µs
CLK Period[3]	t_{CLK}	480			ns
Calibration Time	t_{CT}			85,530	t_{CLK}
Sampling Time (Included in t_C)	t_S	2			µs
CAL to BUSY Delay	t_{CALB}		75	150	ns
BUSY to SAMPLE Delay	t_{BS}	2			µs
SAMPLE to BUSY Delay	t_{SB}		15	100	ns
CLK HIGH[4]	t_{CH}	50			ns
CLK LOW[4]	t_{CL}	50			ns
SAMPLE LOW to 1st CLK Delay	t_{SC}	50			ns
SAMPLE LOW	t_{SL}	100			ns
Output Delay	t_{OD}		125	200	ns
Status Delay	t_{SD}	50			ns
CAL HIGH Time	t_{CALH}	50			ns

NOTES
[1]See the "CONVERSION CONTROL" and "AUTOCALIBRATION" sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The maximum conversion time is specified to account for the droop of the internal sample/hold function. Longer conversion times may degrade performance. See "General Conversion Guidelines" for additional explanation of maximum conversion time.
[3]580 ns is recommended for optimal accuracy over temperature.
[4]$t_{CH} + t_{CL} = t_{CLK}$ and must be greater than 480 ns.

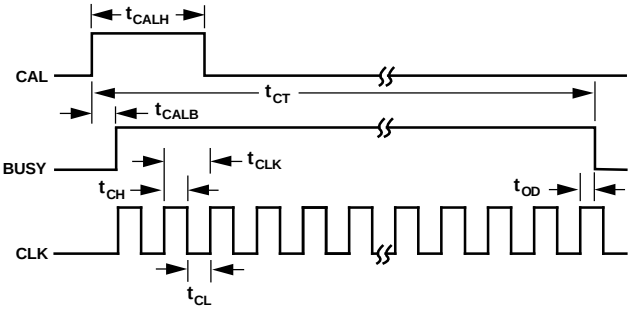


Figure 1. Calibration Timing

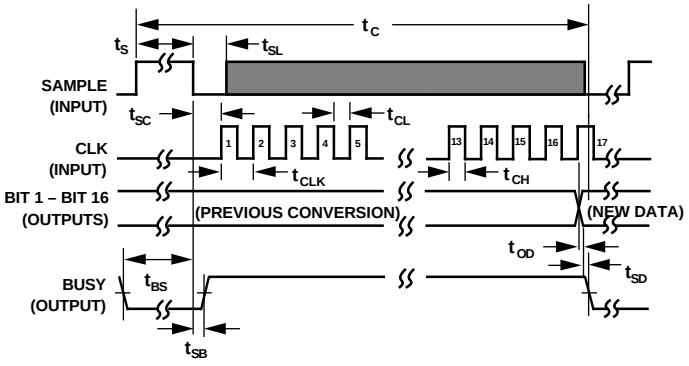


Figure 2a. General Conversion Timing

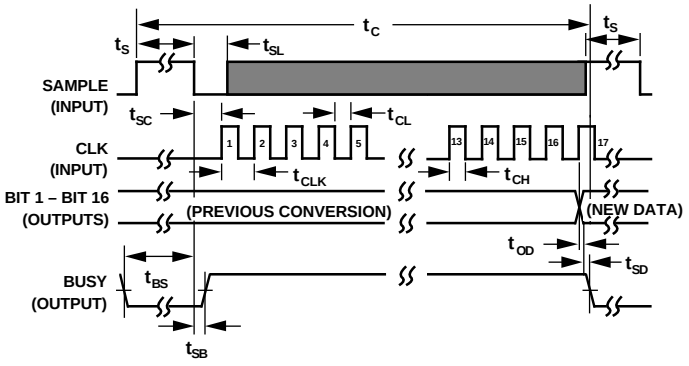


Figure 2b. Continuous Conversion Timing

ORDERING GUIDE

Model	Temperature Range[1]	S/(N+D)	Max INL	Package Description	Package Option[2]
AD676JD	0°C to +70°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676KD	0°C to +70°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28
AD676AD	–40°C to +85°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676BD	–40°C to +85°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the AD676/883 data sheet.
[2]D = Ceramic DIP.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . –0.3 V to +26.4 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
V_{CC} to AGND . . . . . –0.3 V to +18 V
V_{EE} to AGND . . . . . –18 V to +0.3 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 V to +5.5 V
Analog Inputs, V_{REF} to AGND
. . . . . (V_{CC} + 0.3 V) to (V_{EE} – 0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . –65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

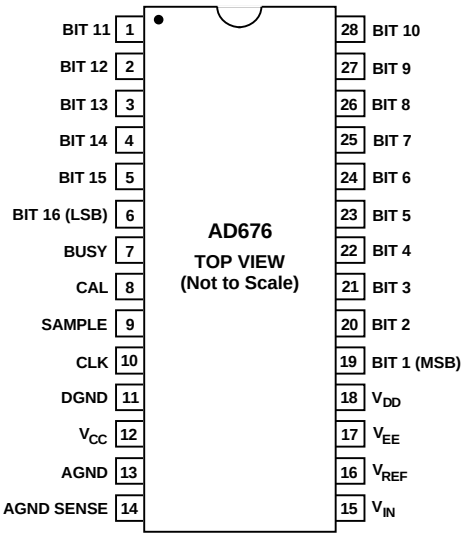
The AD676 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD676 has been classified as a Category 1 Device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD Precaution. Refer to Analog Devices' *ESD Prevention Manual.*

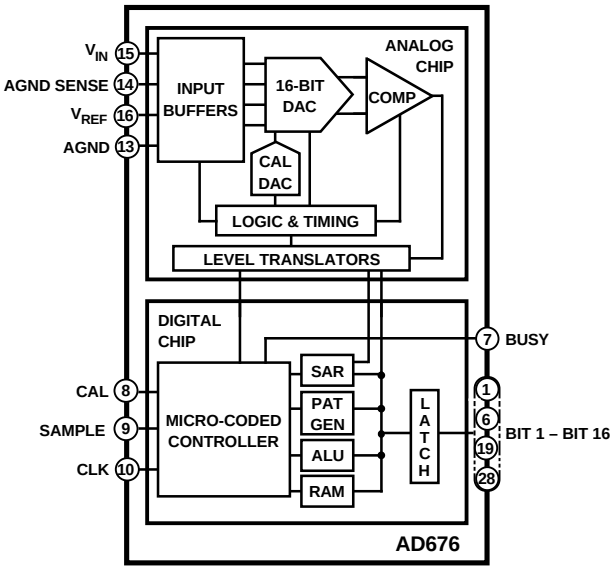
PIN DESCRIPTION

Pin	Name	Type	Description
1–6	BIT 11-BIT 16	DO	BIT 11–BIT 16 represent the six LSBs of data.
7	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress. BUSY should be buffered when capacitively loaded.
8	CAL	DI	Calibration Control Pin (Asynchronous).
9	SAMPLE	DI	V_{IN} Acquisition Control Pin. Active HIGH. During conversion, SAMPLE controls the state of the internal sample-hold amplifier and the falling edge initiates conversion (see "Conversion Control" paragraph). During calibration, SAMPLE should be held LOW. If HIGH during calibration, diagnostic information will appear on the two LSBs (Pins 5 and 6).
10	CLK	DI	Master Clock Input. The AD676 requires 17 clock cycles to execute a conversion.
11	DGND	P	Digital Ground.
12	V_{CC}	P	+12 V Analog Supply Voltage.
13	AGND	P/AI	Analog Ground.
14	AGND SENSE	AI	Analog Ground Sense.
15	V_{IN}	AI	Analog Input Voltage.
16	V_{REF}	AI	External Voltage Reference Input.
17	V_{EE}	P	–12 V Analog Supply Voltage. Note: the lid of the ceramic package is internally connected to V_{EE}.
18	V_{DD}	P	+5 V Logic Supply Voltage.
19–28	BIT 1–BIT 10	DO	BIT 1–BIT 10 represent the ten MSB of data.

Type: AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power



Package Pinout



Functional Block Diagram