2.7 V to 5.5 V, 2.3 μs, 10-Bit ADC in 8-Lead microSOIC/DIP

AD7810

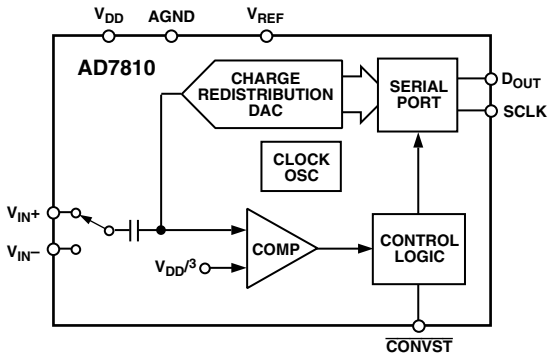
FEATURES

10-Bit ADC with 2.3 μs Conversion Time
Small Footprint 8-Lead microSOIC Package
Specified Over a –40°C to +105°C Temperature Range
Inherent Track-and-Hold Functionality
Operating Supply Range: 2.7 V to 5.5 V
Specifications at 2.7 V to 5.5 V
Microcontroller-Compatible Serial Interface
Optional Automatic Power-Down at End of Conversion
Low Power Operation
270 μW at 10 kSPS Throughput Rate
2.7 mW at 100 kSPS Throughput Rate
Analog Input Range: 0 V to V_{REF}
Reference Input Range: 0 V to V_{DD}

APPLICATIONS

Low Power, Hand-Held Portable Applications that Require Analog-to-Digital Conversion with 10-Bit Accuracy; e.g., Battery Powered Test Equipment, Battery-Powered Communications Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7810 is a high speed, low power, 10-bit A/D converter that operates from a single 2.7 V to 5.5 V supply. The part contains a 2.3 μs successive approximation A/D converter, with inherent track/hold functionality, a pseudo differential input and a high speed serial interface that interfaces to most microcontrollers. The AD7810 is fully specified over a temperature range of –40°C to +105°C.

By using a technique that samples the state of the $\overline{\text{CONVST}}$ (convert start) signal at the end of a conversion, the AD7810 may be used in an automatic power-down mode. When used in this mode, the AD7810 automatically powers down at the end of a conversion and "wakes up" at the start of a new conversion. This feature significantly reduces the power consumption of the part at lower throughput rates. The AD7810 can also operate in a high speed mode where the part is not powered down between conversions. In this high speed mode of operation, the conversion time of the AD7810 is 2.3 μs. The maximum throughput rate is dependent on the speed of the serial interface of the microcontroller.

The part is available in a small 8-lead, 0.3" wide, plastic dual-in-line package (mini-DIP); in an 8-lead, small outline IC (SOIC); and in an 8-lead microSOIC package.

PRODUCT HIGHLIGHTS

1. Complete, 10-Bit ADC in 8-Lead Package
   The AD7810 is a 10-bit 2.3 μs ADC with inherent track/hold functionality and a high speed serial interface—all in an 8-lead microSOIC package. V_{REF} may be connected to V_{DD} to eliminate the need for an external reference. The result is a high speed, low power, space saving ADC solution.
2. Low Power, Single Supply Operation
   The AD7810 operates from a single 2.7 V to 5.5 V supply and typically consumes only 9 mW of power while converting. The power dissipation can be significantly reduced at lower throughput rates by using the automatic power-down mode, e.g., at a throughput rate of 10 kSPS the power consumption is only 270 μW.
3. Automatic Power-Down
   The automatic power-down mode, whereby the AD7810 powers down at the end of a conversion and "wakes up" before the next conversion, means the AD7810 is ideal for battery powered applications. See Power vs. Throughput Rate section.
4. Serial Interface
   An easy to use, fast serial interface allows connection to most popular microprocessors with no external circuitry.

REV. B

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AD7810–SPECIFICATIONS (GND = 0 V, V_{REF} = V_{DD}. All specifications –40°C to +105°C unless otherwise noted.)

Parameter	Y Version	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz, f_{SAMPLE} = 350 kHz
Signal to (Noise + Distortion) Ratio[1]	58	dB min	
Total Harmonic Distortion[1]	–64	dB max	
Peak Harmonic or Spurious Noise	–64	dB max	
Intermodulation Distortion[2]			fa = 48 kHz, fb = 48.5 kHz
2nd Order Terms	–67	dB typ	
3rd Order Terms	–67	dB typ	
DC ACCURACY			
Resolution	10	Bits	
Relative Accuracy[1]	±1	LSB max	
Differential Nonlinearity (DNL)[1]	±1	LSB max	
Offset Error[1]	±2	LSB max	
Gain Error[1]	±2	LSB max	
Minimum Resolution for Which			
No Missing Codes Are Guaranteed	10	Bits	
ANALOG INPUT			
Input Voltage Range	0	V min	
	V_{REF}	V max	
Input Leakage Current[2]	±1	µA max	
Input Capacitance[2]	15	pF max	
REFERENCE INPUTS[2]			
V_{REF} Input Voltage Range	1.2	V min	
	V_{DD}	V max	
Input Leakage Current	±3	µA max	
Input Capacitance	20	pF max	
LOGIC INPUTS[2]			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.4	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	8	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
High Impedance Leakage Current	±10	µA max	
High Impedance Capacitance	15	pF max	
CONVERSION RATE			
Conversion Time	2.3	µs max	
Track/Hold Acquisition Time[1]	100	ns max	See DC Acquisition Time Section
POWER SUPPLY			
V_{DD}	2.7–5.5	Volts	For Specified Performance
I_{DD}	3.5	mA max	Sampling at 350 kSPS and Logic
Power Dissipation	17.5	mW max	Inputs at V_{DD} or 0 V. V_{DD} = 5 V
Power-Down Mode			
I_{DD}	1	µA max	V_{DD} = 5 V; V_{DD} = 3 V
Power Dissipation	5	µW max	
Automatic Power Down			
1 kSPS Throughput	27	µW max	
10 kSPS Throughput	270	µW max	
100 kSPS Throughput	2.7	mW max	

NOTES
[1]See Terminology section.
[2]Sample tested during initial release and after any redesign or process change that may affect this parameter.

Specifications subject to change without notice.

Timing Characteristics[1, 2] (–40°C to +105°C, $V_{REF} = V_{DD}$, unless otherwise noted)

Parameter	V_{DD} = 5 V ± 10%	V_{DD} = 3 V ± 10%	Unit	Conditions/Comments
t_1	2.3	2.3	µs (max)	Conversion Time Mode 1 Operation (High Speed Mode)
t_2	20	20	ns (min)	$\overline{CONVST}$ Pulsewidth
t_3	25	25	ns (min)	SCLK High Pulsewidth
t_4	25	25	ns (min)	SCLK Low Pulsewidth
t_5[3]	5	5	ns (min)	$\overline{CONVST}$ Rising Edge to SCLK Rising Edge Set-Up Time
t_6[3]	10	10	ns (max)	SCLK Rising Edge to D_{OUT} Data Valid Delay
t_7[3]	5	5	ns (max)	Data Hold Time after Rising Edge SCLK
t_8[3, 4]	20	20	ns (max)	Bus Relinquish Time after Falling Edge of SCLK
	10	10	ns (min)	
$t_{POWER\ UP}$	1.5	1.5	µs (max)	Power-Up Time after Rising Edge of $\overline{CONVST}$

NOTES
[1]Sample tested to ensure compliance.
[2]See Figures 14, 15 and 16.
[3]These numbers are measured with the load circuit of Figure 1. They are defined as the time required for the o/p to cross 0.8 V or 2.4 V for V_{DD} = 5 V ± 10% and 0.4 V or 2 V for V_{DD} = 3 V ± 10%.
[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND
($\overline{CONVST}$, SCLK) . . . . . –0.3 V, V_{DD} + 0.3 V
Digital Output Voltage to GND
(D_{OUT}) . . . . . –0.3 V, V_{DD} + 0.3 V
V_{REF} to GND . . . . . –0.3 V, V_{DD} + 0.3 V
Analog Inputs
(V_{IN+}, V_{IN-}) . . . . . –0.3 V, V_{DD} + 0.3 V
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
Plastic DIP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 125°C/W
θ_{JC} Thermal Impedance . . . . . 50°C/W
Lead Temperature Soldering (10 sec) . . . . . 260°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 160°C/W
θ_{JC} Thermal Impedance . . . . . 56°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C
MicroSOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 206°C/W
θ_{JC} Thermal Impedance . . . . . 44°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Linearity Error (LSB)	Temperature Range	Package Description	Package Options	Branding Information
AD7810YN	±1 LSB	–40°C to +105°C	Plastic DIP	N-8	
AD7810YR	±1 LSB	–40°C to +105°C	Small Outline IC (SOIC)	SO-8	
AD7810YRM	±1 LSB	–40°C to +105°C	microSOIC	RM-8	C1Y

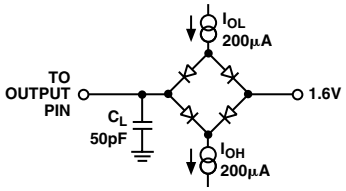
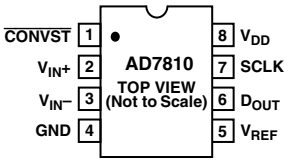


Figure 1. Load Circuit for Digital Output Timing Specifications

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	$\overline{\text{CONVST}}$	Convert Start. Falling edge puts the track-and-hold into hold mode and initiates a conversion. A rising edge on the $\overline{\text{CONVST}}$ pin enables the serial port of the AD7810. This is useful in multi-package applications where a number of devices share the same serial bus. The state of this pin at the end of conversion also determines whether the part is powered down or not. See Operating Modes section of this data sheet.
2	V_{IN+}	Positive input of the pseudo differential analog input.
3	V_{IN-}	Negative input of the pseudo differential analog input.
4	GND	Ground reference for analog and digital circuitry.
5	V_{REF}	External reference is connected here.
6	D_{OUT}	Serial data is shifted out on this pin.
7	SCLK	Serial Clock. An external serial clock is applied here.
8	V_{DD}	Positive Supply Voltage 2.7 V to 5.5 V.

PIN CONFIGURATION
DIP/SOIC



Typical Performance Characteristics

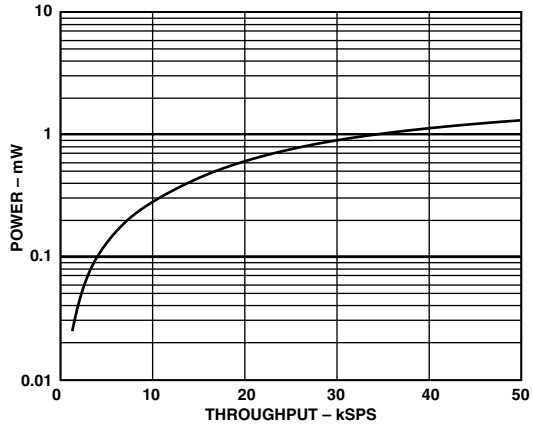


Figure 2. Power vs. Throughput

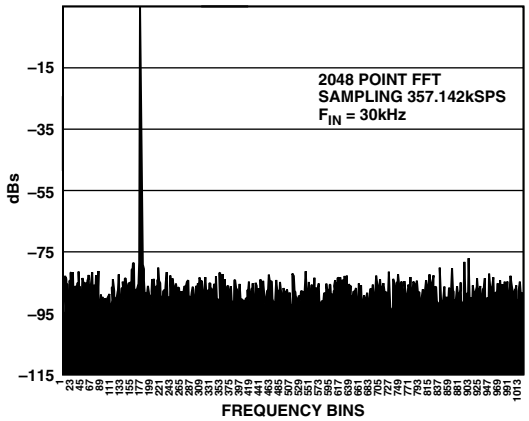


Figure 3. AD7810 SNR

TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for a 10-bit converter, this is 62 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7810 it is defined as:

$$THD(dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6^2 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms values of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7810 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Gain Error

This is the deviation of the last code transition (1111 . . . 110) to (1111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time

Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the V_{IN+} input of the AD7810. It means that the user must wait for the duration of the track/hold acquisition time, after the end of conversion or after a step input change to V_{IN+}, before starting another conversion to ensure that the part operates to specification.