

FEATURES

Designed for 210°C operation

Low noise

1 nV/ $\sqrt{\text{Hz}}$ input noise

45 nV/ $\sqrt{\text{Hz}}$ output noise

High CMRR

126 dB CMRR (minimum), $G = 100$

80 dB CMRR (minimum) to 5 kHz, $G = 1$

Excellent ac specifications

15 MHz bandwidth ($G = 1$)

1.2 MHz bandwidth ($G = 100$)

22 V/ μs slew rate

THD: 130 dB (1 kHz, $G = 1$)

Versatile

$\pm 4\text{ V}$ to $\pm 17\text{ V}$ dual supply

Gain set with single resistor ($G = 1$ to 1000)

Temperature range: -40°C to $+210^\circ\text{C}$

APPLICATIONS

Down-hole instrumentation

Harsh environment data acquisition

Exhaust gas measurements

Vibration analysis

GENERAL DESCRIPTION

The AD8229 is an ultralow noise instrumentation amplifier designed for measuring small signals in the presence of large common-mode voltages and high temperatures.

The AD8229 has been designed for high temperature operation. The process is dielectrically isolated to avoid leakage currents at high temperatures. The design architecture was chosen to compensate for the low V_{BE} voltages at high temperatures. To enhance long term reliability, the wire bonding in the packaging is designed to avoid intermetallic absorption at high temperatures.

The AD8229 excels at distinguishing tiny signals. It delivers industry leading 1 nV/ $\sqrt{\text{Hz}}$ input noise performance. The AD8229's high CMRR prevents unwanted signals from corrupting the acquisition. The CMRR increases as the gain increases, offering high rejection when it is most needed.

FUNCTIONAL BLOCK DIAGRAM

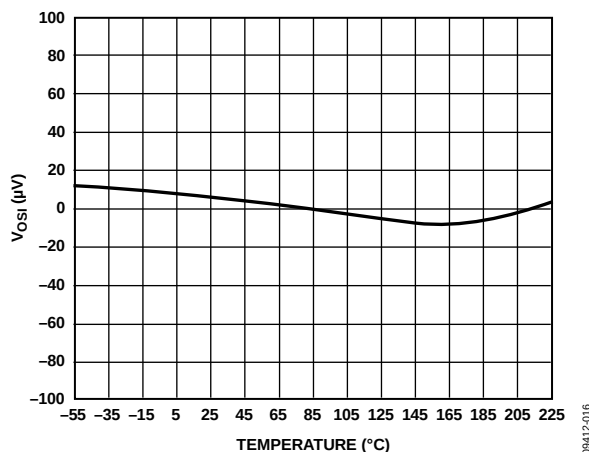
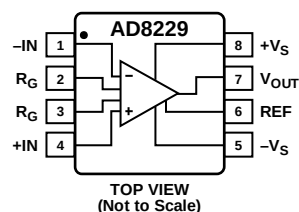


Figure 2. Typical Input Offset vs. Temperature ($G = 100$)

The AD8229 is one of the fastest instrumentation amplifiers available. Its current feedback architecture provides bandwidth that is quite high, even at high gains, for example, 1.2 MHz at $G = 100$. With the high bandwidth comes excellent distortion performance, allowing use in demanding applications such as vibration analysis.

Gain is set from 1 to 1000 with a single resistor. A reference pin allows the user to offset the output voltage. This feature is useful when interfacing with analog-to-digital converters.

The AD8229 is available in an 8-pin ceramic DIP package.

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Architecture	17
Applications.....	1	Gain Selection.....	17
General Description	1	Reference Terminal	17
Functional Block Diagram	1	Input Voltage Range.....	18
Revision History	2	Layout	18
Specifications.....	3	Input Bias Current Return Path	19
Absolute Maximum Ratings.....	6	Input Protection	19
Thermal Resistance	6	Radio Frequency Interference (RFI).....	19
ESD Caution.....	6	Calculating the Noise of the Input Stage.....	20
Pin Configuration and Function Descriptions.....	7	Outline Dimensions	21
Typical Performance Characteristics	8	Ordering Guide	21
Theory of Operation	17		

REVISION HISTORY

1/11—Revision 0: Initial Version

SPECIFICATIONS

$+V_S = 15\text{ V}$, $-V_S = -15\text{ V}$, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, $G = 1$, $R_L = 10\text{ k}\Omega$, unless otherwise noted.

Table 1.

Parameter	Test Conditions	DIP package			Unit
		Min	Typ	Max	
COMMON-MODE REJECTION RATIO (CMRR)					
CMRR DC to 60 Hz with 1 kΩ Source Imbalance G = 1 Temperature Drift G = 10 Temperature Drift G = 100 Temperature Drift G = 1000	V _{CM} = ±10 V T _A = −40°C to +210°C T _A = −40°C to +210°C T _A = −40°C to +210°C T _A = −40°C to +210°C	86 106 126 134		300 30 3	dB nV/V/°C dB nV/V/°C dB nV/V/°C dB
CMRR at 5 kHz G = 1 G = 10 G = 100 G = 1000	V _{CM} = ±10 V	80 90 90 90			dB dB dB dB
VOLTAGE NOISE					
Spectral Density ¹ : 1 kHz Input Voltage Noise, e _{ni} Output Voltage Noise, e _{no} Peak to Peak: 0.1 Hz to 10 Hz G = 1 G = 1000	V _{IN+} , V _{IN−} = 0 V		1 45 2 100	1.1 50 	nV/√Hz nV/√Hz μV p-p nV p-p
CURRENT NOISE					
Spectral Density: 1 kHz Peak to Peak: 0.1 Hz to 10 Hz			1.5 100		pA/√Hz pA p-p
VOLTAGE OFFSET					
Input Offset, V _{OSI} Average TC Output Offset, V _{OSO} Average TC Offset RTI vs. Supply (PSR) G = 1 G = 10 G = 100 G = 1000	V _{OS} = V _{OSI} + V _{OSO} /G −40°C to +210°C −40°C to +210°C V _S = ±5 V to ±15 V −40°C to +210°C −40°C to +210°C −40°C to +210°C −40°C to +210°C	 86 106 126 130	 0.1 3	100 1 1000 10	μV μV/°C μV μV/°C dB dB dB dB
INPUT CURRENT					
Input Bias Current High Temperature Input Offset Current High Temperature	T _A = 210°C T _A = 210°C			70 200 35 50	nA nA nA nA

AD8229

Parameter	Test Conditions	Min	DIP package		Unit	
			Typ	Max		
DYNAMIC RESPONSE						
Small Signal Bandwidth – 3 dB	10 V step		15		MHz	
G = 1			4		MHz	
G = 10			1.2		MHz	
G = 100			0.15		MHz	
G = 1000						
Settling Time 0.01%						
G = 1			0.75		μs	
G = 10			0.65		μs	
G = 100			0.85		μs	
G = 1000			5		μs	
Settling Time 0.001%	10 V step					
G = 1			0.9		μs	
G = 10			0.9		μs	
G = 100			1.2		μs	
G = 1000			7		μs	
Slew Rate						
G = 1 to 100			22		V/μs	
GAIN ²						
Gain Range	G = 1 + (6 kΩ/R _G)	1		1000	V/V	
Gain Error	V _{OUT} = ±10 V					
G = 1			0.01	0.03	%	
G = 10			0.05	0.3	%	
G = 100			0.05	0.3	%	
G = 1000			0.1	0.3	%	
Gain Nonlinearity	V _{OUT} = –10 V to +10 V					
G = 1 to 1000	R _L = 10 kΩ		2		ppm	
Gain vs. Temperature						
G = 1	–40°C to +210°C		2	5	ppm/°C	
G > 10	–40°C to +210°C			–100	ppm/°C	
INPUT						
Impedance (Pin to Ground) ³			1.5 3		GΩ pF	
Input Operating Voltage Range ⁴	V _S = ±5 V to ±18 V for dual supplies	–V _S + 2.8		+V _S – 2.5	V	
Over Temperature	–40°C to +210°C	–V _S + 2.8		+V _S – 2.5	V	
OUTPUT						
Output Swing	R _L = 2 kΩ	–V _S + 1.9		+V _S – 1.5	V	
High Temperature	T _A = 210°C	–V _S + 1.1		+V _S – 1.1	V	
Output Swing	R _L = 10 kΩ	–V _S + 1.8		+V _S – 1.2	V	
High Temperature	T _A = 210°C	–V _S + 1.1		+V _S – 1.1	V	
Short-Circuit Current			35		mA	
REFERENCE INPUT						
R _{IN}	V _{IN+} , V _{IN–} = 0 V		10		kΩ	
I _{IN}			70		μA	
Voltage Range			–V _S		+V _S	V
Reference Gain to Output				1		V/V
Reference Gain Error				0.01		%

Parameter	Test Conditions	DIP package		Unit
		Min	Typ Max	
POWER SUPPLY				
Operating Range		±4	±17	V
Quiescent Current			6.7	mA
High Temperature	T = 210°C		12	mA
TEMPERATURE RANGE				
For Specified Performance ⁵		−40	+210	°C

¹ Total Voltage Noise = $\sqrt{(e_{ni})^2 + (e_{no}/G)^2 + e_{ng}^2}$. See the Theory of Operation section for more information.

² These specifications do not include the tolerance of the external gain setting resistor, R_G. For G>1, R_G errors should be added to the specifications given in this table.

³ Differential and common-mode input impedance can be calculated from the pin impedance: Z_{DIFF} = 2(Z_{PIN}); Z_{CM} = Z_{PIN}/2.

⁴ Input voltage range of the AD8229 input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more details.

⁵ Performance at 210°C is guaranteed for 1000 hours.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	$\pm 17\text{ V}$
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at $-IN$, $+IN$ ¹	$\pm V_S$
Differential Input Voltage ¹	
Gain ≤ 4	$\pm V_S$
$4 > \text{Gain} > 50$	$\pm 50\text{ V/Gain}$
Gain ≥ 50	$\pm 1\text{ V}$
Maximum Voltage at REF	$\pm V_S$
Storage Temperature Range	
CERDIP	-65°C to $+150^\circ\text{C}$
Specified Temperature Range	
CERDIP	-40°C to $+210^\circ\text{C}$
Maximum Junction Temperature	
CERDIP	245°C

¹For voltages beyond these limits, use input protection resistors. See the Applications section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device in free air.

Table 3.

Package	θ_{JA}	Unit
8-Lead, Size BrazeD, CERDIP, 4-Layer JEDEC Board	100	$^\circ\text{C/W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

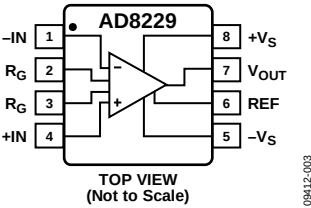


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN	Negative Input Terminal.
2, 3	R _G	Gain Setting Terminals. Place resistor across the R _G pins to set the gain. $G = 1 + (6\text{ k}\Omega/R_G)$.
4	+IN	Positive Input Terminal.
5	−V _S	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level-shift the output.
7	V _{OUT}	Output Terminal.
8	+V _S	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

$T = 25^{\circ}\text{C}$, $V_S = \pm 15$, $V_{\text{REF}} = 0$, $R_L = 2\text{ k}\Omega$, unless otherwise noted.

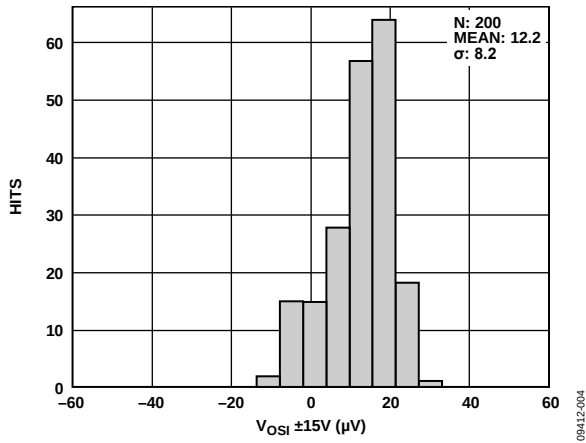


Figure 4. Typical Distribution of Input Offset Voltage

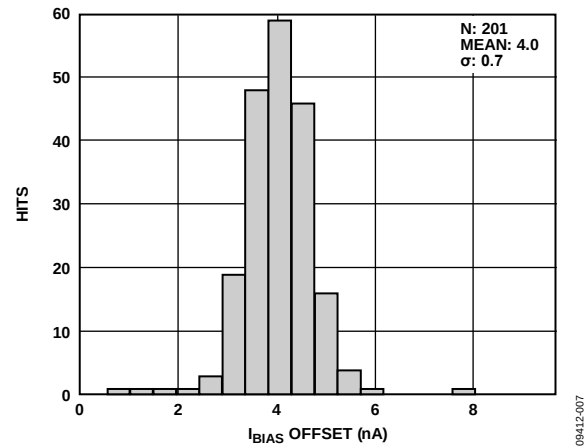


Figure 7. Typical Distribution of Input Offset Current

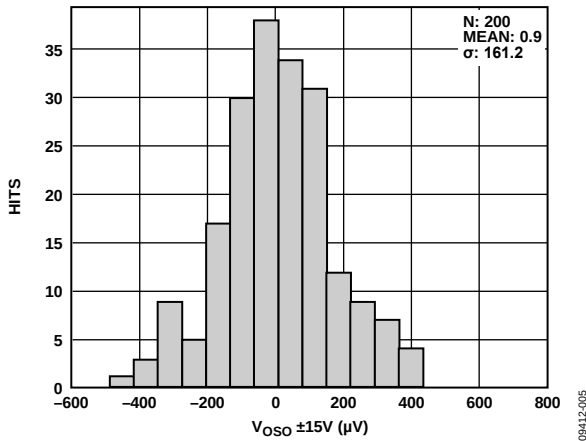


Figure 5. Typical Distribution of Output Offset Voltage

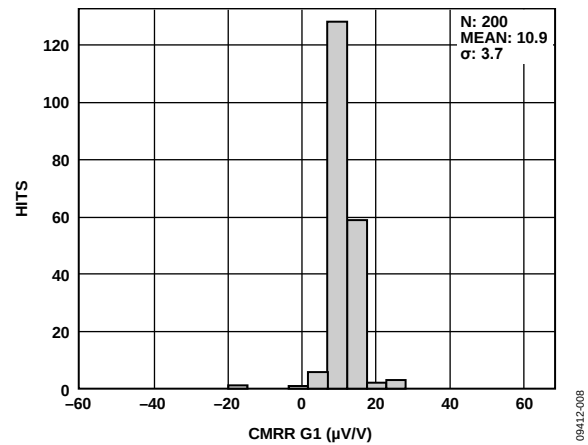


Figure 8. Typical Distribution of Common Mode Rejection, $G = 1$

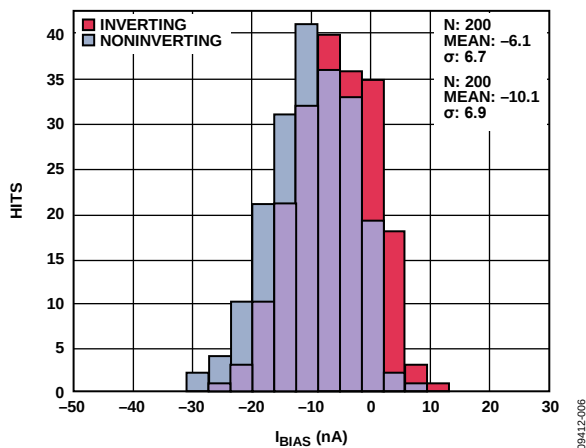


Figure 6. Typical Distribution of Input Bias Current

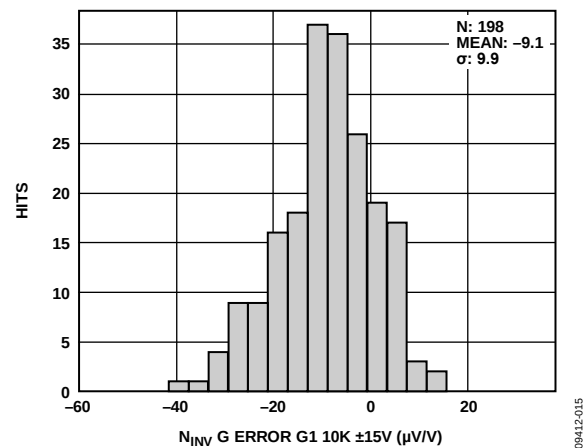


Figure 9. Typical Distribution of Gain Error, $G = 1$

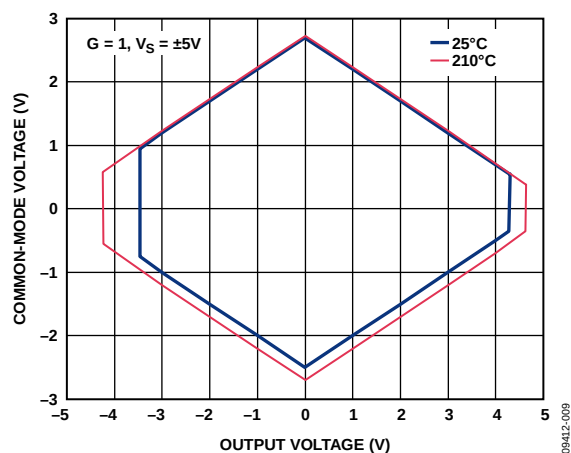


Figure 10. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm 5V$; $G = 1$

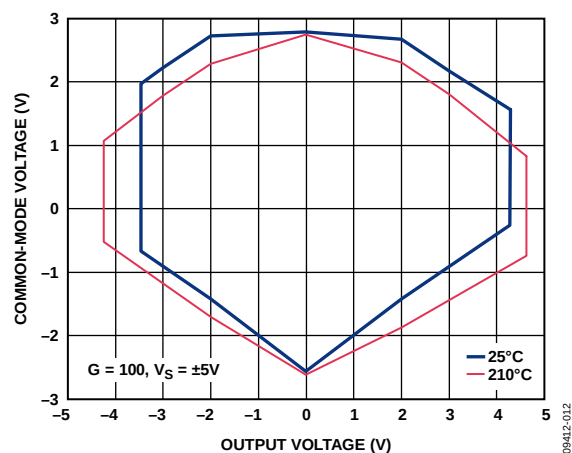


Figure 13. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm 5V$; $G = 100$

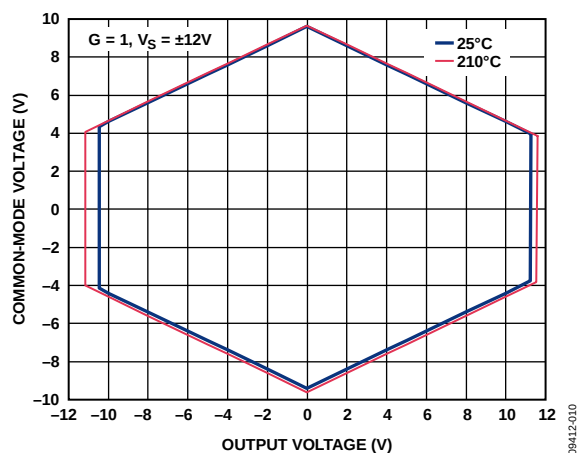


Figure 11. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm 12V$; $G = 1$

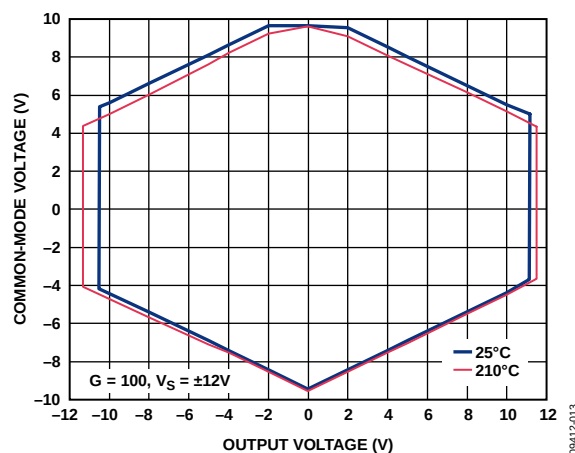


Figure 14. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm 12V$; $G = 100$

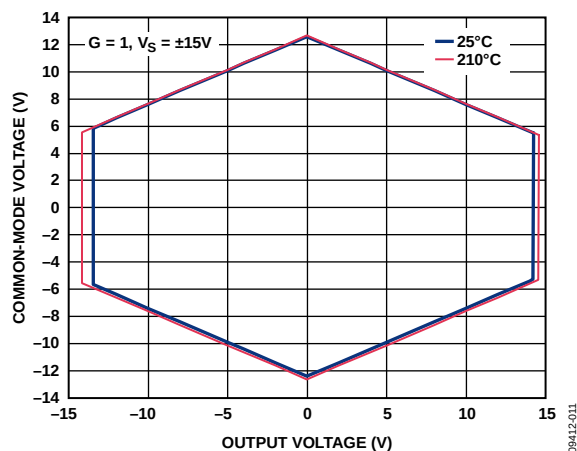


Figure 12. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm 15V$; $G = 1$

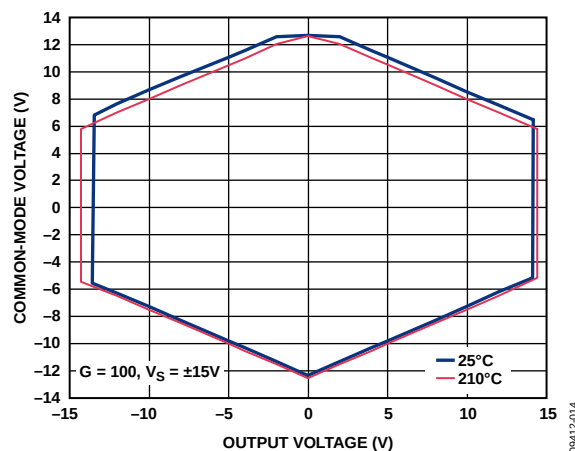


Figure 15. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm 15V$; $G = 100$

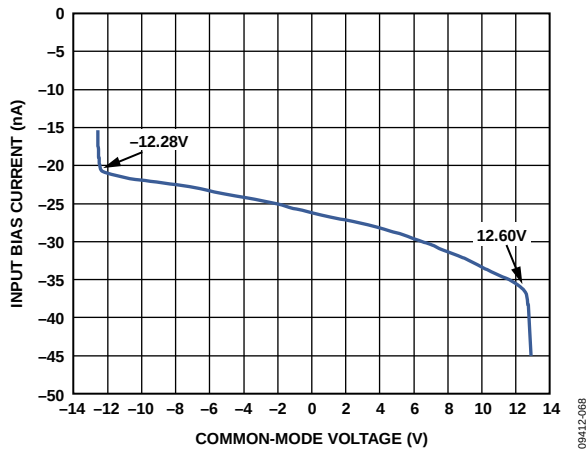


Figure 16. Input Bias Current vs. Common-Mode Voltage

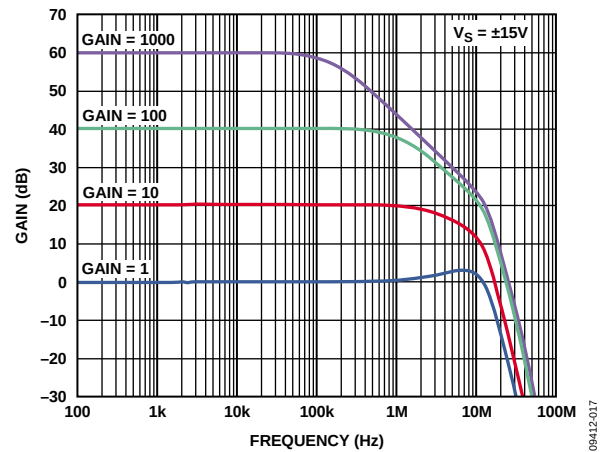


Figure 19. Gain vs. Frequency

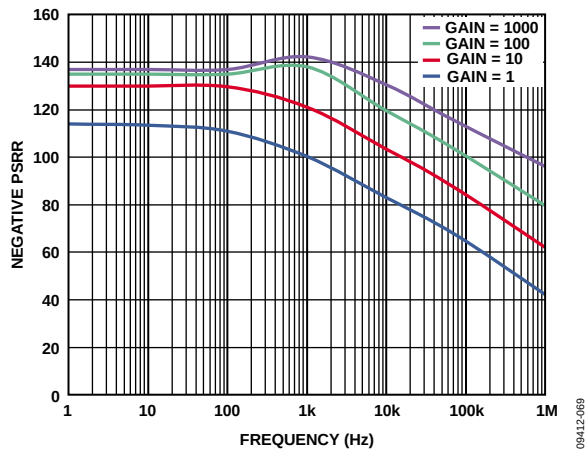


Figure 17. Positive PSRR vs. Frequency

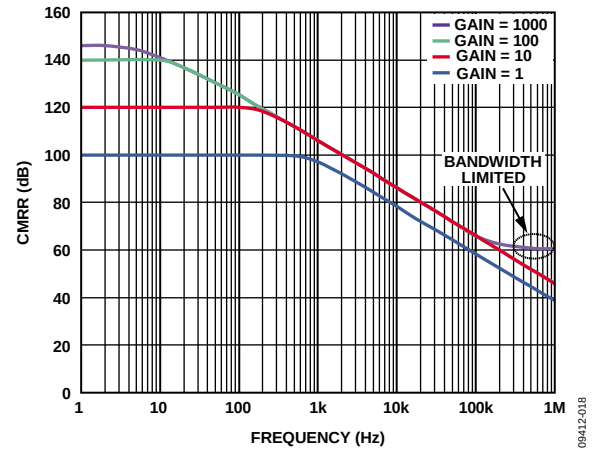


Figure 20. CMRR vs. Frequency

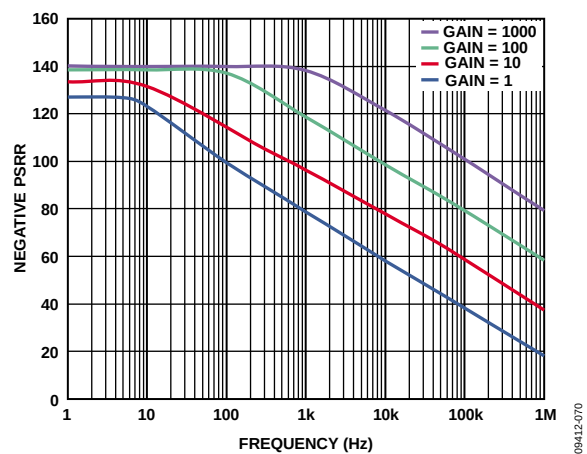


Figure 18. Negative PSRR vs. Frequency

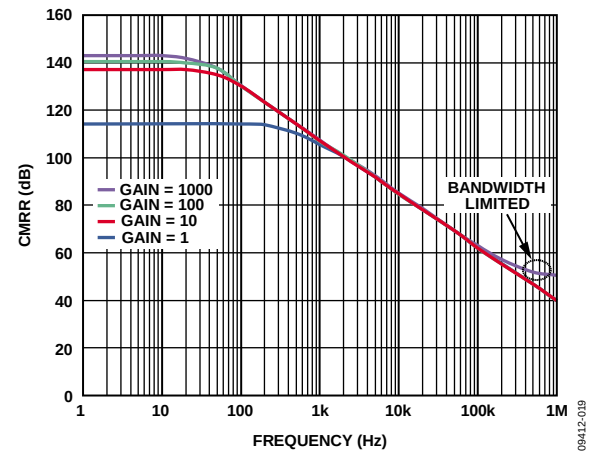


Figure 21. CMRR vs. Frequency, 1 kΩ Source Imbalance

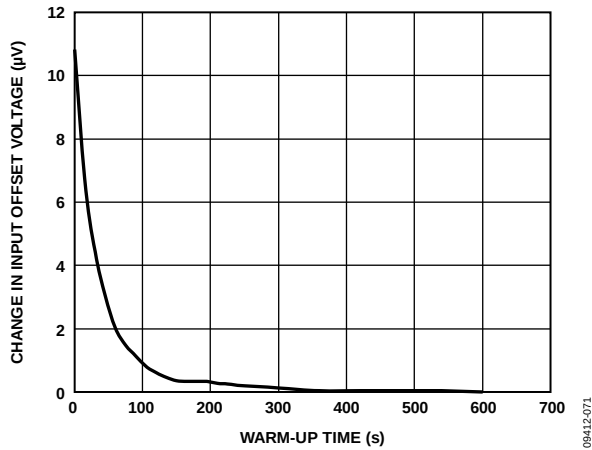


Figure 22. Change in Input Offset Voltage (V_{OSI}) vs. Warm-Up Time

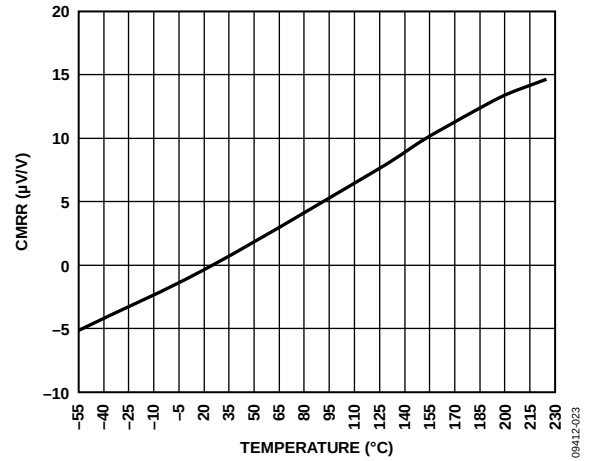


Figure 25. CMRR vs. Temperature, $G = 1$, Normalized at 25°C

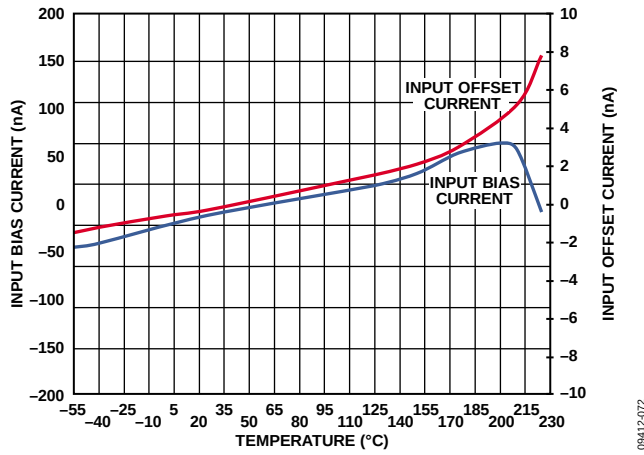


Figure 23. Input Bias Current and Input Offset Current vs. Temperature

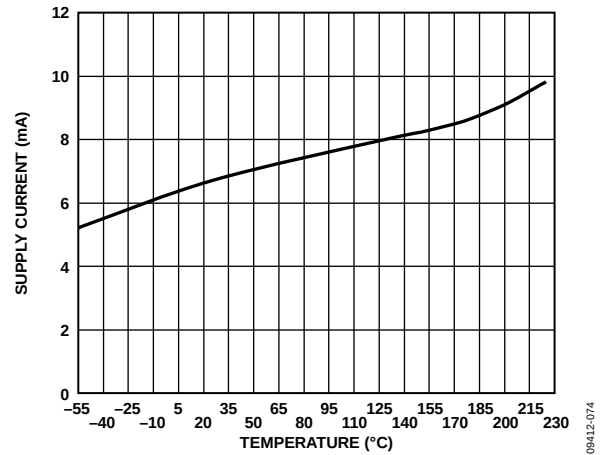


Figure 26. Supply Current vs. Temperature, $G = 1$

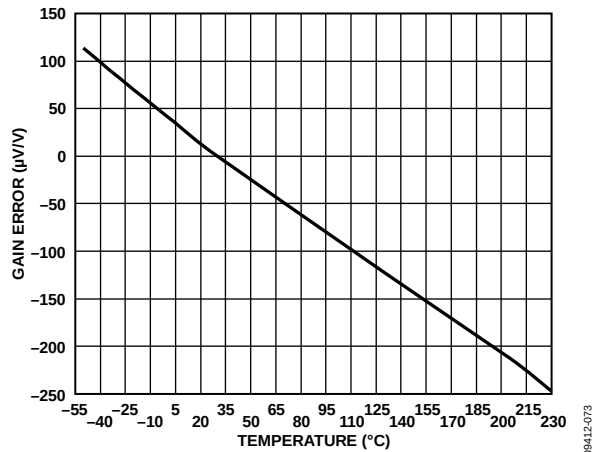


Figure 24. Gain Error vs. Temperature, $G = 1$, Normalized at 25°C

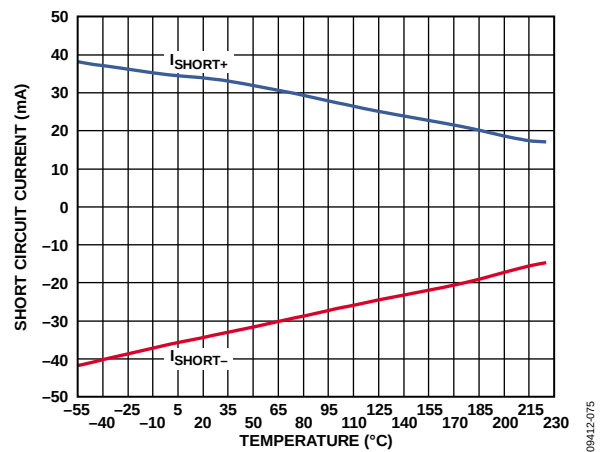
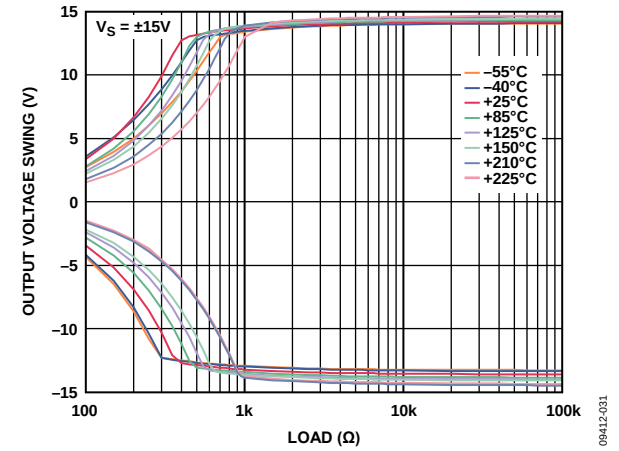
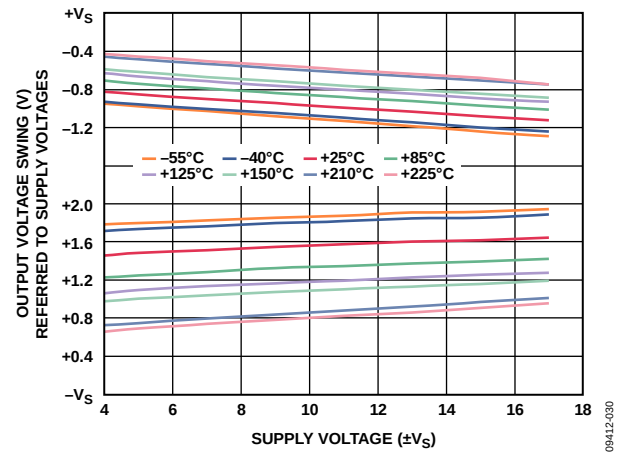
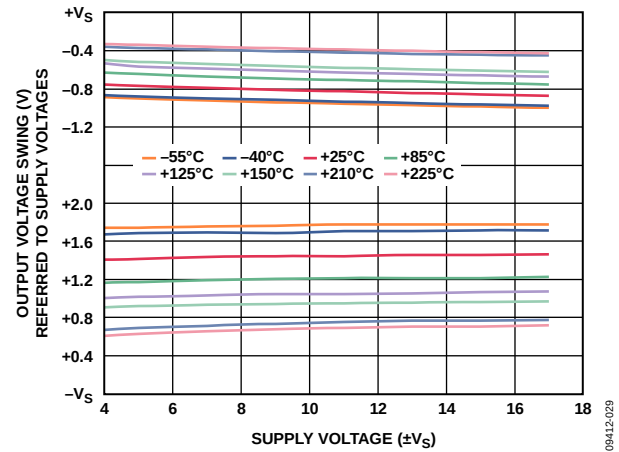
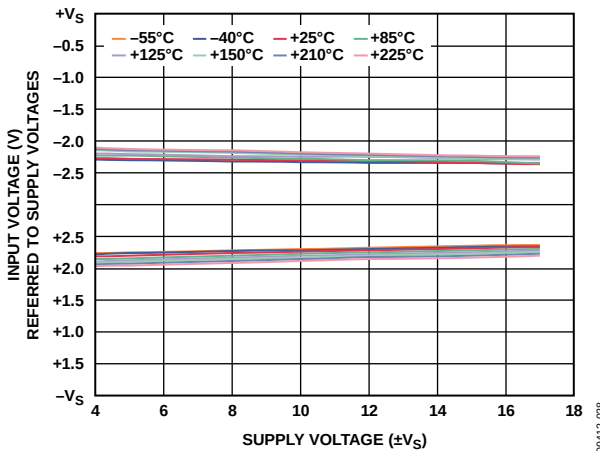
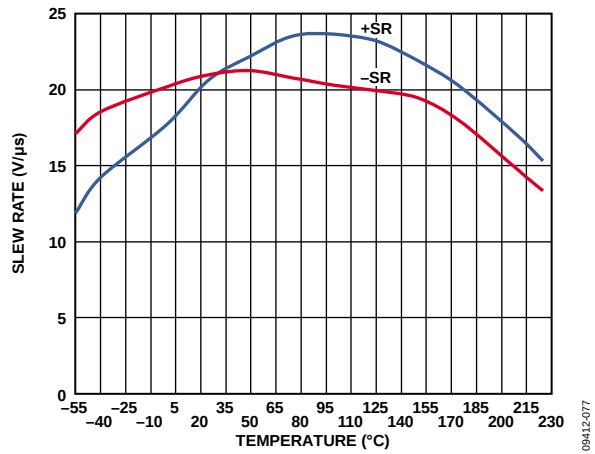
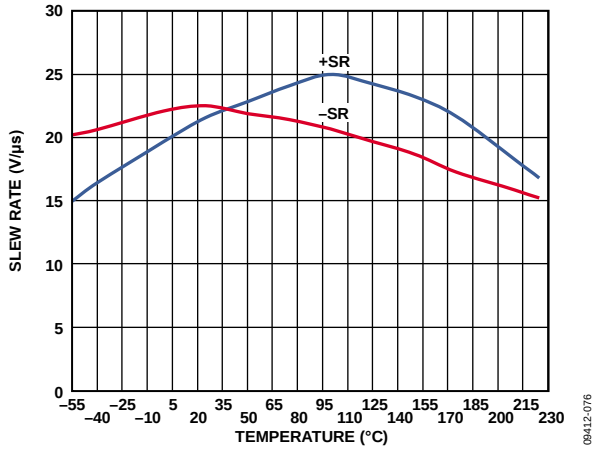


Figure 27. Short-Circuit Current vs. Temperature, $G = 1$



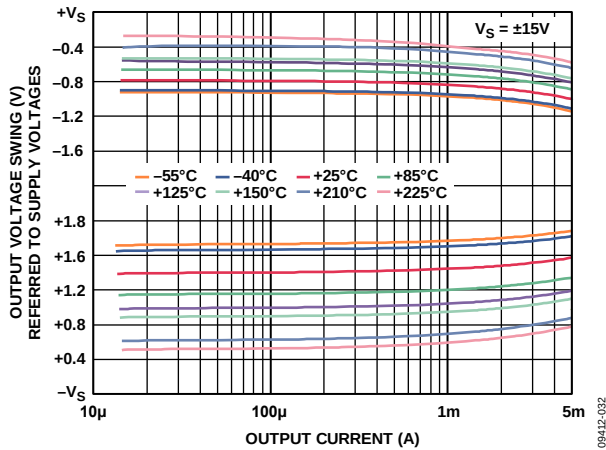


Figure 34. Output Voltage Swing vs. Output Current

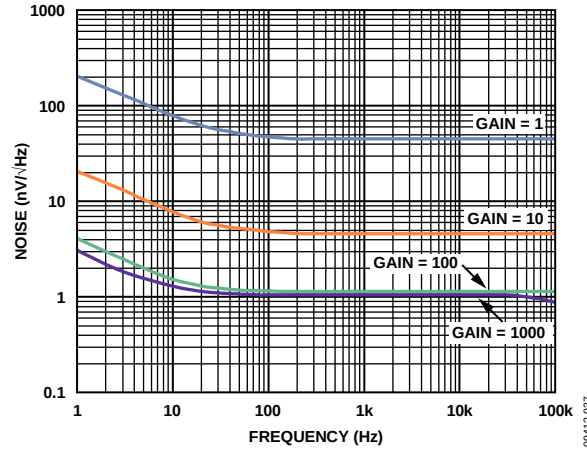


Figure 37. Voltage Noise Spectral Density vs. Frequency

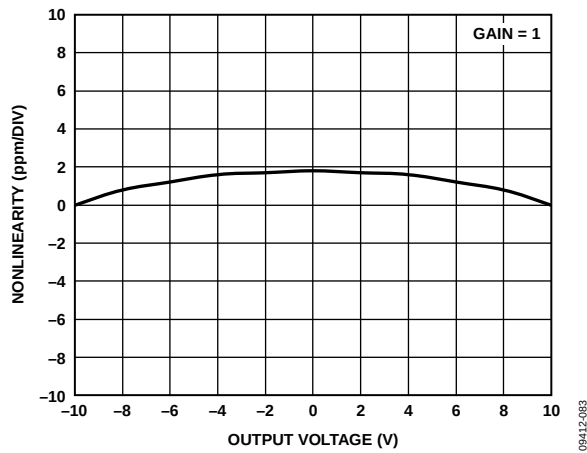


Figure 35. Gain Nonlinearity, $G = 1$, $R_L = 10\text{ k}\Omega$

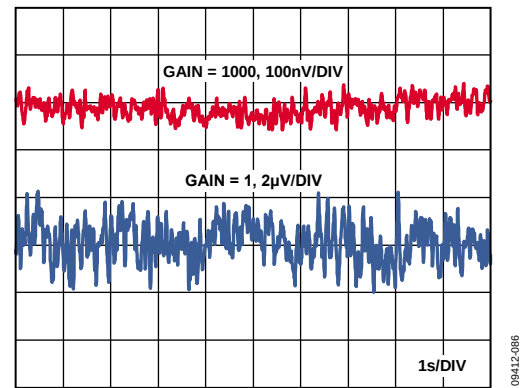


Figure 38. 0.1 Hz to 10 Hz RTI Voltage Noise, $G = 1$, $G = 1000$

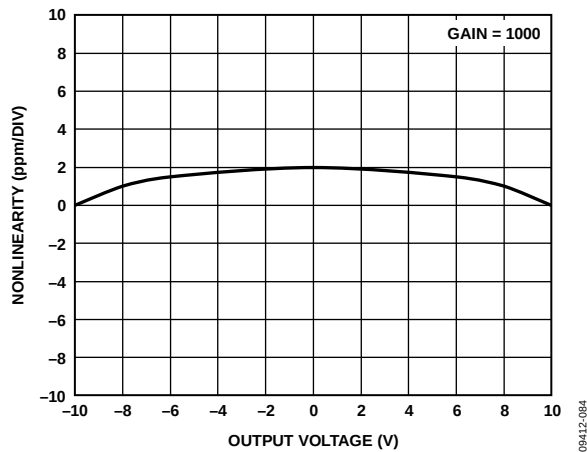


Figure 36. Gain Nonlinearity, $G = 1000$, $R_L = 10\text{ k}\Omega$

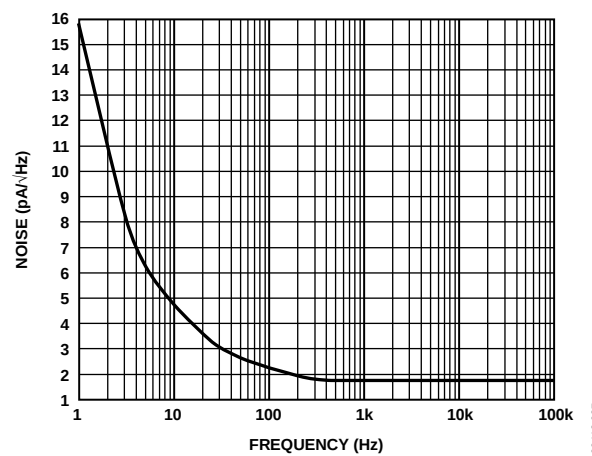


Figure 39. Current Noise Spectral Density vs. Frequency

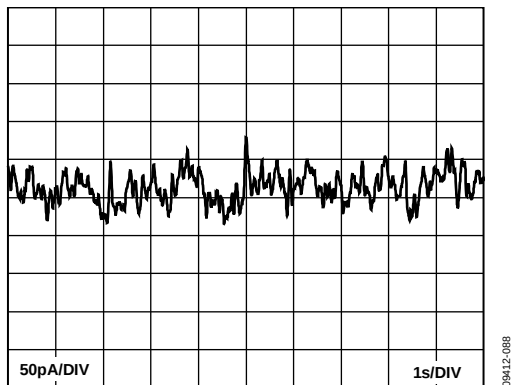


Figure 40. 1 Hz to 10 Hz Current Noise

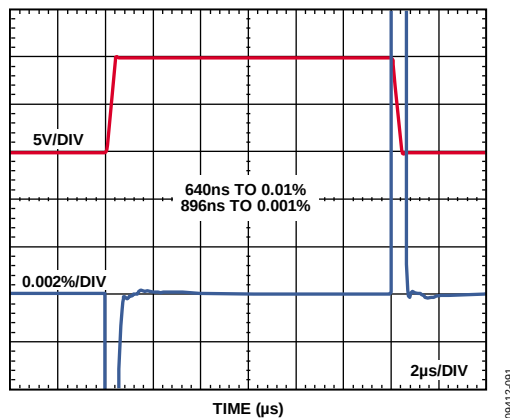
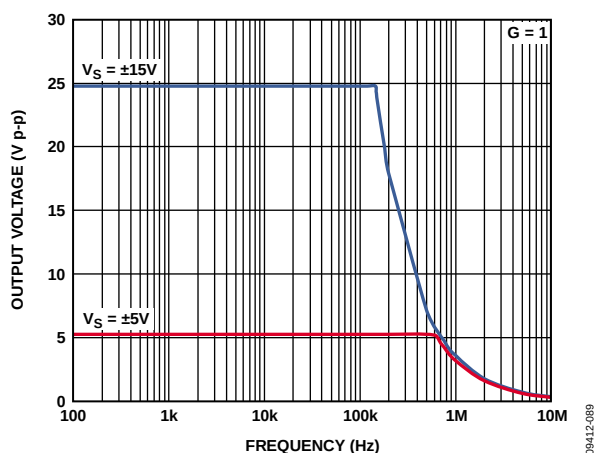
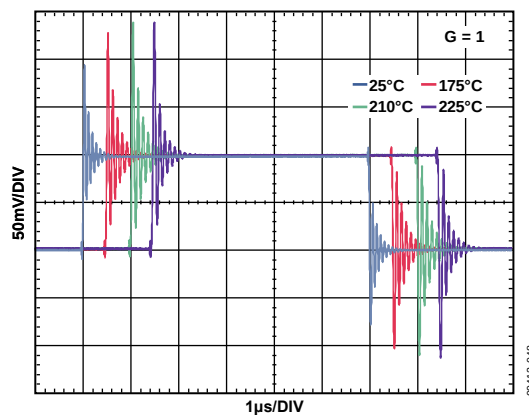
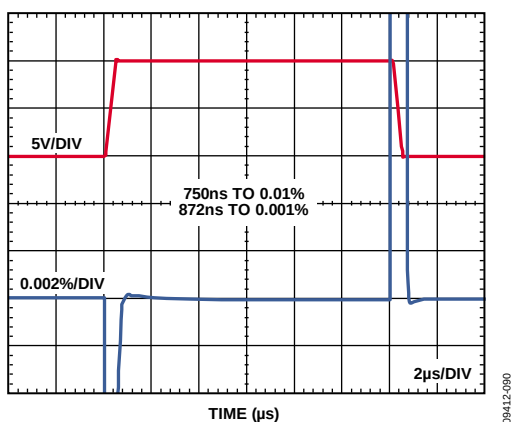
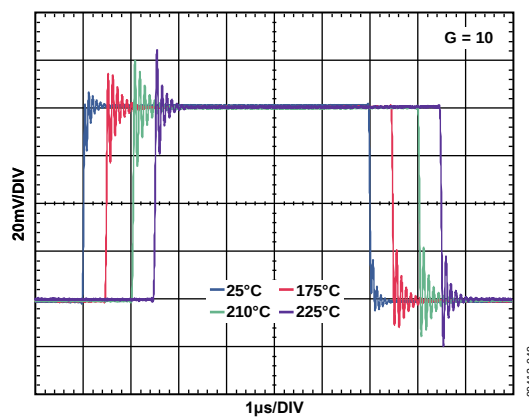
Figure 43. Large Signal Pulse Response and Settling Time ($G = 10$), 10 V Step, $V_S = \pm 15$ V

Figure 41. Large Signal Frequency Response

Figure 44. Small Signal Response, $G = 1$, $R_L = 10$ k Ω , $C_L = 100$ pFFigure 42. Large Signal Pulse Response and Settling Time ($G = 1$), 10 V Step, $V_S = \pm 15$ VFigure 45. Small Signal Response, $G = 10$, $R_L = 10$ k Ω , $C_L = 100$ pF

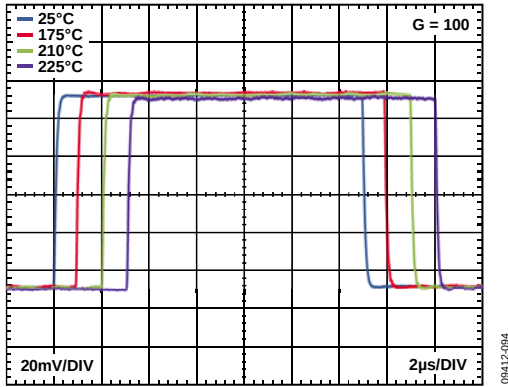


Figure 46. Small Signal Response, $G = 100$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$

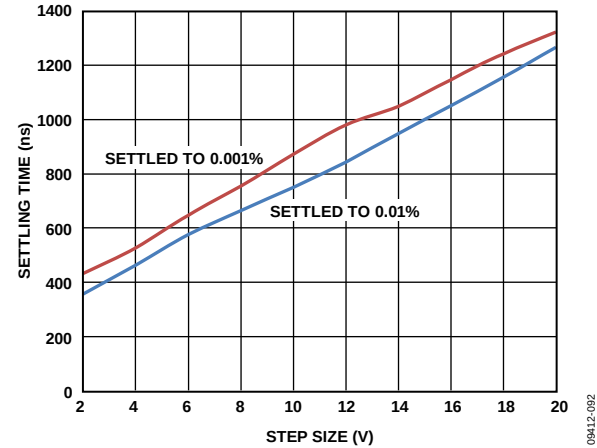


Figure 49. Settling Time vs. Step Size, $G = 1$

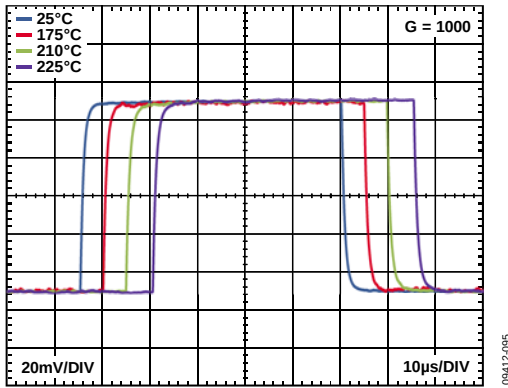


Figure 47. Small Signal Response, $G = 1000$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$

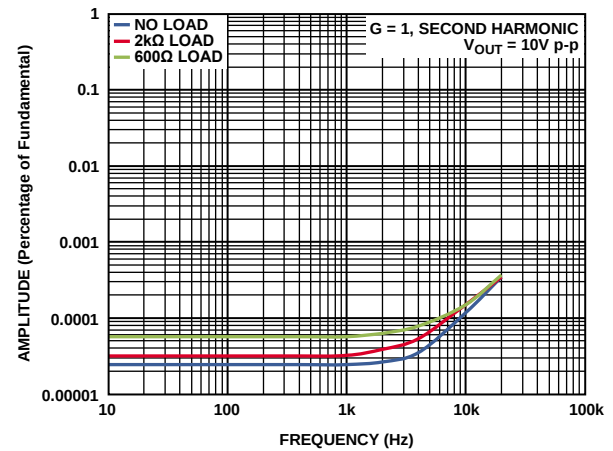


Figure 50. Second Harmonic Distortion vs. Frequency, $G = 1$

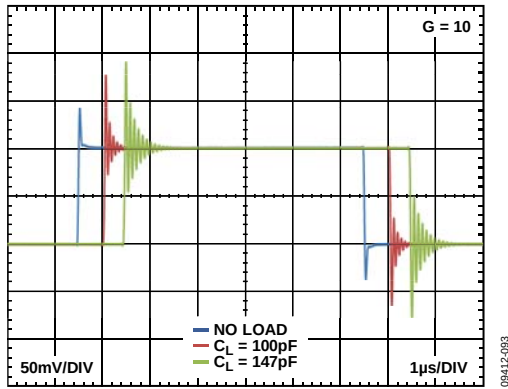


Figure 48. Small Signal Response with Various Capacitive Loads, $G = 1$, $R_L = \text{Infinity}$

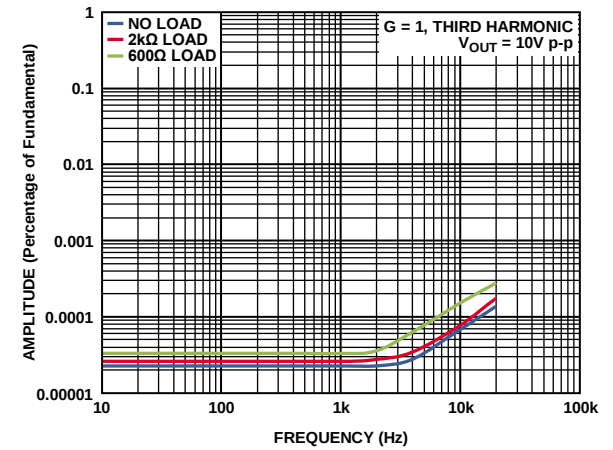


Figure 51. Third Harmonic Distortion vs. Frequency, $G = 1$

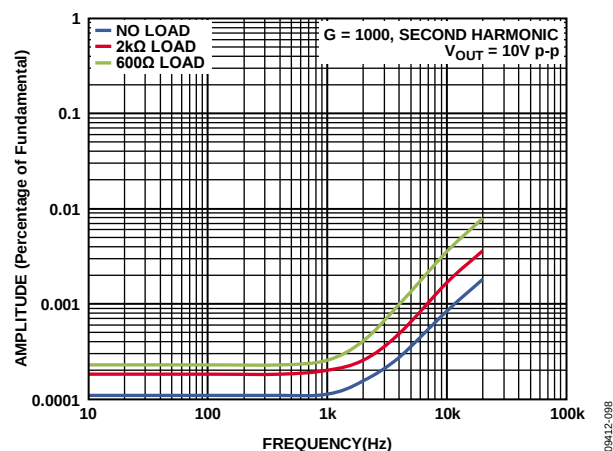


Figure 52. Second Harmonic Distortion vs. Frequency, G = 1000

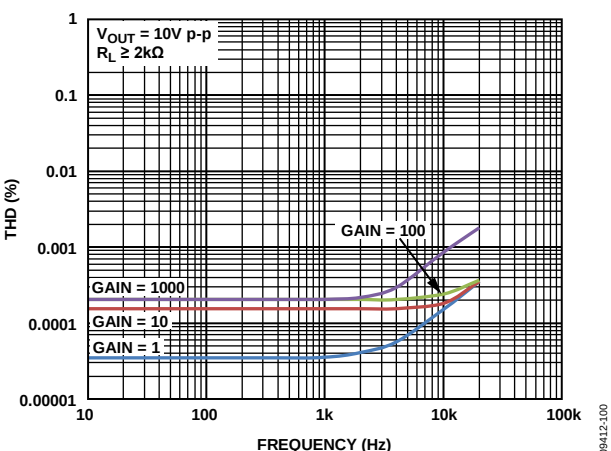


Figure 54. THD vs. Frequency

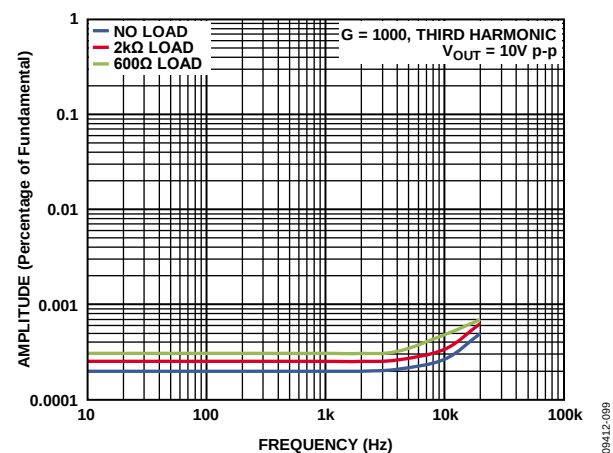


Figure 53. Third Harmonic Distortion vs. Frequency, G = 1000

THEORY OF OPERATION

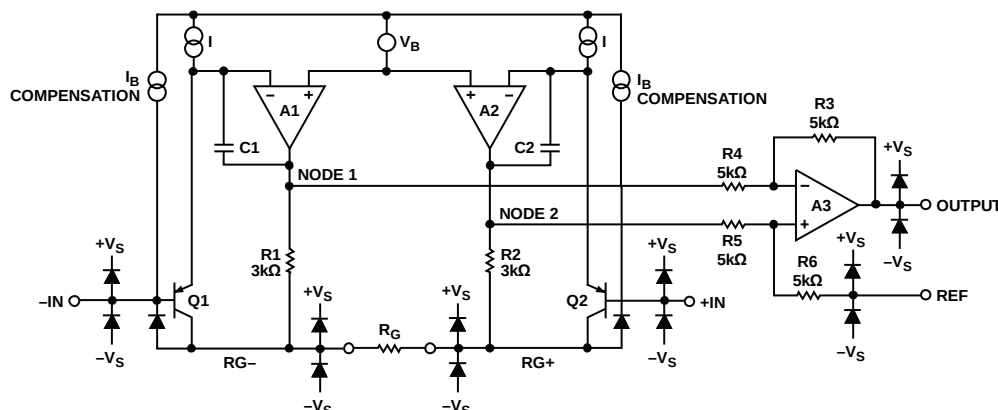


Figure 55. Simplified Schematic

09412-058

ARCHITECTURE

The AD8229 is based on the classic 3-op-amp topology. This topology has two stages: a preamplifier to provide differential amplification followed by a difference amplifier that removes the common-mode voltage and provides additional amplification. Figure 55 shows a simplified schematic of the AD8229.

The first stage works as follows. To keep its two inputs matched, Amplifier A1 must keep the collector of Q1 at a constant voltage. It does this by forcing R_{G-} to be a precise diode drop from $-IN$. Similarly, A2 forces R_{G+} to be a constant diode drop from $+IN$. Therefore, a replica of the differential input voltage is placed across the gain setting resistor, R_G . The current that flows through this resistance must also flow through the $R1$ and $R2$ resistors, creating a gained differential signal between the A2 and A1 outputs.

The second stage is a $G = 1$ difference amplifier, composed of Amplifier A3 and the $R3$ through $R6$ resistors. This stage removes the common-mode signal from the amplified differential signal.

The transfer function of the AD8229 is

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF}$$

where:

$$G = 1 + \frac{6 \text{ k}\Omega}{R_G}$$

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8229, which can be calculated by referring to Table 5 or by using the following gain equation:

$$R_G = \frac{6 \text{ k}\Omega}{G - 1}$$

Table 5. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (Ω)	Calculated Gain
6.04 k	1.993
1.5 k	5.000
665	10.02
316	19.99
121	50.59
60.4	100.34
30.1	200.34
12.1	496.9
6.04	994.4
3.01	1994.355

The AD8229 defaults to $G = 1$ when no gain resistor is used. The tolerance and gain drift of the R_G resistor should be added to the AD8229's specifications to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

R_G Power Dissipation

The AD8229 duplicates the differential voltage across its inputs onto the R_G resistor. The R_G resistor size should be chosen to handle the expected power dissipation.

REFERENCE TERMINAL

The output voltage of the AD8229 is developed with respect to the potential on the reference terminal. This is useful when the output signal must be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8229 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to the REF terminal should be kept well below 1 Ω. As shown in Figure 55, the reference terminal, REF, is at one end of a 5 kΩ resistor. Additional impedance at the REF terminal adds to this 5 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional R_{REF} can be calculated as follows:

$$2(5 \text{ k}\Omega + R_{REF}) / (10 \text{ k}\Omega + R_{REF})$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.

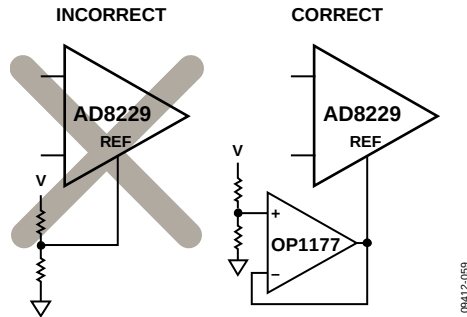


Figure 56. Driving the Reference Pin

INPUT VOLTAGE RANGE

Figure 10 through Figure 15 show the allowable common-mode input voltage ranges for various output voltages and supply voltages. The 3-op-amp architecture of the AD8229 applies gain in the first stage before removing common-mode voltage with the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 55) experience a combination of a gained signal, a common-mode signal, and a diode drop. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not limited.

LAYOUT

To ensure optimum performance of the AD8229 at the PCB level, care must be taken in the design of the board layout. The pins of the AD8229 are arranged in a logical manner to aid in this task.

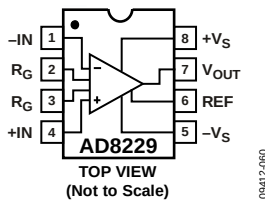


Figure 57. Pinout Diagram

Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR over frequency high, the input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input path (for example, for input protection) should be placed close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), the component should be chosen so that the parasitic capacitance is as small as possible.

Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 19 and Figure 20 for more information.

A 0.1 μF capacitor should be placed as close as possible to each supply pin. As shown in Figure 58, a 10 μF tantalum capacitor can be used farther away from the part. In most cases, it can be shared by other precision integrated circuits.

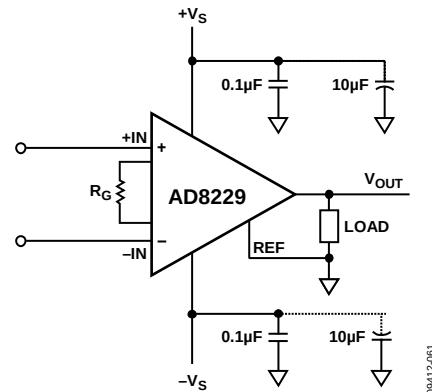


Figure 58. Supply Decoupling, REF, and Output Referred to Local Ground

Reference Pin

The output voltage of the AD8229 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8229 must have a return path to ground. When using a floating source without a current return path, such as a thermocouple, a current return path should be created, as shown in Figure 59.

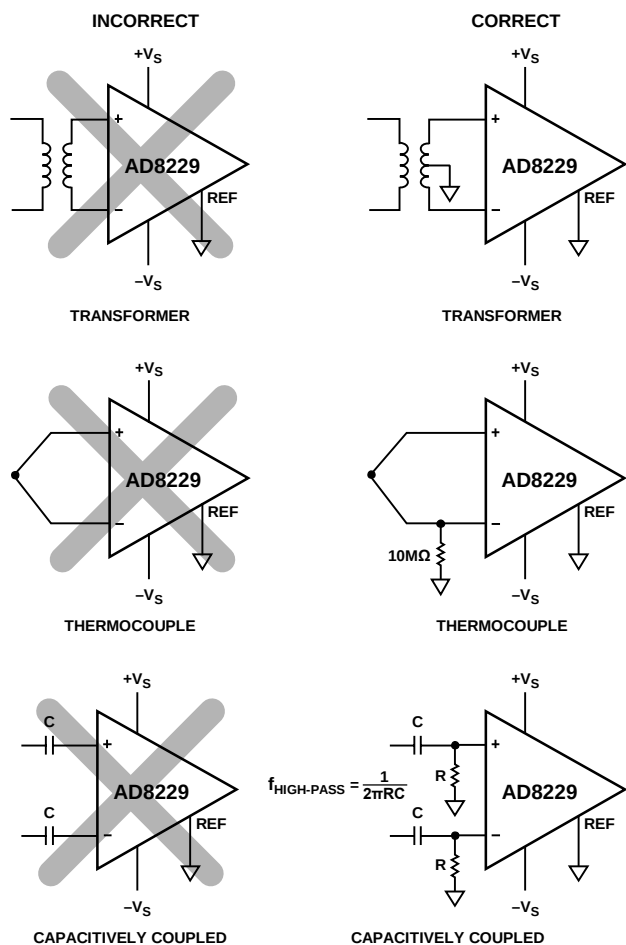


Figure 59. Creating an Input Bias Current Return Path

INPUT PROTECTION

The inputs to the AD8229 should be kept within the ratings stated in the Absolute Maximum Ratings section of this data sheet. If this cannot be done, protection circuitry can be added in front of the AD8229 to limit the current into the inputs to a maximum current, I_{MAX} .

Input Voltages Beyond the Rails

If voltages beyond the rails are expected, an external resistor should be used in series with each input to limit current during overload conditions. The limiting resistor at the input can be computed from

$$R_{PROTECT} \geq \frac{|V_{IN} - V_{SUPPLY}|}{I_{MAX}}$$

Noise-sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used at the inputs to shunt current away from the AD8229 inputs

and therefore allow smaller protection resistor values. To ensure current flows primarily through the external protection diodes, place a small value resistor, such as a 33 Ω, between the diodes and the AD8229.

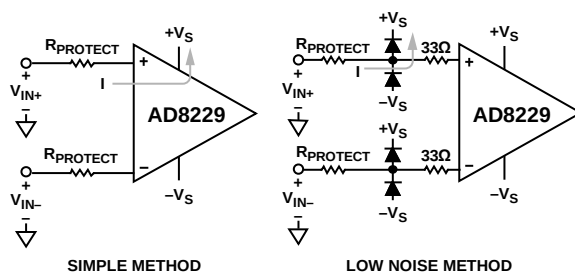


Figure 60. Protection for Voltages Beyond the Rails

Large Differential Input Voltage at High Gain

If large differential voltages at high gain are expected, an external resistor should be used in series with each input to limit current during overload conditions. The limiting resistor at each input can be computed from

$$R_{PROTECT} \geq \frac{1}{2} \left(\frac{|V_{DIFF}| - 1V}{I_{MAX}} - R_G \right)$$

Noise-sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used across the inputs to shunt current away from the AD8229 inputs and therefore allow smaller protection resistor values.

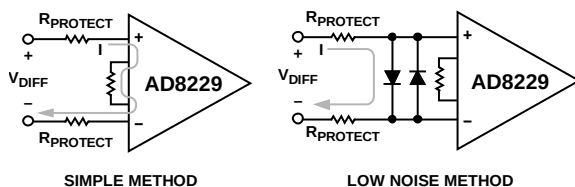


Figure 61. Protection for Large Differential Voltages

I_{MAX}

The maximum current into the AD8229 inputs, I_{MAX} , depends both on time and temperature. At room temperature, the part can withstand a current of 10 mA for at least a day. This time is cumulative over the life of the part. At 210°C, current should be limited to 2 mA for the same period of time. The part can withstand 5 mA at 210°C for an hour, cumulative over the life of the part.

RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications that have strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 62. The filter limits the input signal bandwidth, according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$\text{FilterFrequency}_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10 C_C$.

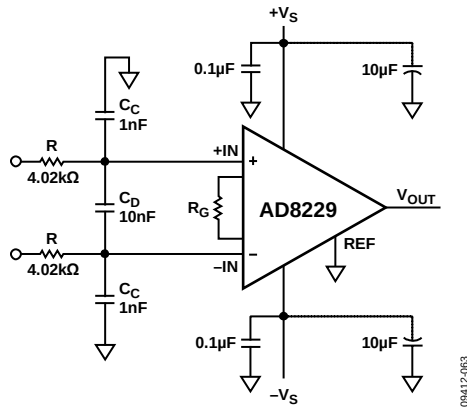


Figure 62. RFI Suppression

C_D affects the difference signal, and C_C affects the common-mode signal. Values of R and C_C should be chosen to minimize RFI. A mismatch between $R \times C_C$ at the positive input and $R \times C_C$ at the negative input degrades the CMRR of the AD8229. By using a value of C_D one magnitude larger than C_C , the effect of the mismatch is reduced, and performance is improved.

Resistors add noise; therefore, the resistor and capacitor values chosen depend on the desired tradeoff between noise, input impedance at high frequencies, and RFI immunity. The resistors used for the RFI filter can be the same as those used for input protection.

CALCULATING THE NOISE OF THE INPUT STAGE

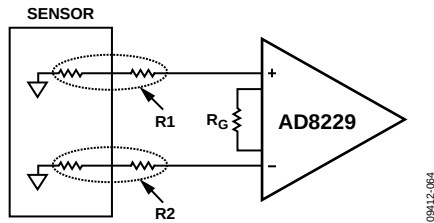


Figure 63. AD8229 with Source Resistance from Sensor and Protection Resistors

The total noise of the amplifier front end depends on much more than the $1 \text{ nV}/\sqrt{\text{Hz}}$ headline specification of this data sheet. The total noise is dependent on three main factors: the source resistance, the voltage noise of the instrumentation amplifier, and the current noise of the instrumentation amplifier.

In the following calculations, noise is referred to the input (RTI). In other words, everything is calculated as if it appeared at the amplifier input. To calculate the noise referred to the amplifier output (RTO), simply multiple the RTI noise by the gain of the instrumentation amplifier.

Source Resistance Noise

Any sensor connected to the AD8229 has some output resistance. There may also be resistance placed in series with inputs for protection from either overvoltage or radio frequency interference. This combined resistance is labeled R_1 and R_2 in Figure 63. Any resistor, no matter how well made, has a minimum level of noise. This noise is proportional to the square root of the resistor value. At room temperature, the value is approximately equal to $4 \text{ nV}/\sqrt{\text{Hz}} \times \sqrt{(\text{resistor value in k}\Omega)}$.

For example, assuming that the combined sensor and protection resistance on the positive input is $4 \text{ k}\Omega$ and on the negative input is $1 \text{ k}\Omega$, the total noise from the resistance is

$$\sqrt{(4 \times \sqrt{4})^2 + (4 \times \sqrt{1})^2} = \sqrt{64 + 16} = 8.9 \text{ nV}/\sqrt{\text{Hz}}$$

Voltage Noise of the Instrumentation Amplifier

The voltage noise of the instrumentation amplifier is calculated using three parameters: the part input noise, output noise, and the R_G resistor noise. It is calculated as follows:

Total Voltage Noise =

$$\sqrt{(\text{Output Noise}/G)^2 + (\text{Input Noise})^2 + (\text{Noise of } R_G \text{ Resistor})^2}$$

For example, for a gain of 100, the gain resistor is 60.4Ω . Therefore, the voltage noise of the in-amp is

$$\sqrt{(43/100)^2 + 1^2 + (4 \times \sqrt{0.0604})^2} = 1.5 \text{ nV}/\sqrt{\text{Hz}}$$

Current Noise of the Instrumentation Amplifier

Current noise is calculated by multiplying the source resistance by the current noise.

For example, if the R_1 source resistance in Figure 63 is $4 \text{ k}\Omega$, and the R_2 source resistance is $1 \text{ k}\Omega$, the total effect from the current noise is calculated as follows:

$$\sqrt{((4 \times 1.5)^2 + (1 \times 1.5)^2)} = 6.2 \text{ nV}/\sqrt{\text{Hz}}$$

Total Noise calculation

To determine the total noise of the in-amp, referred to input, combine the source resistance noise, voltage noise, and current noise contribution by the sum of squares method.

For example, if the R_1 source resistance in Figure 63 is $4 \text{ k}\Omega$, the R_2 source resistance is $1 \text{ k}\Omega$, and the gain of the in-amps is 100, the total noise, referred to input, is

$$\sqrt{8.9^2 + 1.5^2 + 6.2^2} = 11.0 \text{ nV}/\sqrt{\text{Hz}}$$

OUTLINE DIMENSIONS

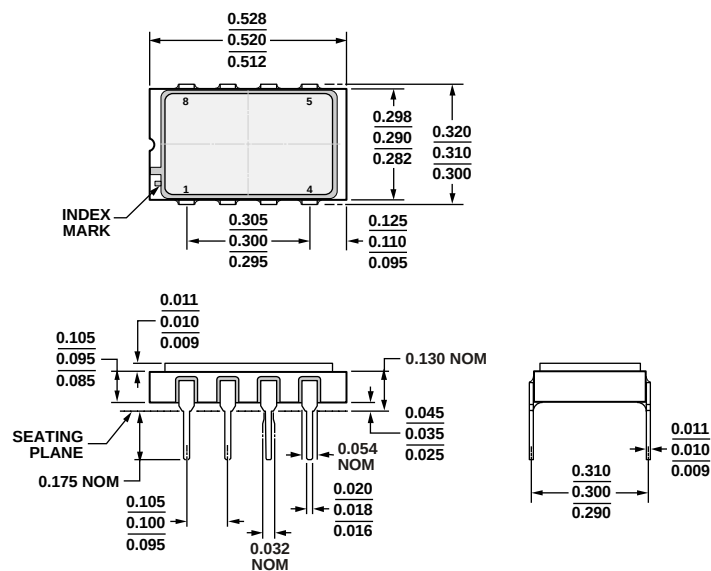


Figure 64. 8-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] (D-8-1))
Dimensions shown in inches

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD8229HDZ	−40°C to +210°C	Ceramic Dual In-Line Package [SBDIP]	D-8-1

¹ Z = RoHS Compliant Part.

AD8229

NOTES

NOTES

AD8229

NOTES