High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- 120 MHz Bandwidth, Gain = –1
- 230 V/μs Slew Rate
- 90 ns Settling Time to 0.1%

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase

Low Noise
- 1.7 nV/√Hz Input Voltage Noise
- 1.5 pA/√Hz Input Current Noise

Excellent DC Precision
- 1 mV Max Input Offset Voltage (Over Temp)
- 0.3 mV/°C Input Offset Drift

Flexible Operation
- Specified for ±5 V to ±15 V Operation
- ±3 V Output Swing into a 150 Ω Load
- External Compensation for Gains 1 to 20
- 5 mA Supply Current

Available in Tape and Reel in Accordance with EIA-481A Standard

GENERAL DESCRIPTION

The AD829 is a low noise (1.7 nV/√Hz), high speed op amp with custom compensation that provides the user with gains of ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth while requiring only 5 mA of current from power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the –3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. The AD829's output can also be clamped at its external compensation pin.

The AD829 exhibits excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 1.7 nV/√Hz, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

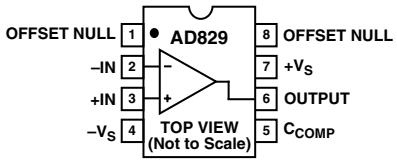
This op amp is also useful in multichannel, high speed data conversion where its fast (90 ns to 0.1%) settling time is important. In such applications, the AD829 serves as an input buffer for 8-bit to 10-bit A/D converters and as an output I/V converter for high speed DACs.

REV. G

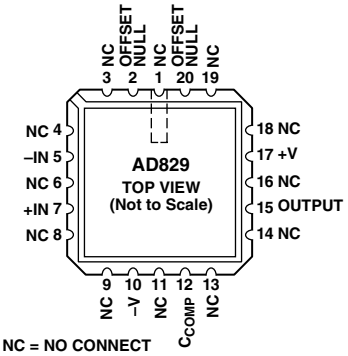
CONNECTION DIAGRAMS

8-Lead

PDIP(N), Cerdip (Q), and SOIC (R) Packages



20-Lead LCC Pinout



NC = NO CONNECT

Operating as a traditional voltage feedback amplifier, the AD829 provides many of the advantages a transimpedance amplifier offers. A bandwidth greater than 50 MHz can be maintained for a range of gains through the replacement of the external compensation capacitor. The AD829 and the transimpedance amplifier are both unity gain stable and provide similar voltage noise performance (1.7 nV/√Hz); however, the current noise of the AD829 (1.5 pA/√Hz) is less than 10% of the noise of transimpedance amps. The inputs of the AD829 are symmetrical.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/√Hz, current noise of 1.5 pA/√Hz, and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make the op amp an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. The AD829 is available in plastic, CERDIP, and small outline packages. Chips and MIL-STD-883B parts are also available. The SOIC-8 package is available for the extended temperature range of –40°C to +125°C.

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AD829—SPECIFICATIONS (@ T_A = 25°C and V_S = ±15 V dc, unless otherwise noted.)

Model	Conditions	V_S	AD829JR Min	AD829JR Typ	AD829JR Max	AD829AR Min	AD829AR Typ	AD829AR Max	AD829AQ/S Min	AD829AQ/S Typ	AD829AQ/S Max	Unit
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.2	1		0.1	0.5	mV
	T_{MIN} to T_{MAX}				1			1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7		3.3	7	µA
	T_{MIN} to T_{MAX}				8.2			9.5			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500		50	500	nA
	T_{MIN} to T_{MAX}				500			500			500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V										
	R_{LOAD} = 500 Ω		30	65		30	65		30	65		V/mV
	T_{MIN} to T_{MAX}		20			20			20			V/mV
	R_{LOAD} = 150 Ω			40			40			40		V/mV
	V_{OUT} = ±10 V	±15 V										
	R_{LOAD} = 1 kΩ		50	100		50	100		50	100		V/mV
	T_{MIN} to T_{MAX}		20			20			20			V/mV
	R_{LOAD} = 500 Ω			85			85			85		V/mV
DYNAMIC PERFORMANCE												
Gain Bandwidth Product		±5 V		600			600			600		MHz
		±15 V		750			750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p-p											
	R_{LOAD} = 500 Ω	±5 V		25			25			25		MHz
	V_O = 20 V p-p											
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230			230		V/µs
Settling Time to 0.1%	A_V = –19											
	–2.5 V to +2.5 V	±5 V		65			65			65		ns
	10 V Step	±15 V		90			90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V										
	R_{LOAD} = 1 kΩ			60			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V										
	C_{COMP} = 30 pF			0.02			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V										
	C_{COMP} = 30 pF			0.04			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		100	120		dB
	T_{MIN} to T_{MAX}		96			96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		98	120		dB
	T_{MIN} to T_{MAX}		94			94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		1.7	2		1.7	2		1.7	2	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3			+4.3		V
				–3.8			–3.8			–3.8		V
		±15 V		+14.3			+14.3			+14.3		V
				–13.8			–13.8			–13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	±3.0	±3.6		±3.0	±3.6		±3.0	±3.6		V
	R_{LOAD} = 150 Ω	±5 V	±2.5	±3.0		±2.5	±3.0		±2.5	±3.0		V
	R_{LOAD} = 50 Ω	±5 V		±1.4			±1.4			±1.4		V
	R_{LOAD} = 1 kΩ	±15 V	±12	±13.3		±12	±13.3		±12	±13.3		V
	R_{LOAD} = 500 Ω	±15 V	±10	±12.2		±10	±12.2		±10	±12.2		V
Short Circuit Current		±5 V, ±15 V		32			32			32		mA
INPUT CHARACTERISTICS												
Input Resistance (Differential)				13			13			13		kΩ
Input Capacitance (Differential)[4]				5			5			5		pF
Input Capacitance (Common Mode)				1.5			1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2			2		mΩ

Model	Conditions	V_S	AD829JR Min	AD829JR Typ	AD829JR Max	AD829AR Min	AD829AR Typ	AD829AR Max	AD829AQ/S Min	AD829AQ/S Typ	AD829AQ/S Max	Unit
POWER SUPPLY												
Operating Range			±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		±15 V		5	6.5		5	6.5		5	6.5	mA
	T_{MIN} to T_{MAX}				8.0			8.0			8.2/8.7	mA
		±15 V		5.3	6.8		5.3	6.8		5.3	6.8	mA
	T_{MIN} to T_{MAX}				8.3			9.0			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors			46			46			46		

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL and SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18 V
Internal Power Dissipation[2]	
PDIP (N)	1.3 W
SOIC (R)	0.9 W
CERDIP (Q)	1.3 W
LCC (E)	0.8 W
Input Voltage	±V
Differential Input Voltage[3]	±6 V
Output Short Circuit Duration	Indefinite
Storage Temperature Range (Q, E)	–65°C to +150°C
Storage Temperature Range (N, R)	–65°C to +125°C
Operating Temperature Range	
AD829J	0°C to 70°C
AD829A	–40°C to +125°C
AD829S	–55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

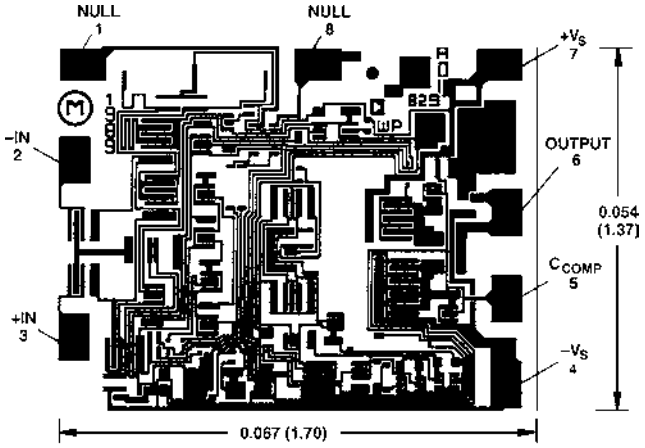
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Maximum internal power dissipation is specified so that T_J does not exceed 150°C at an ambient temperature of 25°C.
Thermal characteristics:
8-lead PDIP package: θ_{JA} = 100°C/W (derate at 8.7 mW/°C)
8-lead CERDIP package: θ_{JA} = 110°C/W (derate at 8.7 mW/°C)
20-lead LCC package: θ_{JA} = 77°C/W
8-lead SOIC package: θ_{JA} = 125°C/W (derate at 6 mW/°C).

[3] If the differential voltage exceeds 6 V, external series protection resistors should be added to limit the input current.

METALLIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



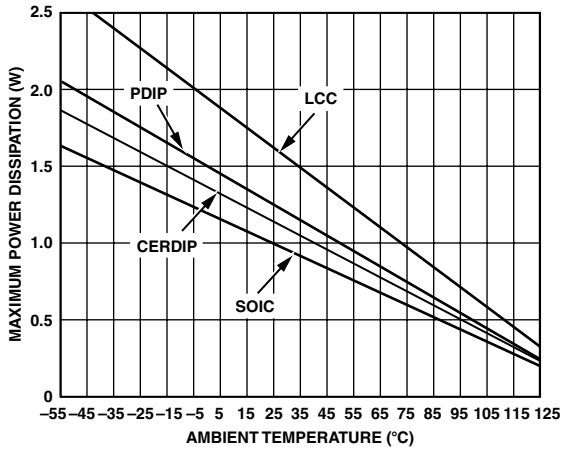


Figure 1. Maximum Power Dissipation vs. Temperature

CAUTION

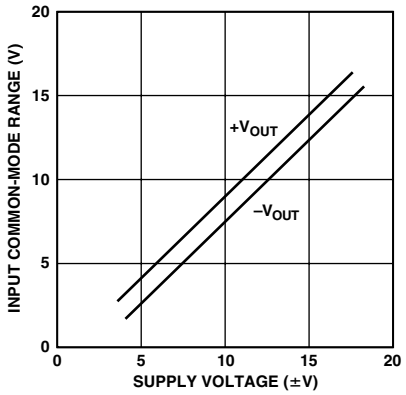
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD829 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

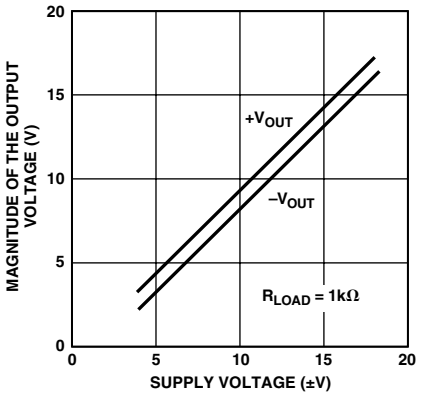
Model	Temperature Range	Package Description	Package Option
AD829AR	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829AR-REEL	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829AR-REEL7	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ*	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ-REEL*	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829ARZ-REEL7*	–40°C to +125°C	8-Lead Plastic SOIC	R-8
AD829JN	0°C to 70°C	8-Lead Plastic PDIP	N-8
AD829JR	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829JR-REEL	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829JR-REEL7	0°C to 70°C	8-Lead Plastic SOIC	R-8
AD829AQ	–40°C to +125°C	8-Lead CERDIP	Q-8
AD829SQ	–55°C to +125°C	8-Lead CERDIP	Q-8
AD829SQ/883B	–55°C to +125°C	8-Lead CERDIP	Q-8
5962-9312901MPA	–55°C to +125°C	8-Lead CERDIP	Q-8
AD829SE/883B	–55°C to +125°C	20-Lead LCC	E-20A
5962-9312901M2A	–55°C to +125°C	20-Lead LCC	E-20A
AD829JCHIPS		Die	
AD829SCHIPS		Die	

*Z = Pb-free part.

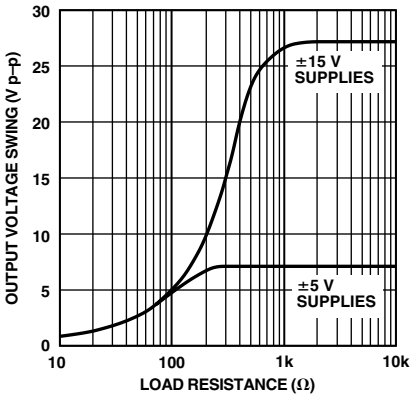
AD829–Typical Performance Characteristics



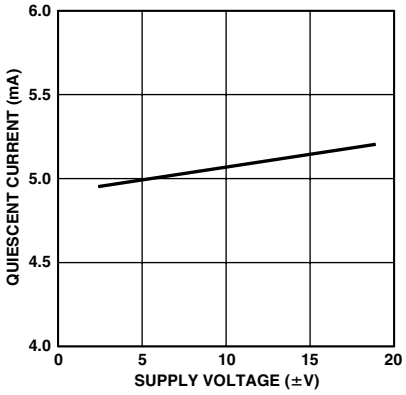
TPC 1. Input Common-Mode Range vs. Supply Voltage



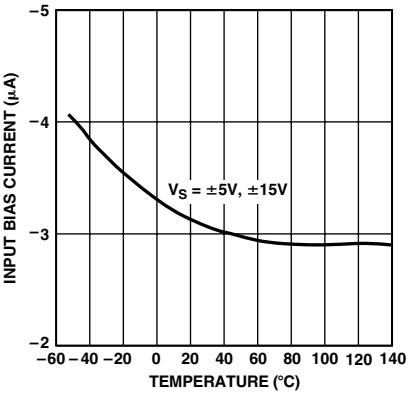
TPC 2. Output Voltage Swing vs. Supply Voltage



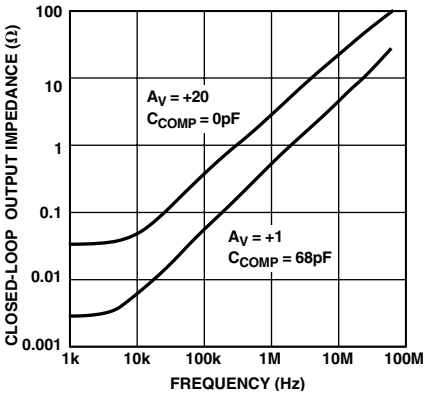
TPC 3. Output Voltage Swing vs. Resistive Load



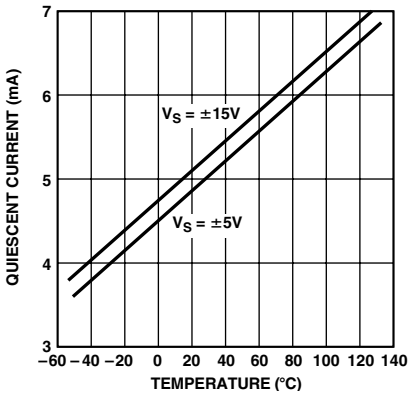
TPC 4. Quiescent Current vs. Supply Voltage



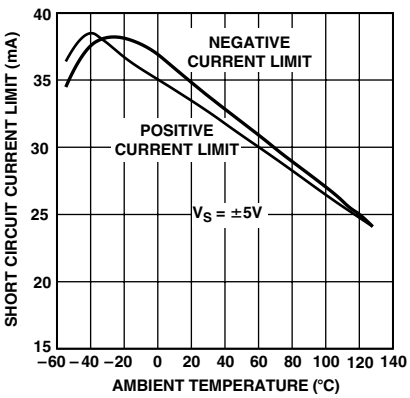
TPC 5. Input Bias Current vs. Temperature



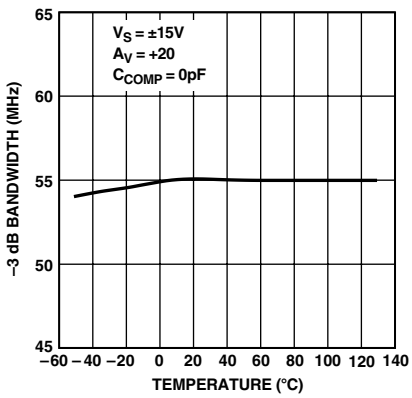
TPC 6. Closed-Loop Output Impedance vs. Frequency



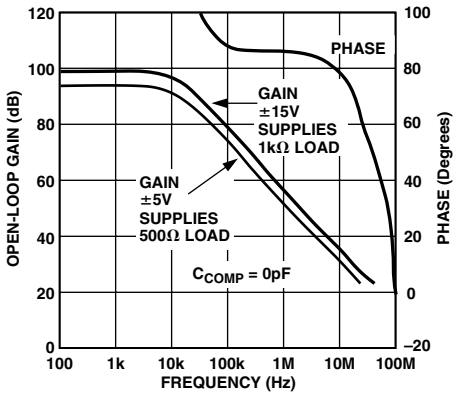
TPC 7. Quiescent Current vs. Temperature



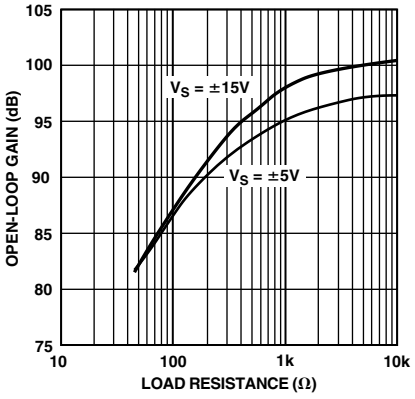
TPC 8. Short-Circuit Current Limit vs. Temperature



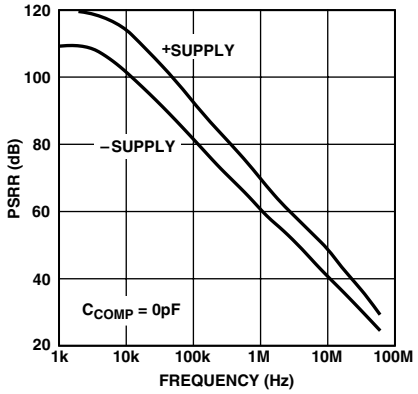
TPC 9. –3 dB Bandwidth vs. Temperature



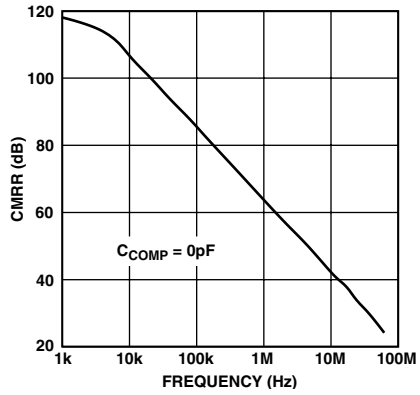
TPC 10. Open-Loop Gain and Phase Margin vs. Frequency



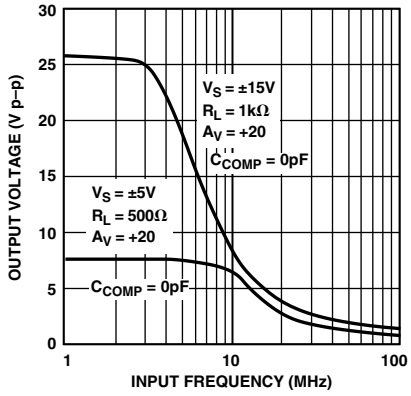
TPC 11. Open-Loop Gain vs. Resistive Load



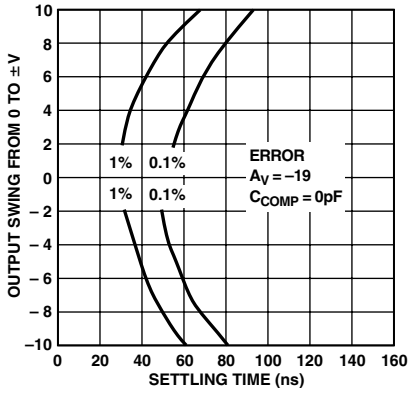
TPC 12. Power Supply Rejection Ratio (PSRR) vs. Frequency



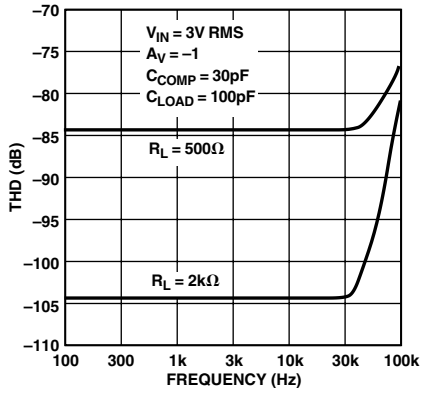
TPC 13. Common-Mode Rejection Ratio vs. Frequency



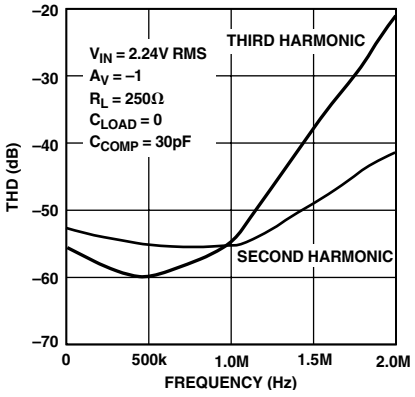
TPC 14. Large Signal Frequency Response



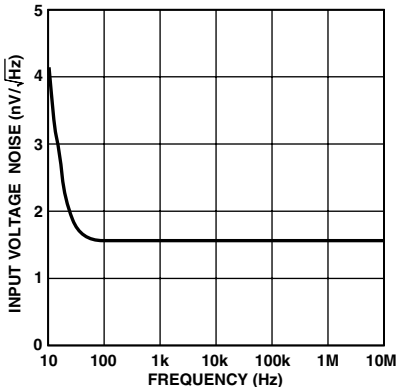
TPC 15. Output Swing and Error vs. Settling Time



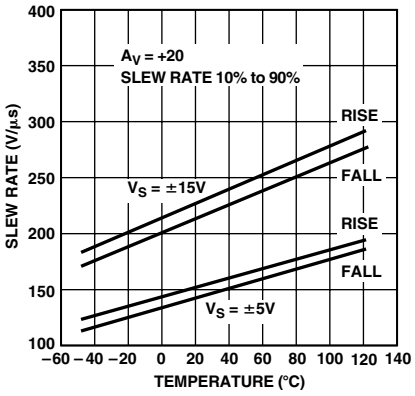
TPC 16. Total Harmonic Distortion (THD) vs. Frequency



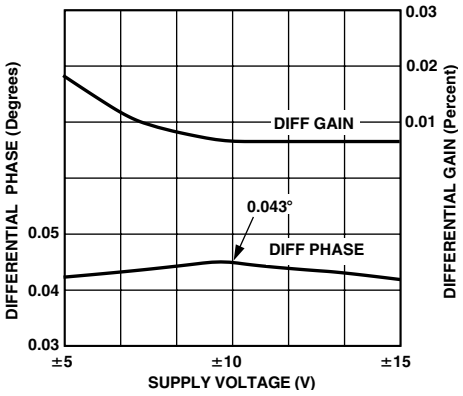
TPC 17. Second and Third Harmonic Distortion vs. Frequency



TPC 18. Input Voltage Noise Spectral Density



TPC 19. Slew Rate vs. Temperature



TPC 20. Differential Gain and Phase vs. Supply

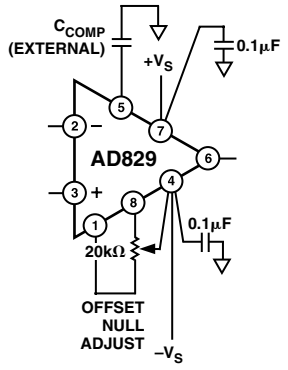


Figure 2. Offset Null and External Shunt Compensation Connections

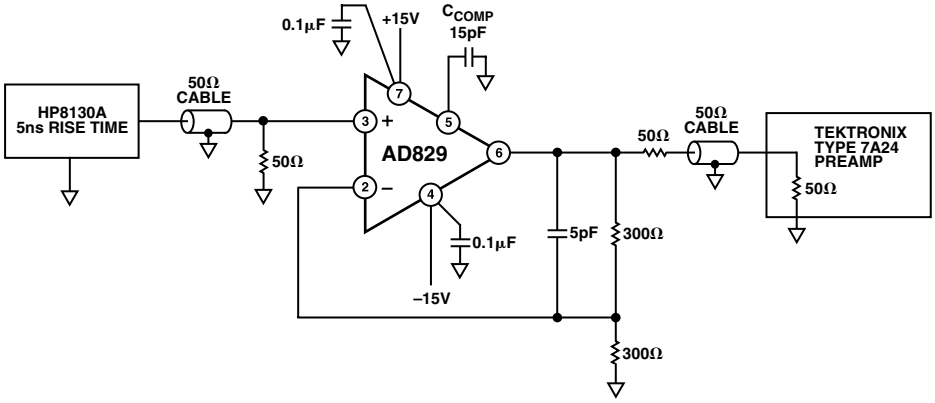


Figure 3a. Follower Connection. Gain = +2

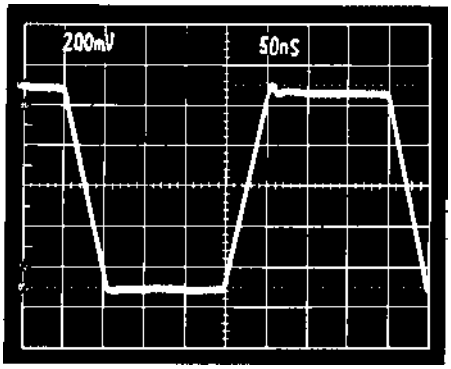


Figure 3b. Gain-of-2 Follower Large Signal Pulse Response

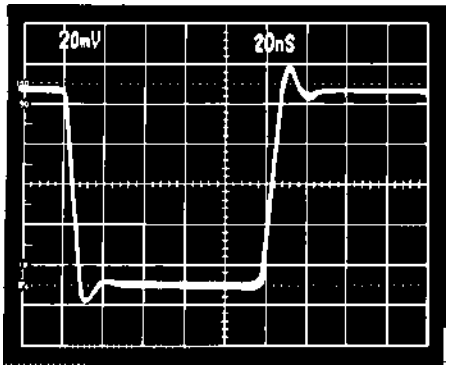


Figure 3c. Gain-of-2 Follower Small Signal Pulse Response

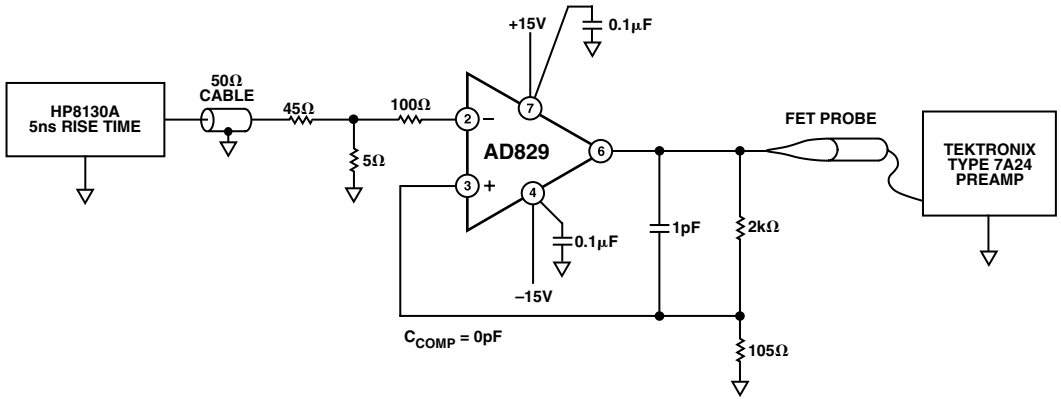


Figure 4a. Follower Connection. Gain = +20

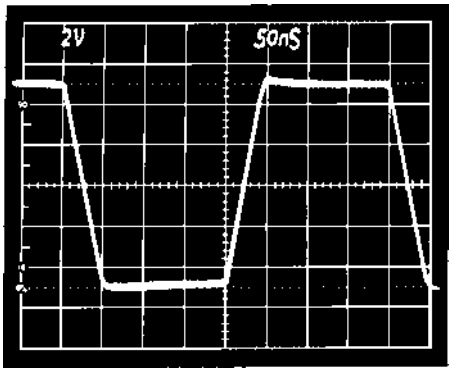


Figure 4b. Gain-of-20 Follower Large Signal Pulse Response

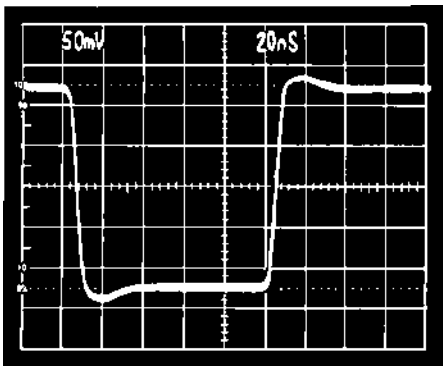


Figure 4c. Gain-of-20 Follower Small Signal Pulse Response

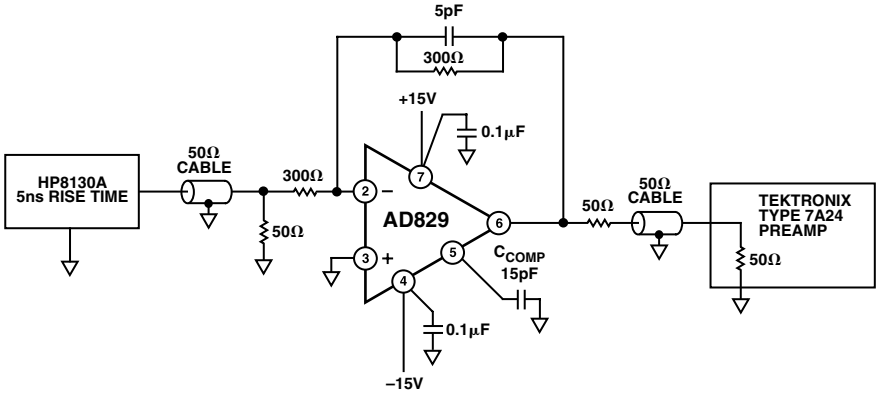


Figure 5a. Unity Gain Inverter Connection

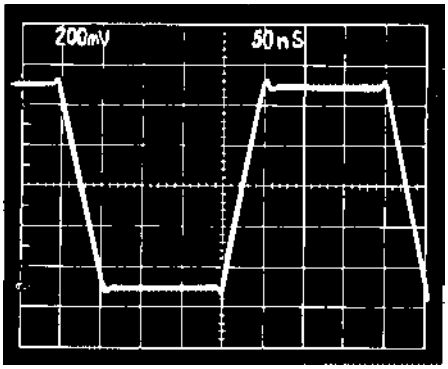


Figure 5b. Unity Gain Inverter Large Signal Pulse Response

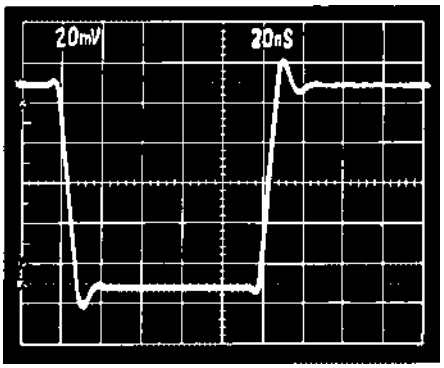


Figure 5c. Unity Gain Inverter Small Signal Pulse Response

THEORY OF OPERATION

The AD829 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process, which provides PNP and NPN transistors with similar f_Ts of 600 MHz. As shown in Figure 6, the AD829 input stage consists of an NPN differential pair in which each transistor operates at 600 μA collector current. This gives the input devices a high transconductance, which in turn gives the AD829 a low noise figure of 2 nV/√Hz @ 1 kHz.

The input stage drives a folded cascode that consists of a fast pair of PNP transistors. These PNPs drive a current mirror that provides a differential-input-to-single-ended-output conversion. The high speed PNPs are also used in the current-amplifying output stage, which provides high current gain of 40,000. Even under conditions of heavy loading, the high f_Ts of the NPN and PNPs, produced using the CB process, permits cascading two stages of emitter followers while maintaining 60° phase margin at closed-loop bandwidths greater than 50 MHz.

Two stages of complementary emitter followers also effectively buffer the high impedance compensation node (at the C_{COMP} pin) from the output so the AD829 can maintain a high dc open-loop gain, even into low load impedances: 92 dB into a 150 Ω load and 100 dB into a 1 kΩ load. Laser trimming and PTAT biasing ensure low offset voltage and low offset voltage drift, enabling the user to eliminate ac coupling in many applications.

For added flexibility, the AD829 provides access to the internal frequency compensation node. This allows the user to customize frequency response characteristics for a particular application.

Unity gain stability requires a compensation capacitance of 68 pF (Pin 5 to ground), which will yield a small signal bandwidth of 66 MHz and slew rate of 16 V/μs. The slew rate and gain bandwidth product will vary inversely with compensation capacitance. Table I and Figure 8 show the optimum compensation capacitance and the resulting slew rate for a desired noise gain. For gains between 1 and 20, C_{COMP} can be chosen to keep the small signal bandwidth relatively constant. The minimum gain that will still provide stability depends on the value of external compensation capacitance.

An RC network in the output stage (Figure 6) completely removes the effect of capacitive loading when the amplifier is compensated for closed-loop gains of 10 or higher. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C is bootstrapped and does not contribute to the compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage this reduces the gain, and subsequently, C is incompletely bootstrapped. Therefore, some fraction of C contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is further increased, the bandwidth continues to fall and the amplifier remains stable.

Externally Compensating the AD829

The AD829 is stable with no external compensation for noise gains greater than 20. For lower gains, two different methods of frequency compensating the amplifier can be used to achieve closed-loop stability: shunt and current feedback compensation.

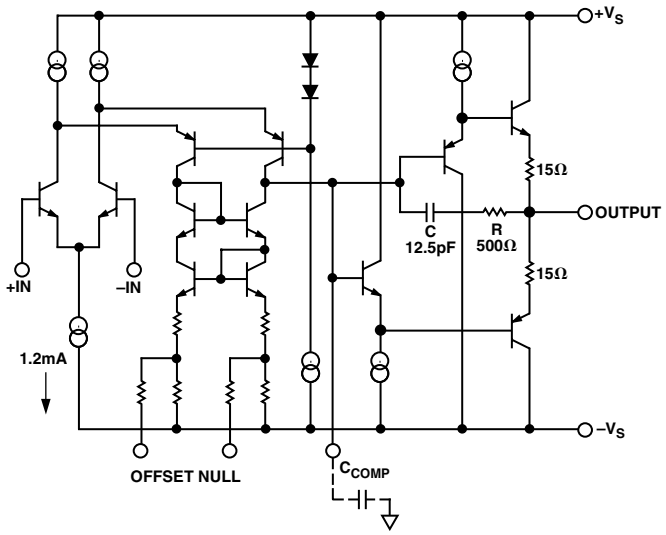


Figure 6. Simplified Schematic

Shunt Compensation

Figures 7 and 8 show that shunt compensation has an external compensation capacitor, C_{COMP}, connected between the compensation pin and ground. This external capacitor is tied in parallel with approximately 3 pF of internal capacitance at the compensation node. In addition, a small capacitance, C_{LEAD}, in parallel with resistor R2, compensates for the capacitance at the amplifier's inverting input.

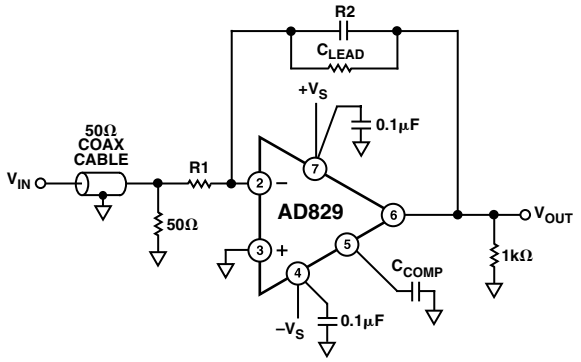


Figure 7. Inverting Amplifier Connection Using External Shunt Compensation

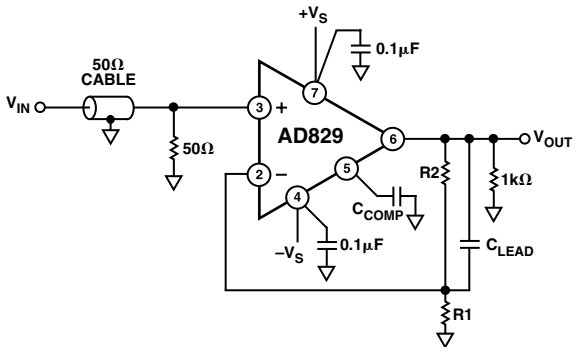


Figure 8. Noninverting Amplifier Connection Using External Shunt Compensation

Table I. Component Selection for Shunt Compensation

Follower Gain	Inverter Gain	R1 (Ω)	R2 (Ω)	C_L (pF)	C_{COMP} (pF)	Slew Rate (V/μs)	–3 dB Small Signal Bandwidth (MHz)
1		Open	100	0	68	16	66
2	–1	1 k	1 k	5	25	38	71
5	–4	511	2.0 k	1	7	90	76
10	–9	226	2.05 k	0	3	130	65
20	–19	105	2 k	0	0	230	55
25	–24	105	2.49	0	0	230	39
100	–99	20	2 k	0	0	230	7.5

Table I gives the recommended C_{COMP} and C_{LEAD} values, as well as the corresponding slew rates and bandwidth. The capacitor values were selected to provide a small signal frequency response with less than 1 dB of peaking and less than 10% overshoot. For this table, supply voltages of ±15 V should be used. Figure 9 is a graphical extension of the table that shows the slew rate/gain trade-off for lower closed-loop gains, when using the shunt compensation scheme.

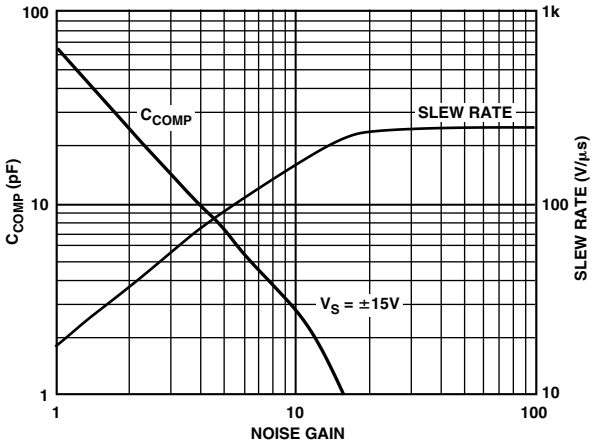


Figure 9. Value of C_{COMP} and Slew Rate vs. Noise Gain

Current Feedback Compensation

Bipolar, nondegenerated, single pole, and internally compensated amplifiers have their bandwidths defined as

$$f_T = \frac{1}{2\pi r_e C_{COMP}} = \frac{I}{2\pi \frac{kT}{q} C_{COMP}}$$

where
f_T is the unity gain bandwidth of the amplifier.
I is the collector current of the input transistor.
C_{COMP} is the compensation capacitance.
r_e is the inverse of the transconductance of the input transistors.
kT/q approximately equals 26 mV @ 27°C.

Since both f_T and slew rate are functions of the same variables, the dynamic behavior of an amplifier is limited. Since

$$Slew\ Rate = \frac{2I}{C_{COMP}}$$

then

$$\frac{Slew\ Rate}{f_T} = 4\pi \frac{kT}{q}$$

This shows that the slew rate will be only 0.314 V/μs for every MHz of bandwidth. The only way to increase slew rate is to increase the f_T, and that is difficult because of process limitations. Unfortunately, an amplifier with a bandwidth of 10 MHz can only slew at 3.1 V/μs, which is barely enough to provide a full power bandwidth of 50 kHz.

The AD829 is especially suited to a new form of compensation that allows for the enhancement of both the full power bandwidth and slew rate of the amplifier. The voltage gain from the inverting input pin to the compensation pin is large; therefore, if a capacitance is inserted between these pins, the amplifier's bandwidth becomes a function of its feedback resistor and the capacitance. The slew rate of the amplifier is now a function of its internal bias (2I) and the compensation capacitance.

Since the closed-loop bandwidth is a function of R_F and C_{COMP} (Figure 10), it is independent of the amplifier closed-loop gain, as shown in Figure 12. To preserve stability, the time constant of R_F and C_{COMP} needs to provide a bandwidth of less than 65 MHz. For example, with C_{COMP} = 15 pF and R_F = 1 kΩ, the small signal bandwidth of the AD829 is 10 MHz. Figure 11 shows that the slew rate is in excess of 60 V/μs. As shown in Figure 12, the closed-loop bandwidth is constant for gains of –1 to –4; this is a property of current feedback amplifiers.

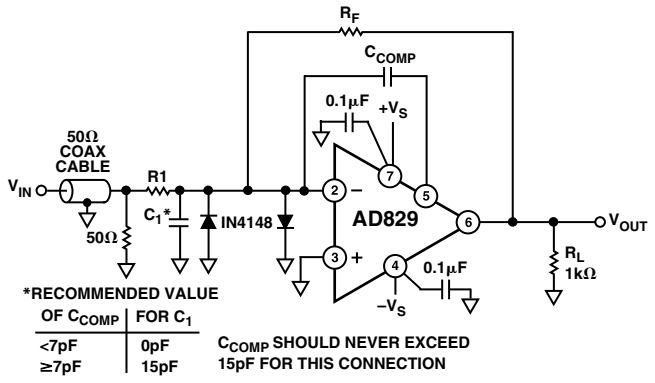


Figure 10. Inverting Amplifier Connection Using Current Feedback Compensation

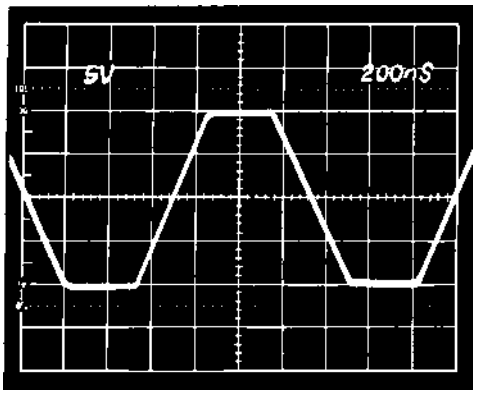


Figure 11. Large Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation, C_{COMP} = 15 pF, C1 = 15 pF, R_F = 1 kΩ, R1 = 1 kΩ

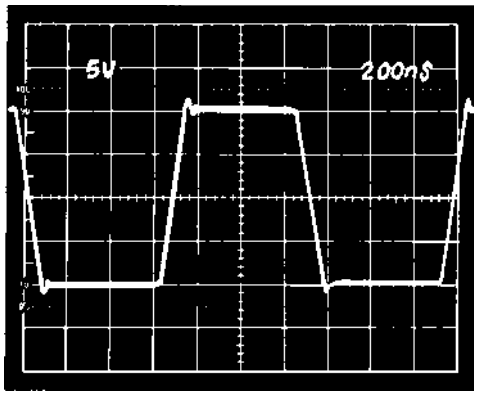


Figure 13. Large Signal Pulse Response of the Inverting Amplifier Using Current Feedback Compensation, C_{COMP} = 1 pF, R_F = 3 kΩ, R1 = 3 kΩ

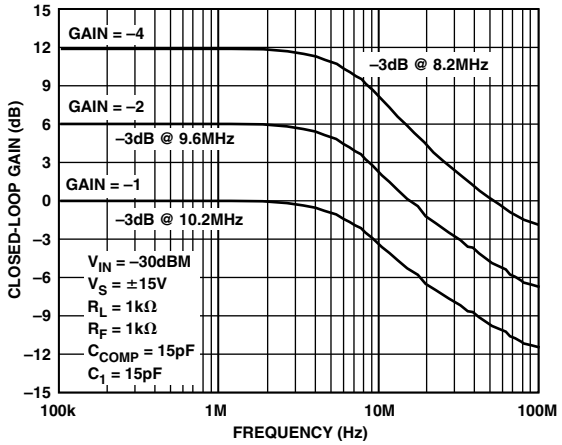


Figure 12. Closed-Loop Gain vs. Frequency for the Circuit of Figure 9

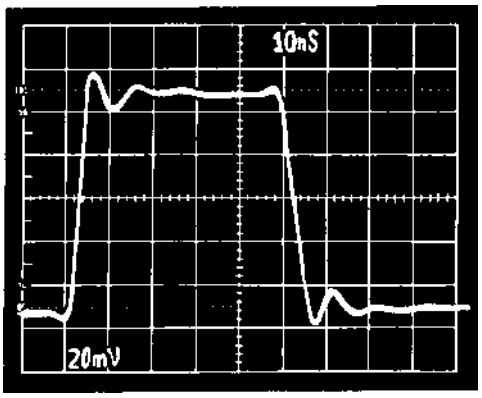


Figure 14. Small Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation, C_{COMP} = 4 pF, R_F = 1 kΩ, R1 = 1 kΩ

Figure 13 is an oscilloscope photo of the pulse response of a unity gain inverter that has been configured to provide a small signal bandwidth of 53 MHz and a subsequent slew rate of 180 V/μs; resistor R_F = 3 kΩ and capacitor C_{COMP} = 1 pF. Figure 14 shows the excellent pulse response as a unity gain inverter, this using component values of R_F = 1 kΩ and C_{COMP} = 4 pF.

Figures 15 and 16 show the closed-loop frequency response of the AD829 for different closed-loop gains and different supply voltages.

If a noninverting amplifier configuration using current feedback compensation is needed, the circuit of Figure 17 is recommended. This circuit provides a slew rate twice that of the shunt compensated noninverting amplifier of Figure 18 at the expense of gain flatness. Nonetheless, this circuit delivers 95 MHz bandwidth with ±1 dB flatness into a back terminated cable, with a differential gain error of only 0.01% and a differential phase error of only 0.015° at 4.43 MHz.

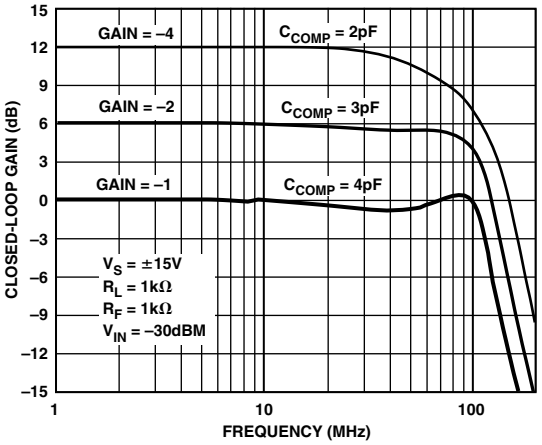


Figure 15. Closed-Loop Frequency Response for the Inverting Amplifier Using Current Feedback Compensation

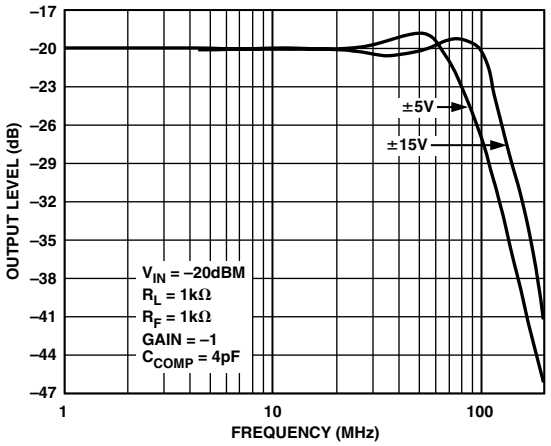


Figure 16. Closed-Loop Frequency Response vs. Supply for the Inverting Amplifier Using Current Feedback Compensation

A Low Error Video Line Driver

The buffer circuit shown in Figure 18 will drive a back-terminated 75 Ω video line to standard video levels (1 V p-p) with 0.1 dB gain flatness to 30 MHz with only 0.04° and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high definition video displays and test equipment, is achieved using only 5 mA quiescent current.

A High Gain, Video Bandwidth, Three Op Amp In Amp

Figure 19 shows a three op amp instrumentation amplifier circuit that provides a gain of 100 at video bandwidths. At a circuit gain of 100, the small signal bandwidth equals 18 MHz into a FET probe. Small signal bandwidth equals 6.6 MHz with a 50 Ω load. The 0.1% settling time is 300 ns.

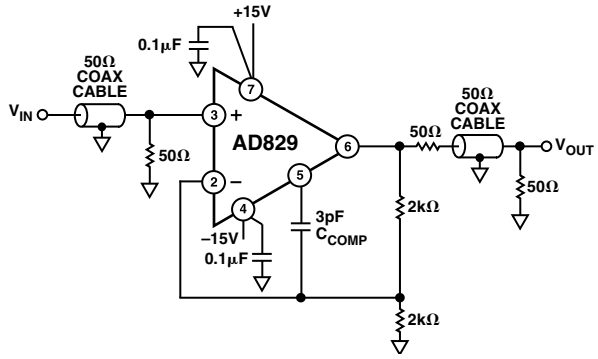


Figure 17. Noninverting Amplifier Connection Using Current Feedback Compensation

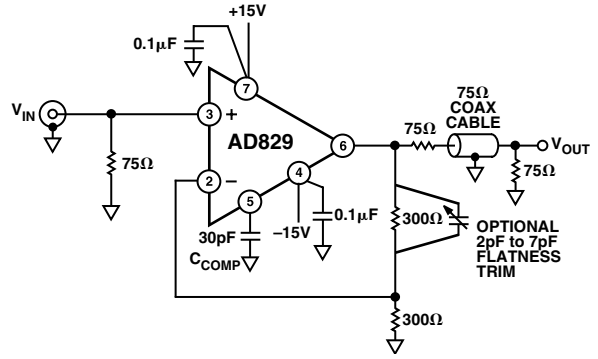
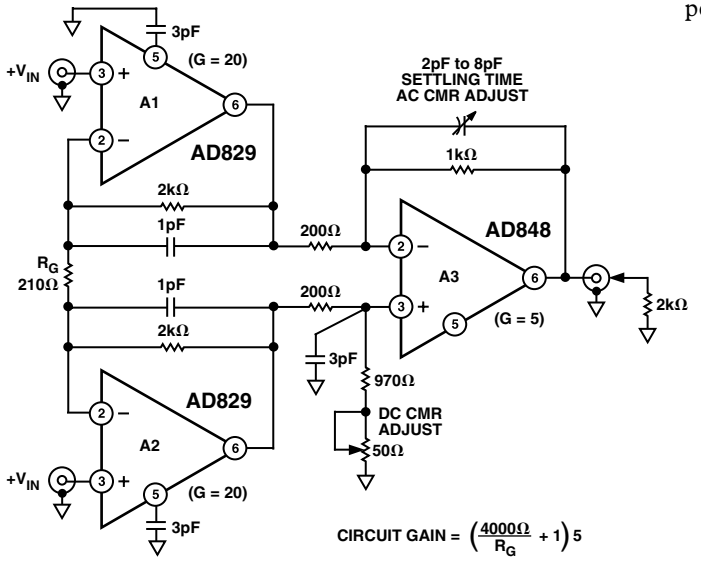


Figure 18. A Video Line Driver with a Flatness over Frequency Adjustment

The input amplifiers operate at a gain of 20, while the output op amp runs at a gain of 5. In this circuit, the main bandwidth limitation is the gain/bandwidth product of the output amplifier. Extra care should be taken while breadboarding this circuit, since even a couple of extra picofarads of stray capacitance at the compensation pins of A1 and A2 will degrade circuit bandwidth.



INPUT FREQUENCY	CMRR
100 Hz	64.6dB
1 MHz	44.7dB
10 MHz	23.9dB

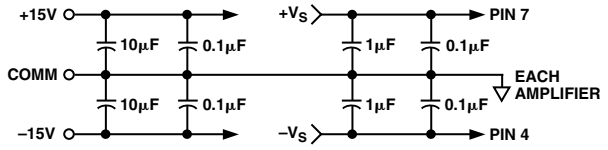
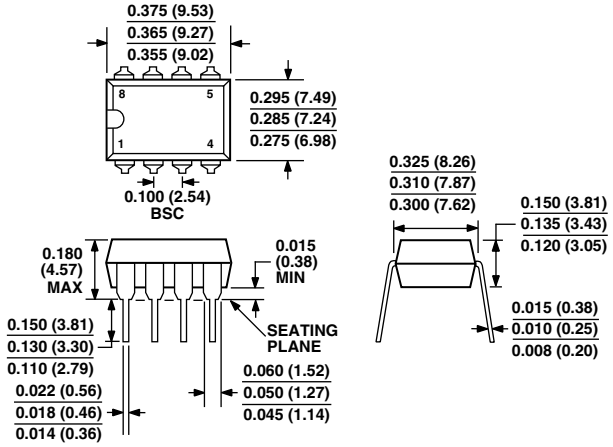


Figure 19. A High Gain, Video Bandwidth, Three Op Amp In Amp Circuit

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)

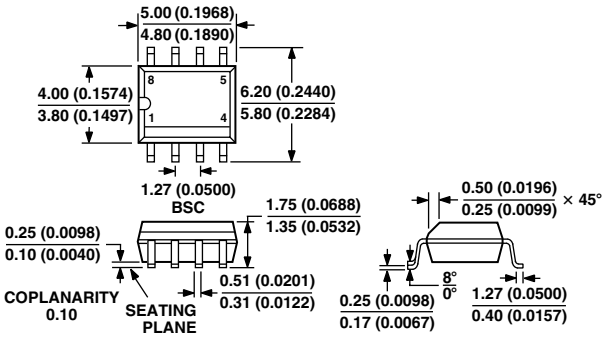
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

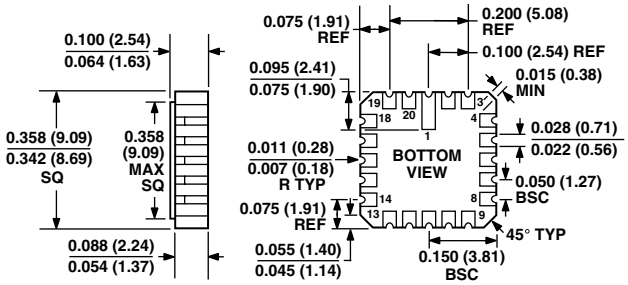
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

20-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-20A)

Dimensions shown in inches and (millimeters)



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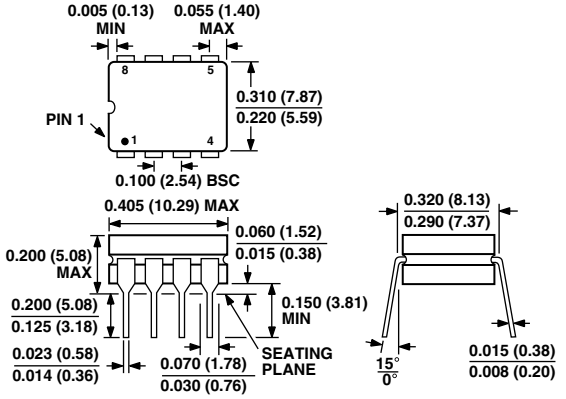
8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)

Dimensions shown in inches and (millimeters)



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Revision History

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Added new Figure 1 and renumbered all figures	4
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Updated Table I	11
Updated Figure 15	12
Updated Figure 16	13
Updated OUTLINE DIMENSIONS	14
2/03—Data Sheet changed from REV. E to REV. F.	
Renumbered Figures	Universal
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Changes made to SPECIFICATIONS	2
Changes made to ABSOLUTE MAXIMUM RATINGS	4
Changes made to ORDERING GUIDE	4
Updated OUTLINE DIMENSIONS	13