High Temperature, Low Power Operational Amplifier

Data Sheet **AD8634**

FEATURES

- **Extreme high temperature operation**
  - **−40°C to +210°C, FLATPACK package**
  - **−40°C to +175°C, SOIC package**
- **Rail-to-rail output**
- **Low power: 1.3 mA maximum**
- **Gain bandwidth product: 9.7 MHz typical at A_V = 100**
- **Low offset voltage: 250 µV maximum**
- **Unity-gain stable**
- **High slew rate: 5.0 V/µs typical at 210°C**
- **Low noise: 4.2 nV/√Hz typical at 1 kHz and 210°C**

APPLICATIONS

- **Downhole drilling and instrumentation**
- **Avionics**
- **Heavy industrial**
- **High temperature environments**

PIN CONFIGURATION

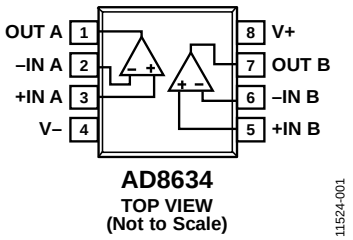

Figure 1. SOIC and FLATPACK Pinout

GENERAL DESCRIPTION

The AD8634 is a precision, 9.7 MHz bandwidth, dual amplifier that features rail-to-rail outputs. The AD8634 is guaranteed to operate from 3 V to 30 V (or from ±1.5 V to ±15 V) and at very high temperatures.

The AD8634 is well suited for applications that require both ac and dc precision performance. The combination of wide bandwidth, low noise, and precision makes the AD8634 useful in a wide variety of applications, including filters and interfacing with a variety of sensors.

This dual-channel op amp is offered in an 8-lead SOIC package with an operating temperature range of −40°C to +175°C. It is also available in an 8-lead ceramic flat package (FLATPACK) with an operating temperature range of −40°C to +210°C. Both packages are designed for robustness at extreme temperatures and are qualified for up to 1000 hours of operation at the maximum temperature rating.

The AD8634 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.

Rev. 0 **Document Feedback**

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Tel: 781.329.4700 **Technical Support** **www.analog.com**

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REVISION HISTORY

7/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, V_{SY} = ±15.0 V

V_{SY} = ±15.0 V, V_{CM} = 0 V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/ Comments	SOIC Package −40°C ≤ T_A ≤ +175°C			FLATPACK Package −40°C ≤ T_A ≤ +210°C			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}				250			250	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.35			0.35		µV/°C
Offset Voltage Matching		$T_A = T_{MAX}$			150			150	µV
Input Bias Current	I_B		−200	−45	+200	−200	−40	+200	nA
Input Offset Current	I_{OS}				30			30	nA
Input Voltage Range	V_{IN}		−14.7		+14.7	−14.5		+14.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −14.0 V to +14.0 V	105	120		100	115		dB
Large Signal Voltage Gain	A_{VO}	−13.5 V ≤ V_{OUT} ≤ +13.5 V, R_L = 2 kΩ	104	112		100	108		dB
Input Impedance									
Differential				53||1.1			53||1.1		kΩ||pF
Common-Mode				1.1||2.5			1.1||2.5		GΩ||pF
OUTPUT CHARACTERISTICS									
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	14.8	14.90		14.8	14.90		V
		R_L = 2 kΩ to V_{CM}	14.0	14.5		14.0	14.5		V
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$	14.60	14.75		14.60	14.75		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−14.95	−14.8		−14.95	−14.8	V
		R_L = 2 kΩ to V_{CM}		−14.8	−14.70		−14.75	−14.65	V
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$			−14.70			−14.65	V
Short-Circuit Current	I_{SC}	V_{OUT} = 0 V, $T_A = T_{MAX}$		+100/−20			+105/−18		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_{SY} = ±2 V to ±18 V	105	115		103	113		dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA, $T_A = T_{MAX}$		1.0	1.2		1.1	1.3	mA
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ	3.6	4.9		3.6	5.0		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		9.7			9.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		2.5			2.5		MHz
−3 dB Closed-Loop Bandwidth	−3dB	V_{IN} = 5 mV p-p, A_V = 1		4.9			4.9		MHz
Phase Margin	ΦM			84			82		Degrees
NOISE PERFORMANCE									
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.13			0.13		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		4.2			4.2		nV/√Hz
Current Noise Density	i_n			0.6			0.6		pA/√Hz

ELECTRICAL CHARACTERISTICS, V_{SY} = 3.0 V

V_{SY} = 3.0 V, V_{CM} = 1.5 V, V_{OUT} = 1.5 V, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/ Comments	SOIC Package −40°C ≤ T_A ≤ +175°C			FLATPACK Package −40°C ≤ T_A ≤ +210°C			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}				250			250	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.35			0.35		µV/°C
Offset Voltage Matching		$T_A = T_{MAX}$			150			150	µV
Input Bias Current	I_B		−200	−45	+200	−200	−40	+200	nA
Input Offset Current	I_{OS}				30			30	nA
Input Voltage Range	V_{IN}		0.3		2.7	0.5		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0.3 V to 2.7 V	60	65		55	60		dB
Large Signal Voltage Gain	A_{VO}	0.5 V ≤ V_{OUT} ≤ 2.5 V, R_L = 2 kΩ	104	112		100	108		dB
Input Impedance									
Differential				53||1.1			53||1.1		kΩ||pF
Common-Mode				2.8||2.5			2.8||2.5		GΩ||pF
OUTPUT CHARACTERISTICS									
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	2.8	2.90		2.8	2.90		V
		R_L = 2 kΩ to V_{CM}	2.0	2.5		2.0	2.5		V
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$	2.60	2.75		2.60	2.75		V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		50	200		50	200	mV
		R_L = 2 kΩ to V_{CM}		200	300		250	350	mV
		R_L = 2 kΩ to V_{CM}, $T_A = T_{MAX}$			300			350	mV
Short-Circuit Current	I_{SC}	V_{OUT} = 0 V, $T_A = T_{MAX}$		+65/−13			+70/−11		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_{SY} = ±1.25 V to ±1.75 V	97	102		95	100		dB
Supply Current per Amplifier	I_{SY}	I_{OUT} = 0 mA, $T_A = T_{MAX}$		0.9	1.1		1.0	1.2	mA
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ	3.5	4.9		3.5	5.0		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		9.7			9.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		2.5			2.5		MHz
−3 dB Closed-Loop Bandwidth	−3dB	V_{IN} = 5 mV p-p, A_V = 1		4.9			4.9		MHz
Phase Margin	ΦM			84			82		Degrees
NOISE PERFORMANCE									
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.13			0.13		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		4.2			4.2		nV/√Hz
Current Noise Density	i_n			0.6			0.6		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$V- \le V_{IN} \le V+$
Differential Input Voltage[1]	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
SOIC Package	−40°C to +175°C
FLATPACK Package	−40°C to +210°C
Junction Temperature	
SOIC Package	200°C
FLATPACK Package	245°C
Lead Temperature (Soldering 60 sec)	300°C

[1] For differential input voltages greater than 0.6 V, limit the input current to less than 5 mA to prevent degradation or destruction of the input devices (see the Input Protection section).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PREDICTED LIFETIME vs. OPERATING TEMPERATURE

Comprehensive reliability testing is performed on all Analog Devices high temperature products, including the AD8634. Product lifetimes at extended operating temperature are obtained using high temperature operating life (HTOL). Lifetimes are predicted from the Arrhenius equation, taking into account assumptions about potential design and manufacturing failure mechanisms. HTOL is performed in accordance with JEDEC JESD22-A108. A minimum of three wafer fab and assembly lots are processed through HTOL at the maximum operating temperature.

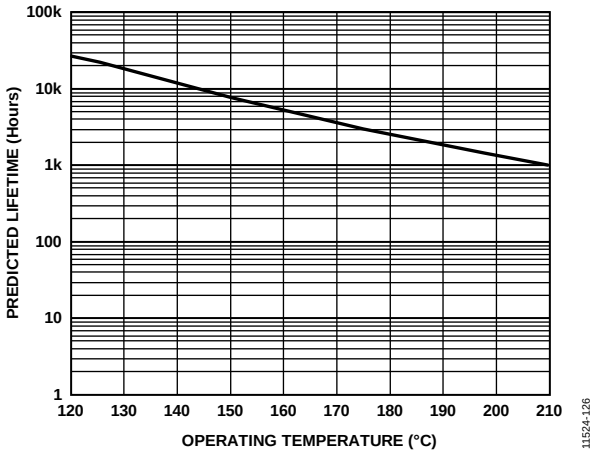

Figure 2. Predicted Lifetime vs. Operating Temperature

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered on a 4-layer JEDEC standard printed circuit board (PCB) with zero airflow.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N	121	43	°C/W
8-Lead FLATPACK	100	15	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

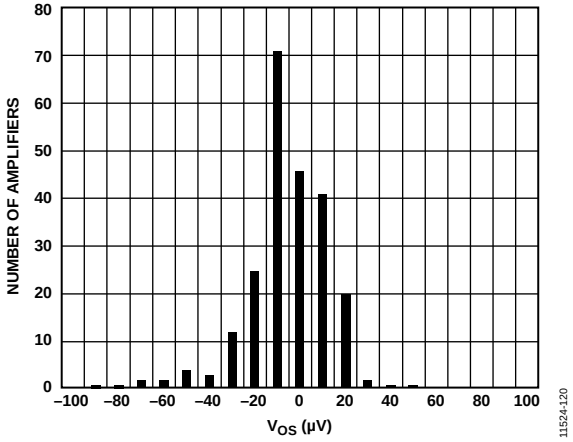

Figure 3. Offset Voltage Distribution, SOIC Package, V_{SY} = ±15.0 V, T_A = 175°C

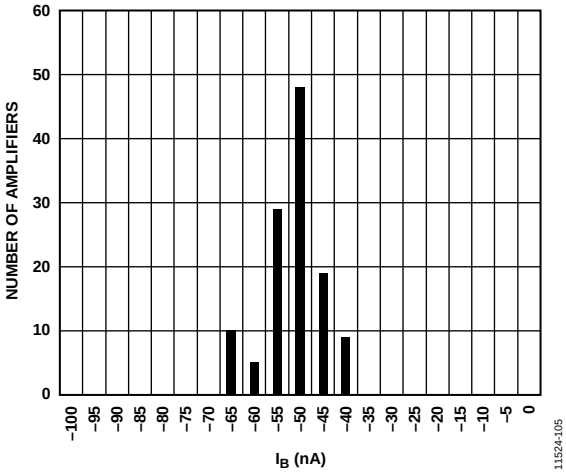

Figure 6. Input Bias Current Distribution, SOIC Package, V_{SY} = ±15.0 V, T_A = 175°C

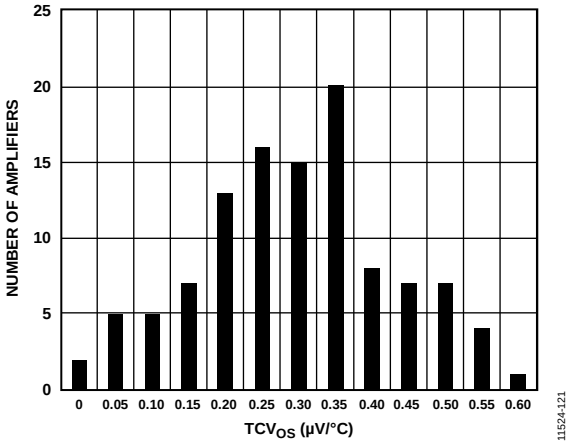

Figure 4. TCV_{OS} Distribution, SOIC Package, V_{SY} = ±15.0 V

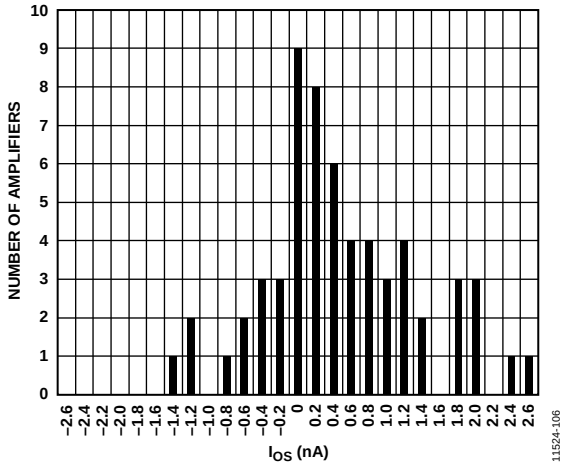

Figure 7. Input Offset Current Distribution, SOIC Package, V_{SY} = ±15.0 V, T_A = 175°C

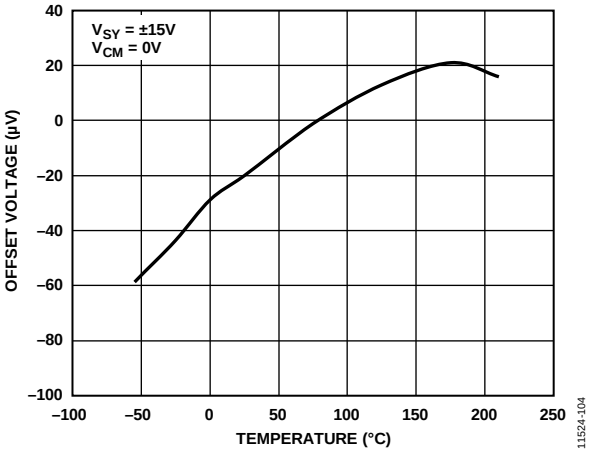

Figure 5. Typical Offset Voltage vs. Temperature

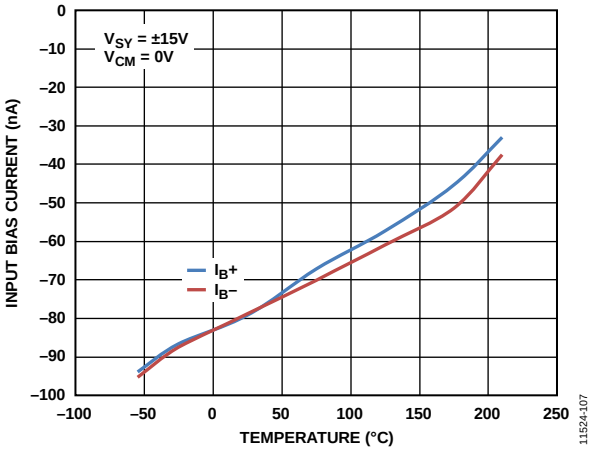

Figure 8. Typical Input Bias Current vs. Temperature

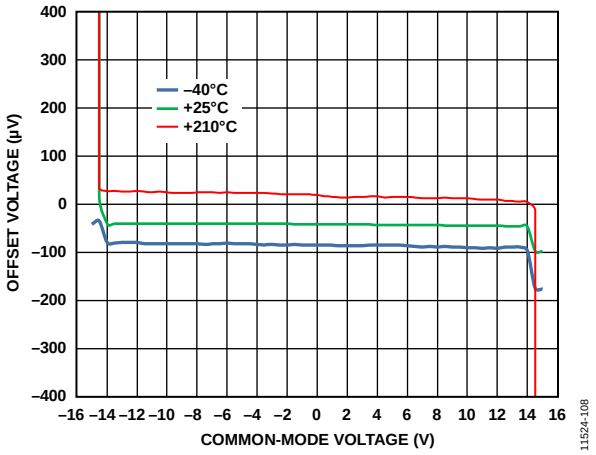

Figure 9. Offset Voltage vs. Common-Mode Voltage and Temperature, V_{SY} = ±15.0 V

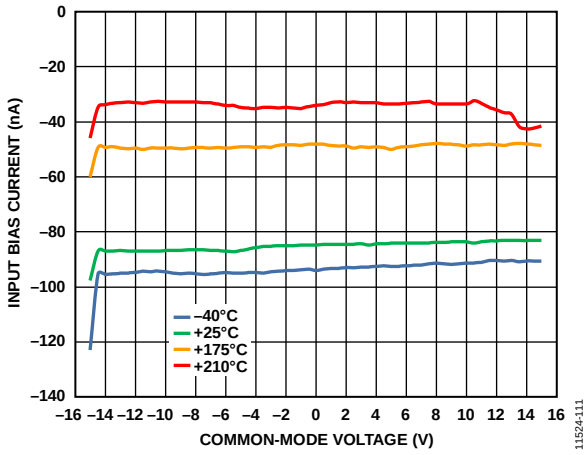

Figure 12. Input Bias Current vs. Common-Mode Voltage and Temperature, V_{SY} = ±15.0 V

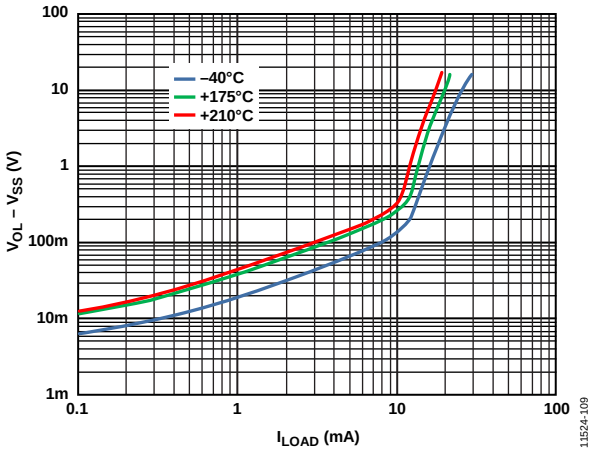

Figure 10. Negative Dropout Voltage vs. Load Current and Temperature

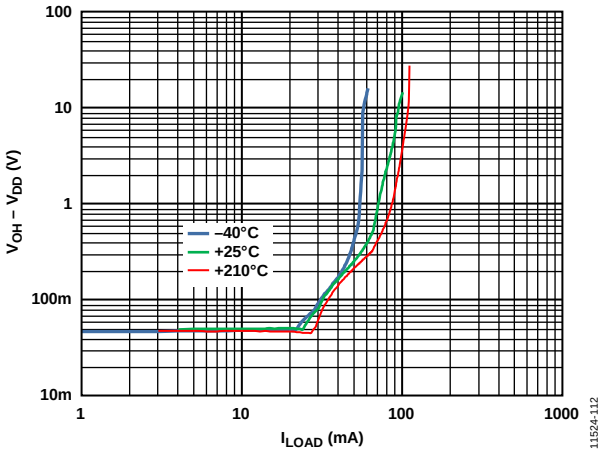

Figure 13. Positive Dropout Voltage vs. Load Current and Temperature

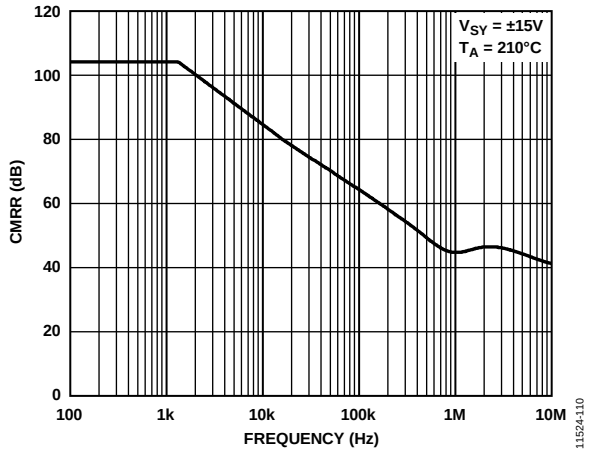

Figure 11. CMRR vs. Frequency, T_A = 210°C

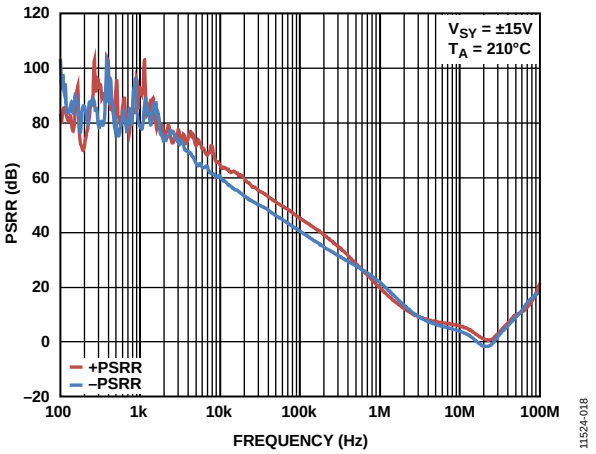

Figure 14. PSRR vs. Frequency

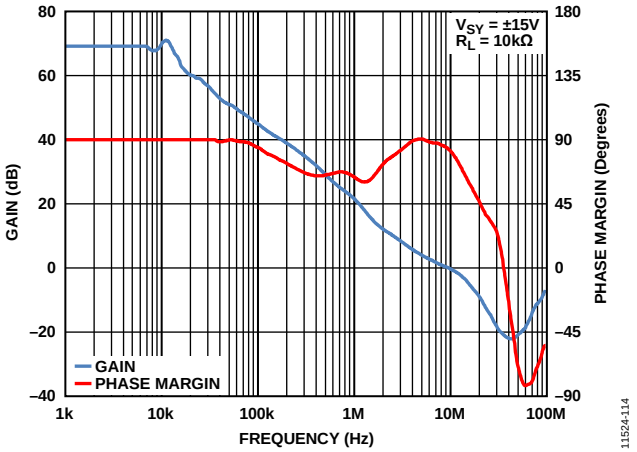

Figure 15. Gain and Phase Margin vs. Frequency, T_A = 210°C

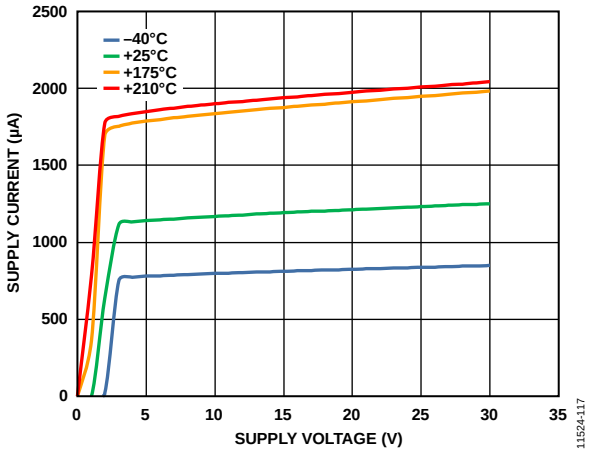

Figure 18. Supply Current vs. Supply Voltage and Temperature

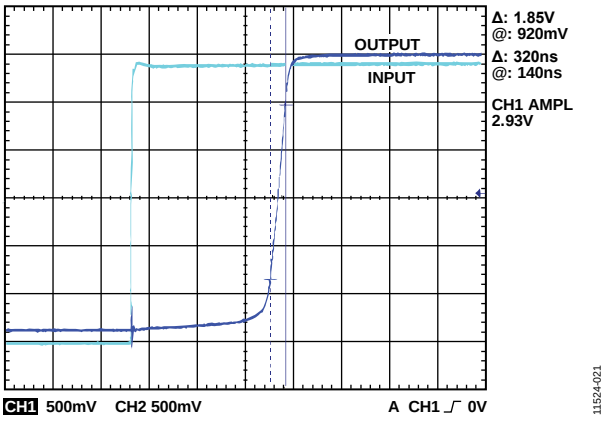

Figure 16. Large Signal Positive Edge Response, V_{SY} = ±15.0 V, T_A = 175°C

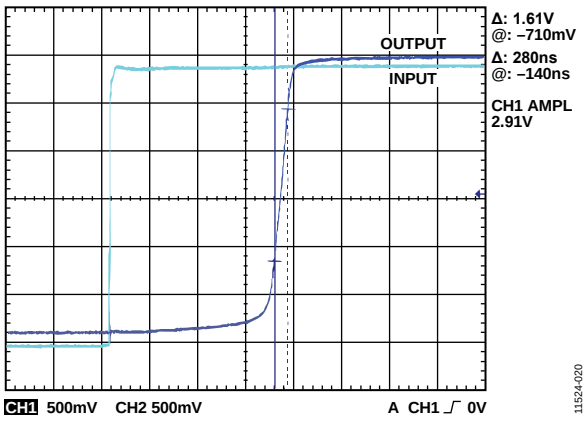

Figure 19. Large Signal Positive Edge Response, V_{SY} = ±15.0 V, T_A = 210°C

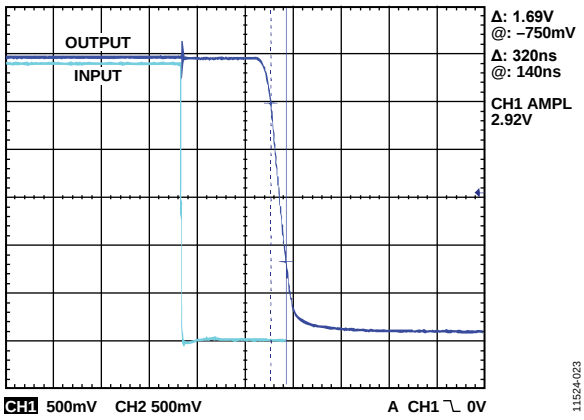

Figure 17. Large Signal Negative Edge Response, V_{SY} = ±15.0 V, T_A = 175°C

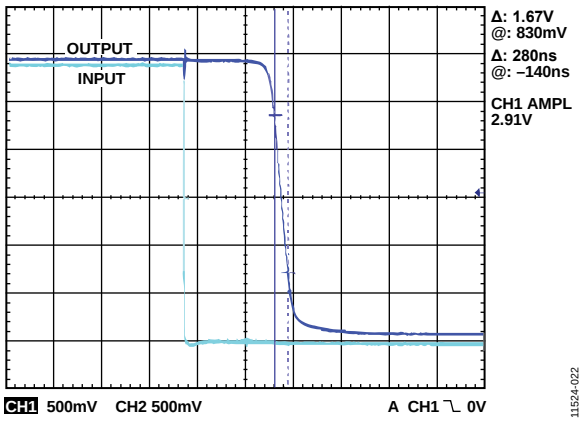

Figure 20. Large Signal Negative Edge Response, V_{SY} = ±15.0 V, T_A = 210°C

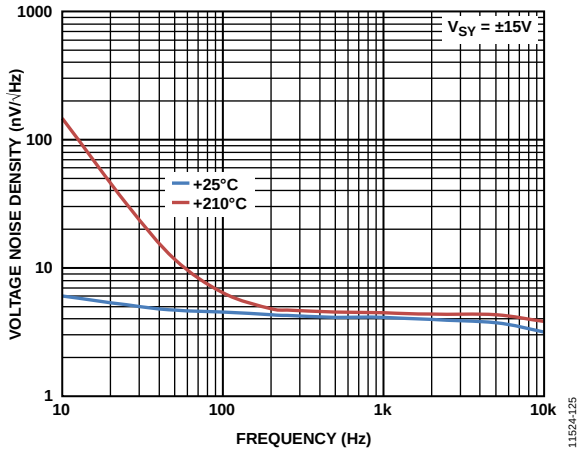

Figure 21. Voltage Noise Density vs. Frequency

APPLICATIONS INFORMATION

Figure 23 illustrates a typical application circuit that uses the AD8634 and other Analog Devices high temperature products.

INPUT PROTECTION

As with any semiconductor device, if the input voltages applied to the AD8634 exceed either supply voltage, the input overvoltage I-to-V characteristic of the device must be considered. When an overvoltage condition occurs, the amplifier can be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current.

The protection diodes between the input and supply pins conduct when the input common-mode voltage exceeds either supply pin by a diode drop. This diode drop varies with temperature and is in the range of 0.3 V to 0.8 V. The AD8634 has no internal current-limiting resistors; therefore, fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, provided that it is limited to 5 mA or less. If a fault condition causes more than 5 mA to flow, an external series resistor should be added at the expense of additional thermal noise.

Figure 22 illustrates a typical noninverting configuration for an overvoltage-protected amplifier where the series resistance, R_S, is chosen such that

$$R_S = (V_{IN\,(MAX)} - V_{SUPPLY})/5\text{ mA}$$

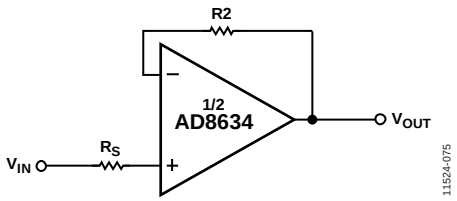

Figure 22. Resistance in Series with Inputs Limits Overvoltage Currents to Safe Values

For example, a 1 kΩ resistor protects the AD8634 against input signals up to 5 V above and below the supplies. Note that the thermal noise of a 1 kΩ resistor at room temperature is 4 nV/√Hz, which is close to the voltage noise of the AD8634.

For configurations where both inputs are used, add a series resistor at each input to protect the inputs against damage. To ensure optimum dc and ac performance, it is recommended that source impedance levels be balanced.

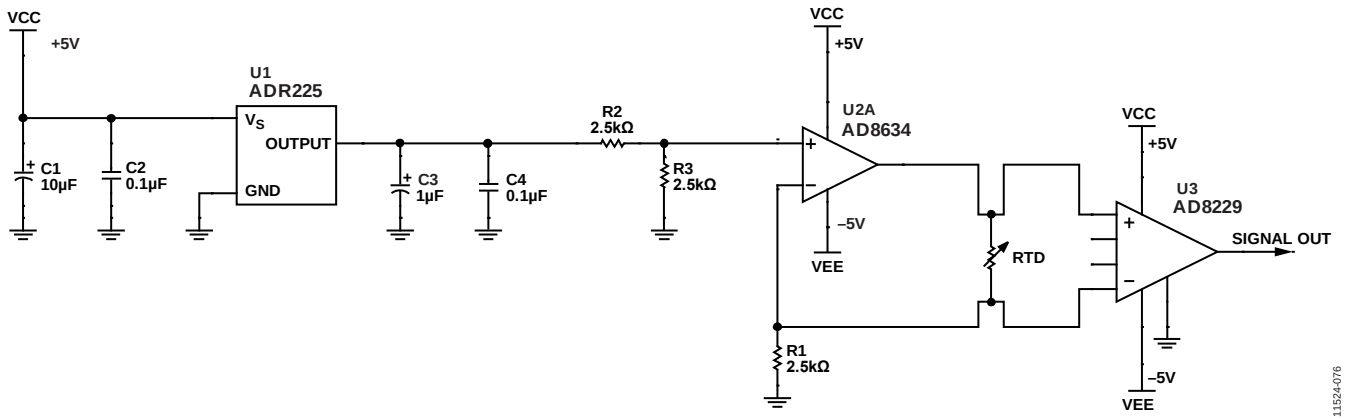

Figure 23. Typical High Temperature RTD Signal Conditioning Circuit

OUTLINE DIMENSIONS

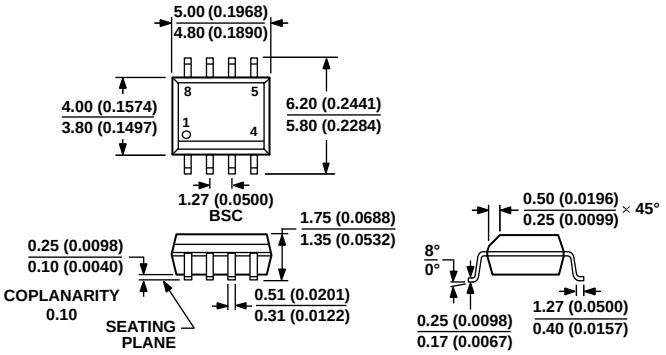

Figure 24. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

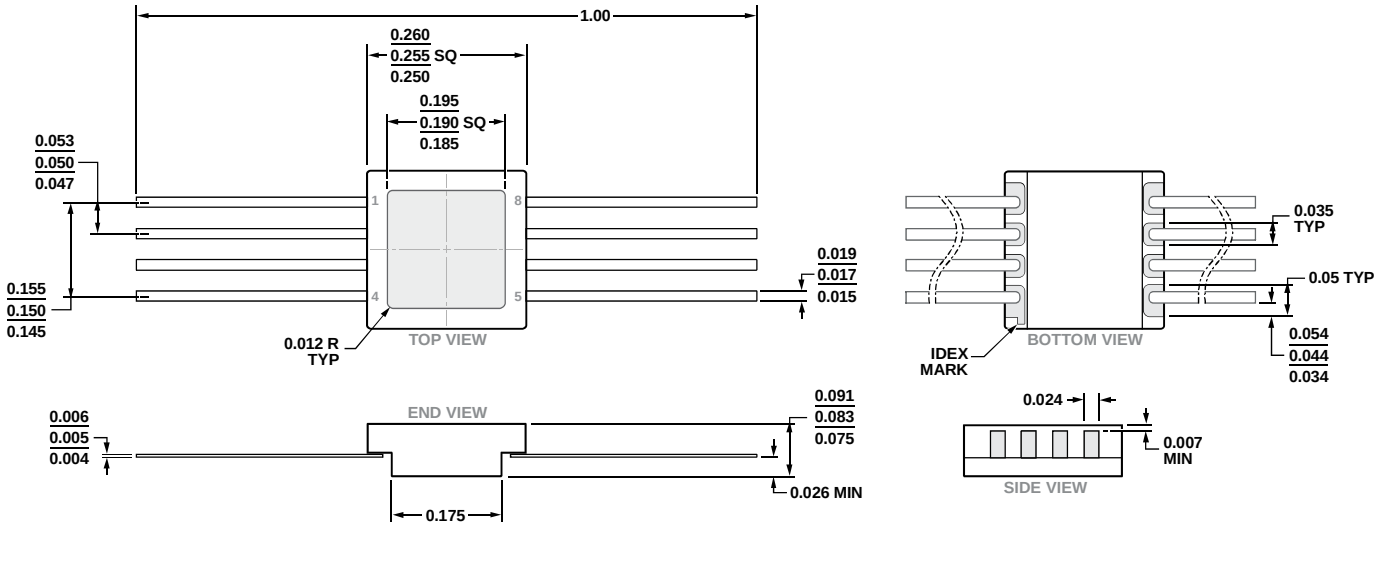

Figure 25. 8-Lead Ceramic Flat Package [FLATPACK]
(F-8-2)
Dimensions shown in inches

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD8634HRZN	−40°C to +175°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8634HFZ	−40°C to +210°C	8-Lead Ceramic Flat Package [FLATPACK]	F-8-2

[1] Z = RoHS Compliant Part.
[2] The FLATPACK is prerelease only.

NOTES

D11524-0-7/13(0)