

FEATURES

JESD204B (Subclass 1) coded serial digital outputs

Lane rates up to 15 Gbps

1.74 W total power at 1 GSPS

435 mW per ADC channel

SFDR = TBD dBFS at 305 MHz (1.80 V p-p input range)

SNR = TBD dBFS at 305 MHz (1.80 V p-p input range)

Noise density = -151.5 dBFS/Hz (1.80 V p-p input range)

0.975 V, 1.8 V, and 2.5 V dc supply operation

No missing codes

Internal ADC voltage reference

Analog input buffer

On-chip dithering to improve small signal linearity

Flexible differential input range

1.44 V p-p to 2.16 V p-p (1.80 V p-p nominal)

1.4 GHz analog input full power bandwidth

Amplitude detect bits for efficient AGC implementation

4 integrated wideband digital processors

48-bit NCO, up to 4 cascaded half-band filters

Differential clock input

Integer clock divide by 1, 2, 4, or 8

On-chip temperature diode

Flexible JESD204B lane configurations

APPLICATIONS

LIDAR

Communications

DSO

Ultrawideband satellite receivers

Instrumentation

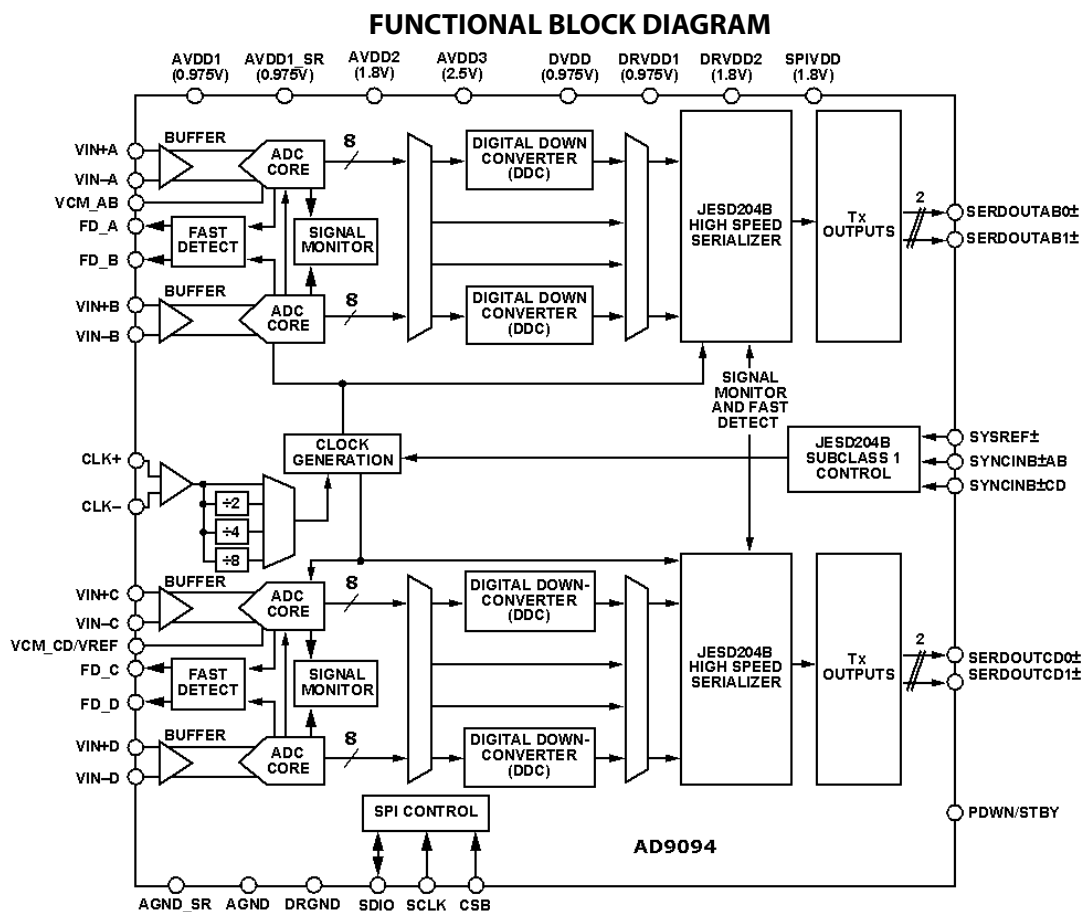


Figure 1.

Rev. PrC

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GENERAL DESCRIPTION

The AD9094 is a quad, 8-bit, 1 GSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This device is designed for sampling wide bandwidth analog signals of up to 1.4 GHz. The AD9094 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The quad ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The analog inputs and clock signals are differential inputs. Each pair of ADC data outputs is internally connected to two DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 48-bit frequency translator, NCO, and up to four half-band decimation filters.

In addition to the DDC blocks, the AD9094 has several functions that simplify the automatic gain control (AGC) function in the communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

Users can configure each pair of intermediate frequency (IF) receiver outputs onto either one or two lanes of Subclass 1 JESD204B-based high speed serialized outputs, depending on the decimation ratio and the acceptable lane rate of the receiving logic device. Multiple device synchronization is supported through the SYSREF \pm , SYNCINB \pm AB, and SYNCINB \pm CD input pins.

The AD9094 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using the 1.8 V capable, 3-wire SPI.

The AD9094 is available in a Pb-free, 72-lead LFCSP and is specified over the -40°C to $+105^{\circ}\text{C}$ junction temperature range. This product may be protected by one or more U.S. or international patents.

PRODUCT HIGHLIGHTS

1. Low power consumption per channel.
2. JESD204B lane rate support up to 15 Gbps.
3. Wide full power bandwidth supports IF sampling of signals up to 1.4 GHz.
4. Buffered inputs ease filter design and implementation.
5. Four integrated wideband decimation filters and numerically controlled oscillator (NCO) blocks supporting multiband receivers.
6. Programmable fast overrange detection.
7. On-chip temperature diode for system thermal management.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, $A_{IN} = -1.0$ dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of -40°C to $+105^{\circ}\text{C}$. Typical specifications represent performance at $T_J = 50^{\circ}\text{C}$ ($T_A = 25^{\circ}\text{C}$).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error		0		% FSR
Offset Matching		0		% FSR
Gain Error	TBD		TBD	% FSR
Gain Matching		TBD	TBD	% FSR
Differential Nonlinearity (DNL)	TBD	TBD	TBD	LSB
Integral Nonlinearity (INL)	TBD	TBD	TBD	LSB
TEMPERATURE DRIFT				
Offset Error		TBD		ppm/ $^{\circ}\text{C}$
Gain Error		TBD		ppm/ $^{\circ}\text{C}$
INTERNAL VOLTAGE REFERENCE		0.5		V
INPUT REFERRED NOISE		2.6		LSB rms
ANALOG INPUTS				
Differential Input Voltage Range (Programmable)	1.44	1.80	2.16	V p-p
Common-Mode Voltage (V_{CM})		1.34		V
Differential Input Capacitance ¹		1.75		pF
Differential Input Resistance		200		Ω
Analog Input Full Power Bandwidth		1.4		GHz
POWER SUPPLY				
AVDD1	0.95	0.975	1.00	V
AVDD1_SR	0.95	0.975	1.00	V
AVDD2	1.71	1.8	1.89	V
AVDD3	2.44	2.5	2.56	V
DVDD	0.95	0.975	1.00	V
DRVDD1	0.95	0.975	1.00	V
DRVDD2	1.71	1.8	1.89	V
SPIVDD	1.71	1.8	1.89	V
I_{AVDD1}		470	TBD	mA
I_{AVDD1_SR}		20	TBD	mA
I_{AVDD2}		453	TBD	mA
I_{AVDD3}		40	TBD	mA
I_{DVDD}^2		201	TBD	mA
I_{DRVDD1}^1		112	TBD	mA
I_{DRVDD2}^1		25	TBD	mA
I_{SPIVDD}		<1	TBD	mA
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers) ²		1.74	TBD	W
Power-Down Dissipation		TBD		mW
Standby ³		TBD		W

¹ All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.

² Full bandwidth mode.

³ Standby mode is controlled by the SPI.

DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.8 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, 500 MSPS, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, $A_{IN} = -1.0$ dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of -40°C to $+105^{\circ}\text{C}$. Typical specifications represent performance at $T_J = 50^{\circ}\text{C}$ ($T_A = 25^{\circ}\text{C}$).

Table 2.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK-)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	600	800	1600	mV p-p
Input Common-Mode Voltage		0.69		V
Input Resistance (Differential)		32		k Ω
Input Capacitance			0.9	pF
SYSTEM REFERENCE (SYSREF) INPUTS (SYSREF+, SYSREF-) ¹				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		k Ω
Input Capacitance (Single-Ended per Pin)		0.7		pF
LOGIC INPUTS (PDWN/STBY)				
Logic Compliance		CMOS		
Logic 1 Voltage	$0.65 \times \text{SPIVDD}$			V
Logic 0 Voltage	0		$0.35 \times \text{SPIVDD}$	V
Input Resistance		10		M Ω
LOGIC INPUTS (SDIO, SCLK, CSB)				
Logic Compliance		CMOS		
Logic 1 Voltage	$0.65 \times \text{SPIVDD}$			V
Logic 0 Voltage	0		$0.35 \times \text{SPIVDD}$	V
Input Resistance		56		k Ω
LOGIC OUTPUT (SDIO)				
Logic Compliance		CMOS		
Logic 1 Voltage ($I_{OH} = 800 \mu\text{A}$)	$\text{SPIVDD} - 0.45 \text{ V}$			V
Logic 0 Voltage ($I_{OL} = 50 \mu\text{A}$)	0		0.45	V
SYNCIN INPUT (SYNCINB+AB/SYNCINB-AB/ SYNCINB+CD/SYNCINB-CD)				
Logic Compliance		LVDS/LVPECL/CMOS		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage	0.6	0.69	2.2	V
Input Resistance (Differential)	18	22		k Ω
Input Capacitance (Single Ended per Pin)		0.7		pF
LOGIC OUTPUTS (FD_A, FD_B, FD_C, FD_D)				
Logic Compliance		CMOS		
Logic 1 Voltage	$0.8 \times \text{SPIVDD}$			V
Logic 0 Voltage	0		0.5	V
Input Resistance		56		k Ω
DIGITAL OUTPUTS (SERDOUTABx \pm /SERDOUTCDx \pm , x = 0 OR 1)				
Logic Compliance		CML		
Differential Output Voltage		455.8		mV p-p
Short-Circuit Current ($I_{D\text{ SHORT}}$)		15		mA
Differential Termination Impedance		100		Ω

¹ DC-coupled input only.

TIMING SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS	See Figure 3				
t_{SU_SR}	Device clock to SYSREF+ setup time		-44.8		ps
t_{H_SR}	Device clock to SYSREF+ hold time		64.4		ps
SPI TIMING REQUIREMENTS	See Figure 4				
t_{DS}	Setup time between the data and the rising edge of SCLK	4			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the CSB rising edge (not shown in Figure 4)	10			ns

Timing Diagrams

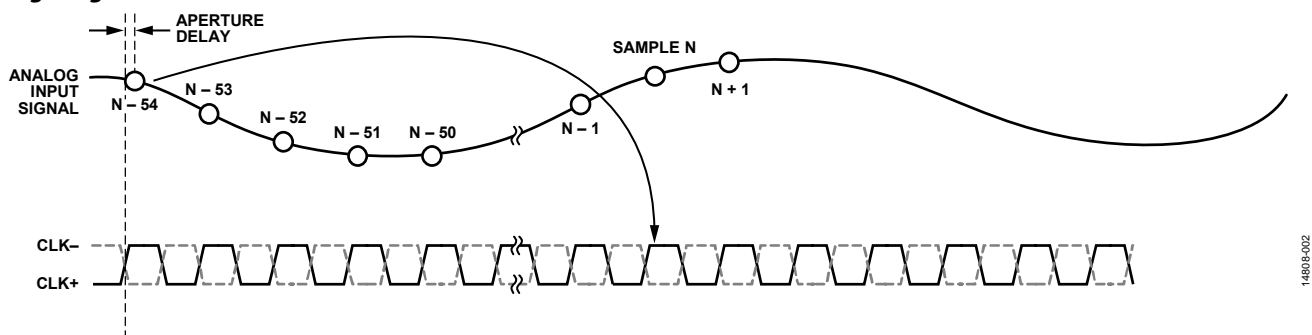
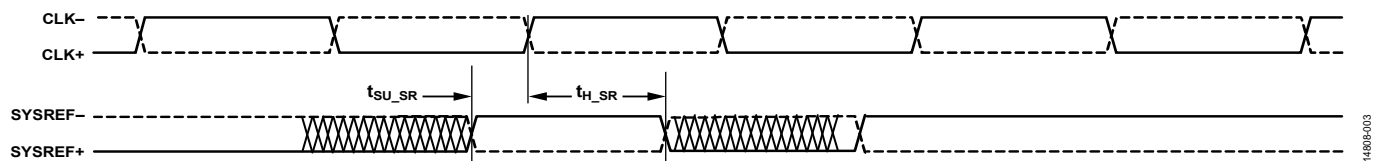
Figure 2. Data Output Timing (Full Bandwidth Mode; $L = 4, M = 2, F = 1$)

Figure 3. SYSREF± Setup and Hold Timing

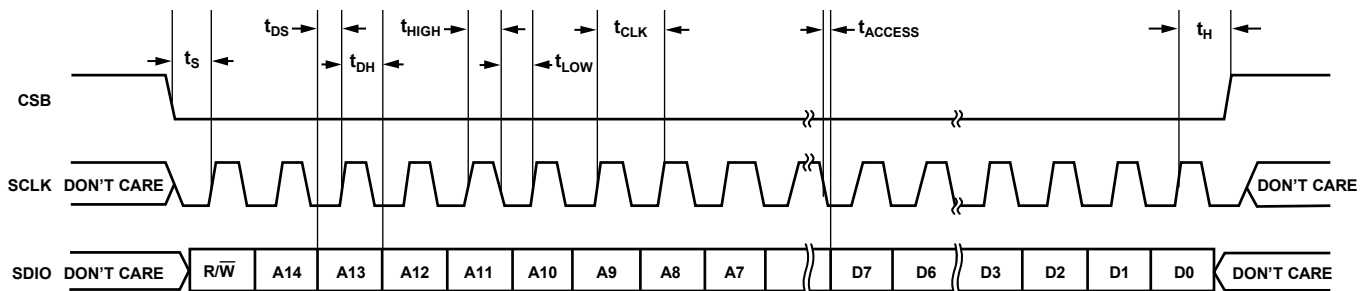


Figure 4. Serial Port Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.00 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.00 V
SPIVDD to AGND	2.00 V
VIN±x to AGND	−0.3 V to AVDD3 + 0.3 V
CLK± to AGND	−0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	−0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	−0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND_SR	0 V to 2.5 V
SYNCINB±AB/SYNCINB±CD to DRGND	0 V to 2.5 V
Environmental	
Operating Junction Temperature Range	−40°C to +105°C
Maximum Junction Temperature	125°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC_BOT} is the bottom junction to case thermal resistance.

Table 5. Thermal Resistance

PCB Type	Airflow Velocity (m/sec)	θ_{JA}	θ_{JC_BOT}	Unit
JEDEC 2s2p Board	0.0	21.58 ^{1,2}	1.95 ^{1,4}	°C/W
	1.0	17.94 ^{1,2}	N/A ³	°C/W
	2.5	16.58 ^{1,2}	N/A ³	°C/W
10-Layer Board	0.0	9.74	1.00	°C/W

¹ Per JEDEC 51-7, plus JEDEC 51-5 2s2p test board.

² Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

³ N/A means not applicable.

⁴ Per MIL-STD 883, Method 1012.1.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

The diagram shows the top view of the AD9094 chip, a square integrated circuit with a central rectangular area labeled "AD9094" and "TOP VIEW (Not to Scale)". The chip has a large circular feature on the left side. Pin connections are listed around the perimeter of the chip, numbered 1 through 55. The pins are arranged in a square grid pattern, with pins 1 through 16 on the left, 17 through 37 on the right, 38 through 55 on the bottom, and 56 through 72 on the top. The pin names are listed next to their corresponding numbers.

Pin Connections:

- Pin 1:** AVDD3
- Pin 2:** VIN-A
- Pin 3:** VIN+A
- Pin 4:** AVDD2
- Pin 5:** AVDD2
- Pin 6:** AVDD3
- Pin 7:** VIN+B
- Pin 8:** VIN-B
- Pin 9:** AVDD2
- Pin 10:** AVDD1
- Pin 11:** AVDD1
- Pin 12:** VCM_AB
- Pin 13:** DVDD
- Pin 14:** DGND
- Pin 15:** DRVDD2
- Pin 16:** PDWN/STBY
- Pin 17:** FD_A
- Pin 18:** FD_B
- Pin 19:** SYNCINB-AB
- Pin 20:** SYNCINB-AB
- Pin 21:** DRGND
- Pin 22:** DRVDD1
- Pin 23:** SERROUTAB0-
- Pin 24:** SERROUTAB0+
- Pin 25:** SERROUTAB1-
- Pin 26:** SERROUTAB1+
- Pin 27:** SERROUTC01-
- Pin 28:** SERROUTC01+
- Pin 29:** SERROUTC00-
- Pin 30:** SERROUTC00+
- Pin 31:** DRVDD1
- Pin 32:** DRGND
- Pin 33:** SYNCINB-CD
- Pin 34:** SYNCINB-CD
- Pin 35:** FD_C
- Pin 36:** FD_C
- Pin 37:** SDIO
- Pin 38:** SCLK
- Pin 39:** CSB
- Pin 40:** SPIVDD
- Pin 41:** DGND
- Pin 42:** DVDD
- Pin 43:** VCM_CD/VREF
- Pin 44:** AVDD1
- Pin 45:** AVDD1
- Pin 46:** AVDD2
- Pin 47:** VIN-D
- Pin 48:** VIN+D
- Pin 49:** AVDD3
- Pin 50:** AVDD2
- Pin 51:** AVDD2
- Pin 52:** VIN+C
- Pin 53:** VIN-C
- Pin 54:** AVDD3
- Pin 55:** AVDD2
- Pin 56:** AVDD1
- Pin 57:** AVDD1
- Pin 58:** AVDD1
- Pin 59:** CLK+
- Pin 60:** CLK-
- Pin 61:** AGND
- Pin 62:** AGND
- Pin 63:** AGND
- Pin 64:** AGND
- Pin 65:** SYSREF+
- Pin 66:** SYSREF-
- Pin 67:** AGND
- Pin 68:** AGND
- Pin 69:** AVDD1
- Pin 70:** AVDD1
- Pin 71:** AVDD1
- Pin 72:** AVDD2

1. EXPOSED PAD. ANALOG GROUND. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE GROUND REFERENCE FOR AVDD_x, SPIVDD, DVDD, DRVDD1, AND DRVDD2. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Table 6. Pin Function Descriptions

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Pin No.	Mnemonic	Type	Description
21, 32	DRGND	Ground	Ground Reference for DRVDD1 and DRVDD2.
22, 31	DRVDD1	Supply	Digital Power Supply for SERDOUTABx±/SERDOUTCDx± Pins (0.975 V Nominal).
23, 24	SERDOUTAB0−, SERDOUTAB0+	Output	Lane 0 Output Data Complement/True for Channel A and Channel B.
25, 26	SERDOUTAB1−, SERDOUTAB1+	Output	Lane 1 Output Data Complement/True for Channel A and Channel B.
27, 28	SERDOUTCD1+, SERDOUTCD1−	Output	Lane 1 Output Data True/Complement for Channel C and Channel D.
29, 30	SERDOUTCD0+, SERDOUTCD0−	Output	Lane 0 Output Data True/Complement for Channel C and Channel D.
33	SYNCINB+CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input True for Channel C and Channel D.
34	SYNCINB−CD	Input	Active Low JESD204B LVDS/CMOS/LVPECL Sync Input Complement for Channel C and Channel D.
37	SDIO	Input/output	SPI Serial Data Input/Output.
38	SCLK	Input	SPI Serial Clock.
39	CSB	Input	SPI Chip Select (Active Low).
40	SPIVDD	Supply	Digital Power Supply for SPI (1.8 V Nominal).
43	VCM_CD/VREF	Output/input	Common-Mode Level Bias Output for Analog Input Channel C and Channel D/0.5 V Reference Voltage Input. This pin is configurable through the SPI as an output or an input. Use this pin as the common-mode level bias output if using the internal reference. This pin requires a 0.5 V reference voltage input if using an external voltage reference source.
47, 48	VIN−D, VIN+D	Input	ADC D Analog Input Complement/True.
52, 53	VIN+C, VIN−C	Input	ADC C Analog Input True/Complement.
60, 61	CLK+, CLK−	Input	Clock Input True/Complement.
63, 67	AGND_SR	Ground	Ground Reference for SYSREF±.
64	AVDD1_SR	Supply	Analog Power Supply for SYSREF± (0.975 V Nominal).
65, 66	SYSREF+, SYSREF−	Input	Active Low JESD204B LVDS System Reference Input True/Complement. DC-coupled input only.
	EPAD		Exposed Pad. Analog ground. The exposed thermal pad on the bottom of the package provides the ground reference for AVDDX, SPIVDD, DVDD, DRVDD1, and DRVDD2. This exposed pad must be connected to ground for proper operation.

TYPICAL PERFORMANCE CHARACTERISTICS

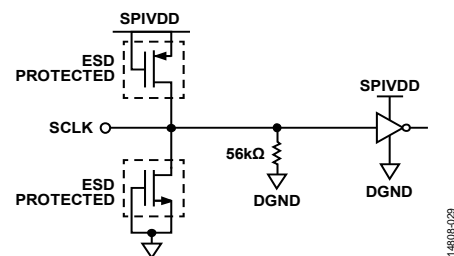
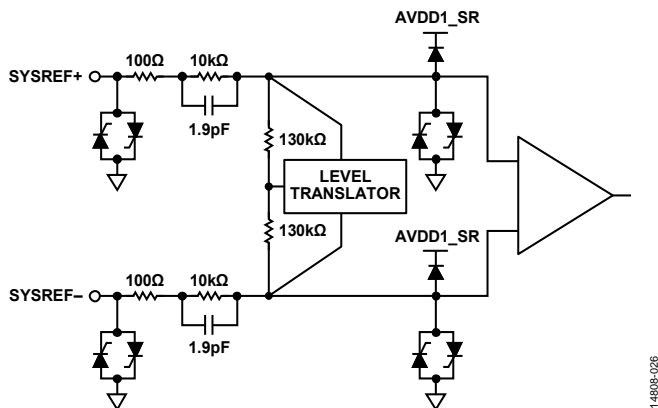
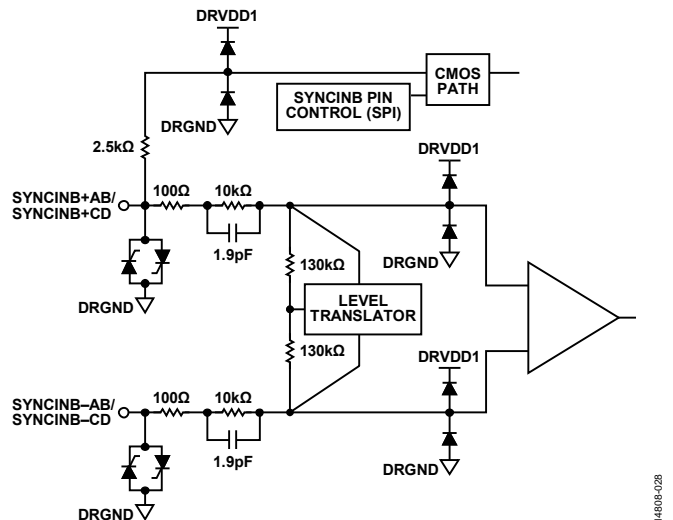
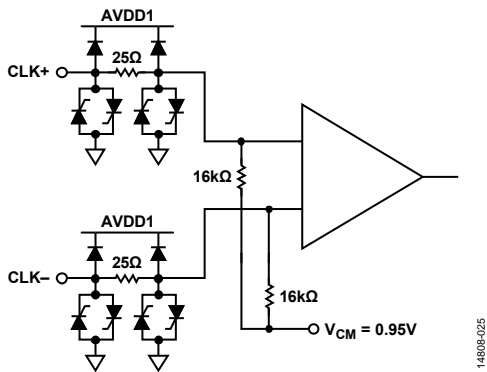
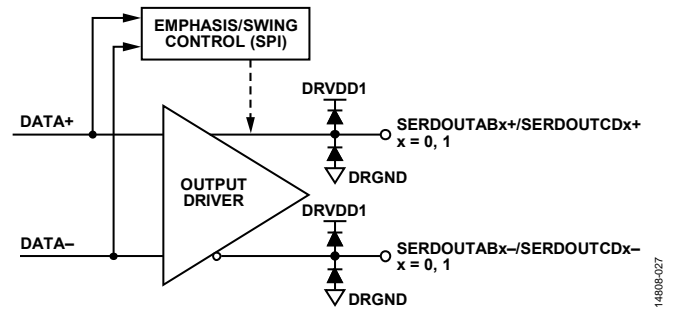
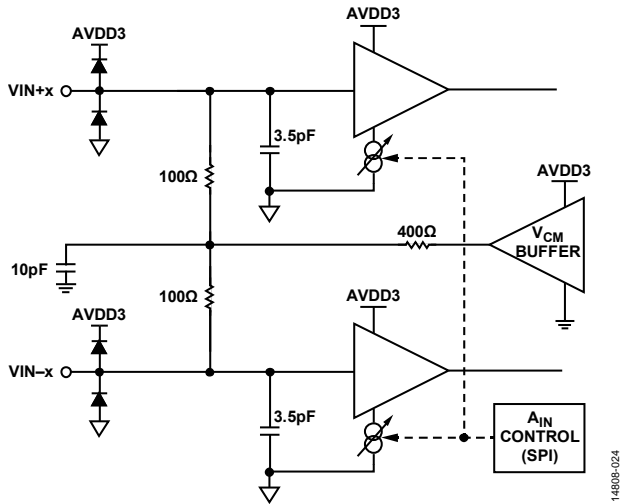
AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.80 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.8 V, SPIVDD = 1.8 V, specified maximum sampling rate, clock divider = 4, 1.80 V p-p full-scale differential input, 0.5 V internal reference, $A_{IN} = -1.0$ dBFS, default SPI settings, unless otherwise noted. Minimum and maximum specifications are guaranteed for the full operating junction temperature (T_J) range of -40°C to $+105^{\circ}\text{C}$. Typical specifications represent performance at $T_J = 50^{\circ}\text{C}$ ($T_A = 25^{\circ}\text{C}$).



TBD

Figure 6.

EQUIVALENT CIRCUITS



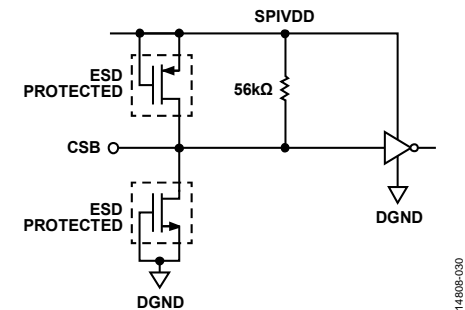


Figure 13. CSB Input

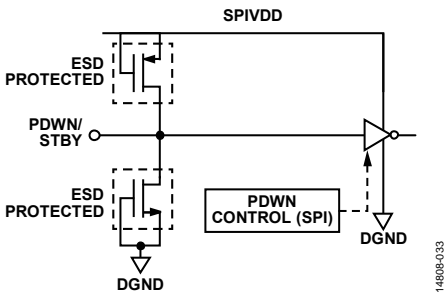


Figure 16. PDWN/STBY Input

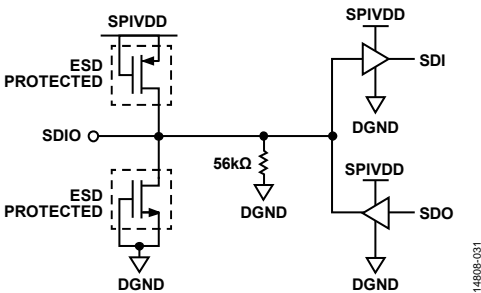


Figure 14. SDIO Input

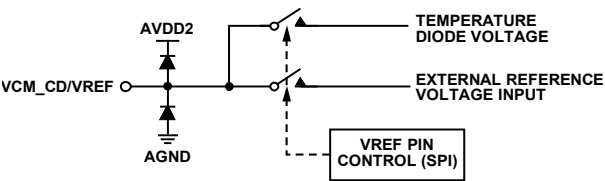


Figure 17. VCM_CD/VREF Input/Output

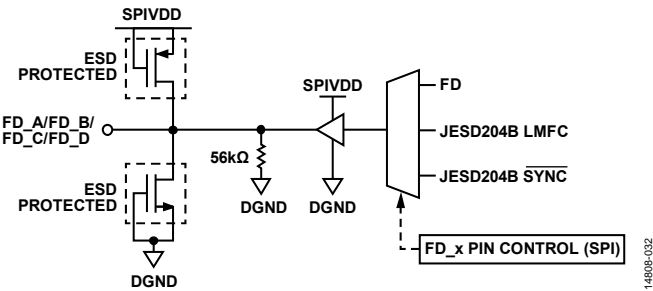


Figure 15. FD_A/FD_B/FD_C/FD_D Outputs

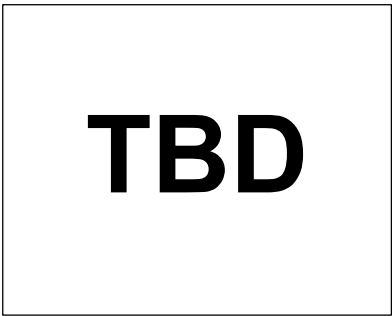


Figure 18. Temperature Diode Voltage vs. Junction Temperature

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD9094 contains fast detect circuitry for individual channels to monitor the threshold and to assert the FD_A, FD_B, FD_C, and FD_D pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

FAST THRESHOLD DETECTION (FD_A, FD_B, FD_C, AND FD_D)

The fast detect (FD) bits in Register 0x0040 are immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bits are cleared only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bits from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 19.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x0247 and Register 0x0248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 30 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\text{Upper Threshold Magnitude (dBFS)} = 20\log (\text{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x0249 and Register 0x024A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\text{Lower Threshold Magnitude (dBFS)} = 20\log (\text{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of -6 dBFS, write 0xFFF to Register 0x0247 and Register 0x0248. To set a lower threshold of -10 dBFS, write 0xA1D to Register 0x0249 and Register 0x024A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x024B and Register 0x024C. See the Memory Map section (Register 0x0040, and Register 0x0245 to Register 0x024C in Table 11) for more details.

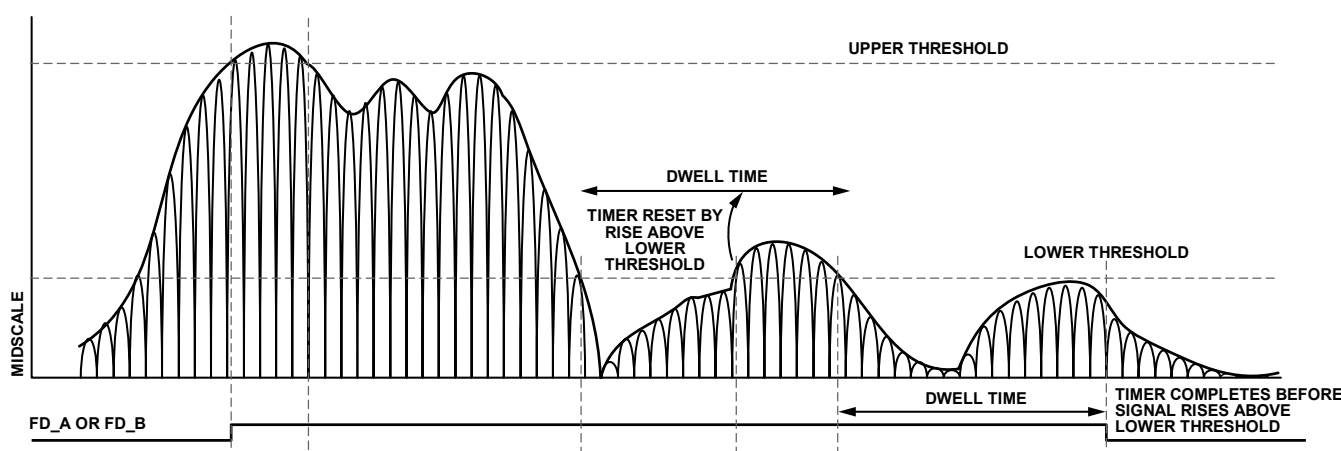


Figure 19. Threshold Settings for the FD_A and FD_B Signals

CONFIGURING THE JESD204B LINK

The AD9094 has two JESD204B links. The device offers an easy way to set up the JESD204B link through the JESD204B JTX quick configuration register (Register 0x570). One link consists of the SERDOUTAB0± and SERDOUTAB1± serial outputs and the second link consists of the SERDOUTCD0± and SERDOUTCD1± serial outputs. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDCs are used for on-chip digital processing, M represents the number of virtual converters.

The maximum lane rate allowed by the JESD204B specification is 15 Gbps. The lane line rate is related to the JESD204B parameters using the following equation:

$$\text{Lane Line Rate} = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where:

Table 7. Virtual Converter Mapping (Per Link)

Number of Virtual Converters Supported	Chip Application Mode (Register 0x0200, Bits[3:0])	Chip Q Ignore (Register 0x0200, Bit 5)	Virtual Converter Mapping			
			0	1	2	3
1 to 2	Full bandwidth mode (0x0)	Real or complex (0x0)	ADC A/ADC C samples	ADC B/ADC D samples	Unused	Unused
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC 0 I samples	Unused	Unused	Unused
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	Unused	Unused
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC 0 I samples	DDC 1 I samples	Unused	Unused
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC 0 I samples	DDC 0 Q samples	DDC 1 I samples	DDC 1 Q samples

Table 8. JESD204B Output Configurations for N' = 8 (Per Link)

Number of Virtual Converters Supported (Same Value as M)	JESD204B Quick Configuration (Register 0x0570)	Serial Lane Rate ¹	JESD204B Transport Layer Settings								
			L	M	F	S	HD	N	N'	CS	K ²
1	0x00	10 × f _{OUT}	1	1	1	1	0	7 to 8	8	0 to 1	Only valid K values which are divisible by 4 are supported
	0x01	10 × f _{OUT}	1	1	2	2	0	7 to 8	8	0 to 1	
	0x40	5 × f _{OUT}	2	1	1	2	0	7 to 8	8	0 to 1	
	0x41	5 × f _{OUT}	2	1	2	4	0	7 to 8	8	0 to 1	
	0x42	5 × f _{OUT}	2	1	4	8	0	7 to 8	8	0 to 1	
2	0x09	20 × f _{OUT}	1	2	2	1	0	7 to 8	8	0 to 1	
	0x48	10 × f _{OUT}	2	2	1	1	0	7 to 8	8	0 to 1	
	0x49	10 × f _{OUT}	2	2	2	2	0	7 to 8	8	0 to 1	

¹ f_{OUT} = output sample rate is the ADC sample rate/chip decimation ratio. The JESD204B serial line rate must be ≥1687.5 Mbps and ≤15,000 Mbps. When the serial lane rate is ≤15 Gbps and >13.5 Gbps, set Bits[7:4] to 0x3 in Register 0x056E. When the serial lane rate is ≤13.5 Gbps and >6.75 Gbps, set Bits[7:4] to 0x0 in Register 0x056E. When the serial lane rate is ≤6.75 Gbps and >3.375 Gbps, set Bits[7:4] to 0x1 in Register 0x056E. When the serial lane rate is ≤3.375 Gbps and ≥1687.5 Mbps, set Bits[7:4] to 0x5 in Register 0x056E.

² For F = 1, K = 20, 24, 28, and 32. For F = 2, K = 12, 16, 20, 24, 28, and 32. For F = 4, K = 8, 12, 16, 20, 24, 28, and 32. For F = 8 and F = 16, K = 4, 8, 12, 16, 20, 24, 28, and 32.

$$f_{OUT} = \frac{f_{ADC_CLOCK}}{\text{Decimation Ratio}}$$

The decimation ratio (DCM) is the parameter programmed in Register 0x0201.

Use the following steps to configure the output:

1. Power down the link.
2. Select the quick configuration options.
3. Configure any detailed options.
4. Set the output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.

If the lane line rate calculated is less than 6.75 Gbps, select the low line rate option by programming a value of 0x10 to Register 0x056E.

Table 8 shows the JESD204B output configurations supported for N' = 8 for a given number of virtual converters. Take care to ensure that the serial line rate for a given configuration is within the supported range of 1.6875 Gbps to 15 Gbps.

LATENCY

END TO END TOTAL LATENCY

Total latency in the AD9094 is dependent on the chip application mode and the JESD204B configuration. For any given combination of these parameters, the latency is deterministic, however, the value of this deterministic latency must be calculated as described in the Example Latency Calculations section.

Table 9 shows the combined latency through the ADC and DSP for the different chip application modes supported by the AD9094. Table 10 shows the latency through the JESD204B block for each application mode based on the M/L ratio. For both Table 9 and Table 10, latency is typical and is in units of the encode clock. The latency through the JESD204B block does not depend on the output data type (real or complex). Therefore, data type is not included in Table 10.

To determine the total latency, select the appropriate ADC + DSP latency from Table 9 and add it to the appropriate JESD204B latency from Table 10. Example calculations are provided in the following section.

EXAMPLE LATENCY CALCULATIONS

Example Configuration 1

In this example, the ADC application mode is full bandwidth with the following conditions:

- Real outputs
- $L = 4$, $M = 2$, $F = 1$, $S = 1$ (JESD204B mode)
- M/L ratio = 0.5

$$\text{Latency} = 31 + 25 = 56 \text{ encode clocks}$$

Example Configuration 2

In this example, the ADC application mode is decimate by 4, DCM4, with the following conditions:

- Complex outputs
- $L = 4$, $M = 2$, $F = 1$, $S = 1$ (JESD204B mode)
- M/L ratio = 0.5

$$\text{Latency} = 162 + 88 = 250 \text{ encode clocks}$$

LMFC REFERENCED LATENCY

Some FPGA vendors may require the end user to know the LMFC referenced latency to make the appropriate deterministic latency adjustments. If they are required, the latency values in Table 9 and Table 10 can be used for the analog input to LMFC latency value and the LMFC to data output latency value.

Table 9. Latency Through the ADC + DSP Blocks (Number of Sample Clocks)

Chip Application Mode ¹	Enabled Filters	ADC and DSP Latency
Full Bandwidth	Not applicable	31

¹ DCMx indicates the decimation ratio.

Table 10. Latency Through JESD204B Block (Number of Sample Clocks)

Chip App Mode	M/L Ratio ^{1, 2}				
	0.5	1	2	4	8
Full BW	25	14	7	4	2

¹ M/L ratio is the number of converters divided by the number of lanes for the configuration.

² N/A means not applicable, indicating the application mode is not supported at the M/L ratio listed.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is divided into four sections: the Analog Devices SPI registers (Register 0x0000 to Register 0x000D and Register 0x18A6 to Register 0x1A4D, the ADC function registers (Register 0x003F to Register 0x027A, Register 0x0701, and Register 0x073B), the DDC function registers (Register 0x0300 to Register 0x0347), and the digital outputs and test modes registers (Register 0x0550 to Register 0x1262).

Table 11 (see the Memory Map section) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x0561, the output sample mode register, has a hexadecimal default value of 0x01. This default value means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see Table 11.

Unassigned and Reserved Locations

All address and bit locations that are not included in Table 11 are not currently supported for this device. Write unused bits of a valid address location with 0s unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Address 0x0561). If the entire address location is open (for example, Address 0x0013), do not write to this address location.

Default Values

After the AD9094 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 11.

Logic Levels

An explanation of logic level terminology follows:

- “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”
- X denotes a don't care bit.

ADC Pair Addressing

The AD9094 functionally operates as two pairs of dual IF receiver channels. There are two ADCs and two DDCs in each pair making for a total of four of each for the AD9094 device. To access the SPI registers for each pair, the pair index must be written in Register 0x0009. The pair index register must be written prior to any other SPI write to the AD9094.

Channel Specific Registers

Some channel setup functions, such as the fast detect control (Register 0x0247), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 11 as local. These local registers and bits can be accessed by setting the appropriate Channel A/Channel C or Channel B/Channel D bits in Register 0x0008. The particular channel that is addressed is dependent upon the pair selection written to Register 0x0009. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A/Channel C or Channel B/Channel D to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. If both pairs and both channels are selected via Register 0x0009 and Register 0x0008, the device returns the value for Channel A.

The names of the registers listed Table 11 are prefixed with either global map, channel map, JESD204B map, or pair map. Registers in the pair map and JESD204B map apply to a pair of channels, either Pair A/B or Pair C/D. To write registers in the pair map and JESD204B map, the pair index register (Register 0x0009) must be written to address the appropriate pair. The SPI Configuration A (Register 0x0000), SPI Configuration B (Register 0x0001), and pair index (Register 0x0009) registers are the only registers that reside in the global map. Registers in the channel map are local to each channel: Channel A, Channel B, Channel C, or Channel D. To write registers in the channel map, the pair index register (Register 0x0009) must be written first to address the desired pair (Pair A/B or Pair C/D) followed by writing the device index register (Register 0x0008) to select the desired channel (Channel A/Channel C or Channel B/Channel D).

For example, to write Channel A to a test mode (set by Register 0x0550), first write 0x01 to Register 0x0009 to select Pair A/B, followed by writing 0x01 to Register 0x0008 to select Channel A. Then, write Register 0x0550 to the value for the desired test mode. To write all channels to a test mode (set by Register 0x0550), first write Register 0x0009 to a value of 0x03 to select both Pair A/B and Pair C/D, followed by writing Register 0x0008 to a value of 0x03 to select Channel A, Channel B, Channel C, and Channel D. Next, write Register 0x0550 to the value for the desired test mode.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x0000, the AD9094 requires 5 ms to recover. When programming the AD9094 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP REGISTER TABLE—DETAILS

All address locations that are not included in Table 11 are not currently supported for this device and must not be written.

Table 11. Memory Map Details

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0000	Global map SPI Configuration A	7	Soft reset (self clearing)	0	When a soft reset is issued, the user must wait 5 ms before writing to any other register. This wait provides sufficient time for the boot loader to complete.	0x0	R/W
				1	Do nothing. Reset the SPI and registers (self clearing).		
		6	LSB first mirror	1	LSB shifted first for all SPI operations.	0x0	R/W
				0	MSB shifted first for all SPI operations.		
		5	Address ascension mirror	0	Multibyte SPI operations cause addresses to auto-increment.	0x0	R/W
				1	Multibyte SPI operations cause addresses to auto-increment.		
		4	Reserved		Reserved.	0x0	R
		3	Reserved		Reserved.	0x0	R
		2	Address ascension	0	Multibyte SPI operations cause addresses to auto-increment.	0x0	R/W
				1	Multibyte SPI operations cause addresses to auto-increment.		
0x0001	Global map SPI Configuration B	1	LSB first	1	MSB shifted first for all SPI operations.	0x0	R/W
				0	MSB shifted first for all SPI operations.		
		0	Soft reset (self clearing)	0	When a soft reset is issued, the user must wait 5 ms before writing to any other register. This wait provides sufficient time for the boot loader to complete.	0x0	R/W
				1	Do nothing. Reset the SPI and registers (self clearing).		
		7	Single instruction	0	SPI streaming enabled.	0x0	R/W
				1	Streaming (multibyte read/write) is disabled. Only one read or write operation is performed regardless of the state of the CSB line.		
		[6:2]	Reserved		Reserved.	0x0	R
		1	Datapath soft reset (self clearing)			0x0	R/W
				0	Normal operation.		
				1	Datapath soft reset (self clearing)		
		0	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0002	Channel map chip configuration	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Channel power modes		Channel power modes.	0x0	R/W
				00	Normal mode (power up).		
				10	Standby mode. The digital data path clocks are disabled, the JESD204B interface is enabled, and the outputs are enabled.		
				11	Power-down mode. The digital data path clocks are disabled, the digital data path is held in reset, the JESD204B interface is disabled, and the outputs are disabled.		
0x0003	Pair map chip type	[7:0]	CHIP_TYPE	0x3	Chip type. High speed ADC.	0x3	R
0x0004	Pair map chip ID LSB	[7:0]	CHIP_ID		Chip ID.	0xDB	R
0x0006	Pair map chip grade	[7:4]	CHIP_SPEED_GRADE	0	Chip speed grade. 1GSPS	0x0	R
		[3:0]	Reserved		Reserved.	0x0	R
0x0008	Pair map device index	[7:2]	Reserved		Reserved.	0x0	R
		1	Channel B/D	0	ADC Core B/D does not receive the next SPI command.	0x1	R/W
				1	ADC Core B/D receives the next SPI command.		
		0	Channel A/C	0	ADC Core A/C does not receive the next SPI command.	0x1	R/W
				1	ADC Core A/C receives the next SPI command.		
0x0009	Global map pair index	[7:2]	Reserved		Reserved.	0x0	R
		1	Pair C/D	0	ADC Pair C/D does not receive the next read/write command from the SPI interface.	0x1	R/W
				1	ADC Pair C/D does not receive the next read/write command from the SPI interface.		
		0	Pair A/B	0	ADC Pair A/B does not receive the next read/write command from the SPI interface.	0x1	R/W
				1	ADC Pair A/B does receive the next read/write command from the SPI interface.		
0x000A	Pair map scratch pad	[7:0]	Scratch pad		Chip scratch pad register. Used to provide a consistent memory location for software debug.	0x7	R/W
0x000B	Pair map SPI revision	[7:0]	SPI_REVISION		SPI revision register. (0x01 = Revision 1.0)	0x1	R
				00000001	Revision 1.0.		
0x000C	Pair map vendor ID LSB	[7:0]	CHIP_VENDOR_ID[7:0]		Vendor ID.	0x56	R
0x000D	Pair map vendor ID MSB	[7:0]	CHIP_VENDOR_ID[15:8]		Vendor ID.	0x4	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x003F	Channel map chip power-down pin	7	PDWN/STBY disable	0	Used in conjunction with Register 0x0040. Power-down pin (PDWN/STBY) enabled. Global pin control selection enabled (default).	0x0	R/W
				1	Power-down pin (PDWN/STBY) disabled/ignored. Global pin control selection ignored.		
		[6:0]	Reserved		Reserved.	0x0	R
0x0040	Pair Map Chip Pin Control 1	[7:6]	PDWN/STBY function	00	Power-down pin. Assertion of the external power-down pin (PDWN/STBY) causes the chip to enter full power-down mode.	0x0	R/W
				01	Standby pin. Assertion of the external power-down (PDWN/STBY) causes the chip to enter standby mode.		
				10	Pin disabled. Assertion of the external power-down pin (PDWN/STBY) is ignored.		
		[5:3]	Fast Detect B/D (FD_B/FD_D)	000 001 010 111	Fast Detect B/D output. JESD204B LMFC output. JESD204B internal SYNC~ output. Disabled (configured as input with weak pull-down resistor.	0x7	R/W
		[2:0]	Fast Detect A/C (FD_A/FD_C)	000 001 010 111	Fast Detect A/C output. JESD204B LMFC output. JESD204B internal SYNC~ output. Disabled (configured as input with weak pull-down resistor.		
0x0108	Pair map clock divider control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock divider	000 001 011 111	Divide by 1. Divide by 2. Divide by 4. Divide by 8.	0x1	R/W
0x0109	Channel map clock divider phase	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase offset	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	0 input clock cycles delayed. ½ input clock cycles delayed (invert clock). 1 input clock cycle delayed. 1 ½ input clock cycles delayed. 2 input clock cycles delayed. 2 ½ input clock cycles delayed. 3 input clock cycles delayed. 3 ½ input clock cycles delayed. 4 input clock cycles delayed. 4 ½ input clock cycles delayed. 5 input clock cycles delayed. 5 ½ input clock cycles delayed.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				1100 1101 1110 1111	6 input clock cycles delayed. 6 ½ input clock cycles delayed. 7 input clock cycles delayed. 7 ½ input clock cycles delayed.		
0x010A	Pair map clock divider SYSREF± control	7	Clock divider autophase adjust	0 1	Clock divider phase is not changed by SYSREF± (disabled). Clock divider phase is automatically adjusted by SYSREF± (enabled).	0x0	R/W
		[6:4]	Reserved		Reserved.	0x0	R
		[3:2]	Clock divider negative skew window	00 01 10 11	No negative skew: SYSREF± must be captured accurately. ½ device clocks of negative skew. 1 device clock of negative skew. 1 ½ device clocks of negative skew.	0x0	R/W
		[1:0]	Clock divider positive skew window	00 01 10 11	No positive skew: SYSREF± must be captured accurately. ½ device clocks of positive skew. 1 device clock of positive skew. 1 ½ device clocks of positive skew.	0x0	R/W
0x0110	Pair map clock delay control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock delay mode select	000 001 010 011 100 101 110	Clock delay mode select. Used in conjunction with Register 0x0111 and Register 0x0112. No clock delay. Reserved. Fine delay: only Delay Step 0 to Delay Step 16 valid. Fine delay (lowest jitter): only Delay Step 0 to Delay Step 16 valid. Fine delay: all 192 delay steps valid. Reserved (same as 100). Fine delay enabled (all 192 delay steps valid); super fine delay enabled (all 128 delay steps valid).	0x0	R/W
0x0111	Channel map clock super fine delay	[7:0]	Clock super fine delay adjust		Clock super fine delay adjust: this is an unsigned control to adjust the super fine sample clock delay in 0.25 ps steps. 0x00 = 0 delay steps. ... 0x08 = 8 delay steps. ... 0x80 = 128 delay steps.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0112	Channel map clock fine delay	[7:0]	Clock fine delay adjust		Clock fine delay adjust: this is an unsigned control to adjust the fine sample clock skew in 1.725 ps steps. 0x00 = 0 delay steps. ... 0x08 = 8 delay steps. ... 0xC0 = 192 delay steps.	0xC0	R/W
0x011A	Clock detection control	[7:5]	Reserved		Reserved.	0x0	R/W
		[4:3]	Clock detection threshold	01 11	Clock detection threshold. Threshold 1 for sample rate \geq 300 MSPS Threshold 2 for sample rate $<$ 300 MSPS	0x1	R/W
		[2:0]	Reserved		Reserved	0x1	R/W
0x011B	Pair map clock status	[7:1]	Reserved		Reserved.	0x0	R
		0	Input clock detect	0 1	Clock detection status Input clock not detected. Input clock detected/locked.	0x0	R
0x011C	Clock DCS Control 1	[7:3]	Reserved		Reserved	0x1	R/W
		1	Clock DCS 1 enable	0 1	DCS 1 bypassed. DCS 1 enabled.	0x0	R/W
		0	Clock DCS 1 power-up	0 1	DCS 1 powered down DCS 1 powered up. The DCS must be powered up before being enabled.	0x0	R/W
0x011E	Clock DCS Control 2 (this register needs to be set to the value same as DCS Control 1)	[7:3]	Reserved		Reserved	0x11	R/W
		1	Clock DCS 2 enable	0 1	DCS 2 bypassed. DCS 2 enabled.	0x0	R/W
		0	Clock DCS 2 power-up	0 1	DCS 2 powered down. DCS 2 powered up. The DCS must be powered up before being enabled.	0x0	R/W
0x011F	Clock DCS Control 3	[7:0]	Clock DCS 3 enable	0x84	DCS 3 bypassed.	0x84	R/W
				0x81	DCS 3 enabled.		
0x0120	Pair map SYSREF Control 1	7	Reserved		Reserved.	0x0	R
		6	SYSREF \pm flag reset	0 1	Normal flag operation. SYSREF \pm flags held in reset (setup/hold error flags cleared).	0x0	R/W
		5	Reserved		Reserved.	0x0	R
		4	SYSREF \pm transition select	0 1	SYSREF \pm is valid on low to high transitions using selected CLK \pm edge. When changing this setting, SYSREF \pm mode select must be set to disabled. SYSREF \pm is valid on high to low transitions using selected CLK \pm edge. When changing this setting, SYSREF \pm mode select must be set to disabled.	0x0	R/W
		3	CLK \pm edge select	0 1	Captured on rising edge of CLK \pm input. Captured on falling edge of CLK \pm input.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		[2:1]	SYSREF± mode select	00 01 10	Disabled. Continuous. N shot.	0x0	R/W
		0	Reserved		Reserved.	0x0	R
		[7:4]	Reserved		Reserved.	0x0	R
0x0121	Pair map SYSREF Control 2	[3:0]	SYSREF± N shot ignore counter select	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Next SYSREF± only (do not ignore). Ignore the first SYSREF± transition. Ignore the first two SYSREF± transitions. Ignore the first three SYSREF± transitions. Ignore the first four SYSREF± transitions. Ignore the first five SYSREF± transitions. Ignore the first six SYSREF± transitions. Ignore the first seven SYSREF± transitions. Ignore the first eight SYSREF± transitions. Ignore the first nine SYSREF± transitions. Ignore the first 10 SYSREF± transitions. Ignore the first 11 SYSREF± transitions. Ignore the first 12 SYSREF± transitions. Ignore the first 13 SYSREF± transitions. Ignore the first 14 SYSREF± transitions. Ignore the first 15 SYSREF± transitions.	0x0	R/W
0x0123	Pair map SYSREF Control 4	7	Reserved		Reserved.	0x0	R
		[6:0]	SYSREF± timestamp delay, Bits[6:0]		SYSREF± timestamp delay (in converter sample clock cycles). 0: 0 sample clock cycle delay. 1: 1 sample clock cycle delay. ... 127: 127 sample clock cycle delay.	0x40	R/W
0x0128	Pair map SYSREF Status 1	[7:4]	SYSREF± hold status, Bits[7:4]		SYSREF± hold status.	0x0	R
		[3:0]	SYSREF± setup status, Bits[3:0]		SYSREF± setup status.	0x0	R
0x0129	Pair map SYSREF Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase when SYSREF± was captured		SYSREF± divider phase. Represents the phase of the divider when SYSREF± was captured. 0000 = in phase. 0001 = SYSREF± is ½ cycle delayed from clock. 0010 = SYSREF± is 1 cycle delayed from clock. 0011 = 1½ input clock cycles delayed. 0100 = 2 input clock cycles delayed. 0101 = 2½ input clock cycles delayed. ... 1111 = 7½ input clock cycles delayed.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x012A	Pair map SYSREF Status 3	[7:0]	SYSREF counter, Bits[7:0] increments when a SYSREF± is captured		SYSREF± count. Running counter that increments whenever a SYSREF± event is captured. Reset by Register 0x0120, Bit 6. Wraps around at 255. Read these bits only while Register 0x0120, Bits[2:1] is set to disabled.	0x0	R
0x01FF	Pair map chip sync	[7:1]	Reserved		Reserved.	0x0	R
		0	Synchronization mode	0x0 0x1	Sample synchronization mode. SYSREF± signal resets all internal sample dividers. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any of the dividers needs to change, the JESD204B link goes down. Partial synchronization/timestamp mode. SYSREF± signal does not reset sample internal dividers. In this mode, the JESD204B link, the signal monitor, the parallel interface clocks are not affected by the SYSREF± signal. The SYSREF± signal simply timestamps a sample as it passes through the ADC.	0x0	R/W
0x0200	Pair map chip mode	[7:6]	Reserved		Reserved.	0x0	R/W
		5	Chip Q ignore	0 1	Chip real (I) only selection. Both real (I) and complex (Q) selected. Only real (I) selected. Complex (Q) is ignored.	0x0	R/W
		4	Reserved		Reserved.	0x0	R
		[3:0]	Chip application mode	0000 0001 0010	Full bandwidth mode. One DDC mode (DDC 0 only). Two DDC mode (DDC 0 and 1 only).	0x0	R/W
0x0201	Pair map chip decimation ratio	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Chip decimation ratio select	000 001 010 011 100	Chip decimation ratio. Decimate by 1 (full sample rate). Decimate by 2. Decimate by 4. Decimate by 8. Decimate by 16.	0x0	R/W
0x0228	Channel map custom offset	[7:0]	Offset adjust in LSBs from +127 to -128		Digital data path offset. Twos complement offset adjustment aligned with least significant converter resolution bit.	0x0	R/W
0x0245	Channel map fast detect control	[7:4]	Reserved		Reserved.	0x0	R
		3	Force FD_A/FD_B/FD_C/FD_D pins	0 1	Normal operation of fast detect pin. Force a value on fast detect pin (see Bit 2).	0x0	R/W
		2	Force value of FD_A/FD_B/FD_C/FD_D pins (if force pins is true, this value is output on FD_x pins)		The fast detect output pin for this channel is set to this value when the output is forced.	0x0	R/W
		1	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Enable fast detect output	0 1	Fine fast detect disabled. Fine fast detect enabled.	0x0	R/W
0x0247	Channel map fast detect upper threshold LSB	[7:0]	Fast detect upper threshold, Bits[7:0]		LSBs of fast detect upper threshold. 8 LSBs of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x0248	Channel map fast detect upper threshold MSB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect upper threshold, Bits[12:8]		LSBs of fast detect upper threshold. 8 LSBs of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x0249	Channel map fast detect lower threshold LSB	[7:0]	Fast detect lower threshold, Bits[7:0]		LSBs of fast detect lower threshold. 8 LSBs of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024A	Channel map fast detect lower threshold MSB	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect lower threshold, Bits[12:8]		LSBs of fast detect lower threshold. 8 LSBs of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024B	Channel map fast detect dwell time LSB	[7:0]	Fast detect dwell time, Bits[7:0]		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x024C	Channel map fast detect dwell time MSB	[7:0]	Fast detect dwell time, Bits[15:8]		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x026F	Pair map signal monitor sync control	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Signal monitor synchronization mode	0 1	Synchronization disabled. Only the next valid edge of the SYSREF± pin is used to synchronize the signal monitor block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF± is received, this bit is cleared. The SYSREF± input pin must be enabled to synchronize the signal monitor blocks.	0x0	R/W
0x0270	Channel map signal monitor control	[7:2]	Reserved		Reserved.	0x0	R
		1	Peak detector	0 1	Peak detector disabled. Peak detector enabled.	0x0	R/W
		0	Reserved		Reserved.	0x0	R
0x0271	Channel Map Signal Monitor Period 0	[7:0]	Signal monitor period, Bits[7:0]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x80	R/W
0x0272	Channel Map Signal Monitor Period 1	[7:0]	Signal monitor period, Bits[15:8]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0273	Channel Map Signal Monitor Period 2	[7:0]	Signal monitor period, Bits[23:16]		This 24-bit value sets the number of output clock cycles over which the signal monitor performs its operation. Bit 0 is ignored.	0x0	R/W
0x0274	Channel map signal monitor status control	[7:5]	Reserved		Reserved.	0x0	R
		4	Result update	1	Status update based on Bits[2:0] (self clearing).	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	Result selection	001	Peak detector placed on status readback signals.	0x1	R/W
0x0275	Channel Map Signal Monitor Status 0	[7:0]	Signal monitor result, Bits[7:0]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0276	Channel Map Signal Monitor Status 1	[7:0]	Signal monitor result, Bits[15:8]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0277	Channel Map Signal Monitor Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Signal monitor result, Bits[19:16]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block. The content is dependent on the Register 0x0274, Bits[2:0] bit settings.	0x0	R
0x0278	Channel map signal monitor status frame counter	[7:0]	Period count result, Bits[7:0]		Signal monitor frame counter status bits. Frame counter increments whenever the period counter expires.	0x0	R
0x0279	Channel map signal monitor serial framer control	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Signal monitor SPORT over JESD204B enable	0 1	Disabled. Enabled.	0x0	R/W
0x027A	SPORT over JESD204B input selection (local)	[7:6]	Reserved		Reserved.	0x0	R
		1	SPORT over JESD204B input selection	0 1	Signal monitor serial framer input selection. When each individual bit is a 1, the corresponding signal statistics information is sent within the frame. Disabled. Peak detector data inserted in serial frame.	0x1	R/W
		0	Reserved			0x0	R
0x0300	Pair map DDC sync control	7	Reserved		Reserved.	0x0	R/W
		6	Reserved		Reserved.	0x0	R/W
		5	Reserved		Reserved.	0x0	R
		4	DDC NCO soft reset	0 1	This bit can be used to synchronize all the NCOs inside the DDC blocks. Normal operation. DDC held in reset.	0x0	R/W
		[3:2]	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		1	DDC next sync	0	The SYSREF± pin must be an integer multiple of the NCO frequency for this function to operate correctly in continuous mode. Continuous mode.	0x0	R/W
				1	Only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF± edge is found, the DDC synchronization enable bit is cleared.		
		0	DDC synchronization mode	0 1	The SYSREF± input pin must be enabled to synchronize the DDCs. Synchronization Disabled. If DDC next sync == 1, only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF± edge is received, this bit is cleared.	0x0	R/W
0x0310	Pair map DDC 0 control	7	DDC 0 mixer select	0 1	Real mixer (I and Q inputs must be from the same real channel). Complex mixer (I and Q must be from separate, real and imaginary quadrature ADC receive channels—analog demodulator).	0x0	R/W
		6	DDC 0 gain select	0 1	Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component. 0 dB gain. 6 dB gain (multiply by 2).	0x0	R/W
		[5:4]	DDC 0 IF mode	00 01 10 11	Variable IF mode. 0 Hz IF mode. f _s /4 Hz IF mode. Test mode.	0x0	R/W
		3	DDC 0 complex to real enable	0 1	Complex (I and Q) outputs contain valid data. Real (I) output only. Complex to real enabled. Uses extra f _s /4 mixing to convert to real.	0x0	R/W
		2	Reserved		Reserved.	0x0	R
		[1:0]	DDC 0 decimation rate select	11 00	Decimation filter selection. HB1 filter selection: decimate by 1 (real outputs (complex to real enabled)) or decimate by 2 (complex outputs (complex to real disabled)). HB2 + HB1 filter selection: decimate by 2 (real outputs (complex to real enabled)) or decimate by 4 ((complex outputs (complex to real disabled))).	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
				01 10	HB3 + HB2 + HB1 filter selection: decimate by 4 (real outputs (complex to real enabled)) or decimate by 8 (complex outputs (complex to real disabled)). HB4 + HB3 + HB2 + HB1 filter selection: decimate by 8 (real outputs (complex to real enabled)) or decimate by 16 (complex outputs (complex to real disabled)).		
0x0311	Pair Map DDC 0 input select	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 0 Q input select	0 1	Channel A/Channel C. Channel B/Channel D.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DDC 0 I input select	0 1	Channel A. Channel B.	0x0	R/W
0x0314	Pair Map DDC 0 Phase Increment 0	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[7:0]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0315	Pair Map DDC 0 Phase Increment 1	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[15:8]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0316	Pair Map DDC 0 Phase Increment 2	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[23:16]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0317	Pair Map DDC 0 Phase Increment 3	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[31:24]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0318	Pair Map DDC 0 Phase Increment 4	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[39:32]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x031A	Pair Map DDC 0 Phase Increment 5	[7:0]	DDC 0 NCO frequency value, twos complement, Bits[47:40]		NCO phase increment value; twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x031D	Pair Map DDC 0 Phase Offset 0	[7:0]	DDC 0 NCO phase value, twos complement, Bits[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W
0x031E	Pair Map DDC 0 Phase Offset 1	[7:0]	DDC 0 NCO phase value, twos complement, Bits[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x031F	Pair Map DDC 0 Phase Offset 2	[7:0]	DDC 0 NCO phase value, twos complement, Bits[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0320	Pair Map DDC 0 Phase Offset 3	[7:0]	DDC 0 NCO phase value, twos complement, Bits[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0321	Pair Map DDC 0 phase Offset 4	[7:0]	DDC 0 NCO phase value, twos complement, Bits[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0322	Pair Map DDC 0 Phase Offset 5	[7:0]	DDC 0 NCO phase value, twos complement, Bits[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0327	Pair Map DDC 0 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 0 Q output test mode enable	0 1	Q samples always use Test Mode B/D block. Test mode disabled. Test mode enabled.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DDC 0 I output test mode enable	0 1	I samples always use Test Mode A/C block. Test mode disabled. Test mode enabled.	0x0	R/W
0x0330	Pair Map DDC 1 control	7	DDC 1 mixer select	0 1	Real mixer (I and Q inputs must be from the same real channel). Complex mixer (I and Q must be from separate real and imaginary quadrature ADC receive channels—analog demodulator).	0x0	R/W
		6	DDC 1 gain select	0 1	Gain can be used to compensates for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component. 0 dB gain. 6 dB gain (multiply by 2).	0x0	R/W
		[5:4]	DDC 1 IF mode	00 01 10 11	Variable IF mode. 0 Hz IF mode. $f_s/4$ Hz IF mode. Test mode.	0x0	R/W
		3	DDC 1 complex to real enable	0 1	Complex (I and Q) outputs contain valid data. Real (I) output only. Complex to real enabled. Uses extra $f_s/4$ mixing to convert to real.	0x0	R/W
		2	Reserved		Reserved.	0x0	R
		[1:0]	DDC 1 decimation rate select	11 00 01 10	Decimation filter selection. HB1 filter selection: decimate by 1 (real outputs (complex to real enabled)) or decimate by 2 (complex outputs (complex to real disabled)). HB2 + HB1 filter selection: decimate by 2 (real outputs (complex to real enabled)) or decimate by 4 ((complex outputs (complex to real disabled)). HB3 + HB2 + HB1 filter selection: decimate by 4 (real outputs (complex to real enabled)) or decimate by 8 (complex outputs (complex to real disabled)). HB4 + HB3 + HB2 + HB1 filter selection: decimate by 8 (real outputs (complex to real enabled)) or decimate by 16 (complex outputs (complex to real disabled)).	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0331	Pair Map DDC 1 input select	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 1 Q input select	0 1	Channel A/Channel C. Channel B/Channel D.	0x1	R/W
		1	Reserved		Reserved.	0x0	R
		0	DDC 1 I input select	0 1	Channel A. Channel B.	0x1	R/W
0x0334	Pair Map DDC 1 Phase Increment 0	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[7:0]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0335	Pair Map DDC 1 Phase Increment 1	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[15:8]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0336	Pair Map DDC 1 Phase Increment 2	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[23:16]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0337	Pair Map DDC 1 Phase Increment 3	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[31:24]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x0338	Pair Map DDC 1 Phase Increment 4	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[39:32]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x033A	Pair Map DDC 1 Phase Increment 5	[7:0]	DDC 1 NCO frequency value, twos complement, Bits[47:40]		NCO phase increment value. Twos complement phase increment value for the NCO. Complex mixing frequency = $(\text{DDC phase increment} \times f_s)/2^{48}$.	0x0	R/W
0x033D	Pair Map DDC 1 Phase Offset 0	[7:0]	DDC 1 NCO phase value, twos complement, Bits[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W
0x033E	Pair Map DDC 1 Phase Offset 1	[7:0]	DDC 1 NCO phase value, twos complement, Bits[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x033F	Pair Map DDC 1 Phase Offset 2	[7:0]	DDC 1 NCO phase value, twos complement, Bits[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0340	Pair Map DDC 1 Phase Offset 3	[7:0]	DDC 1 NCO phase value, twos complement, Bits[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0341	Pair Map DDC 1 Phase Offset 4	[7:0]	DDC 1 NCO phase value, twos complement, Bits[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0342	Pair Map DDC 1 Phase Offset 5	[7:0]	DDC 1 NCO phase value, twos complement, Bits[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0347	Pair Map DDC 1 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC 1 Q output test mode enable	0 1	Q samples always use Test Mode B/Test Mode D block. Test mode disabled. Test mode enabled.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	DDC 1 I output test mode enable	0 1	I samples always use Test Mode A/Test Mode C block. Test mode disabled. Test mode enabled.	0x0	R/W
0x0550	Channel map test mode control	7	User pattern selection	0 1	Continuous repeat. Single pattern.	0x0	R/W
		6	Reserved		Reserved.	0x0	R
		5	Reset pseudorandom long generator	0 1	Long PN enabled. Long PN held in reset.	0x0	R/W
		4	Reset PN short gen	0 1	Short PN enabled. Short PN held in reset.	0x0	R/W
		[3:0]	Test mode selection	0000 0001 0010 0011 0100 0101 0110 0111 1000 1111	Off—normal operation. Midscale short. Positive full scale. Negative full scale. Alternating checkerboard. PN sequence—long. PN sequence—short. 1/0 word toggle. User pattern test mode (used with the test mode pattern selection and the User Pattern 1 through User Pattern 4 registers) Ramp output.	0x0	R/W
0x0551	Pair map User Pattern 1 LSB	[7:0]	User Pattern 1, Bits[7:0]		User Test Pattern 1 least significant byte.	0x0	R/W
0x0552	Pair map User Pattern 1 MSB	[7:0]	User Pattern 1, Bits[15:8]		User Test Pattern 1 most significant byte.	0x0	R/W
0x0553	Pair map User Pattern 2 LSB	[7:0]	User Pattern 2, Bits[7:0]		User Test Pattern 2 least significant byte.	0x0	R/W
0x0554	Pair map User Pattern 2 MSB	[7:0]	User Pattern 2, Bits[15:8]		User Test Pattern 2 most significant byte.	0x0	R/W
0x0555	Pair map User Pattern 3 LSB	[7:0]	User Pattern 3, Bits[7:0]		User Test Pattern 3 least significant byte.	0x0	R/W
0x0556	Pair map User Pattern 3 MSB	[7:0]	User Pattern 3, Bits[15:8]		User Test Pattern 3 most significant byte.	0x0	R/W
0x0557	Pair map User Pattern 4 LSB	[7:0]	User Pattern 4, Bits[7:0]		User Test Pattern 4 least significant byte.	0x0	R/W
0x0558	Pair map User Pattern 4 MSB	[7:0]	User Pattern 4, Bits[15:8]		User Test Pattern 4 most significant byte.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0559	Pair map Output Control Mode 0	7	Reserved		Reserved.	0x0	R
		[6:4]	Converter Control Bit 1 selection	000 001 010 011 100 101 110 111	Tie low (1'b0). Overrange bit. Signal monitor (SMON) bit. Fast detect (FD) bit. Reserved. SYSREF±. Reserved. Reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	Converter Control Bit 0 selection	000 001 010 011	Tie low (1'b0). Overrange bit. Signal monitor (SMON) bit. Fast detect (FD) bit.	0x0	R/W
				101 100 110 111	SYSREF±. Reserved. Reserved. Reserved.		
0x055A	Pair map Output Control Mode 1	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Converter control Bit 2 selection	000 001 010 011 100 101 110 111	Tie low (1'b0). Overrange bit. Signal monitor (SMON) bit. Fast detect (FD) bit. Reserved. SYSREF±. Reserved. Reserved.	0x1	R/W
0x0561	Pair map output sample mode	[7:3]	Reserved		Reserved.	0x0	R
		2	Sample invert	0 1	ADC sample data is not inverted. ADC sample data is inverted.	0x0	R/W
		[1:0]	Data format select	00 01	Offset binary. Twos complement (default).	0x1	R/W
0x0564	Pair map output channel select	[7:2]	Reserved		Reserved.	0x0	R
		1	Reserved		Reserved.	0x0	R/W
		0	Converter channel swap control	0 1	Normal channel ordering. Channel swap enabled.	0x0	R/W
0x056E	JESD204B map PLL control	[7:4]	JESD204B lane rate control	0000 0001 0011 0101	Lane rate = 6.75 Gbps to 13.5 Gbps. Lane rate = 3.375 Gbps to 6.75 Gbps. Lane rate = 13.5 Gbps to 15 Gbps. Lane rate = 1.6875 Gbps to 3.375 Gbps.	0x0	R/W
		[3:0]	Reserved		Reserved.	0x0	R

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x056F	JESD204B map PLL STATUS	7	PLL lock status	0 1	Not locked. Locked.	0x0	R
		[6:4]	Reserved		Reserved.	0x0	R
		3	Reserved		Reserved.	0x0	R
		[2:0]	Reserved		Reserved.	0x0	R
0x0570	JESD204B map JTX quick configuration	[7:6]	Quick Configuration L	0 1	Number of lanes (L) = $2^{0x0570[7:6]}$. L = 1. L = 2.	0x1	R/W
		[5:3]	Quick Configuration M	0 1 10	Number of converters (M) = $2^{0x0570[5:3]}$. M = 1. M = 2. M = 4.	0x1	R/W
		[2:0]	Quick Configuration F	0 1 10 11	Number of octets/frame (F) = $2^{0x0570[2:0]}$. F = 1. F = 2. F = 4. F = 8.	0x1	R/W
0x0571	JESD204B map JTX Link Control 1	7	Standby mode	0 1	Standby mode forces zeros for all converter samples. Standby mode forces code group synchronization (/K28.5/ characters).	0x0	R/W
		6	Tail bit (t) PN	0 1	Disable. Enable.	0x0	R/W
		5	Long transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled—long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.	0x0	R/W
		4	Lane synchronization	0 1	Disable FACL uses /K28.7/. Enable FACL uses /K28.3/ and /K28.7/.	0x1	R/W
		[3:2]	ILAS sequence mode	00 01 11	Initial lane alignment sequence disabled— (JESD204B 5.3.3.5). Initial lane alignment sequence enabled— (JESD204B 5.3.3.5). Initial lane alignment t sequence always on test mode—JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) sent on all lanes.	0x1	R/W
		1	FACL	0 1	Frame alignment character insertion enabled (JESD204B 5.3.3.4). Frame alignment character insertion disabled—for debug only (JESD204B 5.3.3.4).	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
		0	Link control	0 1	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNCINB±x pin. JESD204B serial transmit link powered down (held in reset and clock gated).	0x0	R/W
0x0572	JESD204B map JTX Link Control 2	[7:6]	SYNCINB±x pin control	00 10 11	Normal mode. Ignore SYNCINB±x (force CGS). Ignore SYNCINB±x (force ILAS/user data).	0x0	R/W
		5	SYNCINB±x pin invert	0 1	SYNCINB±x pin not inverted. SYNCINB±x pin inverted.	0x0	R/W
		4	SYNCINB±x pin type	0 1	LVDS differential pair SYNC~ input. CMOS single-ended SYNC~ input.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	8-bit/10-bit bypass	0 1	8-bit/10-bit enabled. 8-bit/10-bit bypassed (most significant two bits are 0).	0x0	R/W
		1	8-bit/10-bit invert	0 1	Normal. Invert abcdefghij symbols.	0x0	R/W
		0	Reserved		Reserved.	0x0	R/W
0x0573	JESD204B map JTX Link Control 3	[7:6]	Checksum mode	00 01 10 11	Checksum is the sum of all 8-bit registers in the link configuration table. Checksum is the sum of all individual link configuration fields (LSB aligned). Checksum is disabled (set to zero). For test purposes only. Unused.	0x0	R/W
		[5:4]	Test injection point	0 1 10	N' sample input. 10-bit data at 8-bit/10-bit output (for PHY testing). 8-bit data at scrambler input.	0x0	R/W
		[3:0]	JESD204B test mode patterns	0 1 10 11 100 101 110 111 1000 1110 1111	Normal operation (test mode disabled). Alternating checkerboard. 1/0 word toggle. 31-bit PN sequence: $x^{31} + x^{28} + 1$. 23-bit PN sequence: $x^{23} + x^{18} + 1$. 15-bit PN sequence: $x^{15} + x^{14} + 1$. 9-bit PN sequence: $x^9 + x^5 + 1$. 7-bit PN sequence: $x^7 + x^6 + 1$. Ramp output. Continuous/repeat user test. Single user test.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0574	JESD204B map JTX Link Control 4	[7:4]	ILAS delay	0	Transmit ILAS on first LMFC after SYNCINB±x is deasserted.	0x0	R/W
				1	Transmit ILAS on second LMFC after SYNCINB±x is deasserted.		
				10	Transmit ILAS on third LMFC after SYNCINB±x is deasserted.		
				11	Transmit ILAS on fourth LMFC after SYNCINB±x is deasserted.		
				100	Transmit ILAS on fifth LMFC after SYNCINB±x is deasserted.		
				101	Transmit ILAS on sixth LMFC after SYNCINB±x is deasserted.		
				110	Transmit ILAS on seventh LMFC after SYNCINB±x is deasserted.		
				111	Transmit ILAS on eighth LMFC after SYNCINB±x is deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB±x is deasserted.		
				1001	Transmit ILAS on 10 th LMFC after SYNCINB±x is deasserted.		
				1010	Transmit ILAS on 11 th LMFC after SYNCINB±x is deasserted.		
				1011	Transmit ILAS on 12 th LMFC after SYNCINB±x is deasserted.		
				1100	Transmit ILAS on 13 th LMFC after SYNCINB±x is deasserted.		
				1101	Transmit ILAS on 14 th LMFC after SYNCINB±x is deasserted.		
				1110	Transmit ILAS on 15 th LMFC after SYNCINB±x is deasserted.		
				1111	Transmit ILAS on 16 th LMFC after SYNCINB±x is deasserted.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode	000	Normal operation (link layer test mode disabled).	0x0	R/W
				001	Continuous sequence of /D21.5/ characters.		
				010	Reserved.		
				011	Reserved.		
				100	Modified RPAT test sequence.		
				101	JSPAT test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
0x0578	JESD204B map JTX LMFC offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		Local multiframe clock (LMFC) phase offset value. Reset value for LMFC phase counter when SYSREF± is asserted. Used for deterministic delay applications.	0x0	R/W
0x0580	JESD204B map JTX DID configuration	[7:0]	JESD204B Tx DID value		JESD204x serial device identification (DID) number.	0x0	R/W
0x0581	JESD204B map JTX BID configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B Tx BID value		JESD204x serial bank identification (BID) number (extension to DID).	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0583	JESD204B map JTX LID 0 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204x serial lane identification (LID) number for Lane 0.	0x0	R/W
0x0585	JESD204B map JTX LID 1 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204x serial lane identification (LID) number for Lane 1.	0x2	R/W
0x058B	JESD204B map JTX SCR L configuration	7	JESD204B scrambling (SCR)	0 1	JESD204x scrambler disabled (SCR = 0). JESD204x scrambler enabled (SCR = 1).	0x1	R/W
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B lanes (L)	0x0 0x1	One lane per link (L = 1). Two lanes per link (L = 2).	0x1	R
0x058C	JESD204B map JTX F configuration	[7:0]	Number of octets per frame (F)		Number of octets per frame, F = Register 0x058C, Bits[7:0] + 1.	0x1	R
0x058D	JESD204B map JTX K configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Number of frames per multiframe (K)	00011 00111 01100 01111 10011 10111 11011 11111	JESD204x number of frames per multiframe (K = Register 0x058D, Bits[4:0] + 1). Only values where F × K, which are divisible by 4, can be used. K = 4. K = 8. K = 12. K = 16. K = 20. K = 24. K = 28. K = 32.	0x1F	R/W
0x058E	JESD204B map JTX M configuration	[7:0]	Number of converters per link	00000000 00000001 00000011	Link connected to one virtual converter (M = 1). Link connected to two virtual converters (M = 2). Link connected to four virtual converters (M = 4).	0x1	R
0x058F	JESD204B map JTX CS N configuration	[7:6]	Number of control bits (CS) per sample	00 01 10 11	No control bits (CS = 0). One control bit (CS = 1), Control Bit 2 only. Two control bits (CS = 2), Control Bit 2 and Control Bit 1 only. Three control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).	0x0	R/W
		5	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)	00110 00111	N = 7-bit resolution. N = 8-bit resolution.	0x7	R/W

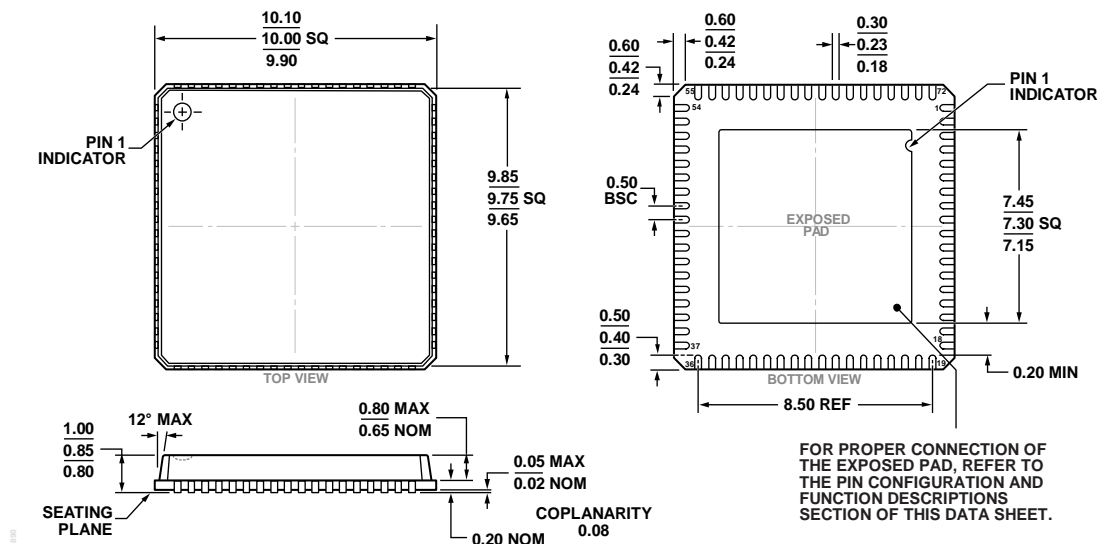
Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0590	JESD204B map JTX Subclass Version NP configuration	[7:5]	Subclass support	000 001	Subclass 0. Subclass 1.	0x1	R/W
		[4:0]	ADC number of bits per sample (N')	00111	N' = 8.	0x7	R/W
0x0591	JESD204B map JTX S configuration	[7:5]	Reserved		Reserved.	0x1	R
		[4:0]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[4:0] + 1).	0x0	R
0x0592	JESD204B map JTX HD CF configuration	7	HD value	0 1	High density format disabled. High density format enabled.	0x0	R
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link (CF = Register 0x0592, Bits[4:0]).	0x0	R
0x05A0	JESD204B map JTX Checksum 0 configuration	[7:0]	Checksum 0 checksum value for SERDOUTx0±		Serial checksum value for Lane 0. Automatically calculated for each lane. SUM(all link configuration parameters for Lane 0) % 256.	0xC3	R
0x05A1	JESD204B map JTX Checksum 1 configuration	[7:0]	Checksum 1 checksum value for SERDOUTx1±		Serial Checksum Value for Lane 1. Automatically calculated for each lane. SUM(all link configuration parameters for Lane 1) % 256.	0xC4	R
0x05B0	SERDOUTx0±/ SERDOUTx1± lane power-down	7	Reserved		Reserved.	0x1	R/W
		6	Reserved		Reserved.	0x1	R/W
		5	Reserved		Reserved.	0x1	R/W
		4	Reserved		Reserved.	0x1	R/W
		3	Reserved		Reserved.	0x1	R/W
		2	SERDOUTx1± Lane 1 power-down		Physical Lane 1 force power-down.	0x0	R/W
		1	Reserved		Reserved.	0x1	R/W
		0	SERDOUTx0± Lane 0 power-down		Physical Lane 0 force power-down.	0x0	R/W
0x05B2	JESD204B map JTX lane Assignment 1	7	Reserved		Reserved.	0x0	R
		[6:4]	Reserved		Reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUTx0± lane assignment	0 1 10 11	Logical Lane 0 (default). Logical Lane 1. Logical Lane 2. Logical Lane 3.	0x0	R/W
0x05B3	JESD204B map JTX lane Assignment 2	7	Reserved		Reserved.	0x0	R
		[6:4]	Reserved		Reserved.	0x1	R/W
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUTx1± lane assignment	0 1 10 11	Logical Lane 0. Logical Lane 1 (default). Logical Lane 2. Logical Lane 3.	0x1	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x05C0	JESD204B map JESD204B serializer drive adjust	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Swing voltage SERDOUTx0±	0 1	1.0 × DRVDD1 (differential). 0.850 × DRVDD1 (differential).	0x1	R/W
0x05C1	JESD204B map JESD204B serializer drive adjust	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Swing voltage SERDOUTx1±	0 1	1.0 × DRVDD1 (differential). 0.850 × DRVDD1 (differential).	0x1	R/W
0x05C4	JESD204B serializer preemphasis selection register for Logical Lane 0	7	Post tap enable	0 1	Disable. Enable.	0x0	R/W
		[6:4]	Sets post tap level	0 1 10 11 100	0 dB (recommended when insertion loss = 0 dB to 4 dB when voltage swing setting is 0). 3 dB (recommended when insertion loss = 4 dB to 9 dB when voltage swing setting is 0). 6 dB (recommended when insertion loss = 9 dB to 14 dB when voltage swing setting is 0). 9 dB (recommended when insertion loss > 14 dB when voltage swing setting is 0). 12 dB.	0x0	R/W
		[3:0]	Reserved		Reserved.	0x0	R
0x05C6	JESD204B serializer preemphasis selection register for Logical Lane 1	7	Post tap polarity	0 1	Disable. Enable.	0x0	R/W
		[6:4]	Sets post tap level	0 1 10 11 100	0 dB (recommended when insertion loss = 0 dB to 4 dB when voltage swing setting is 0). 3 dB (recommended when insertion loss = 4 dB to 9 dB when voltage swing setting is 0). 6 dB (recommended when insertion loss = 9 dB to 14 dB when voltage swing setting is 0). 9 dB (recommended when insertion loss > 14 dB when voltage swing setting is 0). 12 dB.	0x0	R/W
		[3:0]	Reserved		Reserved.	0x0	R
0x0922	Large dither control	[7:0]	Large dither control	1110000 1110001	Enable. Disable.	0x70	R/W
0x1222	PLL calibration	[7:0]	PLL calibration	0x00 0x04	PLL calibration. Normal operation. PLL calibration	0x0	R/W
0x1228	JESD204B start- up circuit reset	[7:0]	JESD204B start-up circuit reset	0x0F 0x4F	JESD204B start-up circuit reset. Normal operation. Start-up circuit reset.	0xF	R/W
0x1262	PLL loss of lock control		PLL loss of lock control	0x00 0x08	PLL loss of lock control. Normal operation. Clear loss of lock.	0x0	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x0701	DC offset calibration control	[7:0]	DC offset calibration control	0x06 0x86	Disable dc offset calibration. Enable dc offset calibration.	0x06	R/W
0x073B	DC Offset Calibration Control 2 (local)	7	DC Offset Calibration Enable 2	0 1	Enabled (must set to 0 when Register 0x0701, Bit 7 = 1). Disabled (must set to 1 when Register 0x0701, Bit 7 = 0).	0x1	R/W
		[6:0]	Reserved	111111	Reserved.	0x3F	R
0x18A6	Pair map VREF control	[7:5]	Reserved		Reserved.	0x0	R
		4	Reserved		Reserved.	0x0	R/W
		[3:1]	Reserved		Reserved.	0x0	R
		0	VREF control	0 1	Internal reference. External reference.	0x0	R/W
0x18E0	External V _{CM} Buffer Control 1	[7:0]	External V _{CM} Buffer Control 1			0x0	R/W
0x18E1	External V _{CM} Buffer Control 2	[7:0]	External V _{CM} Buffer Control 2			0x0	R/W
0x18E2	External V _{CM} Buffer Control 3	[7:0]	External V _{CM} Buffer Control 3			0x0	R/W
0x18E3	External V _{CM} buffer control	7	Reserved		Reserved.	0x0	R/W
		6	External V _{CM} buffer	1 0	Enable. Disable.	0x0	R/W
		[5:0]	External V _{CM} buffer current setting			0x0	R/W
0x18E6	Temperature diode export	[7:1]	Reserved		Reserved.	0x0	R/W
		0	Temperature diode export	1 0	Enable. Disable.	0x0	R/W
0x1908	Channel map analog input control	[7:6]	Reserved		Reserved.	0x0	R
		[5:4]	Reserved		Reserved.	0x0	R/W
		3	Reserved		Reserved.	0x0	R
		2	Analog input dc coupling control	0 1	Analog input dc coupling control. AC coupling. DC coupling.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	Reserved		Reserved.	0x0	R/W
0x1910	Channel map input full-scale range	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Input full-scale control	0000 1010 1011 1100 1101 1110 1111	2.16 V p-p. 1.44 V p-p. 1.56 V p-p. 1.68 V p-p. 1.80 V p-p. 1.92 V p-p. 2.04 V p-p. Reserved.	0xD	R/W

Addr	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x1A4C	Channel map Buffer Control 1	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 1	00110	120 μ A.	0xC	R/W
				01000	160 μ A.		
				01010	200 μ A.		
				01100	240 μ A.		
				01110	280 μ A.		
				10000	320 μ A.		
				10010	360 μ A.		
				10100	400 μ A.		
				10110	440 μ A.		
0x1A4D	Channel map Buffer Control 2	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 2	00110	120 μ A.	0xC	R/W
				01000	160 μ A.		
				01010	200 μ A.		
				01100	240 μ A.		
				01110	280 μ A.		
				10000	320 μ A.		
				10010	360 μ A.		
				10100	400 μ A.		
				10110	440 μ A.		

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 20. 72-Lead Lead Frame Chip Scale Package [LFCSPP]
 10 mm × 10 mm Body and 0.85 mm Package Height
 (CP-72-10)

Dimensions shown in millimeters