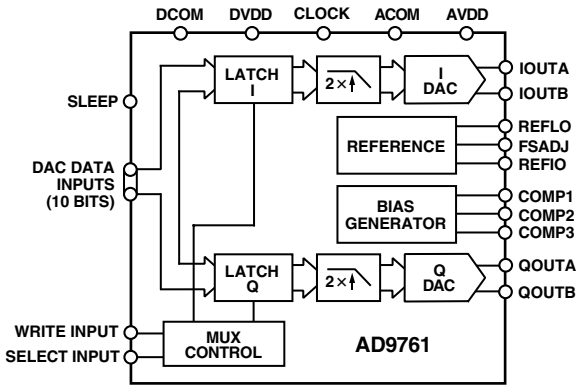
# Dual 10-Bit TxDAC+® with 2× Interpolation Filters

# AD9761

**FEATURES**

**Complete 10-Bit, 40 MSPS Dual Transmit DAC**
**Excellent Gain and Offset Matching**
**Differential Nonlinearity Error: 0.5 LSB**
**Effective Number of Bits: 9.5**
**Signal-to-Noise and Distortion Ratio: 59 dB**
**Spurious-Free Dynamic Range: 71 dB**
**2× Interpolation Filters**
**20 MSPS/Channel Data Rate**
**Single Supply: 3 V to 5.5 V**
**Low Power Dissipation: 93 mW (3 V Supply @ 40 MSPS)**
**On-Chip Reference**
**28-Lead SSOP**

**FUNCTIONAL BLOCK DIAGRAM**




## PRODUCT DESCRIPTION

The AD9761 is a complete dual-channel, high speed, 10-bit CMOS DAC. The AD9761 has been developed specifically for use in wide bandwidth communication applications (e.g., spread spectrum) where digital I and Q information is being processed during transmit operations. It integrates two 10-bit, 40 MSPS DACs, dual 2× interpolation filters, a voltage reference, and digital input interface circuitry. The AD9761 supports a 20 MSPS per channel input data rate that is then interpolated by 2× up to 40 MSPS before simultaneously updating each DAC.

The interleaved I and Q input data stream is presented to the digital interface circuitry, which consists of I and Q latches as well as some additional control logic. The data is de-interleaved back into its original I and Q data. An on-chip state machine ensures the proper pairing of I and Q data. The data output from each latch is then processed by a 2× digital interpolation filter that eases the reconstruction filter requirements. The interpolated output of each filter serves as the input of their respective 10-bit DAC.

The DACs utilize a segmented current source architecture combined with a proprietary switching technique to reduce glitch energy and to maximize dynamic accuracy. Each DAC provides differential current output, thus supporting single-ended or differential applications. Both DACs are simultaneously updated and provide a nominal full-scale current of 10 mA. Also, the full-scale currents between each DAC are matched to within 0.07 dB (i.e., 0.75%), thus eliminating the need for additional gain calibration circuitry.

The AD9761 is manufactured on an advanced low cost CMOS process. It operates from a single supply of 3 V to 5.5 V and consumes 200 mW of power. To make the AD9761 complete, it also offers an internal 1.20 V temperature-compensated band gap reference.

## PRODUCT HIGHLIGHTS

1. Dual 10-Bit, 40 MSPS DACs
   A pair of high performance 40 MSPS DACs optimized for low distortion performance provide for flexible transmission of I and Q information.
2. 2× Digital Interpolation Filters
   Dual matching FIR interpolation filters with 62.5 dB stopband rejection precede each DAC input, thus reducing the DACs' reconstruction filter requirements.
3. Low Power
   Complete CMOS dual DAC function operates on a low 200 mW on a single supply from 3 V to 5.5 V. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for power reduction during idle periods.
4. On-Chip Voltage Reference
   The AD9761 includes a 1.20 V temperature-compensated band gap voltage reference.
5. Single 10-Bit Digital Input Bus
   The AD9761 features a flexible digital interface that allows each DAC to be addressed in a variety of ways including different update rates.
6. Small Package
   The AD9761 offers the complete integrated function in a compact 28-lead SSOP package.
7. Product Family
   The AD9761 Dual Transmit DAC has a pair of Dual Receive ADC companion products, the AD9281 (8 bits) and AD9201 (10 bits).

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# AD9761–SPECIFICATIONS

## DC SPECIFICATIONS ($T_{MIN}$ to $T_{Max}$, AVDD = 5 V, DVDD = 5 V, $I_{OUTFS}$ = 10 mA, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| RESOLUTION | 10 | | | Bits |
| DC ACCURACY[1] | | | | |
| Integral Nonlinearity Error (INL) | | | | |
| $T_A$ = 25°C | –1.75 | ±0.5 | +1.75 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | –2.75 | ±0.7 | +2.75 | LSB |
| Differential Nonlinearity (DNL) | | | | |
| $T_A$ = 25°C | –1 | ±0.4 | +1.25 | LSB |
| $T_{MIN}$ to $T_{MAX}$ | –1 | ±0.5 | +1.75 | LSB |
| Monotonicity (10-Bit) | Guaranteed over Rated Specification Temperature Range | | | |
| ANALOG OUTPUT | | | | |
| Offset Error | –0.05 | ±0.025 | +0.05 | % of FSR |
| Offset Matching between DACs | –0.10 | ±0.05 | +0.10 | % of FSR |
| Gain Error (without Internal Reference) | –5.5 | ±1.0 | +5.5 | % of FSR |
| Gain Error (with Internal Reference) | –5.5 | ±1.0 | +5.5 | % of FSR |
| Gain Matching between DACs | –1.0 | ±0.25 | +1.0 | % of FSR |
| Full-Scale Output Current[2] | | 10 | | mA |
| Output Compliance Range | –1.0 | | +1.25 | V |
| Output Resistance | | 100 | | kΩ |
| Output Capacitance | | 5 | | pF |
| REFERENCE OUTPUT | | | | |
| Reference Voltage | 1.14 | 1.20 | 1.26 | V |
| Reference Output Current[3] | | 100 | | nA |
| REFERENCE INPUT | | | | |
| Input Compliance Range | 0.1 | | 1.25 | V |
| Reference Input Resistance | | 1 | | MΩ |
| TEMPERATURE COEFFICIENTS | | | | |
| Unipolar Offset Drift | | 0 | | ppm/°C |
| Gain Drift (without Internal Reference) | | ±50 | | ppm/°C |
| Gain Drift (with Internal Reference) | | ±140 | | ppm/°C |
| Gain Matching Drift (between DACs) | | ±25 | | ppm/°C |
| Reference Voltage Drift | | ±50 | | ppm/°C |
| POWER SUPPLY | | | | |
| AVDD | | | | |
| Voltage Range | 3.0 | 5.0 | 5.5 | V |
| Analog Supply Current ($I_{AVDD}$) | | 26 | 29 | mA |
| DVDD | | | | |
| Voltage Range | 2.7 | 5.0 | 5.5 | V |
| Digital Supply Current at 5 V ($I_{DVDD}$)[4] | | 15 | 18 | mA |
| Digital Supply Current at 3 V ($I_{DVDD}$)[4] | | 5 | | mA |
| Nominal Power Dissipation[5] | | | | |
| AVDD and DVDD at 3 V | | 93 | | mW |
| AVDD and DVDD at 5 V | | 200 | 250 | mW |
| Power Supply Rejection Ratio (PSRR)–AVDD | –0.25 | | +0.25 | % of FSR/V |
| Power Supply Rejection Ratio (PSRR)–DVDD | –0.02 | | +0.02 | % of FSR/V |
| OPERATING RANGE | –40 | | +85 | °C |

NOTES

[1]Measured at IOUTA and QOUTA, driving a virtual ground.

[2]Nominal full-scale current, $I_{OUTFS}$, is 16× the $I_{REF}$ current.

[3]Use an external amplifier to drive any external load.

[4]Measured at $f_{CLOCK}$ = 40 MSPS and $f_{OUT}$ = 1 MHz.

[5]Measured as unbuffered voltage output into 50 Ω $R_{LOAD}$ at IOUTA, IOUTB, QOUTA, and QOUTB; $f_{CLOCK}$ = 40 MSPS and $f_{OUT}$ = 8 MHz.

Specifications subject to change without notice.

## DYNAMIC SPECIFICATIONS

($T_{MIN}$ to $T_{MAX}$, AVDD = 5 V, DVDD = 5 V, $I_{OUTFS}$ = 10 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | |
| Maximum Output Update Rate | 40 | | | MSPS |
| Output Settling Time ($t_{ST}$ to 0.025%) | | 35 | | ns |
| Output Propagation Delay ($t_{PD}$) | | 55 | | Input Clock Cycles |
| Glitch Impulse | | 5 | | pV-s |
| Output Rise Time (10% to 90%) | | 2.5 | | ns |
| Output Fall Time (10% to 90%) | | 2.5 | | ns |
| AC LINEARITY TO NYQUIST | | | | |
| Signal-to-Noise and Distortion (SINAD) | | | | |
| $f_{OUT}$ = 1 MHz; CLOCK = 40 MSPS | 56 | 59 | | dB |
| Effective Number of Bits (ENOBs) | 9.0 | 9.5 | | Bits |
| Total Harmonic Distortion (THD) | | | | |
| $f_{OUT}$ = 1 MHz; CLOCK = 40 MSPS | | | | |
| $T_A$ = 25°C | | –68 | –58 | dB |
| $T_{MIN}$ to $T_{MAX}$ | | –67 | –53 | dB |
| Spurious-Free Dynamic Range (SFDR) | | | | |
| $f_{OUT}$ = 1 MHz; CLOCK = 40 MSPS; 10 MHz Span | 59 | 68 | | dB |
| Channel Isolation | | | | |
| $f_{OUT}$ = 8 MHz; CLOCK = 40 MSPS; 10 MHz Span | | 90 | | dBc |

Specifications subject to change without notice.

## DIGITAL SPECIFICATIONS

($T_{MIN}$ to $T_{MAX}$, AVDD = 5 V, DVDD = 5 V, $I_{OUTFS}$ = 10 mA unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| DIGITAL INPUTS | | | | |
| Logic 1 Voltage @ DVDD = 5 V | 3.5 | 5 | | V |
| Logic 1 Voltage @ DVDD = 3 V | 2.4 | 3 | | V |
| Logic 0 Voltage @ DVDD = 5 V | | 0 | 1.3 | V |
| Logic 0 Voltage @ DVDD = 3 V | | 0 | 0.9 | V |
| Logic 1 Current | –10 | | +10 | µA |
| Logic 0 Current | –10 | | +10 | µA |
| Input Capacitance | | 5 | | pF |
| Input Setup Time ($t_S$) | | 3 | | ns |
| Input Hold Time ($t_H$) | | 2 | | ns |
| CLOCK High | | 5 | | ns |
| CLOCK Low | | 5 | | ns |
| Invalid CLOCK/WRITE Window ($t_{CINV}$)* | 1 | | 5 | ns |

*$t_{CINV}$ is an invalid window of 4 ns duration beginning 1 ns *after* the rising edge of WRITE in which the rising edge of CLOCK *must not* occur.

Specifications subject to change without notice.

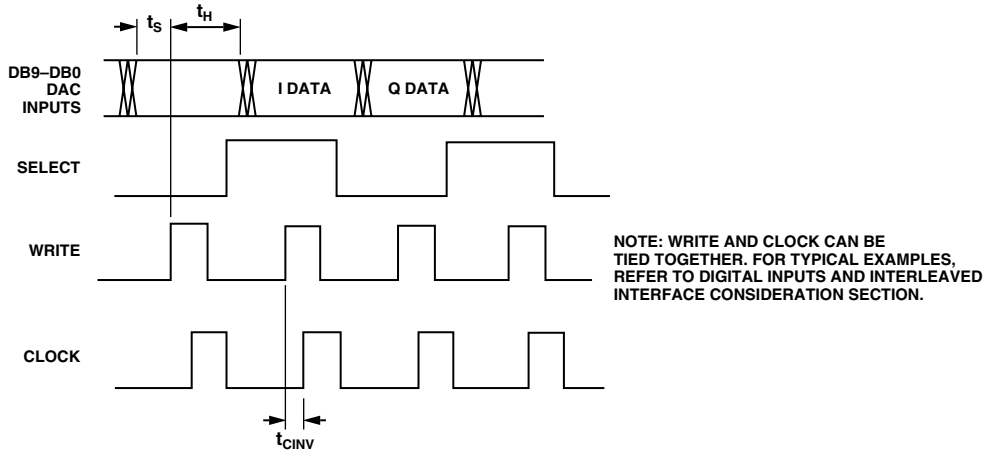


*Figure 1. Timing Diagram*

## DIGITAL FILTER SPECIFICATIONS

($T_{MIN}$ to $T_{MAX}$, AVDD = 2.7 V to 5.5 V, DVDD = 2.7 V to 5.5 V, $I_{OUTFS}$ = 10 mA, unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| MAXIMUM INPUT CLOCK RATE ($f_{CLOCK}$) | 40 | | | MSPS |
| DIGITAL FILTER CHARACTERISTICS | | | | |
| Pass Bandwidth[1]: 0.005 dB | | 0.2010 | | $f_{OUT}/f_{CLOCK}$ |
| Pass Bandwidth: 0.01 dB | | 0.2025 | | $f_{OUT}/f_{CLOCK}$ |
| Pass Bandwidth: 0.1 dB | | 0.2105 | | $f_{OUT}/f_{CLOCK}$ |
| Pass Bandwidth: –3 dB | | 0.239 | | $f_{OUT}/f_{CLOCK}$ |
| Linear Phase (FIR Implementation) | | | | |
| Stop-Band Rejection: 0.3 $f_{CLOCK}$ to 0.7 $f_{CLOCK}$ | | –62.5 | | dB |
| Group Delay[2] | | 32 | | Input Clock Cycles |
| Impulse Response Duration[3] | | | | |
| –40 dB | | 28 | | Input Clock Cycles |
| –60 dB | | 40 | | Input Clock Cycles |

NOTES
[1]Excludes SINx/x characteristic of DAC.
[2]Defined as the number of data clock cycles between impulse input and peak of output response.
[3]55 input clock periods from input to I DAC, 56 to Q DAC. Propagation delay is delay from data input to DAC update.

Specifications subject to change without notice.

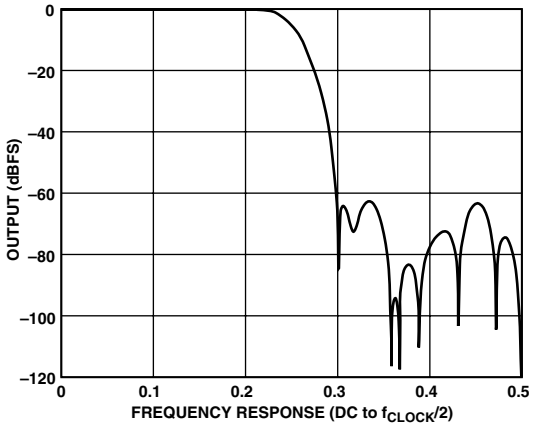


*Figure 2a. FIR Filter Frequency Response*

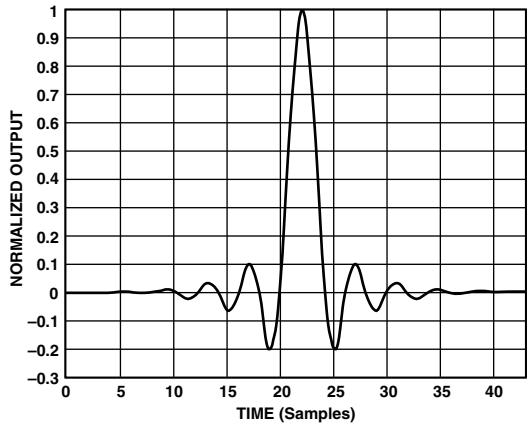


*Figure 2b. FIR Filter Impulse Response*

**Table I. Integer Filter Coefficients for 43-Tap Half-Band FIR Filter**

| Lower Coefficient | Upper Coefficient | Integer Value |
|---|---|---|
| H(1) | H(43) | 1 |
| H(2) | H(42) | 0 |
| H(3) | H(41) | –3 |
| H(4) | H(40) | 0 |
| H(5) | H(39) | 8 |
| H(6) | H(38) | 0 |
| H(7) | H(37) | –16 |
| H(8) | H(36) | 0 |
| H(9) | H(35) | 29 |
| H(10) | H(34) | 0 |
| H(11) | H(33) | –50 |
| H(12) | H(32) | 0 |
| H(13) | H(31) | 81 |
| H(14) | H(30) | 0 |
| H(15) | H(29) | –131 |
| H(16) | H(28) | 0 |
| H(17) | H(27) | 216 |
| H(18) | H(26) | 0 |
| H(19) | H(25) | –400 |
| H(20) | H(24) | 0 |
| H(21) | H(23) | 1264 |
| H(22) | | 1998 |

**ORDERING GUIDE**

| Model | Package Description | Package Option |
|---|---|---|
| AD9761ARS | 28-Lead Shrink Small Outline (SSOP) | RS-28 |
| AD9761ARSRL | 28-Lead Shrink Small Outline (SSOP) | RS-28 |
| AD9761-EB | Evaluation Board | |

**THERMAL CHARACTERISTICS**

**Thermal Resistance**

28-Lead SSOP

$\theta_{JA}$ = 109°C/W

**ABSOLUTE MAXIMUM RATINGS***

| Parameter | With Respect to | Min | Max | Unit |
|---|---|---|---|---|
| AVDD | ACOM | –0.3 | +6.5 | V |
| DVDD | DCOM | –0.3 | +6.5 | V |
| ACOM | DCOM | –0.3 | +0.3 | V |
| AVDD | DVDD | –6.5 | +6.5 | V |
| CLOCK, WRITE | DCOM | –0.3 | DVDD + 0.3 | V |
| SELECT, SLEEP | DCOM | –0.3 | DVDD + 0.3 | V |
| Digital Inputs | DCOM | –0.3 | DVDD + 0.3 | V |
| IOUTA, IOUTB | ACOM | –1.0 | AVDD + 0.3 | V |
| QOUTA, QOUTB | ACOM | –1.0 | AVDD + 0.3 | V |
| COMP1, COMP2 | ACOM | –0.3 | AVDD + 0.3 | V |
| COMP3 | ACOM | –0.3 | AVDD + 0.3 | V |
| REFIO, FSADJ | ACOM | –0.3 | AVDD + 0.3 | V |
| REFLO | ACOM | –0.3 | +0.3 | V |
| Junction Temperature | | | 150 | °C |
| Storage Temperature | | –65 | +150 | °C |
| Lead Temperature (10 sec) | | | 300 | °C |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

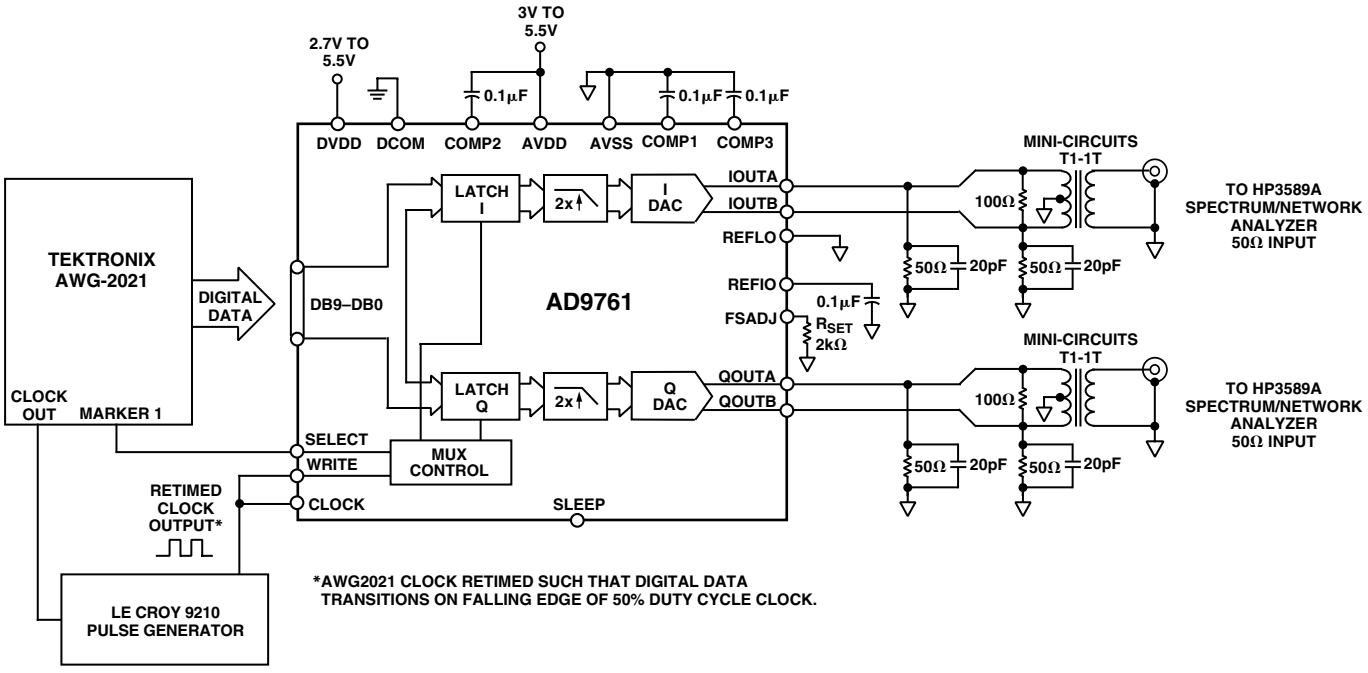


*Figure 3. Basic AC Characterization Test Setup*

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9761 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.