Quad, Low Power JFET-Input Op Amps

Preliminary Technical Data

ADA4062-4

FEATURES

- **Low input bias current: 100 pA maximum**
- **Offset voltage**
  - **1.5 mV maximum for ADA4062-4 B grade**
  - **2.5 mV maximum for ADA4062-4 A grade**
- **Offset voltage drift: 2 µV/°C typical**
- **Slew rate: 4 V/µs typical**
- **CMRR: 90 dB typical**
- **Low supply current: 170 µA typical**
- **Bias current: 100 pA maximum**
- **±15 V operation**
- **Unity-gain stable**

APPLICATIONS

- **Power control and monitoring**
- **Active filters**
- **Industrial/process control**
- **Body probe electronics**
- **Data acquisition**
- **Integrators**
- **Input buffering**

PIN CONFIGURATIONS

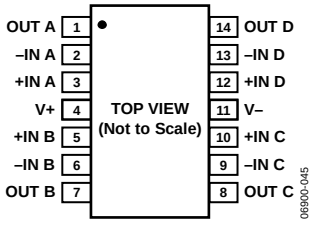

Figure 1. 14-Lead TSSOP (RU-14)

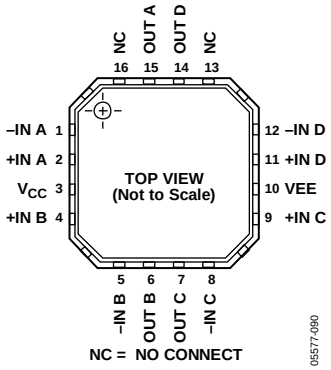

Figure 2. 16-Lead LFCSP
(CP-16-4 Suffix)

GENERAL DESCRIPTION

The ADA4062-4 is a quad JFET-input amplifiers providing industry-leading performance. The ADA4062-4 A and B grades are improved versions of the TL064A B and I grades.

The ADA4062-4 offers lower power, lower noise, lower offset voltage, lower offset drift over temperature, and lower bias current compared with the TL064. In addition, the ADA4062-4 has better common-mode rejection and slew rate.

These op amps are ideal for various applications, including process control, industrial and instrumentation equipment, active filtering, data conversion, buffering, and power control and monitoring.

All devices are available in lead-free 14-lead TSSOP and 16-lead LFCSP (3x3x0.85mm) packages. The ADA4062-4 is specified from −40°C to +125°C.

Table 1. Low Power Op Amps

Supply	40 V	36 V	12 V to 16 V	5 V
Single	OP97	AD820	AD8641 AD8663	AD8541
Dual	OP297	OP282 AD8682 AD822	AD8642 AD8667	AD8542
Quad	OP497	OP482 AD8684 AD824	AD8643 AD8669	AD8544

Rev. PrA

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—±15 V OPERATION

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2. ADA4062-4 A Grade

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			TBD	2.5	mV
		−40°C ≤ T_A ≤ +125°C			TBD	mV
Input Bias Current	I_B			TBD	100	pA
		−40°C ≤ T_A ≤ +125°C			TBD	nA
Input Offset Current	I_{OS}				100	pA
		−40°C ≤ T_A ≤ +125°C			TBD	nA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	−11.5		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −11.5 V to +11.5 V	85	90		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −10 V to +10 V	TBD	86		dB
		−40°C ≤ T_A ≤ +125°C	TBD	73		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		2		µV/°C
Input Resistance	R_{IN}			1		TΩ
Input Capacitance, Differential Mode	C_{INDM}			TBD		pF
Input Capacitance, Common Mode	C_{INCM}			TBD		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	12	13.4		V
		−40°C ≤ T_A ≤ +125°C	12			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−13.4	−12	V
		−40°C ≤ T_A ≤ +125°C			TBD	V
Short-Circuit Current	I_{SC}			±15		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 8 V to 36 V	80	86		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		170	225	µA
		−40°C ≤ T_A ≤ +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = 1	1.5	4		V/µs
Settling Time	t_S	To 0.1%, V_{IN} = 2 V step, C_L = 20 pF, R_L = 1 kΩ, A_V = 1		TBD		µs
Overload Recovery Time				TBD		µs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, A_V = 1		1.5		MHz
Phase Margin	Φ_M	R_L = 10 kΩ, A_V = 1		63		Degrees
Channel Separation	CS	f = 10 kHz		120		dB
Rise Time	t_R	V_{IN} = 20 mV, C_L = 100 pF, R_L = 10 kΩ		0.2		µs
Overshoot Factor		V_{IN} = 20 mV, C_L = 100 pF, R_L = 10 kΩ		5		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		TBD		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz

ELECTRICAL CHARACTERISTICS—±15 V OPERATION

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3. ADA4062-4 B Grade

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			TBD	1.5	mV
		−40°C ≤ T_A ≤ +125°C			TBD	mV
Input Bias Current	I_B			TBD	100	pA
		−40°C ≤ T_A ≤ +125°C			TBD	nA
Input Offset Current	I_{OS}				100	pA
		−40°C ≤ T_A ≤ +125°C			TBD	nA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	−11.5		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −11.5 V to +11.5 V	85	90		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Large-Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −10 V to +10 V	TBD	86		dB
		−40°C ≤ T_A ≤ +125°C	TBD	73		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		2		µV/°C
Input Resistance	R_{IN}			1		TΩ
Input Capacitance, Differential Mode	C_{INDM}			TBD		pF
Input Capacitance, Common Mode	C_{INCM}			TBD		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V_{CM}	13	13.4		V
		−40°C ≤ T_A ≤ +125°C	13			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V_{CM}		−13.4	−13	V
		−40°C ≤ T_A ≤ +125°C			−13	V
Short-Circuit Current	I_{SC}			±15		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 100 kHz, A_V = 1		TBD		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 8 V to 36 V	80	86		dB
		−40°C ≤ T_A ≤ +125°C	TBD			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		170	225	µA
		−40°C ≤ T_A ≤ +125°C			TBD	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 100 pF, A_V = 1	1.5	4		V/µs
Settling Time	t_S	To 0.1%, V_{IN} = 2 V step, C_L = 20 pF, R_L = 1 kΩ, A_V = 1		TBD		µs
Overload Recovery Time				TBD		µs
Gain Bandwidth Product	GBP	R_L = 10 kΩ, A_V = 1		1.5		MHz
Phase Margin	Φ_M	R_L = 10 kΩ, A_V = 1		63		Degrees
Channel Separation	CS	f = 10 kHz		120		dB
Rise Time	t_R	V_{IN} = 20 mV, C_L = 100 pF, R_L = 10 kΩ		0.2		µs
Overshoot Factor		V_{IN} = 20 mV, C_L = 100 pF, R_L = 10 kΩ		5		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		TBD		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	GND to V_{SY}
Input Current[1]	±10 mA
Differential Input Voltage[2]	7 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the supply power pins. The input current should be limited to 10 mA or less whenever input signals exceed the power supply rail by 0.5 V.
[2] Differential input voltage is limited to 7 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 2-layer board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead TSSOP	TBD	TBD	°C/W
16-Lead LFCSP	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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