Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET Operational Amplifier

Data Sheet **ADA4610-2**

FEATURES

Low offset voltage
- **B grade: 0.4 mV maximum**
- **A grade: 1 mV maximum**

Low offset voltage drift
- **B grade: 4 μV/°C maximum**
- **A grade: 8 μV/°C maximum**

Low input bias current: 5 pA typical at V_{SY} = ±15 V
Dual-supply operation: ±4.5 V to ±15 V
Low noise
- **7.3 nV/√Hz typical at f = 1 kHz**
- **0.45 μV p-p at 0.1 Hz to 10 Hz**

Low distortion: 0.00006%
No phase reversal
Rail-to-rail output
Unity gain stable

APPLICATIONS

Instrumentation
Medical instruments
Multipole filters
Precision current measurement
Photodiode amplifiers
Sensors
Audio

PIN CONFIGURATIONS

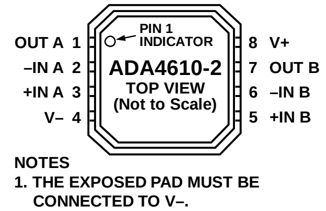

Figure 1. 8-Lead LFCSP (CP Suffix)

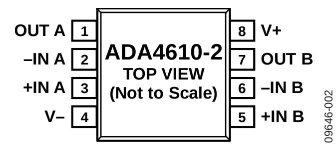

Figure 2. 8-Lead SOIC_N (R Suffix) and 8-Lead MSOP (RM Suffix)

GENERAL DESCRIPTION

The ADA4610-2 is a dual precision JFET amplifier that features low offset voltage, low input bias current, low input voltage noise, low input current noise, and rail-to-rail output.

The combination of low offset, low noise, and very low input bias currents makes this amplifier especially suitable for high impedance sensor amplification and precise current measurements using shunts. The combination of dc precision, low noise, and fast settling time results in superior accuracy in medical instruments, electronic measurement, and automated test equipment. Unlike many competitive amplifiers, the ADA4610-2 maintains fast settling performance even with substantial capacitive loads. Unlike many older JFET amplifiers, the ADA4610-2 does not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

Fast slew rate and great stability with capacitive loads make the ADA4610-2 a perfect fit for high performance filters. Low input bias currents, low offset, and low noise result in a wide dynamic range of photodiode amplifier circuits. Low noise, low distortion, high output current, and excellent speed make the ADA4610-2 a great choice for audio applications.

The ADA4610-2 is specified over the −40°C to +125°C extended industrial temperature range.

The ADA4610-2 is available in the 8-lead narrow SOIC, 8-lead MSOP, and 8-lead LFCSP packages.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

12/11—Revision 0: Initial Version

SPECIFICATIONS

V_{SY} = ±5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade)[1]	V_{OS}			0.2	0.4	mV
		−40°C < T_A < +125°C			0.8	mV
Offset Voltage (A Grade)[1]	V_{OS}			0.4	1	mV
		−40°C < T_A < +125°C			1.8	mV
Offset Voltage Drift (B Grade)[2]	$\Delta V_{OS}/\Delta T$			0.5	4	µV/°C
Offset Voltage Drift (A Grade)[2]	$\Delta V_{OS}/\Delta T$			1	8	µV/°C
Input Bias Current	I_B			5	25	pA
		−40°C < T_A < +125°C			1.5	nA
Input Offset Current	I_{OS}			2	20	pA
		−40°C < T_A < +125°C			0.25	nA
Input Voltage Range			−2.5		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −2.5 V to +2.5 V	94	110		dB
		−40°C < T_A < +125°C	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = −3.5 V to +3.5 V	98	100		dB
		−40°C < T_A < +125°C	86			dB
Input Impedance, Differential		V_{CM} = 0 V		3.1		pF
Input Impedance, Common-Mode		V_{CM} = 0 V		4.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	4.85	4.90		V
		−40°C < T_A < +125°C	4.6			V
		R_L = 600 Ω	4.6	4.89		V
		−40°C < T_A < +125°C	4.05			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−4.95	−4.9	V
		−40°C < T_A < +125°C			−4.75	V
		R_L = 600 Ω		−4.9	−4.8	V
		−40°C < T_A < +125°C			−4.4	V
Short-Circuit Current	I_{SC}			±63		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±18 V	106	125		dB
		−40°C < T_A < +125°C	103			dB
Supply Current/Amplifier	I_S	I_{OUT} = 0 mA		1.5	1.7	mA
		−40°C < T_A < +125°C			1.85	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = 100		15.4		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = −10		9.3		MHz
Phase Margin	φ_M			61		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		10.6		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.45		µV p-p
Voltage Noise Density	e_n	f = 10 Hz		14		nV/√Hz
		f = 100 Hz		8.2		nV/√Hz
		f = 1 kHz		7.3		nV/√Hz
		f = 10 kHz		7.3		nV/√Hz

[1] Offset voltage does not include solder heat resistance.
[2] Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade)[1]	V_{OS}			0.2	0.4	mV
		−40°C < T_A < +125°C			0.8	mV
Offset Voltage (A Grade)[1]	V_{OS}			0.4	1	mV
		−40°C < T_A < +125°C			1.8	mV
Offset Voltage Drift (B Grade)[2]	$\Delta V_{OS}/\Delta T$			0.5	4	µV/°C
Offset Voltage Drift (A Grade)[2]	$\Delta V_{OS}/\Delta T$			1	8	µV/°C
Input Bias Current	I_B			5	25	pA
		−40°C < T_A < +125°C			1.5	nA
Input Offset Current	I_{OS}			2	20	pA
		−40°C < T_A < +125°C			0.25	nA
Input Voltage Range			−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	106	115		dB
		−40°C < T_A < +125°C	96			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_{OUT} = ±13.5 V	104	107		dB
		−40°C < T_A < +125°C	91			dB
Input Impedance, Differential		V_{CM} = 0 V		3.1		pF
Input Impedance, Common-Mode		V_{CM} = 0 V		4.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	14.8	14.9		V
		−40°C < T_A < +125°C	14.65			V
		R_L = 600 Ω	14.25	14.47		V
		−40°C < T_A < +125°C	13.35			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−14.9	−14.85	V
		−40°C < T_A < +125°C			−14.75	V
		R_L = 600 Ω		−14.68	−14.6	V
		−40°C < T_A < +125°C			−14.3	V
Short-Circuit Current	I_{SC}			±79		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±4.5 V to ±18 V	100	125		dB
		−40°C < T_A < +125°C	103			dB
Supply Current/Amplifier	I_{SY}	I_{OUT} = 0 mA		1.6	1.85	mA
		−40°C < T_A < +125°C			2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	±17[2]	+25/−61		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = 100		16.3		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 2 kΩ, A_V = −10		9.3		MHz
Phase Margin	φ_M			66		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		9.50		MHz
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, G = +1, R_L = 2 kΩ, V_{IN} = 6 V rms		0.00006		%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		0.45		μV p-p
Voltage Noise Density	e_n	f = 10 Hz		14		nV/√Hz
		f = 100 Hz		8.5		nV/√Hz
		f = 1 kHz		7.3		nV/√Hz
		f = 10 kHz		7.3		nV/√Hz

[1] Offset voltage does not include solder heat resistance.
[2] Guaranteed by design and characterization.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_S$
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Electrostatic Discharge (Human Body Model)	2500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	°C/W
8-Lead SOIC_N (R-8)	120	43	°C/W
8-Lead LFCSP_VD (CP-8-9)	57	12	°C/W

[1] θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

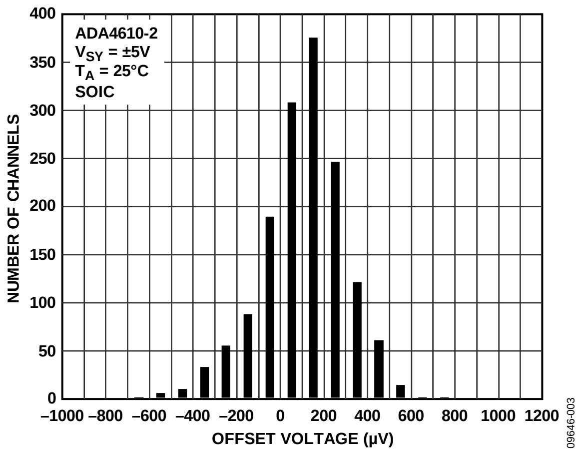

Figure 3. Input Offset Voltage Distribution

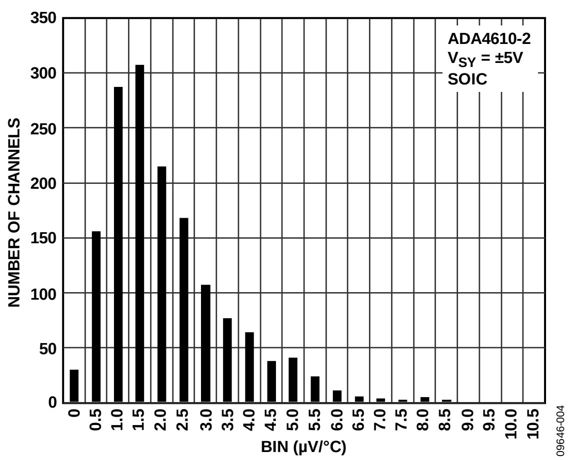

Figure 4. T_CV_{OS} Distribution

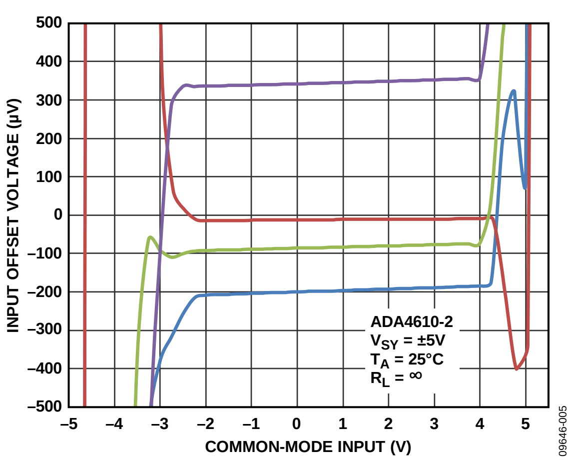

Figure 5. Input Offset Voltage vs. Common-Mode Input Voltage

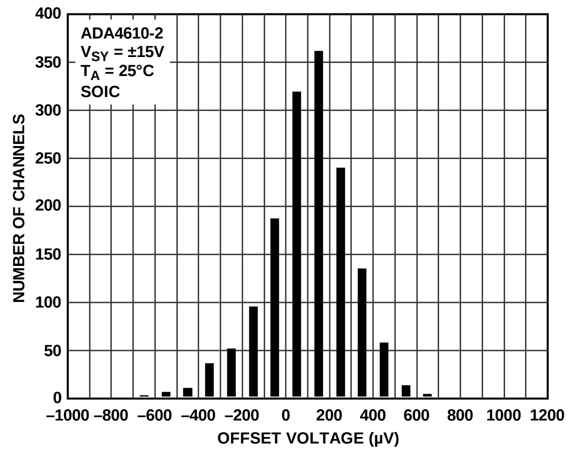

Figure 6. Input Offset Voltage Distribution

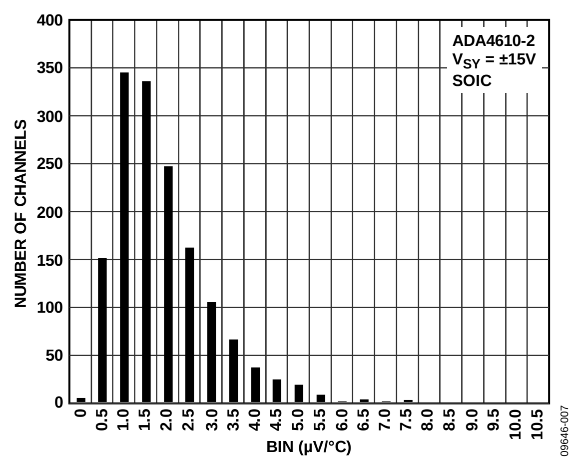

Figure 7. T_CV_{OS} Distribution

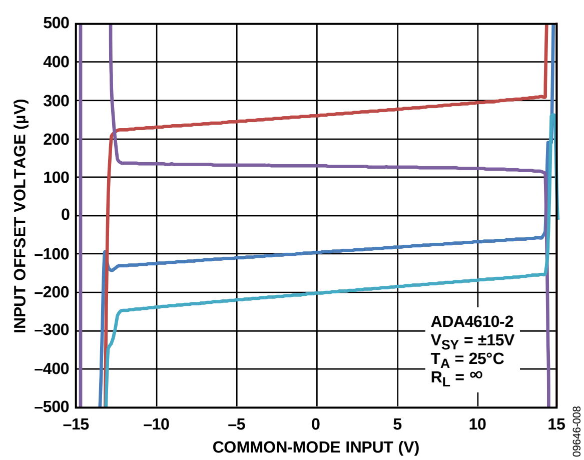

Figure 8. Input Offset Voltage vs. Common-Mode Input Voltage

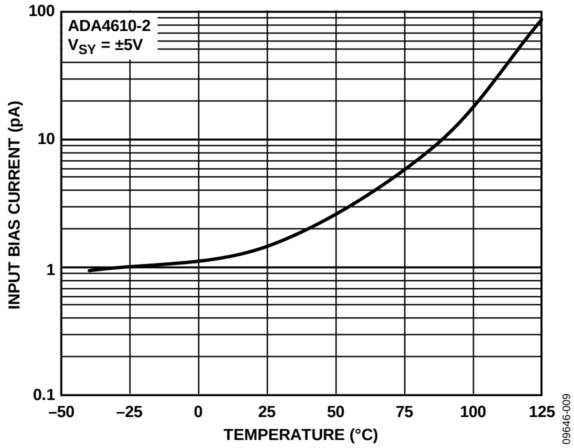

Figure 9. Input Bias Current vs. Temperature

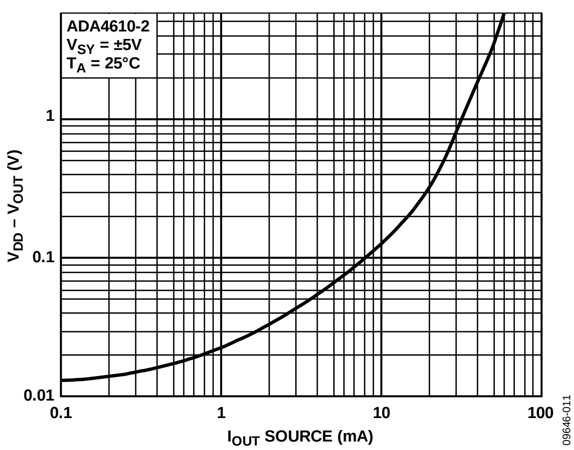

Figure 10. Dropout Voltage vs. Source Current

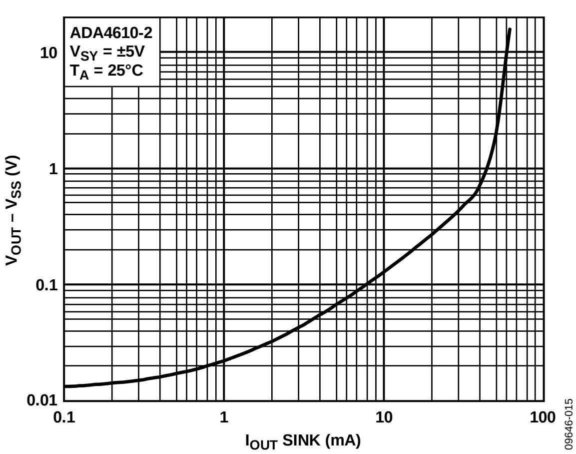

Figure 11. Dropout Voltage vs. Sink Current

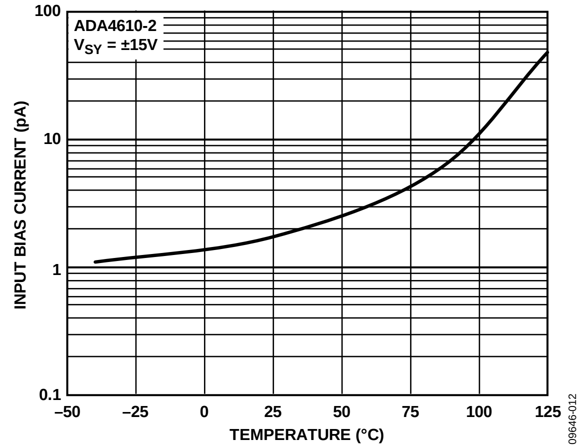

Figure 12. Input Bias Current vs. Temperature

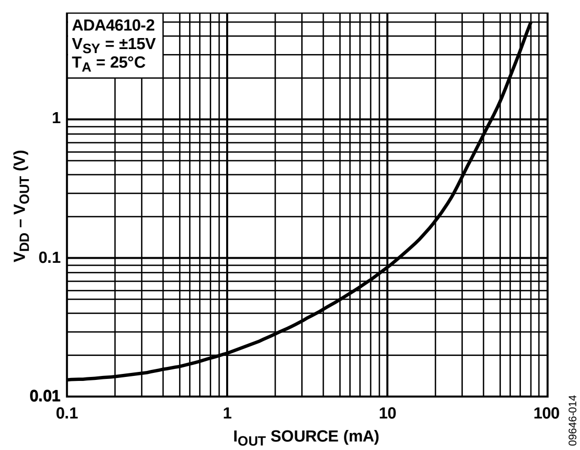

Figure 13. Dropout Voltage vs. Source Current

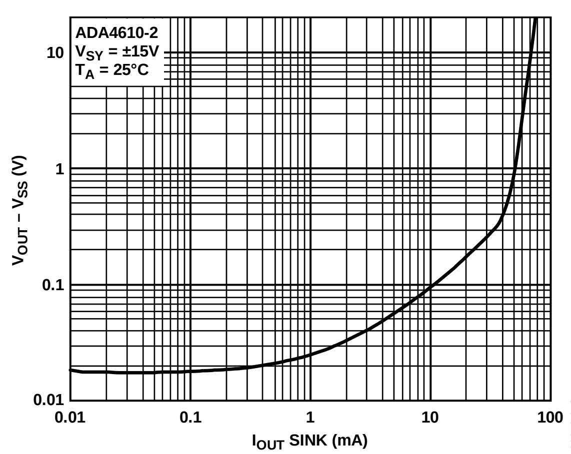

Figure 14. Dropout Voltage vs. Sink Current

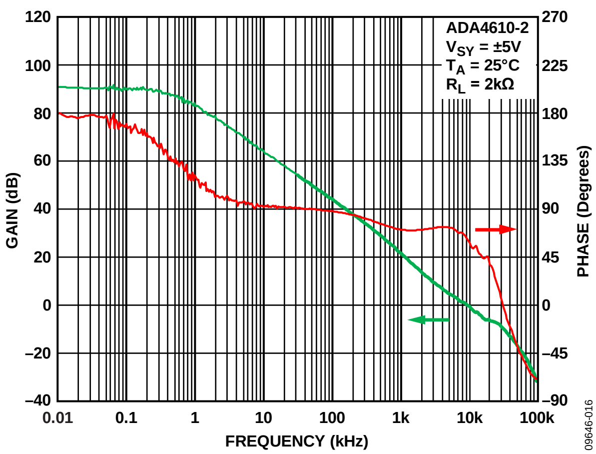

Figure 15. Open-Loop Gain and Phase vs. Frequency

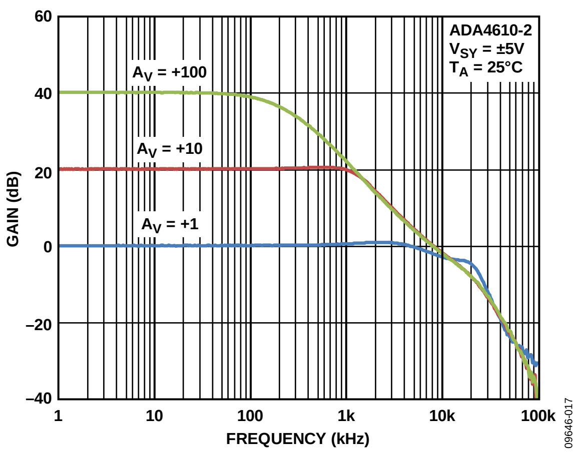

Figure 16. Closed-Loop Gain vs. Frequency

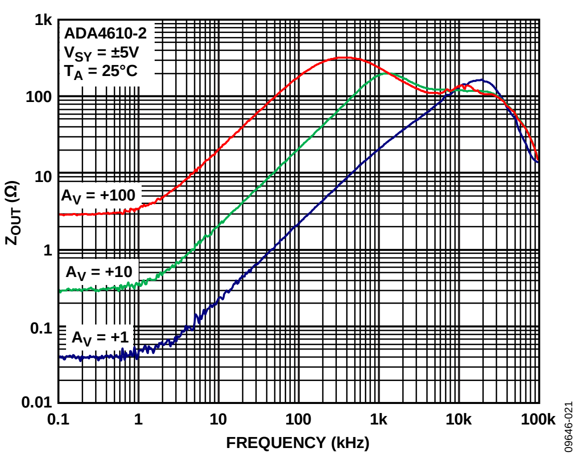

Figure 17. Closed-Loop Output Impedance vs. Frequency

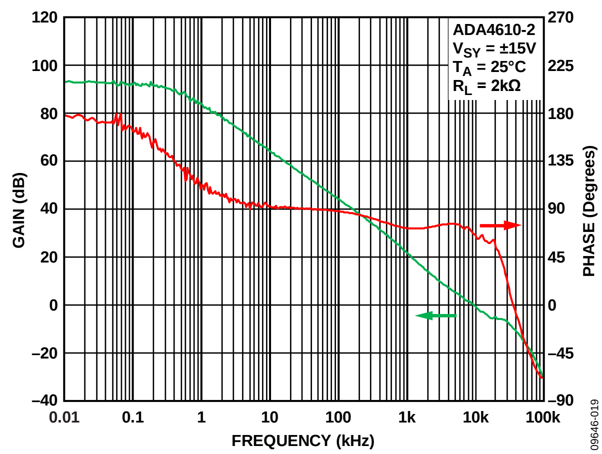

Figure 18. Open-Loop Gain and Phase vs. Frequency

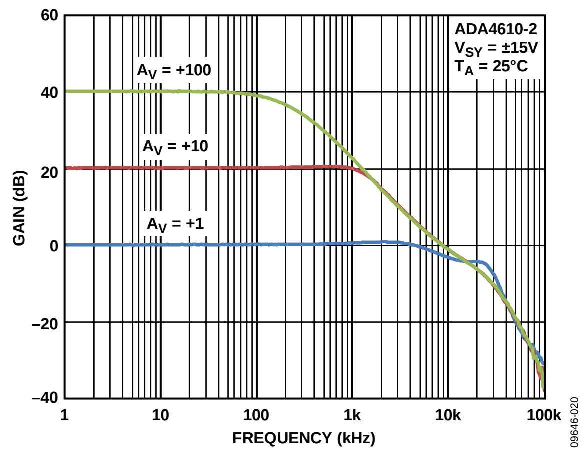

Figure 19. Closed-Loop Gain vs. Frequency

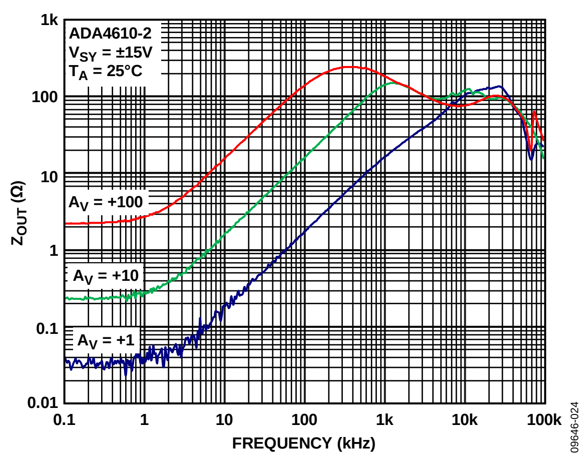

Figure 20. Closed-Loop Output Impedance vs. Frequency

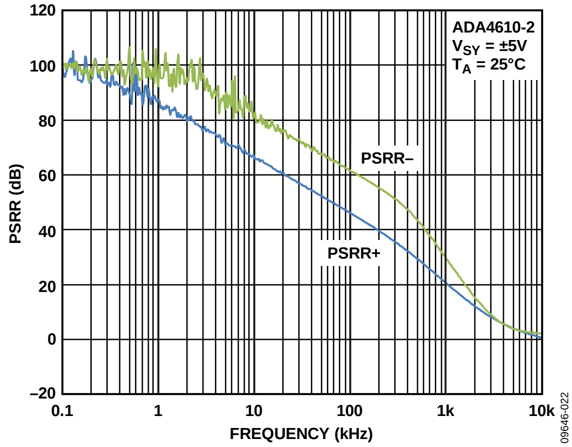

Figure 21. PSRR vs. Frequency

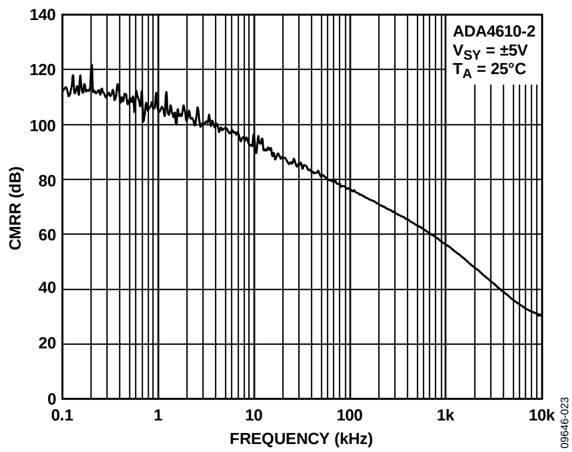

Figure 22. CMRR vs. Frequency

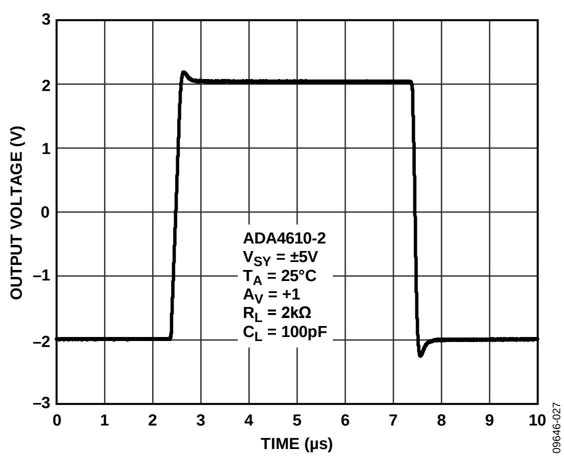

Figure 23. Large Signal Transient Response

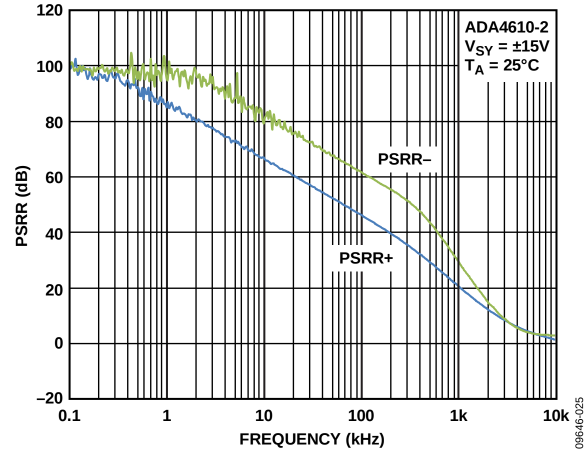

Figure 24. PSRR vs. Frequency

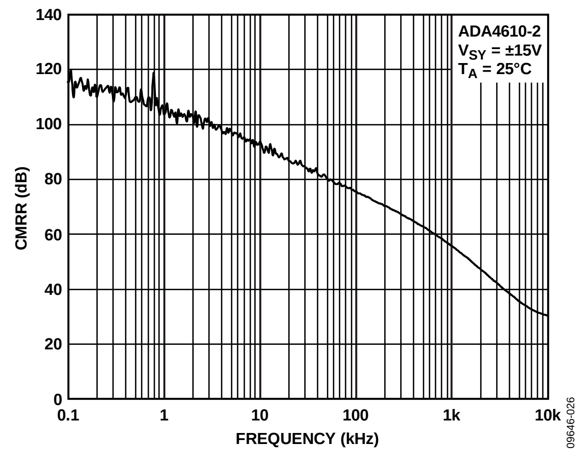

Figure 25. CMRR vs. Frequency

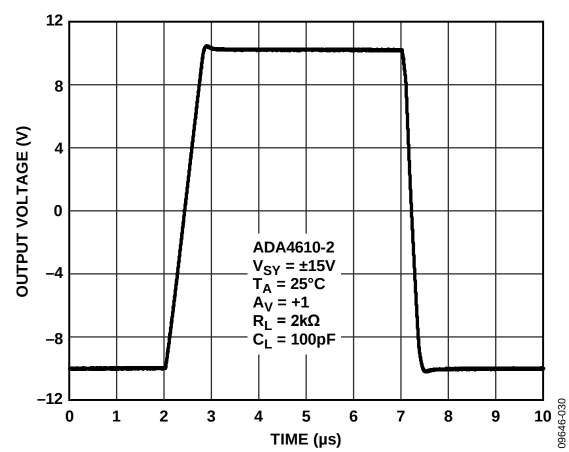

Figure 26. Large Signal Transient Response

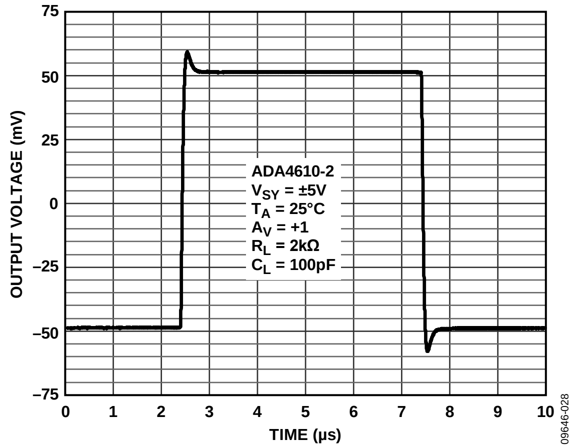

Figure 27. Small Signal Transient Response

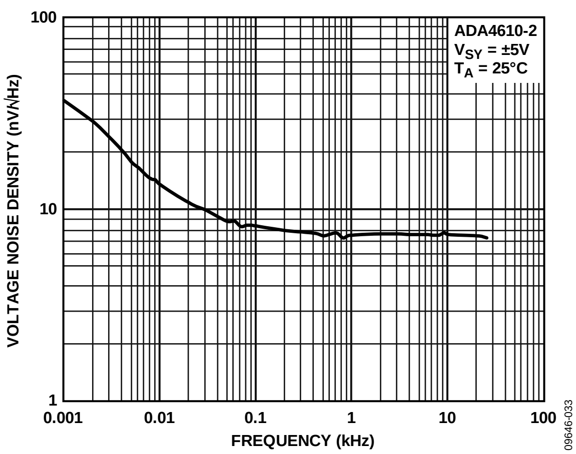

Figure 28. Voltage Noise Density

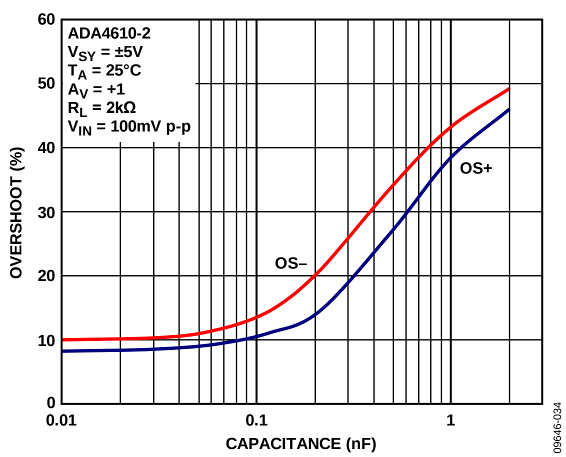

Figure 29. Overshoot vs. Load Capacitance

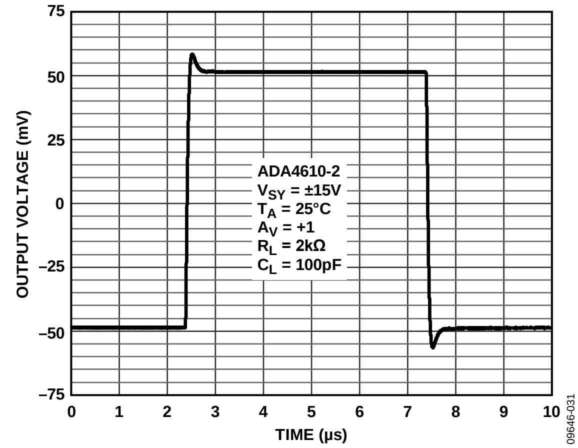

Figure 30. Small Signal Transient Response

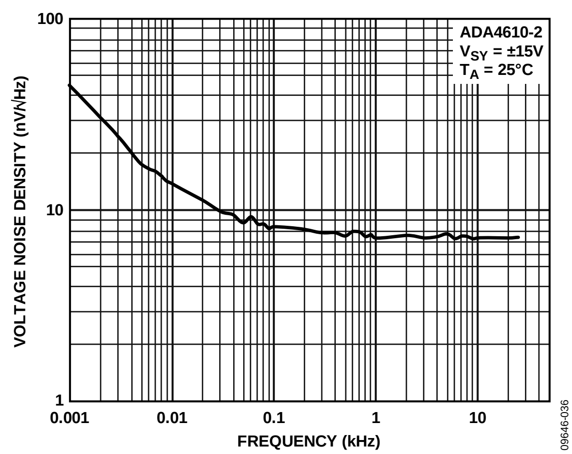

Figure 31. Voltage Noise Density

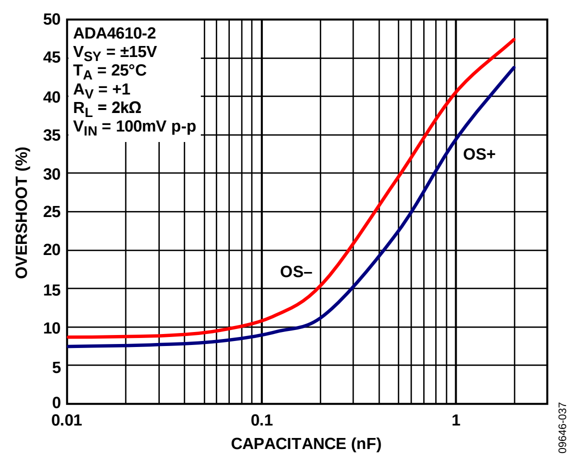

Figure 32. Overshoot vs. Load Capacitance

COMPARATIVE VOLTAGE AND VARIABLE VOLTAGE GRAPHS

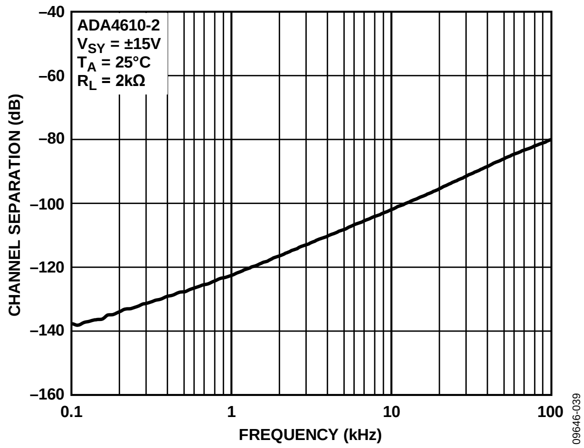

Figure 33. Channel Separation

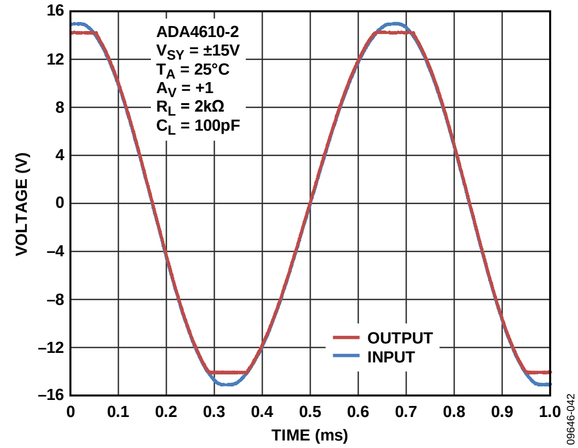

Figure 36. No Phase Reversal

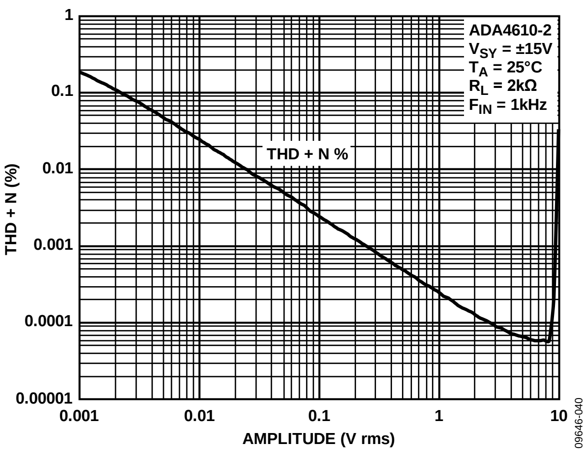

Figure 34. THD + N vs. Amplitude

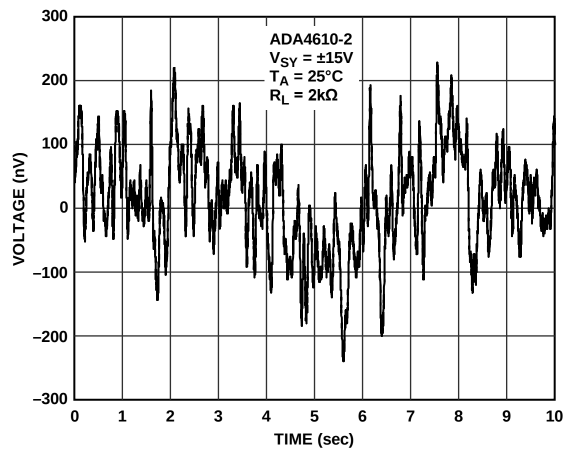

Figure 37. Voltage Noise, 0.1 Hz to 10 Hz

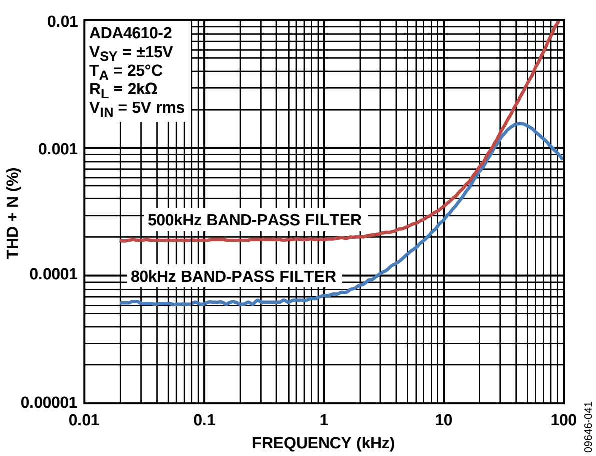

Figure 35. THD + N vs. Frequency

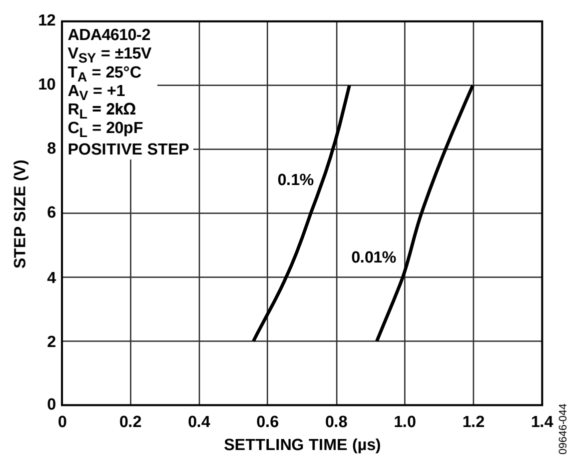

Figure 38. Positive Step Settling Time

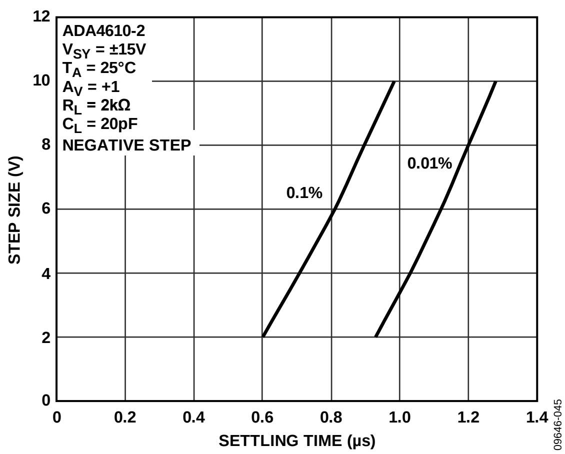

Figure 39 Negative Step Settling Time

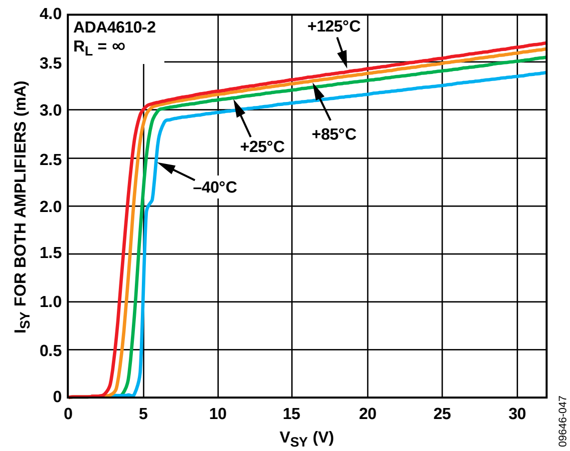

Figure 40. Supply Current vs. Supply Voltage and Temperature

APPLICATIONS INFORMATION

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp may be used as a comparator; however, this is not recommended for any rail-to-rail output op amp. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop. However, the second stage cannot close the loop, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 41). Configuring an unused section as a voltage follower with the noninverting input connected to a voltage within the input voltage range is recommended. The ADA4610-2 has a unique output stage design that reduces the excess supply current, but does not entirely eliminate this effect when the op amp is operating open loop.

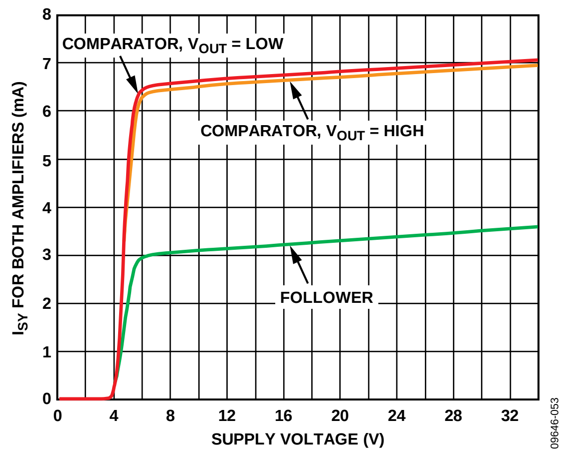

Figure 41. Supply Current vs. Supply Voltage

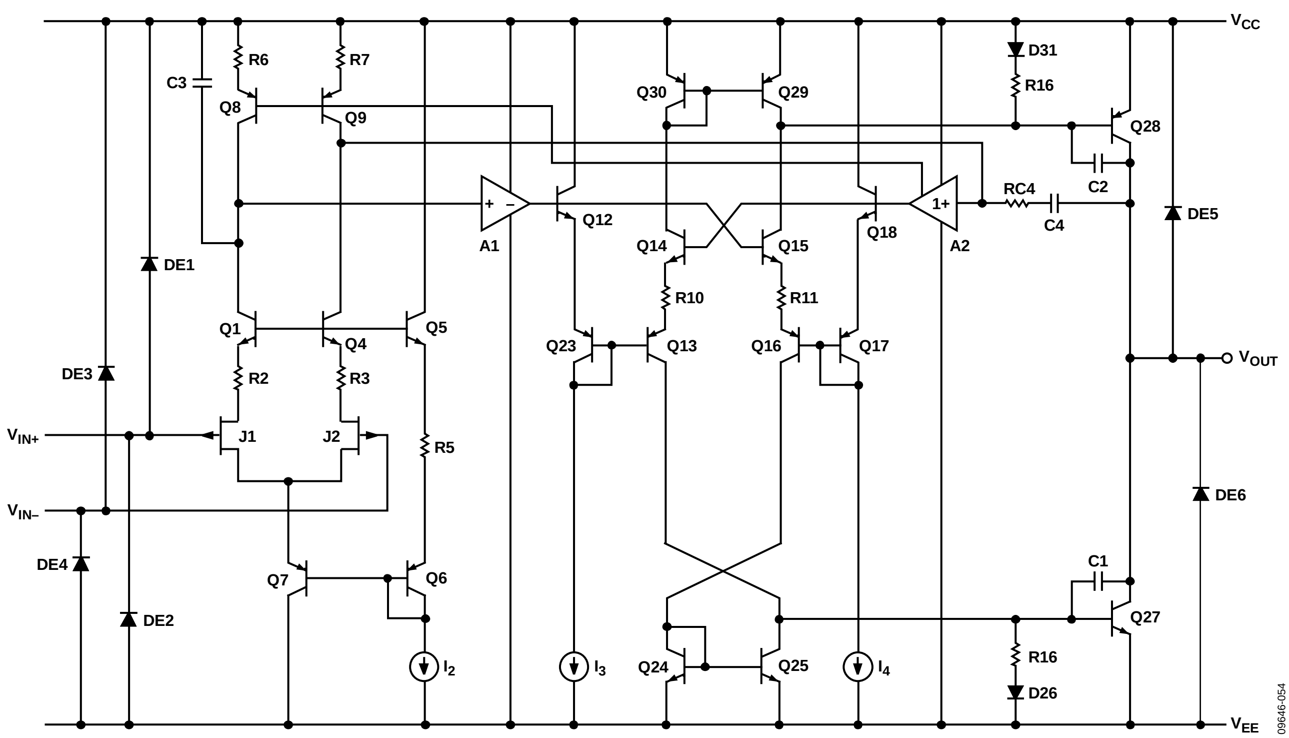

Figure 42. Simplified Schematic

OUTLINE DIMENSIONS

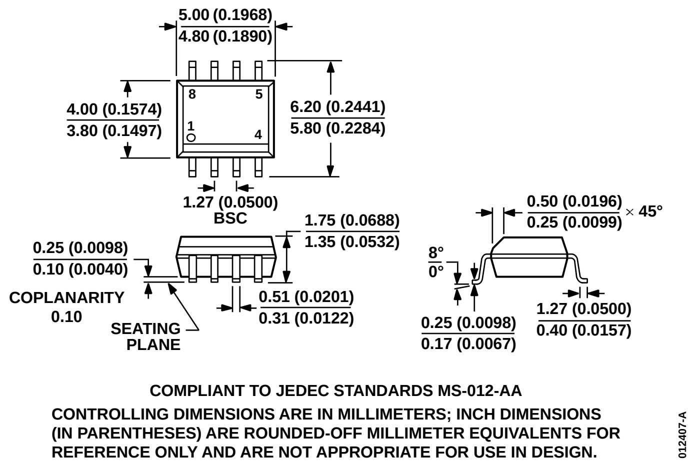

Figure 43. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

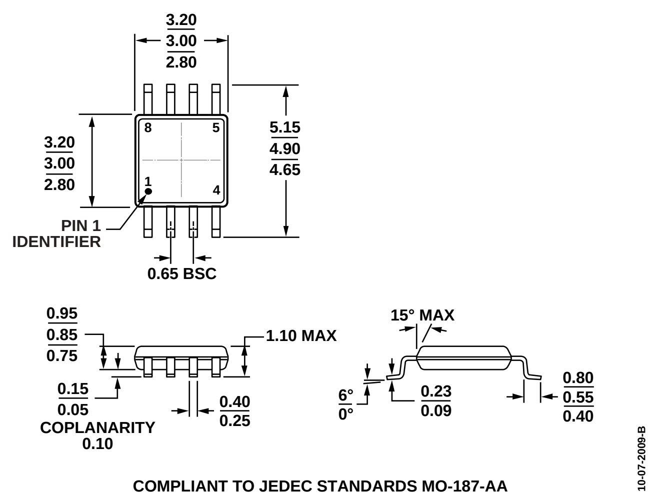

Figure 44. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

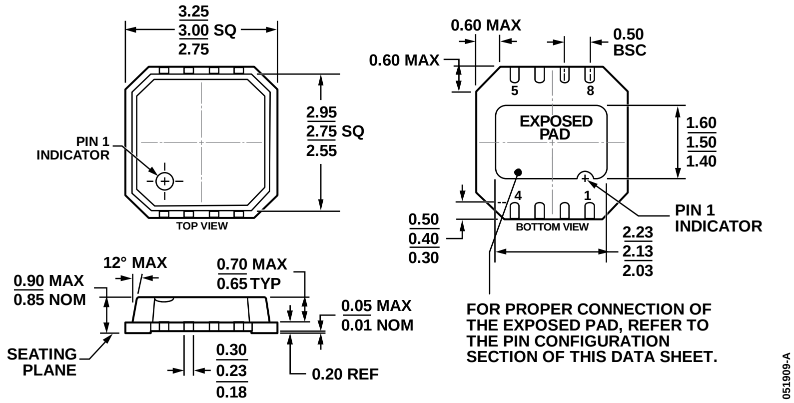

Figure 45. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4610-2ACPZ-R7	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-9	A2U
ADA4610-2ACPZ-RL	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-9	A2U
ADA4610-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	A2U
ADA4610-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP	RM-8	A2U
ADA4610-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2BRZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2BRZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

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