Low Noise and Distortion, Rail-to-Rail Output Amplifier

Known Good Die

ADA4841-2KGD

FEATURES

- Low power: 1.1 mA/amplifier
- Low wideband noise
  - 2.1 nV/√Hz
  - 1.4 pA/√Hz
- Low 1/f noise
  - 7 nV/√Hz at 10 Hz
  - 13 pA/√Hz at 10 Hz
- Low distortion: −105 dBc at 100 kHz, V_O = 2 V p-p
- High speed
  - 80 MHz, −3 dB bandwidth (G = +1)
  - 12 V/µs slew rate
  - 175 ns settling time to 0.1%
- Low offset voltage: 0.3 mV maximum
- Rail-to-rail output
- Wide supply range: 2.7 V to 12 V
- Known good die (KGD): these die are fully guaranteed to data sheet specifications

APPLICATIONS

- Low power, low noise signal processing
- Battery-powered instrumentation
- 16-bit PulSAR® ADC drivers

FUNCTIONAL BLOCK DIAGRAM

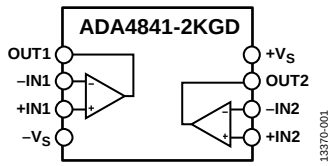

Figure 1.

GENERAL DESCRIPTION

The ADA4841-2KGD is a unity-gain stable, low noise and distortion, rail-to-rail output amplifier that has a quiescent current of 1.5 mA maximum. Its low power consumption notwithstanding, this amplifier offers low wideband voltage noise performance of 2.1 nV/√Hz and 1.4 pA/√Hz current noise, along with excellent spurious-free dynamic range (SFDR) of −105 dBc at 100 kHz. To maintain a low noise environment at lower frequencies, the amplifier has low 1/f noise of 7 nV/√Hz and 13 pA/√Hz at 10 Hz.

The ADA4841-2KGD output can swing to less than 50 mV of either rail. The input common-mode voltage range extends down to the negative supply. The ADA4841-2KGD can drive up to 10 pF of capacitive load with minimal peaking.

The ADA4841-2KGD provides the performance required to efficiently support emerging 16-bit to 18-bit ADCs and is ideal for portable instrumentation, high channel count, industrial measurement, and medical applications. The ADA4841-2KGD is ideally suited to drive the AD7685/AD7686, 16-bit PulSAR ADCs.

Additional application and technical information can be found in the ADA4841-2 data sheet.

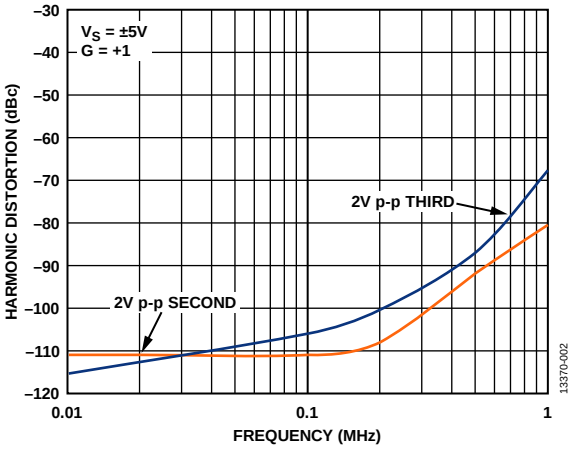

Figure 2. Harmonic Distortion

Rev. 0 Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

9/15—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, R_L = 1 kΩ, G = +1, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.02 V p-p		80		MHz
	V_O = 2 V p-p		3		MHz
Slew Rate	G = +1, V_O = 9 V step, R_L = 1 kΩ		13		V/µs
Settling Time to 0.1%	G = +1, V_O = 8 V step		650		ns
Settling Time to 0.01%	G = +1, V_O = 8 V step		1000		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 100 kHz, V_O = 2 V p-p, G = +1		−111/−105		dBc
	f_C = 1 MHz, V_O = 2 V p-p		−80/−67		dBc
Input Voltage Noise	f = 100 kHz		2.1		nV/√Hz
Input Current Noise	f = 100 kHz		1.4		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			40	300	µV
Input Offset Voltage Drift			1		µV/°C
Input Bias Current			3	5.3	µA
Input Offset Current			0.1	0.5	µA
Open-Loop Gain	V_O = ±4 V	103	120		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			90		MΩ
Differential Mode			25		kΩ
Input Capacitance					
Common Mode			1		pF
Differential Mode			3		pF
Input Common-Mode Voltage Range		−5.1		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = Δ4 V	95	115		dB
MATCHING CHARACTERISTICS					
Input Offset Voltage			70		µV
Input Bias Current			60		nA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	G > +1	±4.9	±4.955		V
Output Current Limit	Sourcing, V_{IN} = +V_S, R_L = 50 Ω to GND		30		mA
	Sinking, V_{IN} = −V_S, R_L = 50 Ω to GND		60		mA
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			1.2	1.5	mA
Positive Power Supply Rejection Ratio	+V_S = +5 V to +6 V, −V_S = −5 V	95	110		dB
Negative Power Supply Rejection Ratio	+V_S = +5 V, −V_S = −5 V to −6 V	96	120		dB

5 V SUPPLY

T_A = 25°C, R_L = 1 kΩ, G = +1, V_{CM} = 2.5 V, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.02 V p-p		80		MHz
	V_O = 2 V p-p		3		MHz
Slew Rate	G = +1, V_O = 4 V step, R_L = 1 kΩ		12		V/µs
Settling Time to 0.1%	G = +1, V_O = 2 V step		175		ns
Settling Time to 0.01%	G = +1, V_O = 2 V step		550		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 100 kHz, V_O = 2 V p-p		−109/−105		dBc
	f_C = 1 MHz, V_O = 2 V p-p		−78/−66		dBc
Input Voltage Noise	f = 100 kHz		2.1		nV/√Hz
Input Current Noise	f = 100 kHz		1.4		pA/√Hz
Crosstalk	f = 100 kHz		−117		dB
DC PERFORMANCE					
Input Offset Voltage			40	300	µV
Input Offset Voltage Drift			1		µV/°C
Input Bias Current			3	5.3	µA
Input Offset Current			0.1	0.4	µA
Open-Loop Gain	V_O = 0.5 V to 4.5 V	103	124		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			90		MΩ
Differential Mode			25		kΩ
Input Capacitance					
Common Mode			1		pF
Differential Mode			3		pF
Input Common-Mode Voltage Range		−0.1		+4	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = Δ1.5 V	88	115		dB
MATCHING CHARACTERISTICS					
Input Offset Voltage			70		µV
Input Bias Current			70		nA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	G > +1	0.08 to 4.92	0.029 to 4.974		V
Output Current Limit	Sourcing, V_{IN} = +V_S, R_L = 50 Ω to V_{CM}		30		mA
	Sinking, V_{IN} = −V_S, R_L = 50 Ω to V_{CM}		60		mA
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			1.1	1.4	mA
Positive Power Supply Rejection Ratio	+V_S = +5 V to +6 V, −V_S = 0 V	95	110		dB
Negative Power Supply Rejection Ratio	+V_S = +5 V, −V_S = 0 V to −1 V	96	120		dB

3 V SUPPLY

T_A = 25°C, R_L = 1 kΩ, G =+1, V_{CM} = 1.5 V, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	V_O = 0.02 V p-p		80		MHz
Slew Rate	G = +1, V_O = 2 V step, R_L = 1 kΩ		12		V/µs
Settling Time to 0.1%	G = +1, V_O = 1 V step		120		ns
Settling Time to 0.01%	G = +1, V_O = 1 V step		250		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion HD2/HD3	f_C = 100 kHz, V_O = 1 V p-p		−97/−100		dBc
	f_C = 1 MHz, V_O = 1 V p-p		−79/−80		dBc
Input Voltage Noise	f = 100 kHz		2.1		nV/√Hz
Input Current Noise	f = 100 kHz		1.4		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			40	300	µV
Input Offset Voltage Drift			1		µV/°C
Input Bias Current			3	5.3	µA
Input Offset Current			0.1	0.5	µA
Open-Loop Gain	V_O = 0.5 V to 2.5 V	101	123		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			90		MΩ
Differential Mode			25		kΩ
Input Capacitance					
Common Mode			1		pF
Differential Mode			3		pF
Input Common-Mode Voltage Range		−0.1		+2	V
Common-Mode Rejection Ratio (CMRR)	V_{CM} = Δ0.4 V	86	115		dB
MATCHING CHARACTERISTICS					
Input Offset Voltage			70		µV
Input Bias Current			60		nA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	G > +1	0.045 to 2.955	0.023 to 2.988		V
Output Current Limit	Sourcing, V_{IN} = +V_S, R_L = 50 Ω to V_{CM}		30		mA
	Sinking, V_{IN} = −V_S, R_L = 50 Ω to V_{CM}		60		mA
Capacitive Load Drive	30% overshoot		30		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			1.1	1.3	mA
Positive Power Supply Rejection Ratio	+V_S = +3 V to +4 V, −V_S = 0 V	95	110		dB
Negative Power Supply Rejection Ratio	+V_S = +3 V, −V_S = 0 V to −1 V	96	120		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Common-Mode Input Voltage	$-V_S - 0.5$ V to $+V_S + 0.5$ V
Differential Input Voltage	±1.8 V
Storage Temperature Range	−65°C to +125°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

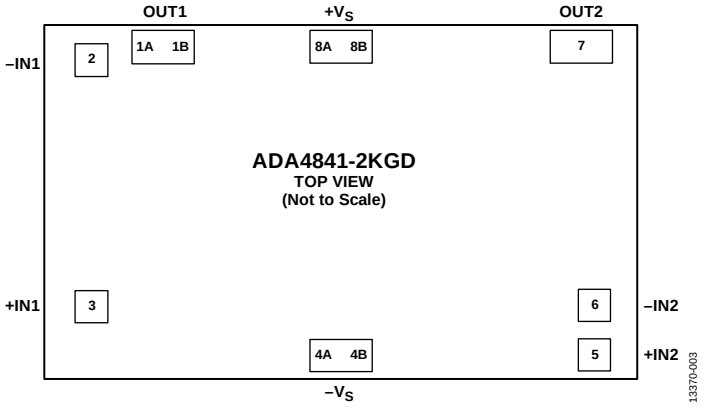

Figure 3. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	X-Axis	Y-Axis	Mnemonic	Description
1A,1B	−463, −393	+363	OUT1	Output 1, Double Bond Pad
2	−597	+334	−IN1	Inverting Input 1
3	−597	−250	+IN1	Noninverting Input 1
4A, 4B	−36, +35	−363	$-V_S$	Negative Supply, Double Bond Pad
5	+603	−363	+IN2	Noninverting Input 2
6	+603	−245	−IN2	Inverting Input 2
7	+568	+363	OUT2	Output 2
8A, 8B	−36, +35	+363	$+V_S$	Positive Supply, Double Bond Pad

OUTLINE DIMENSIONS

Figure 4. 8-Pad Bare Die [CHIP]
(C-8-4)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Scribe Line Width	75	µm
Die Size (Maximum Size)	1525 × 940	µm
Thickness	305	µm
Bond Pads (Minimum Size)	70 × 70	µm
Bond Pad Composition	0.5% AlCu	%
Backside	SOI	Not applicable
Passivation	Doped-oxide/SiN	Not applicable
ESD, Human Body Model (HBM)	2000	V

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Ablestik 84-1LMIS R4
Bonding Method	1 mil gold

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADA4841-2KGD-WP	–40°C to +125°C	8-Pad Bare Die [CHIP]	C-8-4