

FEATURES

- 32-channel, low level current-to-digital converter**
- Up to 24-bit resolution**
- Up to 19.7 kSPS (50.7 μ s integration time)**
- Simultaneous sampling**
- Ultralow noise (down to 0.4 fC [2500e⁻])**
- User-adjustable full-scale range**
- INL: $\pm 0.025\%$ of reading ± 0.75 ppm of FSR**
- Very low power dissipation: 12.5 mW/channel**
- LVDS self-clocked serial data interface**
- SPI configuration registers (daisy-chain)**
- On-board temperature sensor and reference buffer**
- 10 mm $\times$ 10 mm, mini-BGA package**
- Low cost external components**
- Support tools**
 - Evaluation board
 - Reference design with reference layout
 - FPGA Verilog code

APPLICATIONS

- Medical, industrial, and security CT scanner data acquisition
- Photodiode sensors
- Dosimetry and radiation therapy systems
- Optical fiber power monitoring
- X-ray detection systems
- High channel-count data acquisition systems (current or voltage inputs)

GENERAL DESCRIPTION

The [ADAS1126](#) is a 32-channel, current-to-digital, analog-to-digital converter (ADC). It contains 32 low power, low noise, low input current integrators, simultaneous sample-and-holds, and a high speed, high resolution ADCs with configurable sampling rate and resolutions up to 24 bits.

All converted channel results are output on a single LVDS self-clocked serial interface, which reduces external hardware.

An SPI-compatible serial interface allows configuration of the ADC using the SDI input. The SDO output allows the user to daisy-chain several ADCs on a single, 3-wire bus. The [ADAS1126](#) uses the separate supply IOVDD to reduce the digital noise effect on the conversions.

The [ADAS1126](#) is in a 10 mm $\times$ 10 mm, mini-BGA package.

FUNCTIONAL BLOCK DIAGRAM

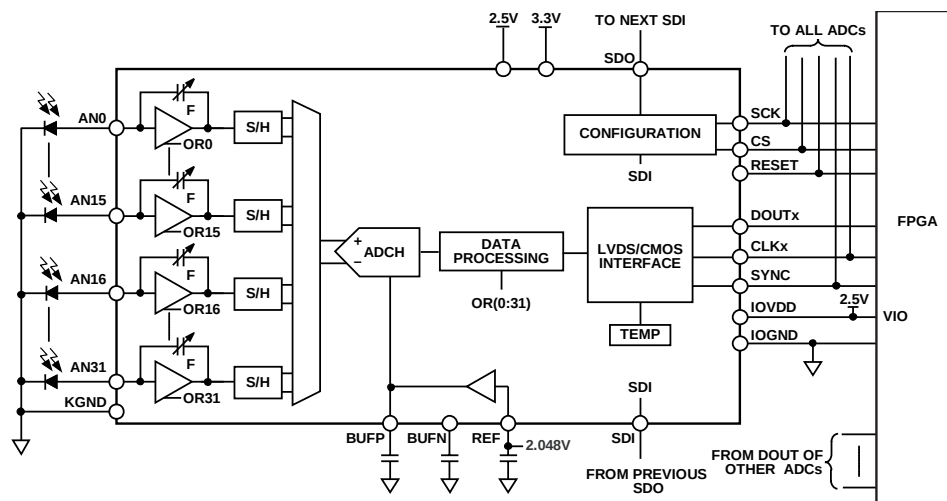


Figure 1.

For more information about the [ADAS1126](#), email: adas@analog.com.

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