

### FEATURES

- 6.0 GHz bandwidth
- 2.7 V to 3.3 V power supply
- Separate charge pump supply ( $V_P$ ) allows extended tuning voltage in 3 V systems
- Programmable dual-modulus prescaler  
8/9, 16/17, 32/33, 64/65
- Programmable charge pump currents
- Programmable antibacklash pulse width
- 3-wire serial interface
- Analog and digital lock detect
- Hardware and software power-down mode
- Support defense and aerospace applications (AQEC)
- Military temperature range ( $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ )
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available upon request

### APPLICATIONS

- Broadband wireless access
- Satellite systems
- Instrumentation
- Wireless LANS
- Base stations for wireless radios

### GENERAL DESCRIPTION

The ADF4106-EP frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A counter and B counter, and a dual-modulus prescaler ( $P/P + 1$ ). The A (6-bit) counter and B (13-bit) counter, in conjunction with the dual-modulus prescaler ( $P/P + 1$ ), implement an N divider ( $N = BP + A$ ). In addition, the 14-bit reference counter (R counter) allows selectable  $\text{REF}_{\text{IN}}$  frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). Its very high bandwidth means that frequency doublers can be eliminated in many high frequency systems, simplifying system architecture and reducing cost.

Additional application and technical information can be found in the [ADF4106](#) data sheet.

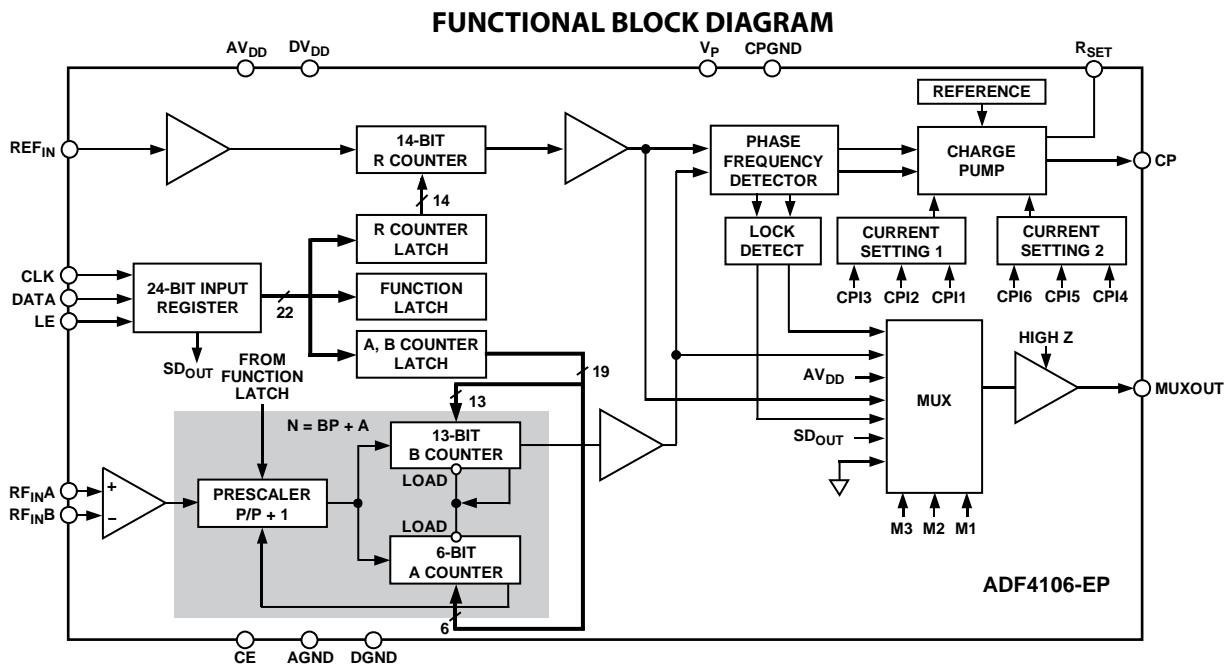


Figure 1.

#### Rev. A

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## REVISION HISTORY

### 11/10—Rev. 0 to Rev. A

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### 8/10—Revision 0: Initial Version

## SPECIFICATIONS

$AV_{DD} = DV_{DD} = 3\text{ V} \pm 10\%$ ,  $AV_{DD} \leq V_P \leq 5.5\text{ V}$ ,  $AGND = DGND = CPGND = 0\text{ V}$ ,  $R_{SET} = 5.1\text{ k}\Omega$ , dBm referred to  $50\ \Omega$ ,  $T_A = T_{MAX}$  to  $T_{MIN}$ , unless otherwise noted.

Table 1.

Parameter	B Version <sup>1</sup>	Unit	Test Conditions/Comments
<b>RF CHARACTERISTICS</b>			
RF Input Frequency (RF <sub>IN</sub> )	0.5/6.0	GHz min/max	For lower frequencies, ensure slew rate (SR) > 320 V/μs
RF Input Sensitivity	-10/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency <sup>2</sup>	300	MHz max	P = 8
	325	MHz	P = 16
<b>REF<sub>IN</sub> CHARACTERISTICS</b>			
REF <sub>IN</sub> Input Frequency	20/300	MHz min/max	For f < 20 MHz, ensure SR > 50 V/μs
REF <sub>IN</sub> Input Sensitivity <sup>3</sup>	0.8/V <sub>DD</sub>	V p-p min/max	Biased at AV <sub>DD</sub> /2 <sup>4</sup>
REF <sub>IN</sub> Input Capacitance	10	pF max	
REF <sub>IN</sub> Input Current	±100	μA max	
<b>PHASE DETECTOR</b>			
Phase Detector Frequency <sup>5</sup>	104	MHz max	ABP = 0, 0 (2.9 ns antbacklash pulse width)
<b>CHARGE PUMP</b>			
I <sub>CP</sub> Sink/Source			
High Value	5	mA typ	With R <sub>SET</sub> = 5.1 kΩ
Low Value	625	μA typ	
Absolute Accuracy	2.5	% typ	With R <sub>SET</sub> = 5.1 kΩ
R <sub>SET</sub> Range	3.0/11	kΩ typ	
I <sub>CP</sub> Three-State Leakage	2	nA max	1 nA typical; T <sub>A</sub> = 25°C
Sink and Source Current Matching	2	% typ	0.5 V ≤ V <sub>CP</sub> ≤ V <sub>P</sub> - 0.5 V
I <sub>CP</sub> vs. V <sub>CP</sub>	1.5	% typ	0.5 V ≤ V <sub>CP</sub> ≤ V <sub>P</sub> - 0.5 V
I <sub>CP</sub> vs. Temperature	2	% typ	V <sub>CP</sub> = V <sub>P</sub> /2
<b>LOGIC INPUTS</b>			
V <sub>IH</sub> , Input High Voltage	1.4	V min	
V <sub>IL</sub> , Input Low Voltage	0.6	V max	
I <sub>INH</sub> , I <sub>INL</sub> , Input Current	±1	μA max	
C <sub>IN</sub> , Input Capacitance	10	pF max	
<b>LOGIC OUTPUTS</b>			
V <sub>OH</sub> , Output High Voltage	1.4	V min	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
	V <sub>DD</sub> - 0.4	V min	CMOS output chosen
I <sub>OH</sub>	100	μA max	
V <sub>OL</sub> , Output Low Voltage	0.4	V max	I <sub>OL</sub> = 500 μA
<b>POWER SUPPLIES</b>			
AV <sub>DD</sub>	2.7/3.3	V min/V max	
DV <sub>DD</sub>	AV <sub>DD</sub>		
V <sub>P</sub>	AV <sub>DD</sub> /5.5	V min/V max	AV <sub>DD</sub> ≤ V <sub>P</sub> ≤ 5.5 V
I <sub>DD</sub> <sup>6</sup> (A <sub>lDD</sub> + D <sub>lDD</sub> )	11	mA max	9.0 mA typical
I <sub>DD</sub> <sup>7</sup> (A <sub>lDD</sub> + D <sub>lDD</sub> )	11.5	mA max	9.5 mA typical
I <sub>DD</sub> <sup>8</sup> (A <sub>lDD</sub> + D <sub>lDD</sub> )	13	mA max	10.5 mA typical
I <sub>P</sub>	0.4	mA max	T <sub>A</sub> = 25°C
Power-Down Mode <sup>9</sup> (A <sub>lDD</sub> + D <sub>lDD</sub> )	10	μA typ	

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Parameter	B Version <sup>1</sup>	Unit	Test Conditions/Comments
<b>NOISE CHARACTERISTICS</b>			
Normalized Phase Noise Floor (PN <sub>SYNTH</sub> ) <sup>10</sup>	-223	dBc/Hz typ	PLL loop BW = 500 kHz
Normalized 1/f Noise (PN <sub>1/f</sub> ) <sup>11</sup>	-122	dBc/Hz typ	Measured at 10 kHz offset; normalized to 1 GHz
Phase Noise Performance <sup>12</sup>			VCO output
900 MHz <sup>13</sup>	-92.5	dBc/Hz typ	1 kHz offset and 200 kHz PFD frequency
5800 MHz <sup>14</sup>	-76.5	dBc/Hz typ	1 kHz offset and 200 kHz PFD frequency
5800 MHz <sup>15</sup>	-83.5	dBc/Hz typ	1 kHz offset and 1 MHz PFD frequency
<b>Spurious Signals</b>			
900 MHz <sup>13</sup>	-90/-92	dBc typ	200 kHz/400 kHz and 200 kHz PFD frequency
5800 MHz <sup>14</sup>	-65/-70	dBc typ	200 kHz/400 kHz and 200 kHz PFD frequency
5800 MHz <sup>15</sup>	-70/-75	dBc typ	1 MHz/2 MHz and 1 MHz PFD frequency

<sup>1</sup> Operating temperature range is -55°C to +125°C.

<sup>2</sup> This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.

<sup>3</sup> AV<sub>DD</sub> = DV<sub>DD</sub> = 3 V.

<sup>4</sup> AC coupling ensures AV<sub>DD</sub>/2 bias.

<sup>5</sup> Guaranteed by design. Sample tested to ensure compliance.

<sup>6</sup> T<sub>A</sub> = 25°C; AV<sub>DD</sub> = DV<sub>DD</sub> = 3 V; P = 16; RF<sub>IN</sub> = 900 MHz.

<sup>7</sup> T<sub>A</sub> = 25°C; AV<sub>DD</sub> = DV<sub>DD</sub> = 3 V; P = 16; RF<sub>IN</sub> = 2.0 GHz.

<sup>8</sup> T<sub>A</sub> = 25°C; AV<sub>DD</sub> = DV<sub>DD</sub> = 3 V; P = 32; RF<sub>IN</sub> = 6.0 GHz.

<sup>9</sup> T<sub>A</sub> = 25°C; AV<sub>DD</sub> = DV<sub>DD</sub> = 3.3 V; R = 16383; A = 63; B = 891; P = 32; RF<sub>IN</sub> = 6.0 GHz.

<sup>10</sup> The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F<sub>PFD</sub>. PN<sub>SYNTH</sub> = PN<sub>TOT</sub> - 10 log F<sub>PFD</sub> - 20 log N.

<sup>11</sup> The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f<sub>RF</sub>, and at a frequency offset, f, is given by PN = P<sub>1/f</sub> + 10log(10 kHz/f) + 20log(f<sub>RF</sub>/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

<sup>12</sup> The phase noise is measured with the EVAL-ADF4106-EB1 evaluation board and the Agilent E4440A spectrum analyzer. The spectrum analyzer provides the REF<sub>IN</sub> for the synthesizer (f<sub>REFOUT</sub> = 10 MHz @ 0 dBm).

<sup>13</sup> f<sub>REFIN</sub> = 10 MHz; f<sub>PFD</sub> = 200 kHz; offset frequency = 1 kHz; f<sub>RF</sub> = 900 MHz; N = 4500; loop B/W = 20 kHz.

<sup>14</sup> f<sub>REFIN</sub> = 10 MHz; f<sub>PFD</sub> = 200 kHz; offset frequency = 1 kHz; f<sub>RF</sub> = 5800 MHz; N = 29,000; loop B/W = 20 kHz.

<sup>15</sup> f<sub>REFIN</sub> = 10 MHz; f<sub>PFD</sub> = 1 MHz; offset frequency = 1 kHz; f<sub>RF</sub> = 5800 MHz; N = 5800; loop B/W = 100 kHz.

## TIMING CHARACTERISTICS

AV<sub>DD</sub> = DV<sub>DD</sub> = 3 V ± 10%, AV<sub>DD</sub> ≤ V<sub>P</sub> ≤ 5.5 V, AGND = DGND = CPGND = 0 V, R<sub>SET</sub> = 5.1 kΩ, dBm referred to 50 Ω, T<sub>A</sub> = T<sub>MAX</sub> to T<sub>MIN</sub>, unless otherwise noted.

Table 2.

Parameter	Limit <sup>1</sup> (B Version)	Unit	Test Conditions/Comments
t <sub>1</sub>	10	ns min	DATA to CLOCK Setup Time
t <sub>2</sub>	10	ns min	DATA to CLOCK Hold Time
t <sub>3</sub>	25	ns min	CLOCK High Duration
t <sub>4</sub>	25	ns min	CLOCK Low Duration
t <sub>5</sub>	10	ns min	CLOCK to LE Setup Time
t <sub>6</sub>	20	ns min	LE Pulse Width

<sup>1</sup> Operating temperature range (B Version) is -40°C to +85°C.

### Timing Diagram

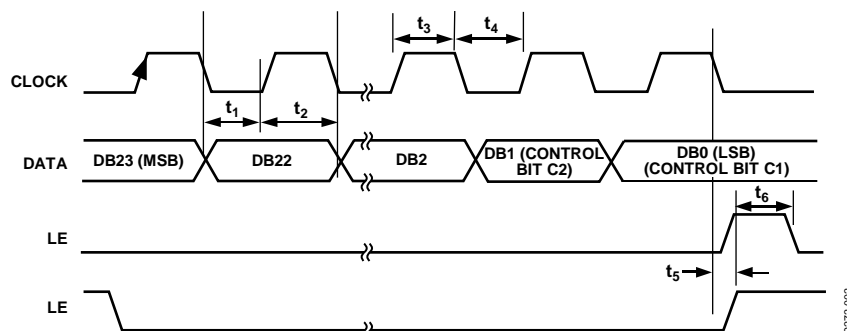


Figure 2. Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

Parameter	Rating
$AV_{DD}$ to GND <sup>1</sup>	-0.3 V to + 3.6 V
$AV_{DD}$ to $DV_{DD}$	-0.3 V to + 0.3 V
$V_P$ to GND	-0.3 V to + 5.8 V
$V_P$ to $AV_{DD}$	-0.3 V to + 5.8 V
Digital I/O Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog I/O Voltage to GND	-0.3 V to $V_P + 0.3$ V
$REF_{IN}$ , $RF_{IN}A$ , $RF_{IN}B$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
Maximum Junction Temperature	150°C
$\theta_{JA}$ Thermal Impedance	
16-Lead TSSOP	112°C/W
20-Lead LFCSP (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6425
Bipolar	303

<sup>1</sup>GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

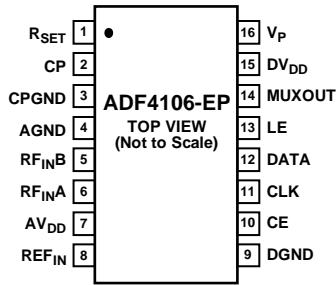
### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADF4106-EP

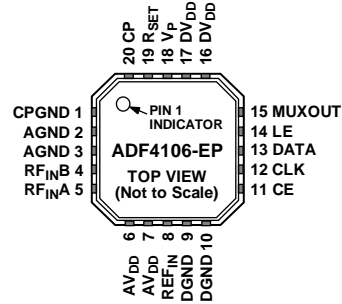
## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES:  
1. TRANSISTOR COUNT 6425 (CMOS),  
303 (BIPOLAR).

09272-003

Figure 3. 16-Lead TSSOP Pin Configuration



NOTES  
1. TRANSISTOR COUNT 6425 (CMOS),  
303 (BIPOLAR).  
2. THE EXPOSED PAD MUST BE  
CONNECTED TO AGND.

09272-004

Figure 4. 20-Lead LFCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No. TSSOP	Pin No. LFCSP	Mnemonic	Description
1	19	R <sub>SET</sub>	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R <sub>SET</sub> pin is 0.66 V. The relationship between I <sub>CP</sub> and R <sub>SET</sub> is $I_{CP\ MAX} = \frac{25.5}{R_{SET}}$ So, with R <sub>SET</sub> = 5.1 kΩ, I <sub>CP</sub> MAX = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I <sub>CP</sub> to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	RF <sub>INB</sub>	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	5	RF <sub>INA</sub>	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
7	6, 7	AV <sub>DD</sub>	Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV <sub>DD</sub> must be the same value as DV <sub>DD</sub> .
8	8	REF <sub>IN</sub>	Reference Input. This is a CMOS input with a nominal threshold of V <sub>DD</sub> /2 and a dc equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches with the latch being selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV <sub>DD</sub>	Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV <sub>DD</sub> must be the same value as AV <sub>DD</sub> .
16	18	V <sub>P</sub> EP	Charge Pump Power Supply. This should be greater than or equal to V <sub>DD</sub> . In systems where V <sub>DD</sub> is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5 V. Exposed Pad. The exposed pad must be connected to AGND.

# TYPICAL PERFORMANCE CHARACTERISTICS

FREQ UNIT	GHz	KEYWORD	R
PARAM TYPE	S	IMPEDANCE	50Ω
DATA FORMAT	MA		
FREQ	MAGS11	ANGS11	FREQ MAGS11 ANGS11
0.500	0.89148	-17.2820	3.300 0.42777 -102.748
0.600	0.88133	-20.6919	3.400 0.42859 -107.167
0.700	0.87152	-24.5386	3.500 0.43365 -111.883
0.800	0.85855	-27.3228	3.600 0.43849 -117.548
0.900	0.84911	-31.0698	3.700 0.44475 -123.856
1.000	0.83512	-34.8623	3.800 0.44800 -130.399
1.100	0.82374	-38.5574	3.900 0.45223 -136.744
1.200	0.80871	-41.9093	4.000 0.45555 -142.766
1.300	0.79176	-45.6990	4.100 0.45313 -149.269
1.400	0.77205	-49.4185	4.200 0.45622 -154.884
1.500	0.75696	-52.8898	4.300 0.45555 -159.680
1.600	0.74234	-56.2923	4.400 0.46108 -164.916
1.700	0.72239	-60.2584	4.500 0.45325 -168.452
1.800	0.69419	-63.1446	4.600 0.45054 -173.462
1.900	0.67288	-65.6464	4.700 0.45200 -176.697
2.000	0.66227	-68.0742	4.800 0.45043 178.824
2.100	0.64758	-71.3530	4.900 0.45282 174.947
2.200	0.62454	-75.5658	5.000 0.44287 170.237
2.300	0.59466	-79.6404	5.100 0.44909 166.617
2.400	0.55932	-82.8246	5.200 0.44294 162.786
2.500	0.52256	-85.2795	5.300 0.44558 158.766
2.600	0.48754	-85.6298	5.400 0.45417 153.195
2.700	0.46411	-86.1854	5.500 0.46038 147.721
2.800	0.45776	-86.4997	5.600 0.47128 139.760
2.900	0.44859	-88.8080	5.700 0.47439 132.657
3.000	0.44588	-91.9737	5.800 0.48604 125.782
3.100	0.43810	-95.4087	5.900 0.50637 121.110
3.200	0.43269	-99.1282	6.000 0.52172 115.400

Figure 5. S-Parameter Data for the RF Input

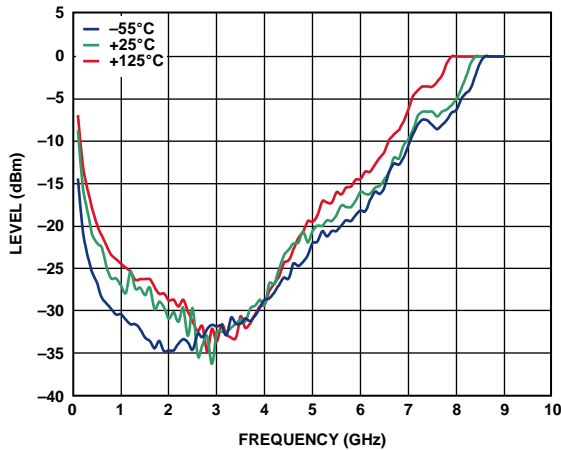


Figure 6. Input Sensitivity

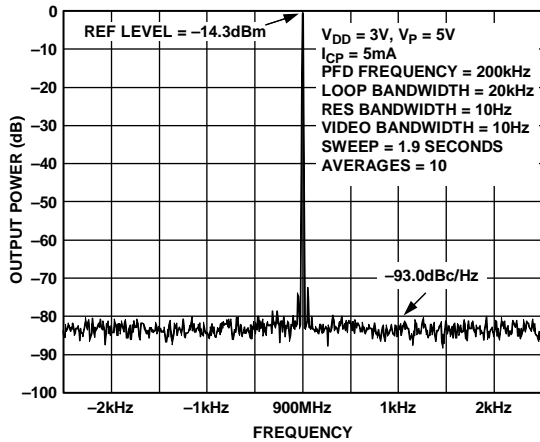


Figure 7. Phase Noise (900 MHz, 200 kHz, and 20 kHz)

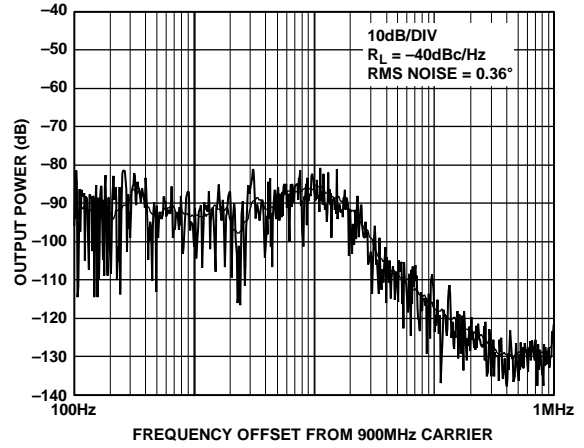


Figure 8. Integrated Phase Noise (900 MHz, 200 kHz, and 20 kHz)

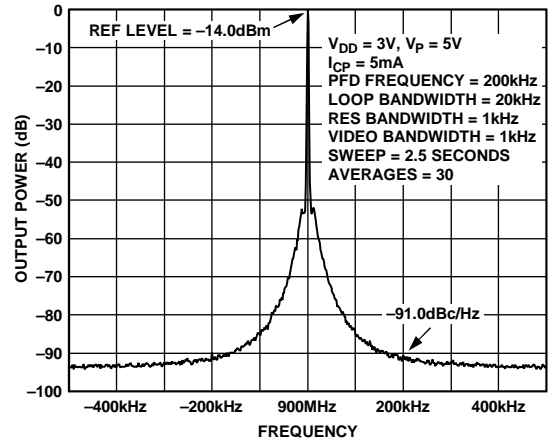


Figure 9. Reference Spurs (900 MHz, 200 kHz, and 20 kHz)

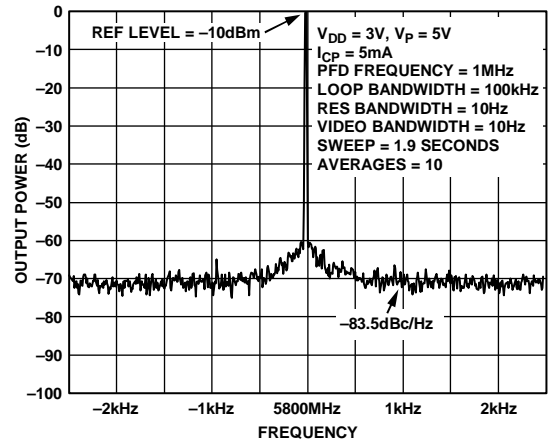


Figure 10. Phase Noise (5.8 GHz, 1 MHz, and 100 kHz)

# ADF4106-EP

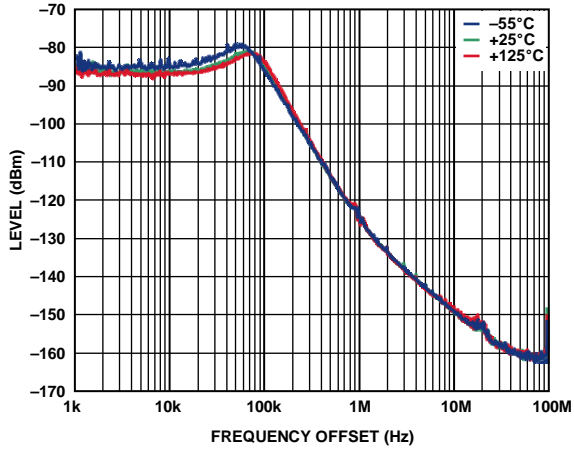


Figure 11. Integrated Phase Noise (5.8 GHz, 1 MHz, and 100 kHz)

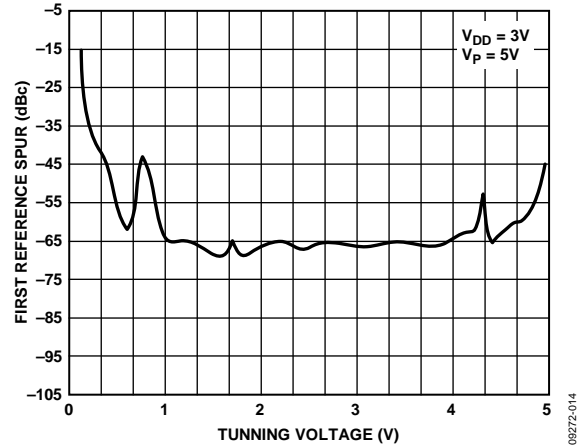


Figure 14. Reference Spurs vs.  $V_{TUNE}$  (5.8 GHz, 1 MHz, and 100 kHz)

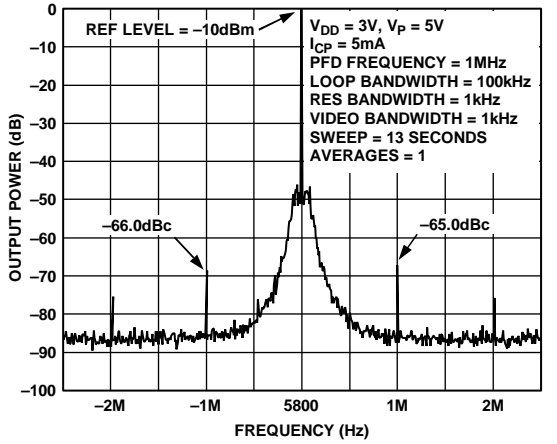


Figure 12. Reference Spurs (5.8 GHz, 1 MHz, and 100 kHz)

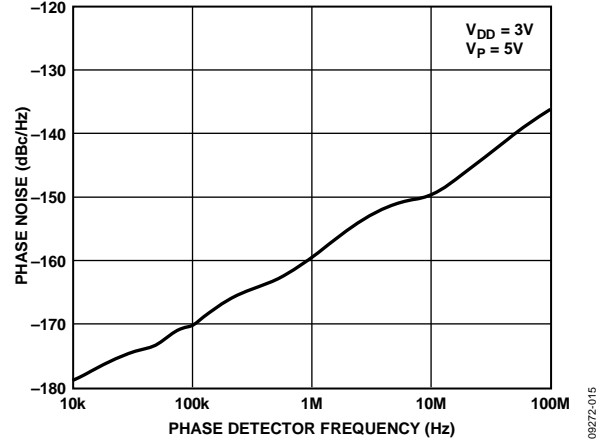


Figure 15. Phase Noise (Referred to CP Output) vs. PFD Frequency

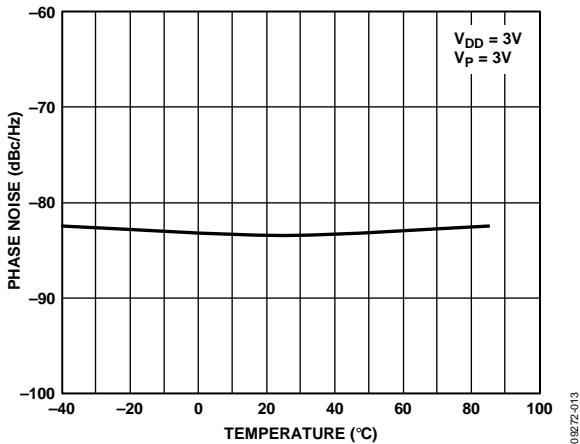


Figure 13. Phase Noise (5.8 GHz, 1 MHz, and 100 kHz) vs. Temperature

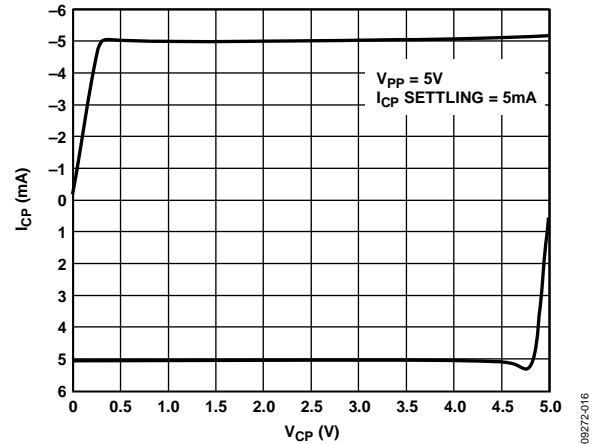


Figure 16. Charge Pump Output Characteristics

## PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the 20-lead LFCSP (CP-20) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the LFCSP has a central thermal pad.

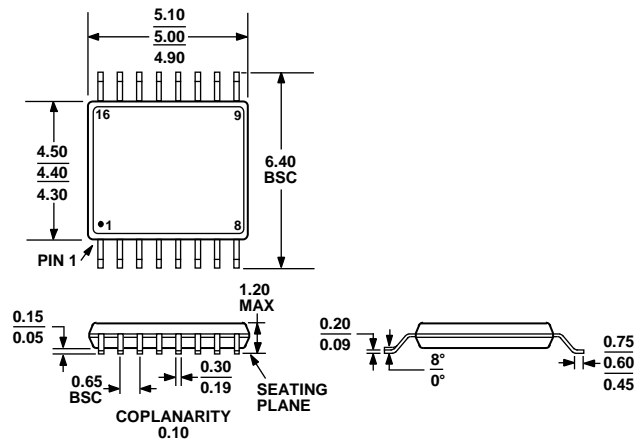
The thermal pad on the PCB should be at least as large as this exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the PCB thermal pad to AGND.

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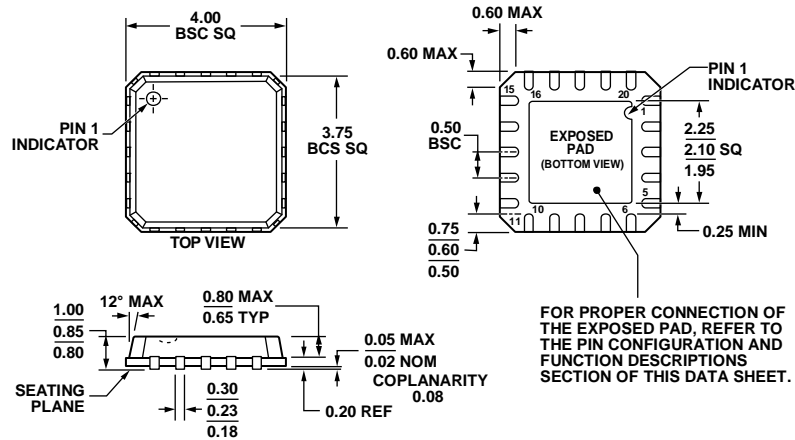
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 17. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 18. 20-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]

4 mm × 4 mm Body, Very Thin Quad

(CP-20-1)

Dimensions shown in millimeters

012508-B

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADF4106-SRU-EP	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4106-SRU-EP-R7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4106-SCPZ-EP	-55°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
ADF4106-SCPZ-EP-R7	-55°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**ADF4106-EP**

**NOTES**