Wideband Synthesizer with Integrated VCO

Preliminary Technical Data

ADF4355-2

FEATURES

Output frequency range: 55 MHz to 4400 MHz
Fractional-N synthesizer and integer-N synthesizer
High resolution Fractional-N
Low phase noise VCO
Programmable divide-by-1/-2/-4/-8/-16/-32/-64 output
Typical rms jitter: 0.18 ps rms
Analog & digital power supplies: 3.3 V
Charge pump and VCO power supplies: 5V.
Logic compatibility: 1.8 V & 3 V
Programmable dual-modulus prescaler of 4/5 or 8/9
Programmable output power level
RF output mute function
3-wire serial interface
Analog and digital lock detect
Cycle slip reduction

APPLICATIONS

Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)
Point to Point / Point to Multipoint Microwave links
Test equipment
Wireless LANs, CATV equipment
Clock generation

GENERAL DESCRIPTION

The ADF4355-2 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and external reference frequency.

The ADF4355-2 has an integrated voltage controlled oscillator (VCO) with a fundamental output frequency ranging from 3500 MHz to 7000 MHz. In addition, divide-by-1/-2/-4/-8/-16/-32/-64 circuits allow the user to generate RF output frequencies as low as 55 MHz. For applications that require isolation, the RF output stage can be muted. The mute function is both pin- and software-controllable. An auxiliary RF output is also available, which can be powered down when not in use.

Control of all on-chip registers is through a simple 3-wire interface. The device operates with analog and digital power supplies ranging from 3.15 V to 3.45 V, with charge pump and VCO supplies to from 4.75V to 5.25V. The part also contains hardware and software power down modes.

FUNCTIONAL BLOCK DIAGRAM

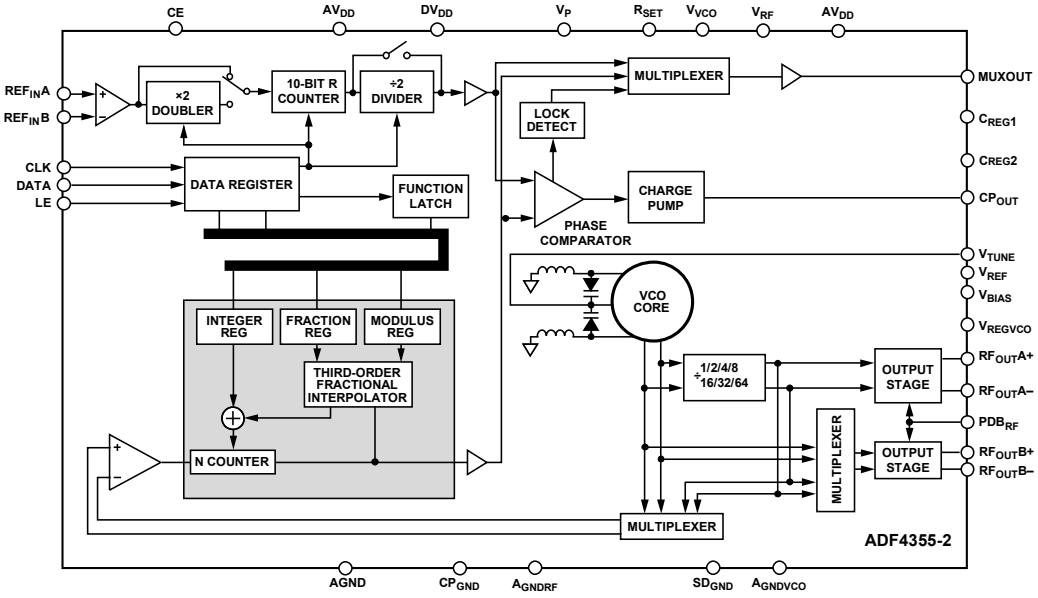


Figure 1.

Rev. Pr G

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

SPECIFICATIONS

AV_{DD} = DV_{DD} = V_{RF} = 3.3 V ± 5%, 4.75 V ≤ V_P ≤ V_{VCO} ≤ 5.25 V, A_{GND} = D_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF_{IN} CHARACTERISTICS					
Input Frequency				MHz	For f < 10 MHz, ensure slew rate > 21 V/µs
Single-ended mode	10		250		
Differential mode	10		500		
Input Sensitivity	0.7		AV_{DD}	V p-p	Biased at AV_{DD}/2; ac coupling ensures AV_{DD}/2 bias
Input Capacitance		10		pF	
Input Current			±60	µA	
PHASE DETECTOR					
Phase Detector Frequency			125	MHz	
CHARGE PUMP					
I_{CP} Sink/Source[1]					R_{SET} = 5.1 kΩ
High Value		5		mA	
Low Value		0.312		mA	
R_{SET} Range		5.1		kΩ	
Sink and Source Current Matching		2		%	0.5 V ≤ V_{CP} ≤ 4.5 V
I_{CP} vs. V_{CP}		1.5		%	0.5 V ≤ V_{CP} ≤ 4.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = 2.0 V
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.5			V	
Input Low Voltage, V_{INL}			0.6	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}		3.0		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} – 0.4			V	CMOS output selected
Output High Current, I_{OH}			500	µA	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	3.15		3.45	V	
DV_{DD} , V_{RF}		AV_{DD}			These voltages must equal AV_{DD}
V_P , V_{VCO}	4.75	5.0	5.25	V	V_P must equal V_{VCO}
DI_{DD} + AI_{DD}[2]		40	TBD	mA	
Output Dividers		TBD		mA	Each output divide-by-2 consumes TBD mA
I_{VCO}		70	80	mA	
I_{RFOUT}		12.5/25/ 37.5/50	TBD	mA	RF output stage is programmable
Low Power Sleep Mode		7	1000	µA	
RF OUTPUT CHARACTERISTICS					
Minimum VCO Output Frequency Using Dividers	54.6875			MHz	3500 MHz fundamental output and divide-by-64 selected (RF_{OUT}A).
VCO Sensitivity, K_V		12		MHz/V	
Frequency Pushing (Open-Loop)		TBD		MHz/V	
Frequency Pulling (Open-Loop)		TBD		kHz	Into 2.00 VSWR load
Harmonic Content (Second)		TBD		dBc	Fundamental VCO output
Harmonic Content (Second)		TBD		dBc	Fundamental VCO output
		TBD		dBc	Divided VCO output

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Harmonic Content (Third)		TBD		dBc	Fundamental VCO output
		TBD		dBc	Divided VCO output
Minimum RF Output Power		−4		dBm	Programmable in 3 dB steps
Maximum RF Output Power		5		dBm	
Output Power Variation		TBD		dB	
Minimum VCO Tuning Voltage		0.5		V	
Maximum VCO Tuning Voltage		4.5		V	
NOISE CHARACTERISTICS					
Fundamental VCO Phase Noise Performance					VCO noise in open-loop conditions
		-116		dBc/Hz	100 kHz offset from 3.5 GHz carrier
		-136		dBc/Hz	800 kHz offset from 3.5 GHz carrier
		-138		dBc/Hz	1 MHz offset from 3.5 GHz carrier
		-155		dBc/Hz	10 MHz offset from 3.5 GHz carrier
		-113		dBc/Hz	100 kHz offset from 5.0 GHz carrier
		-133		dBc/Hz	800 kHz offset from 5.0 GHz carrier
		-135		dBc/Hz	1 MHz offset from 5.0 GHz carrier
		-153		dBc/Hz	10 MHz offset from 5.0 GHz carrier
		-110		dBc/Hz	100 kHz offset from 7.0 GHz carrier
		-130		dBc/Hz	800 kHz offset from 7.0 GHz carrier
		-132		dBc/Hz	1 MHz offset from 7.0 GHz carrier
		-150		dBc/Hz	10 MHz offset from 7.0 GHz carrier
Normalized In-Band Phase Noise Floor[3]		−224		dBc/Hz	
In-Band Phase Noise[4]		−103		dBc/Hz	10 kHz offset from 2113.5 MHz carrier
Integrated RMS Jitter[5]		0.2		ps	
Spurious Signals due to PFD Frequency		−80		dBc	
Level of Signal with RF Mute Enabled		−30		dBm	

[1] I_{CP} is internally modified to maintain constant loop gain over the frequency range.
[2] T_A = 25°C; AV_{DD} = DV_{DD} = V_{RF} = 3.3V, V_{VCO} = V_P = 5.0 V =; prescaler = 4/5; f_{REFIN} = 122.88 MHz; f_{PFD} = 61.44 MHz; f_{RF} = 1650 MHz.
[3] This figure can be used to calculate phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: −224 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode.
[4] f_{REFIN} = 122.88 MHz; f_{PFD} = 61.44 MHz; offset frequency = 10 kHz; VCO frequency = 4227 MHz, output divide-by-2 enabled. RF_{OUT} = 2113.5 MHz; N = 169; loop BW = 40 kHz, I_{CP} = 313 µA; low noise mode.
[5] f_{REFIN} = 100 MHz; f_{PFD} = 25 MHz; VCO frequency = 4400 MHz; RF_{OUT} = 4400 MHz; N = 176; loop BW = 40 kHz, I_{CP} = 313 µA; low noise mode.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = V_{RF} = 3.3 V ± 5%, 4.75 V ≤ V_P ≤ V_{VCO} ≤ 5.25 V, A_{GND} = D_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 2.

Parameter	Limit	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

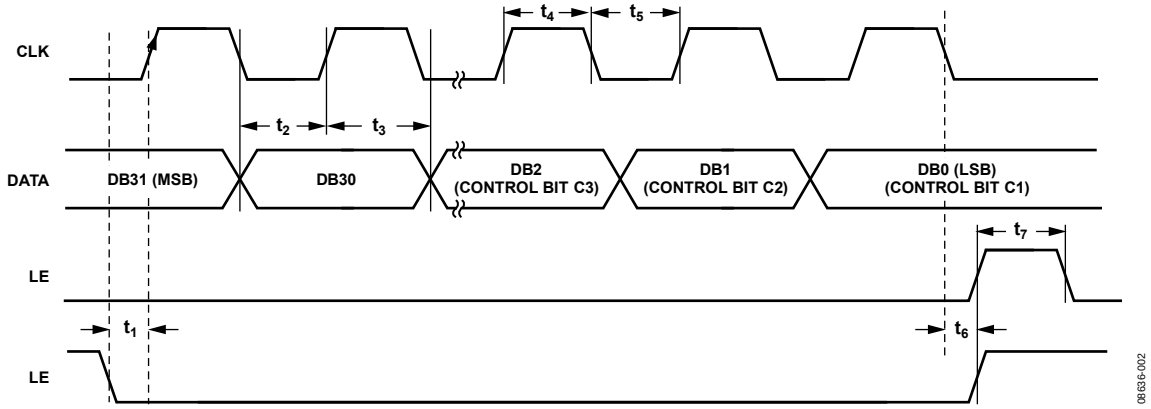


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{RF} , DV_{DD} , AV_{DD} to GND[1]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P , V_{VCO} to GND[1]	−0.3 V to +5.8 V
V_P , V_{VCO} to AV_{DD}	−0.3 V to AV_{DD} +2.5 V
Digital I/O Voltage to GND[1]	−0.3 V to 1.8 V + 0.3 V
Analog I/O Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
REF_{IN} to GND[1]	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA}, Thermal Impedance Paddle Soldered to GND	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = A_{GND} = SD_{GND} = D_{GND} = A_{GNDRF} = A_{GNDVCO} = CP_{GND} = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of TBD kV and is ESD sensitive. Proper precautions should be taken for handling and assembly.

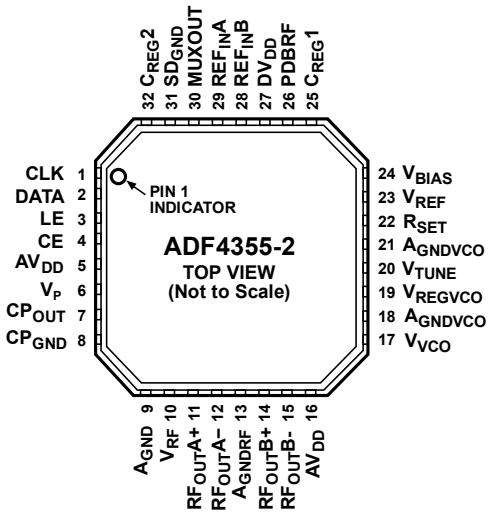
TRANSISTOR COUNT

The transistor count for the ADF4355-2 is TBD (CMOS) and TBD (bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE LFCSP HAS AN EXPOSED PADDLE THAT MUST BE CONNECTED TO GND.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
2	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs as the control bits. This input is a high impedance CMOS input.
3	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the three LSBs.
4	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device, depending on the status of the power-down bits.
5, 16	AV_{DD}	Analog Power Supply. This pin ranges from 3.15 V to 3.45 V. Place decoupling capacitors to the analog ground plane as close to this pin as possible. AV_{DD} must have the same value as DV_{DD}.
6	V_P	Charge Pump Power Supply. V_P must have the same value as V_{VCO}. Place decoupling capacitors to the ground plane as close to this pin as possible.
7	CP_{OUT}	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to V_{TUNE} to drive the internal VCO.
8	CP_{GND}	Charge Pump Ground. This output is the ground return pin for CP_{OUT}.
9	AGND	Analog Ground. Ground return pin for AV_{DD}.
10	V_{RF}	Power Supply for the RF output. This pin ranges from 3.15 V to 3.45 V. Place decoupling capacitors to the analog ground plane as close to these pins as possible. V_{RF} must have the same value as AV_{DD}.
11	$RF_{OUT}A+$	VCO Output. The output level is programmable. The VCO fundamental output or a divided-down version is available.
12	$RF_{OUT}A–$	Complementary VCO Output. The output level is programmable. The VCO fundamental output or a divided-down version is available.
13	A_{GNDRF}	RF output stage ground. Ground return pins for the RF output stage.
14	$RF_{OUT}B+$	Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided-down version is available.
15	$RF_{OUT}B–$	Complementary Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided-down version is available.
17	V_{VCO}	Power Supply for the VCO. This pin ranges from 4.75 V to 5.25 V. Place decoupling capacitors to the analog ground plane as close to these pins as possible.
18, 21	A_{GNDVCO}	VCO ground. Ground return path for the VCO

Pin No.	Mnemonic	Description
19	V_{REGVCO}	VCO compensation node. biased at 4.5V. Place decoupling capacitors to the ground plane as close to this pin as possible. It is possible to overdrive this pin with a voltage equal to V_{VCO}, if a clean, low noise external voltage is available, which requires the internal LDO to be disabled in software. This may improve VCO noise by 1-2 dB.
20	V_{TUNE}	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP_{OUT} output voltage.
22	R_{SET}	Connecting a resistor between this pin and ground sets the charge pump output current.
23	V_{REF}	Internal Compensation Node. Biased at half the tuning range. Place decoupling capacitors to the ground plane as close to this pin as possible.
24	V_{BIAS}	Reference Voltage. Place decoupling capacitors to the ground plane as close to this pin as possible.
25	$C_{REG}1$	Output from LDO. Supply voltage to digital circuits. Nominal voltage of 1.8V. 100 nF decoupling capacitors to GND required.
26	PDB_{RF}	RF Power-Down. A logic low on this pin mutes the RF outputs. This function is also software controllable.
27	DV_{DD}	Digital Power Supply. This pin should be at the same voltage as AV_{DD}. Place decoupling capacitors to the ground plane as close to this pin as possible.
28	$REF_{IN}B$	Complementary Reference Input. If unused AC couple to GND.
29	$REF_{IN}A$	Reference Input.
30	MUXOUT	Multiplexer Output. The multiplexer output allows the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
31	SD_{GND}	Digital Σ-Δ Modulator Ground. Ground return path for the Σ-Δ modulator.
32	$C_{REG}2$	Output from LDO. Supply voltage to digital circuits. Nominal voltage of 1.8V. 100 nF decoupling capacitors to GND required.
EP	Exposed Pad	Exposed Pad. The LFCSP has an exposed pad that must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

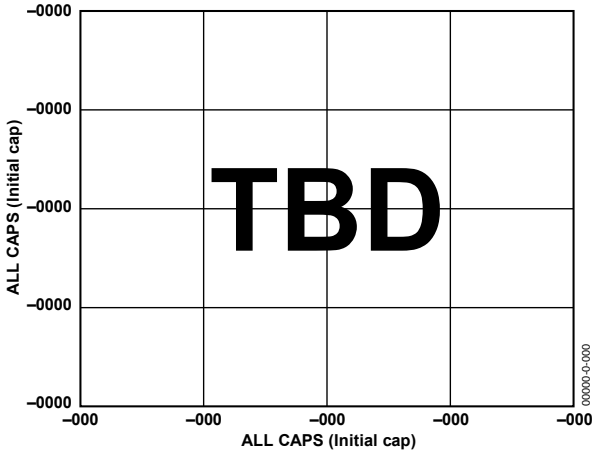


Figure 4. Open-Loop VCO Phase Noise, 3.5 GHz

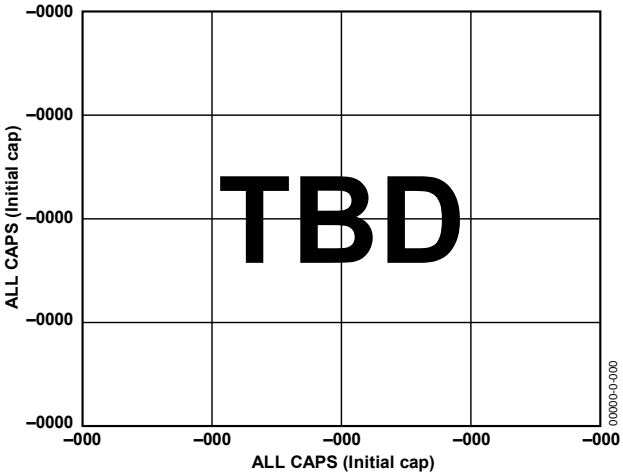


Figure 5. Open-Loop VCO Phase Noise, 5.0 GHz

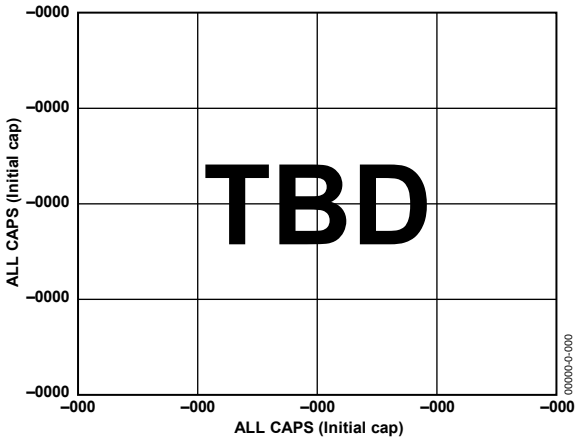


Figure 6. Open-Loop VCO Phase Noise, 7 GHz

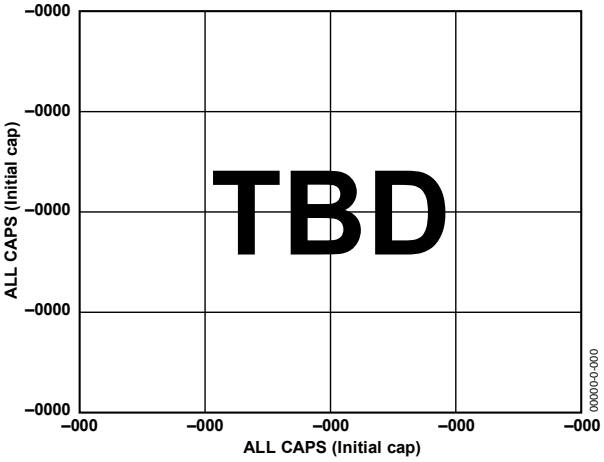


Figure 7. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 3.5 GHz, PFD = 61.44 MHz, Loop Bandwidth = 20 kHz

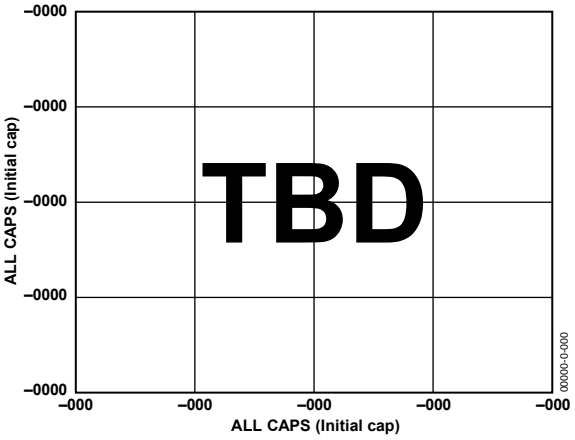


Figure 8. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 5.0 GHz, PFD = 61.44 MHz, Loop Bandwidth = 20 kHz

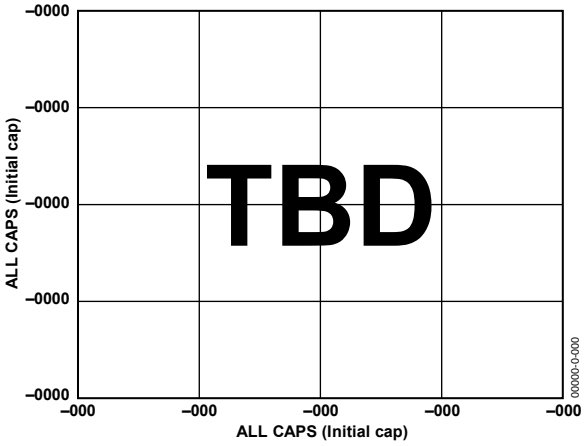


Figure 9. Closed-Loop Phase Noise, Fundamental VCO and Dividers, VCO = 7.0 GHz, PFD = 61.44 MHz, Loop Bandwidth = 20 kHz

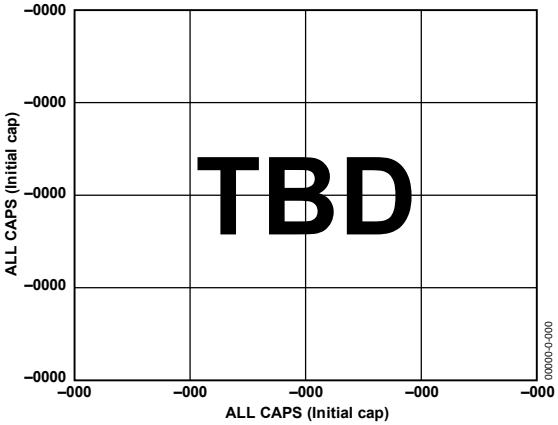


Figure 10. Integer-N Phase Noise and Spur Performance, GSM 900 Band, RF_{OUT} = 904 MHz, REF_{IN} = 122.88 MHz, PFD = 1600 kHz, Output Divide-by-4 Selected; Loop Filter Bandwidth = 10 kHz, Channel Spacing = 160 kHz

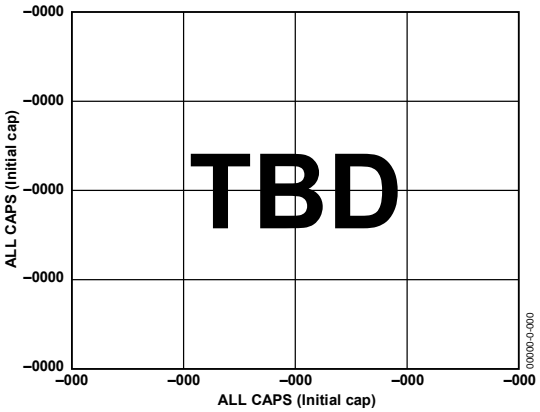


Figure 11. Fractional-N Spur Performance, W-CDMA Band, RF_{OUT} = 2113.5 MHz, REF_{IN} = 122.88 MHz, PFD = 61.44 MHz, Output Divide-by-2 Selected; Loop Filter Bandwidth = 20 kHz, Channel Spacing = 20 kHz

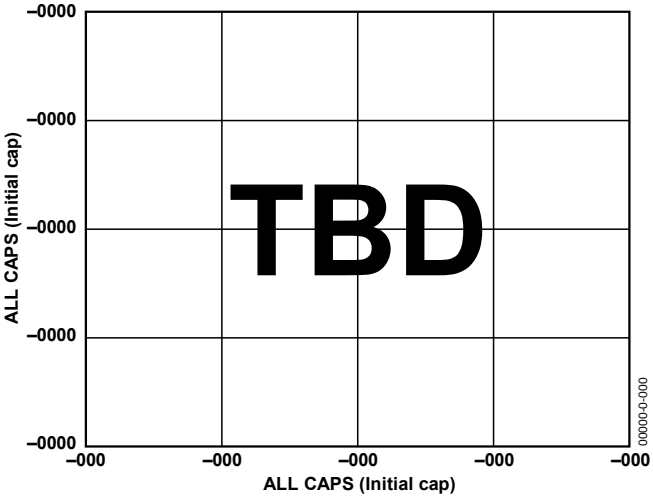


Figure 12. Fractional-N Spur Performance, W-CDMA Band, RF_{OUT} = 2113.5 MHz, REF_{IN} = 122.88 MHz, PFD = 61.44 MHz, Output Divide-by-2 Selected; Loop Filter Bandwidth = 20 kHz, Channel Spacing = 20 kHz

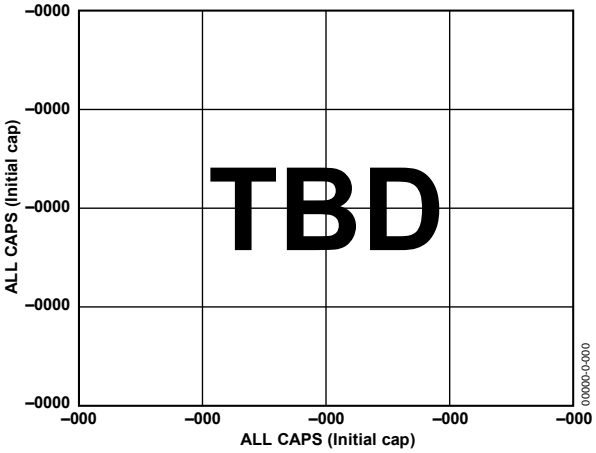


Figure 13. Fractional-N Spur Performance, RF_{OUT} = 2.591 GHz, REF_{IN} = 12.88 MHz, PFD = 61.44 MHz, Output Divide-by-4 Selected; Loop Filter Bandwidth = 20 kHz, Channel Spacing = 20 kHz

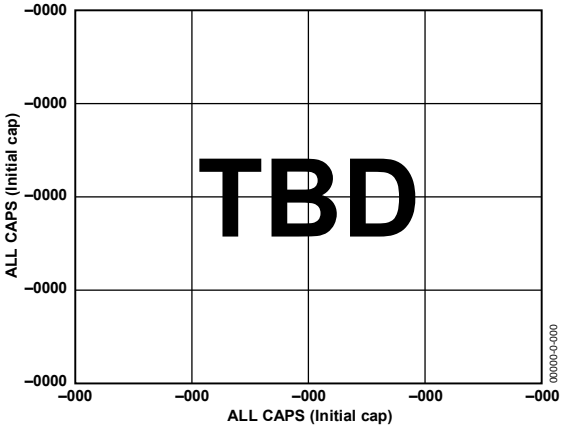


Figure 14. Fractional-N Spur Performance, RF_{OUT} = 2.591 GHz, REF_{IN} = 122.88 MHz, PFD = 61.44 MHz, Output Divide-by-2 Selected; Loop Filter Bandwidth = 10 kHz, Channel Spacing = 20 kHz

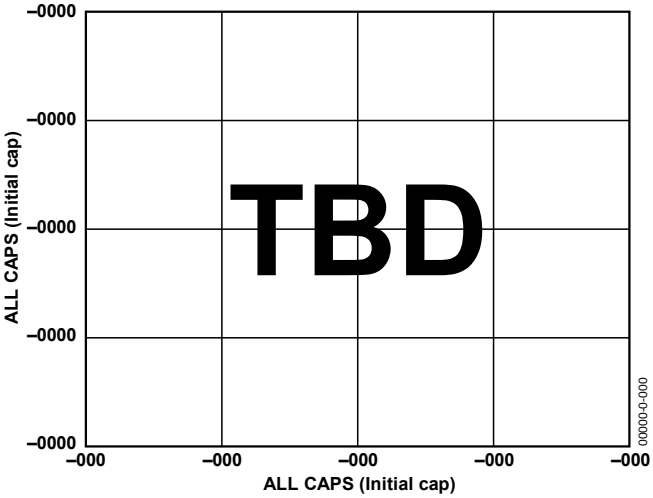


Figure 15. Lock Time for 100 MHz Jump from 3070 MHz to 2970 MHz

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 16. The reference input can accept both single-ended and differential signals, and the choice is controlled by Reference Input Mode bit ([DB9] in Register 4). To use differential signal on reference input, this bit must be programmed high. In this case switches SW1 and SW2 are opened, SW3 and SW4 are closed and the current source driving the differential pair of transistors is switched on. The differential signal is buffered and provided to ECL to CMOS converter. When single-ended signal is used as the reference, bit [DB9] in Register 4 must be programmed to 0. In this case switches SW1 and SW2 are closed, SW3 and SW4 are opened and the current source driving the differential pair of transistors is switched off.

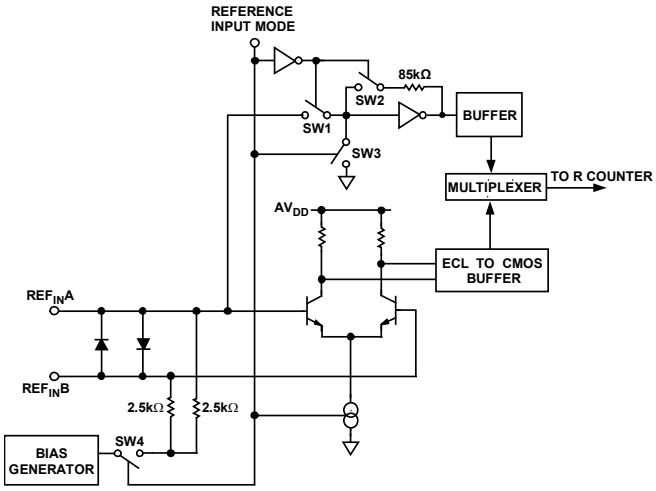


Figure 16. Reference Input Stage

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. The division ratio is determined by the INT, FRAC1, FRAC2 and MOD2 values, which build up this divider (see Figure 17).

INT, FRAC, MOD, and R Counter Relationship

The INT, FRAC, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency. For more information, see the RF Synthesizer—A Worked Example section.

The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times N$$

where:

RF_{OUT} is the output frequency of the external voltage controlled oscillator (VCO) (not using the output divider).

N is the desired value of the feedback counter N.

N is comprised of

$$N = INT + \left[\frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \right]$$

Where:

INT is the preset divide ratio of the binary 16-bit counter (23 to 65,535 for 4/5 prescaler, 75 to 65,535 for 8/9 prescaler).

FRAC1 is the numerator of the primary modulus 1 – 16,777,215.

MOD1 is a fixed value at 2^{24}, (16,777,216).

MOD2 is the programmable auxiliary fractional modulus (2 - 16,383.

FRAC2 is the numerator of the auxiliary modulus 1 – 16,383

This allows for very fine frequency resolution with no residual frequency error.

Simplest way to apply the formula is to

1) Calculate N by dividing RF_{OUT} / F_{PFD}.
2) The integer value of this number forms INT
3) Subtract this value from the full N value,
4) Multiplying the remainder by 2^{24} to calculate FRAC1,
5) Subtract this integer number leaving
6) The remainder, which can generated by a combination of *FRAC2/MOD2*.

The PFD frequency (f_{PFD}) equation is

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit.

R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).

T is the REF_{IN} divide-by-2 bit (0 or 1).

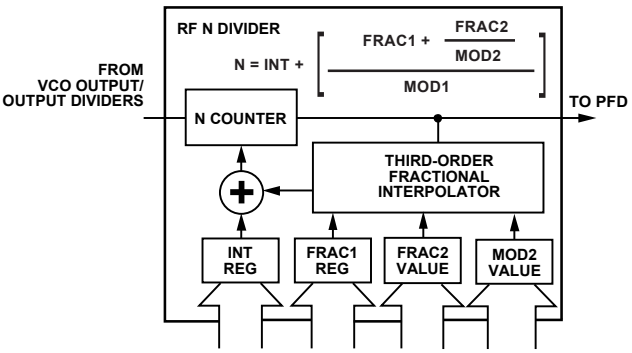


Figure 17. RF N Divider

Integer-N Mode

If FRAC = 0 and the DB23 (ABP) bit in Register 5 is set to 1, the synthesizer operates in integer-N mode. DB8 in Register 4 should be set to 1 for integer-N digital lock detect.

R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The phase frequency detector (PFD) takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 18 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the anti-backlash pulse, which is typically 2 ns for Integer-N applications, and 3 ns for Fractional-N applications. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. The phase detector polarity is set to negative on these parts, due to the inverse tuning of the VCO.

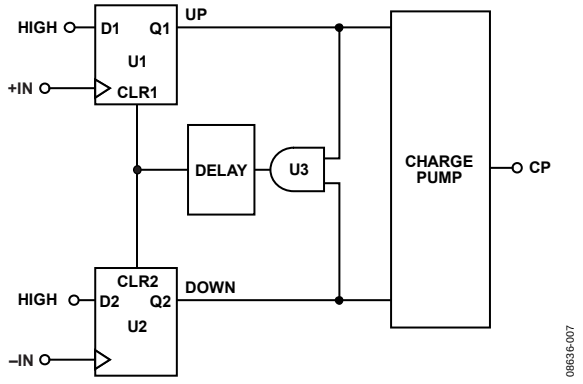


Figure 18. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4355-2 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by the M3, M2, and M1 bits in Register 4 (for details, see Figure 28). Figure 19 shows the MUXOUT section in block diagram form.

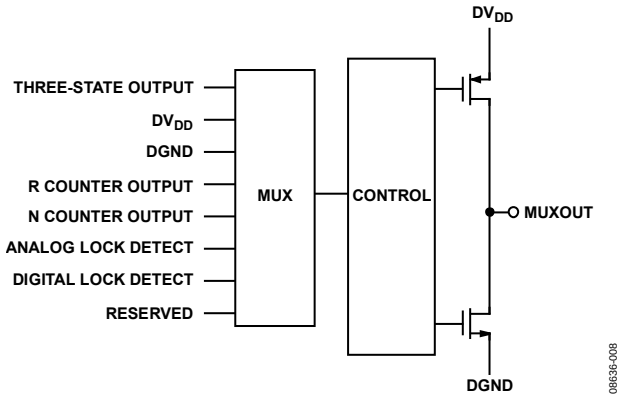


Figure 19. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4355-2 digital section includes a 10-bit RF R counter, a 16-bit RF N counter, a 24-bit FRAC counter, and a 24-bit modulus counter, and a 24-bit auxiliary modulus counter. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of six latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C4, C3, C2, and C1) in the shift register. As shown in Figure 2, these are the four LSBs: DB3, DB2, DB1, and DB0. The truth table for these bits is shown in Table 5. Figure summarizes how the latches are programmed.

Table 5. Truth Table for Control Bits C3, C2, and C1

Control Bits				
C4	**C3**	**C2**	**C1**	**Register**
0	0	0	0	Register 0 (R0)
0	0	0	1	Register 1 (R1)
0	0	1	0	Register 2 (R2)
0	0	1	1	Register 3 (R3)
0	1	0	0	Register 4 (R4)
0	1	0	1	Register 5 (R5)
0	1	1	0	Register 6 (R6)
0	1	1	1	Register 7 (R7)
1	0	0	0	Register 8 (R8)
1	0	0	1	Register 9 (R9)
1	0	1	0	Register 10 (R10)
1	0	1	1	Register 11 (R11)
1	1	0	0	Register 12 (R12)

PROGRAM MODES

Table 5 and Figure through Figure show how the program modes are to be set up in the ADF4355-2.

The following settings in the ADF4355-2 are double buffered: phase value, modulus value, reference doubler, reference divide-by-2, R counter value, and charge pump current setting. This

means that two events must occur before the part uses a new value for any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0.

For example, any time that the modulus value is updated, Register 0 (R0) must be written to, to ensure that the modulus value is loaded correctly. Divider select in Register 4 (R4) is also double buffered, but only if DB13 of Register 4 (R4) is high.

VCO

The VCO core in the ADF4355-2 consists of four separate VCOs, each of which uses 256 overlapping bands, as shown in Figure 20, to allow a wide frequency range to be covered without a large VCO sensitivity (K_V) and resultant poor phase noise and spurious performance.

The correct VCO and band are chosen automatically by the VCO and band select logic at power-up or whenever Register 0 (R0) is updated.

VCO and band selection take TBD PFD cycles. The VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage.

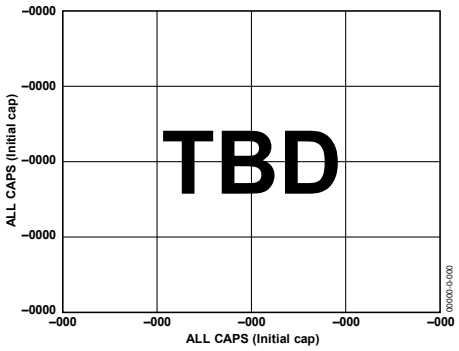


Figure 20. V_{TUNE} vs. Frequency

The R counter output is used as the clock for the band select logic. After band selection, normal PLL action resumes. The nominal value of K_V is 12 MHz/V when the N divider is driven from the VCO output or this value divided by D. D is the output divider value if the N divider is driven from the RF divider output (chosen by programming Bits[D23:D21] in Register 6 (R6)).

The VCO shows variation of K_V as the V_{TUNE} varies within the band and from band to band. For wideband applications covering a wide frequency range (and changing output dividers), a value of 12 MHz/V provides the most accurate K_V, because this value is closest to an average value. Figure 21 shows how K_V varies with fundamental VCO frequency along with an average value for the frequency band. Users may prefer this figure when using narrow-band designs.

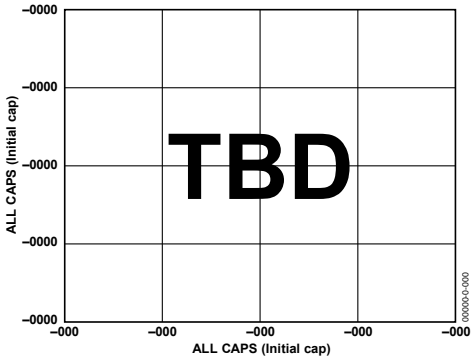


Figure 21. K_V vs. Frequency

OUTPUT STAGE

The $RF_{OUT}A+$ and $RF_{OUT}A-$ pins of the ADF4355-2 are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 22. In this scheme the part contains internal 50 Ohm resistors to VDDTo allow the user to optimize the power dissipation vs. the output power require-ments, the tail current of the differential pair is programmable using Bits[D2:D1] in Register 6 (R6). Four current levels can be set. These levels give output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respectively, using a 50 Ω resistor to AV_{DD} and ac coupling into a 50 Ω load. An external shunt inductor can be added to provide higher power levels, but this is less wideband than the internal bias only. Alternatively, both outputs can be combined in a 1 + 1:1 transformer or a 180° microstrip coupler (see the **Error! Reference source not found.** section). If the outputs are used individually, the optimum output stage consists of a shunt inductor to V_{VCO}. The unused complementary output must be terminated with a similar circuit to the used output.

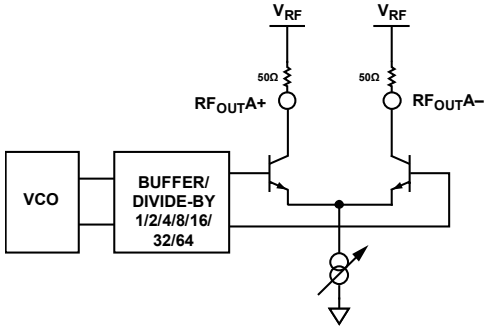


Figure 22. Output Stage

An auxiliary output stage exists on the $RF_{OUT}B+$ and $RF_{OUT}B-$ pins, providing a second set of differential outputs that can be used to drive another circuit, or that can be powered down if unused.

Another feature of the ADF4355-2 is that the supply current to the RF output stage can be shut down until the part achieves lock as measured by the digital lock detect circuitry. This is enabled by the mute till lock detect DB11 (MTLD) bit in Register 6 (R6).

REGISTER MAPS

REGISTER 0

RESERVED										AUTOCAL	PRESCALER	16-BIT INTEGER VALUE (INT)														CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	AC1	PR1	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED				24-BIT MAIN FRACTIONAL VALUE (FRAC1) DBR [1]																						CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2

14-BIT AUXILIARY FRACTIONAL VALUE (FRAC2) DBR [1]														14-BIT AUXILIARY MODULUS VALUE (MOD2) DBR [1]												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED	SD LOAD RESET	PHASE RESYNC	PHASE ADJUST	24-BIT PHASE VALUE (PHASE) DBR [1]																						CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SD1	PR1	PA1	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED	MUXOUT			REFERENCE DOUBLER DBR [1]	RDIV2 DBR [1]	10-BIT R COUNTER DBR [1]										DOUBLE BUFF	CURRENT SETTING DBR [1]				REF MODE	MUX LOGIC	PD POLARITY	PD	CP THREE-STATE	COUNTER RESET	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	CP4	CP3	CP2	CP1	U6	U5	U4	U3	U2	U1	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5

RESERVED							DITHER	ABP	RESERVED			CSR	RESERVED	CLK DIV MODE		12-BIT CLOCK DIVIDER VALUE												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	L1	F3	F2	0	0	F1	0	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C4(0)	C3(1)	C2(0)	C1(1)

REGISTER 6

RESERVED	NEGATIVE BLEED	VCO LDO	RESERVED	FEEDBACK SELECT	DIVIDER SELECT		CHARGE PUMP BLEED CURRENT								VCO POWER-DOWN	MTLD	RESERVED	AUX OUTPUT ENABLE	AUX OUTPUT POWER	RF OUTPUT ENABLE	OUTPUT POWER	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	BLD	LDO	0	0	0	D13	D12	D11	D10	BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1	D9	D8	D7	D6	D5	D4	D3	D2	D1	C4(0)	C3(1)	C2(1)	C1(0)

REGISTER 7

RESERVED						LE SYNC	RESERVED															LD CYCLE COUNT		LOL MODE	FRAC-N LD PRECISION		LD MODE	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD5	LD4	LOL	LD3	LD2	LD1	C4(0)	C3(1)	C2(1)	C1(1)

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2]DBB = DOUBLE BUFFERED BITS—BUFFERED BY THE WRITE TO REGISTER 0, IF AND ONLY IF DB13 OF REGISTER 2 IS HIGH.

Figure 23 Register Summary

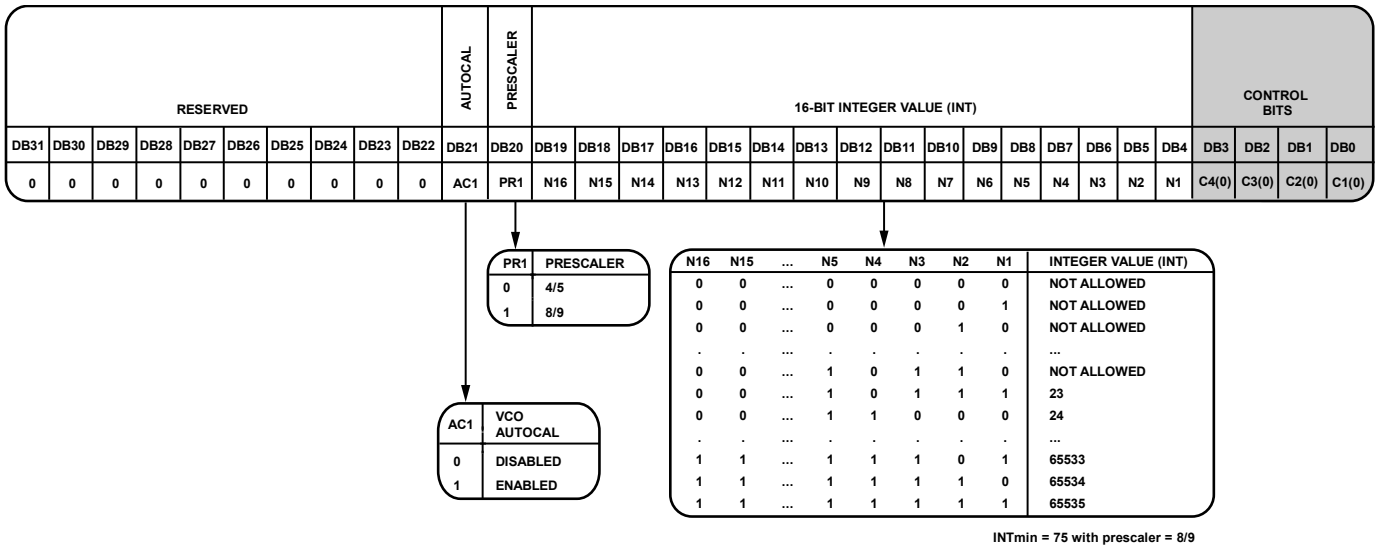


Figure 24. Register 0 (R0)

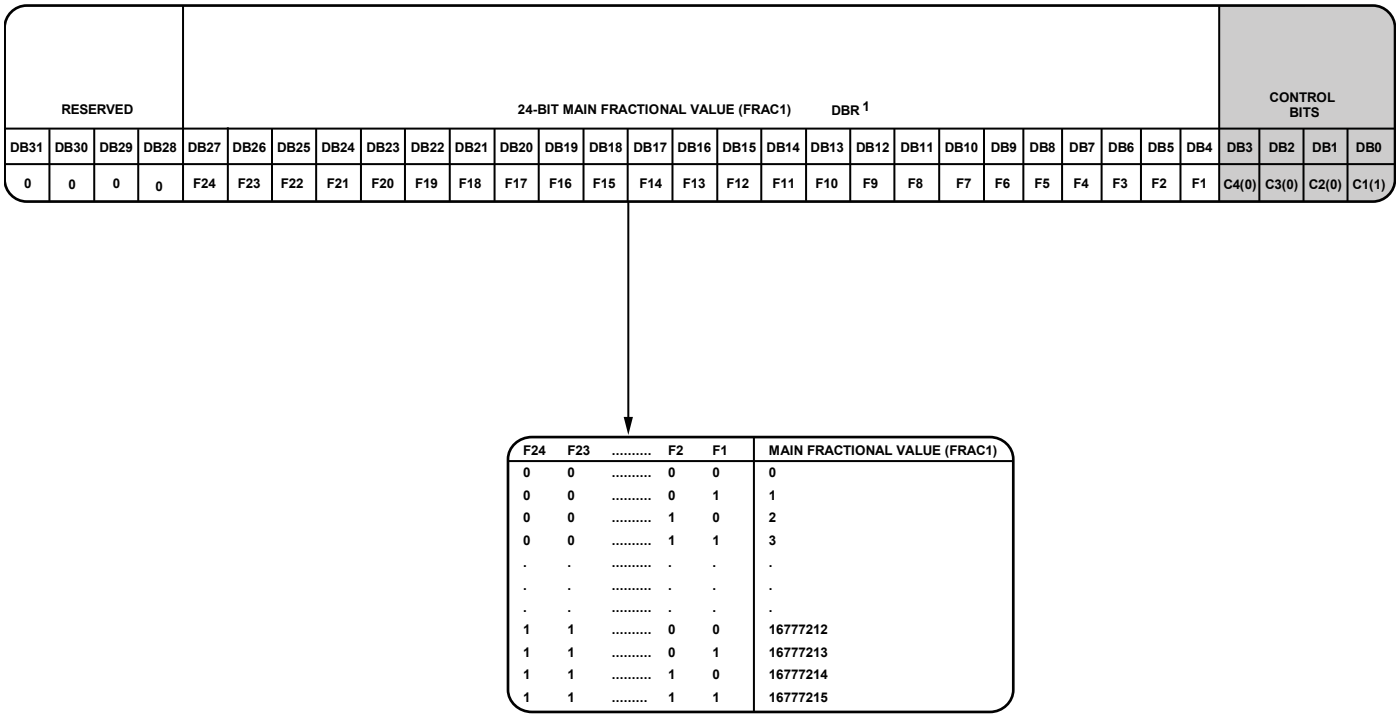


Figure 25. Register 1 (R1)

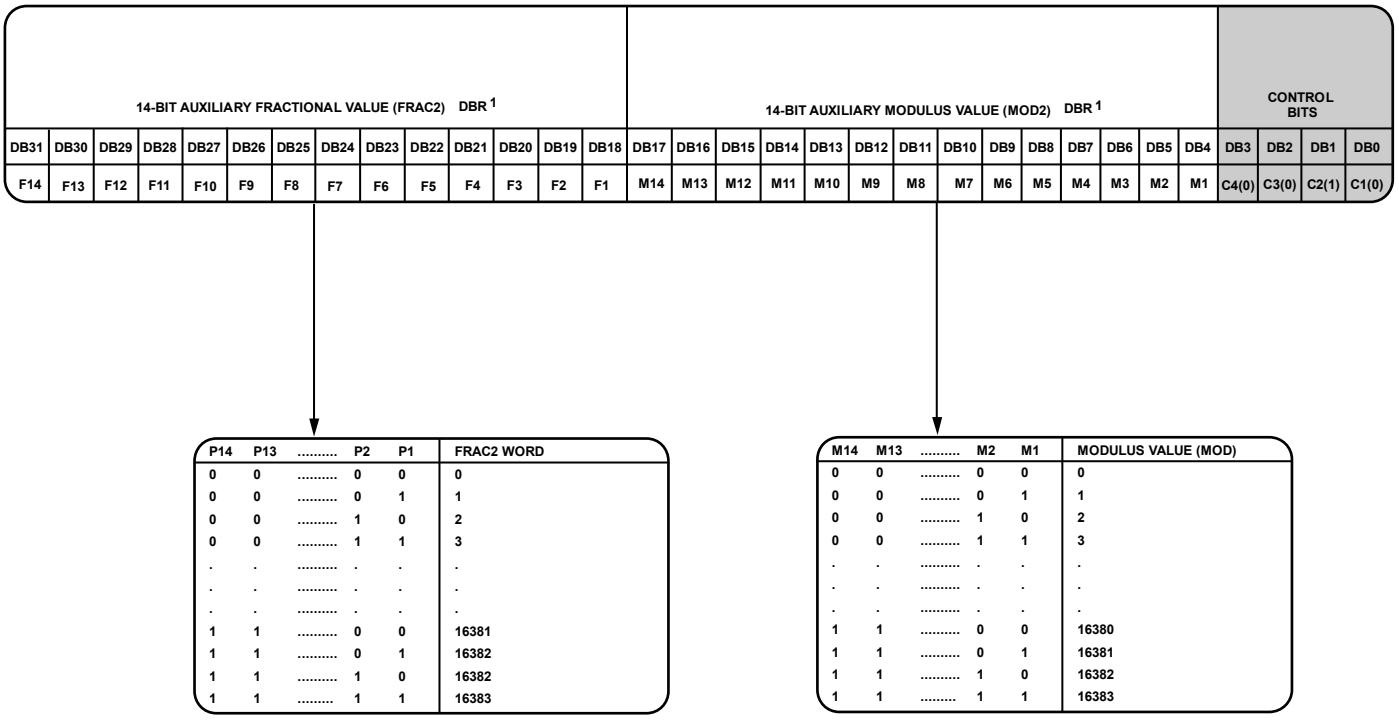


Figure 26. Register 2 (R2)

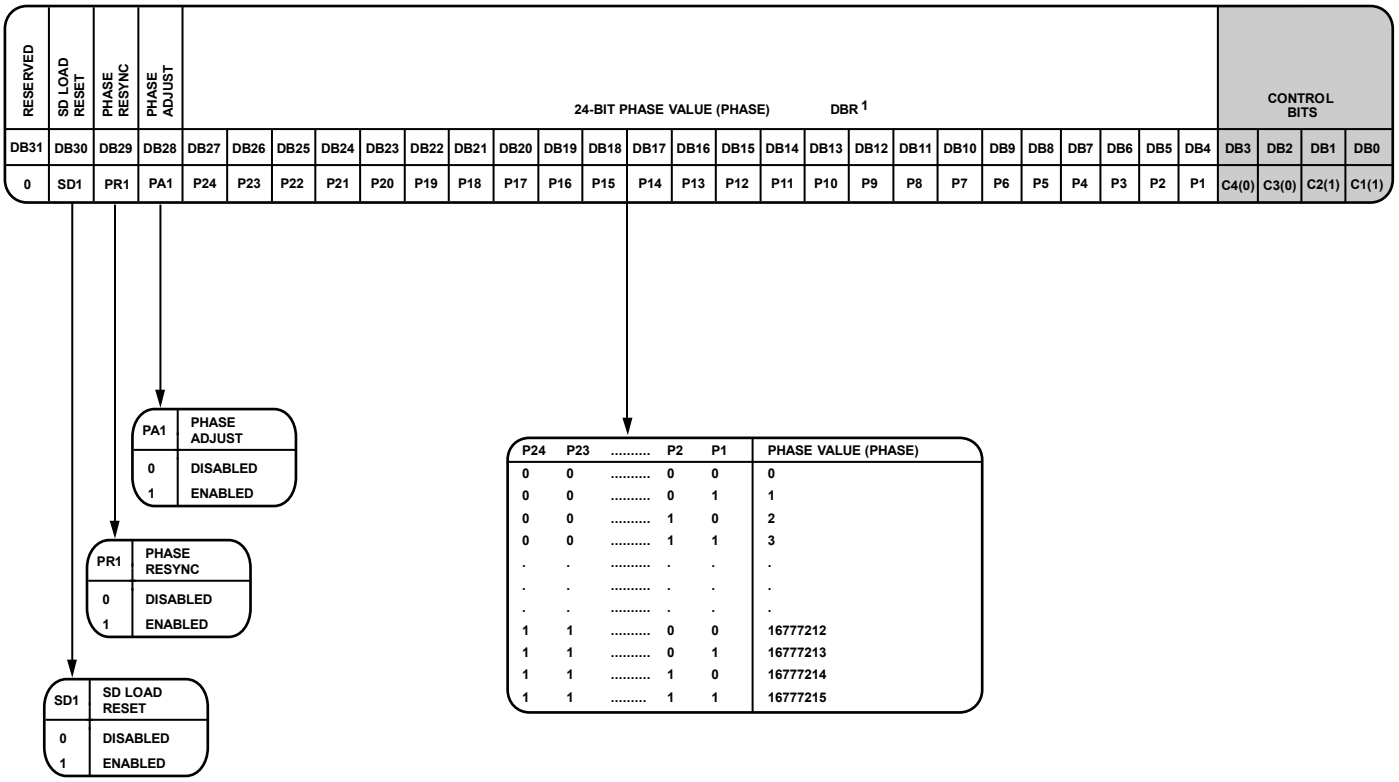


Figure 27. Register 3 (R3)

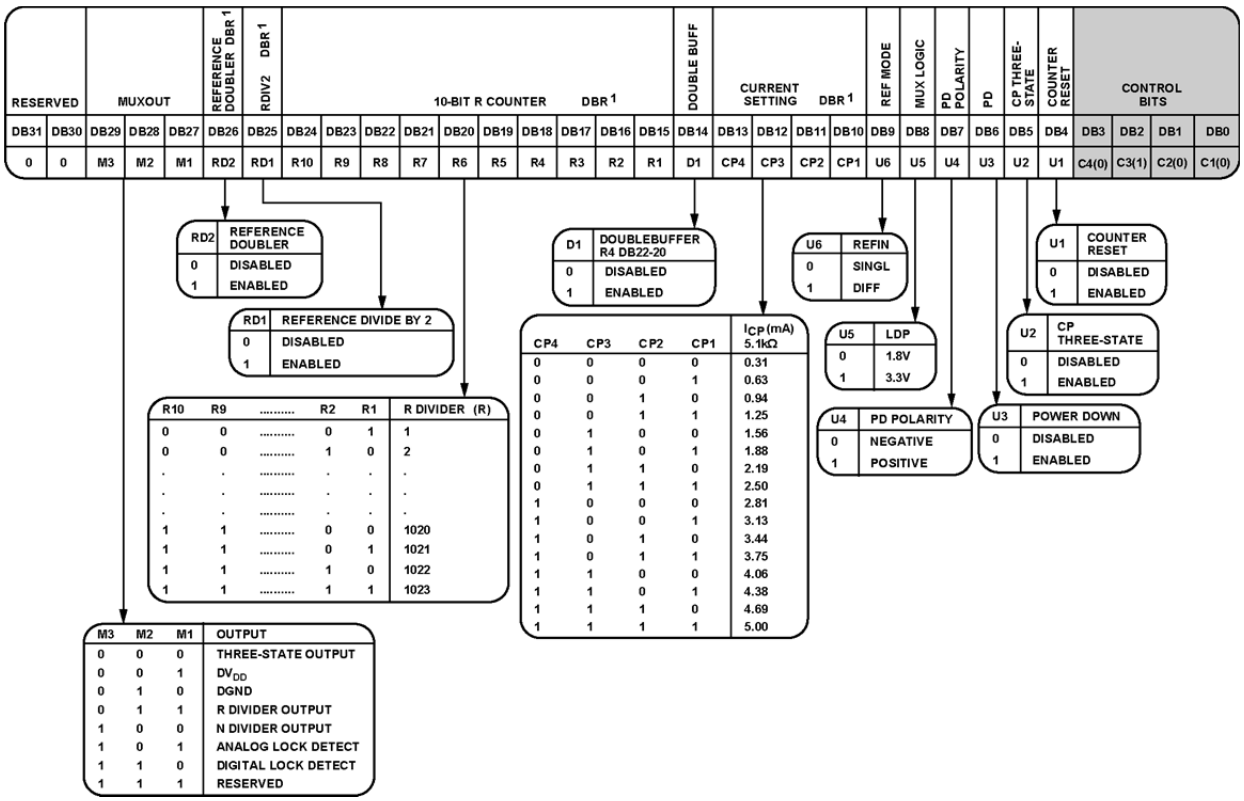


Figure 28. Register 4 (R4)

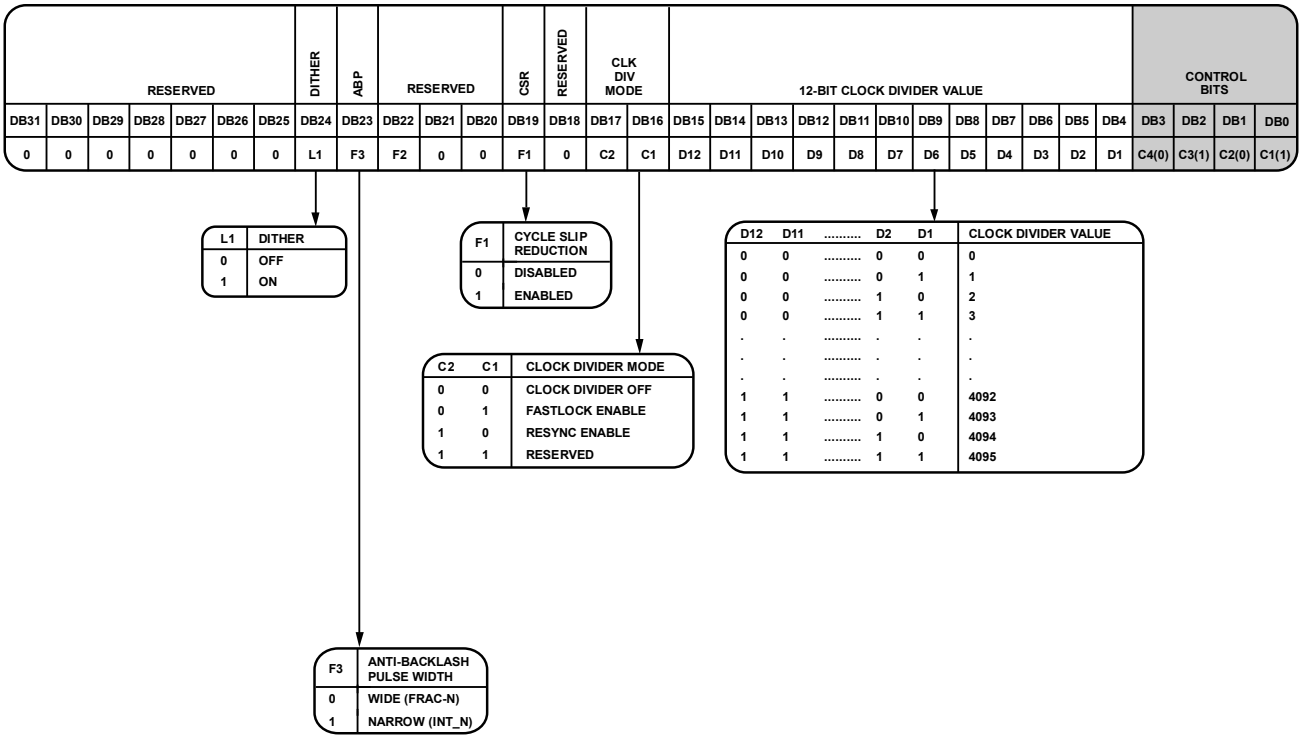


Figure 29. Register 5 (R5)

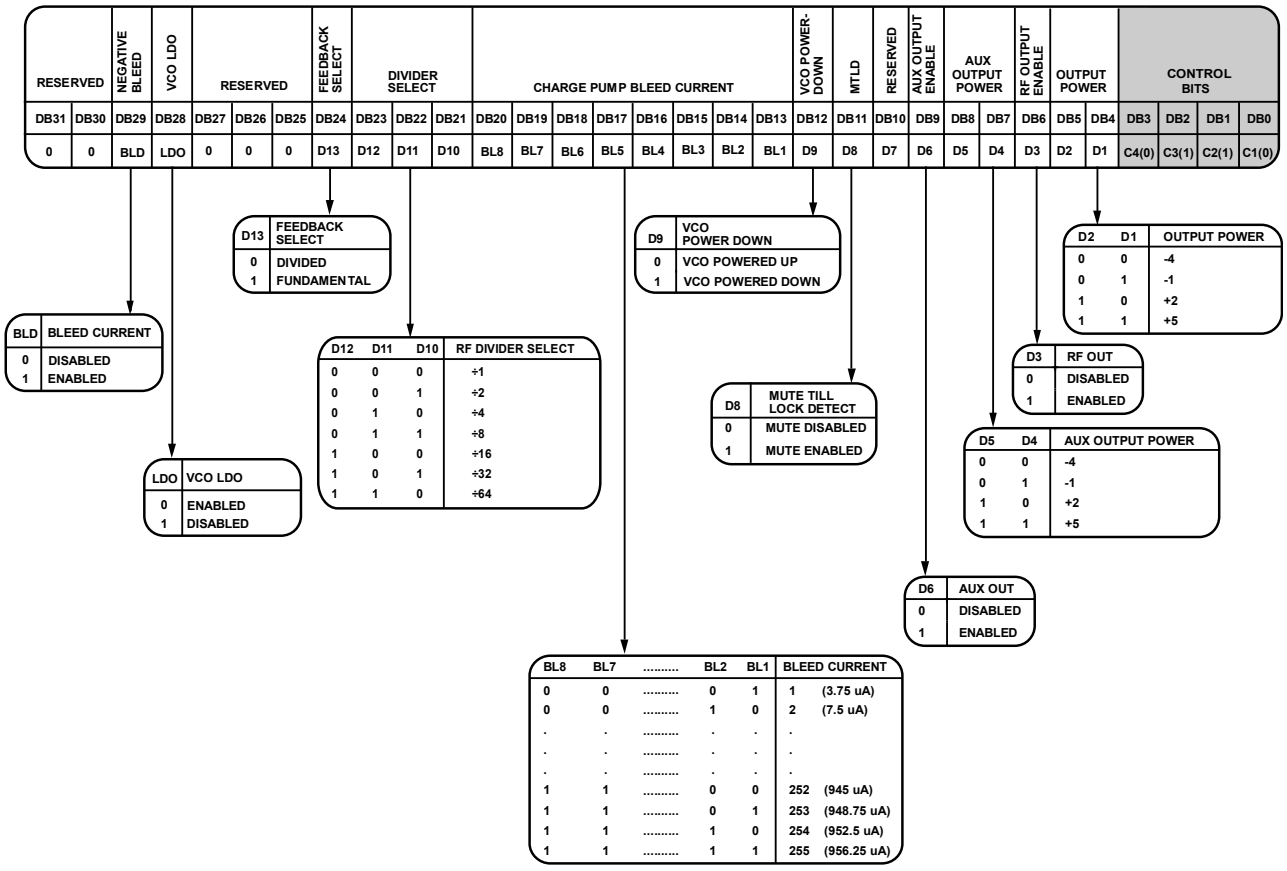


Figure 30. Register 6 (R6)

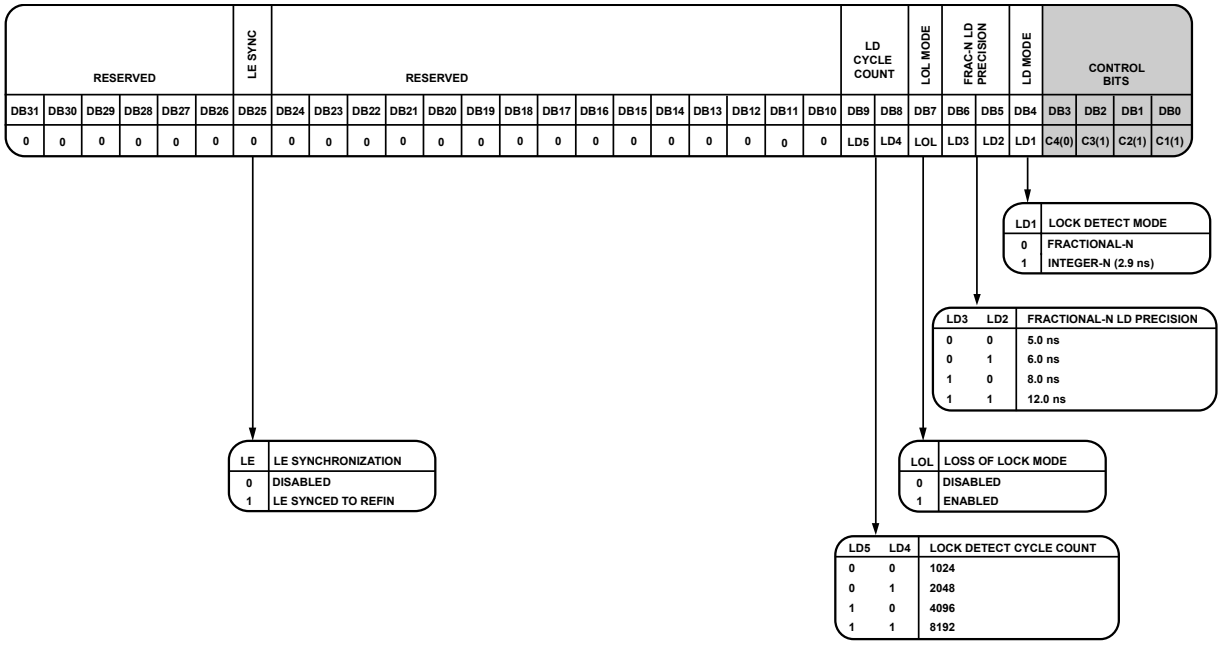


Figure 31. Register 7 (R7)

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	C4(1)	C3(0)	C2(0)	C1(0)

Figure 32 Register 8 (R8), Hex code 000002C8

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C4(1)	C3(0)	C2(0)	C1(1)

Figure 33 Register 9 (R9), Hex code FFFFFFF9

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	C4(1)	C3(0)	C2(1)	C1(0)

Figure 34. Register 10 (R10), Hex code 8400001A

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	C4(1)	C3(0)	C2(1)	C1(1)

Figure 35 Register 11 (R11), Hex code 0070022B

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(0)

Figure 36. Register 12 (R12), Hex code 0000000C

REGISTER 0

Control Bits

With Bits[C4:C1] set to 0000, Register 0 is programmed. Figure 24 shows the input data format for programming this register.

Autocal

VCO automatic calibration to choose the appropriate VCO and VCO sub-band is enacted by default on writing to register R0. Writing a '1' to DB21 disables the auto-calibration, leaving the part in the same band it was already in.

This function should only be used for fixed frequency applications, or very small (< 10 kHz) frequency jumps.

Prescaler Value

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (DB20) in Register 0 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When the prescaler is set to 4/5, it will operate to the maximum allowed RF frequency allowed of 7 GHz. The prescaler limits the INT value: if P is 4/5, N_{MIN} is 23; if P is 8/9, N_{MIN} is 75.

16-Bit Integer Value

The 16 INT bits (Bits[DB19:DB4]) set the INT value, which determines the integer part of the feedback division factor. The INT value is used in Equation 1 (see the INT, FRAC, MOD, and R Counter Relationship section). All integer values from 23 to 32,767 are allowed for the 4/5 prescaler. For the 8/9 prescaler, the minimum integer value is 75, and the maximum value is 65,535.

REGISTER 1

Control Bits

With Bits[C4:C1] set to 0001, Register 1 is programmed. Figure 25 shows the input data format for programming this register.

24-Bit Main Fractional Value

The 24 FRAC1 bits (Bits[DB27:DB4]) set the numerator of the fraction that is input to the Σ-Δ modulator. This fraction, along with the INT value, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC1 values from 0 to (MOD1 – 1) cover channels over a frequency range equal to the PFD reference frequency.

REGISTER 2

Control Bits

With Bits[C4:C1] set to 0010, Register 2 is programmed. Figure 26 shows the input data format for programming this register.

14-Bit Auxiliary Fractional Value

The auxiliary fractional value (Bits[DB17:DB4]) control the auxiliary fractional word. The FRAC2 word must be less than the MOD value programmed in Register 2.

14-Bit Auxiliary MOD2 Value

The 14 MOD2 bits (Bits[DB17:DB4]) set the auxiliary fractional modulus. The auxiliary fractional modulus is to be used to correct any residual error due to the main fractional modulus.

REGISTER 3

Control Bits

With Bits[C4:C1] set to 0011, Register 3 is programmed. Figure 27 shows the input data format for programming this register.

SD Load Reset

On writing to Register 0, the Sigma Delta Modulator is reset. For applications in which the phase is continually adjusted, this may not be desirable, so in these cases the Sigma Delta Reset can be disabled by writing a '1' to DB30.

Phase Resync

To use the phase resynchronization feature, DB29 must be set to '1'. If unused the bit can be programmed to '0'.

Phase Control

The phase of the RF output frequency can be adjusted in 24-bit steps. From 0 degrees (0) to 360 degrees (2^{24}-1).

REGISTER 4

Control Bits

With Bits[C4:C1] set to 0100, Register 4 is programmed. Figure 28 shows the input data format for programming this register.

MUXOUT

The on-chip multiplexer is controlled by Bits[DB29:DB27] (see Figure 28).

Reference Doubler

Setting DB26 to 0 feeds the REF_{IN} signal directly to the 10-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding it into the 10-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the low spur mode (using dither and bleed currents) is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle in the low noise mode (dither off) and when the doubler is disabled.

The maximum allowable REF_{IN} frequency when the doubler is enabled is 30 MHz.

RDIV2

Setting the DB25 bit to 1 inserts a divide-by-2 toggle flip-flop between the R counter and PFD, which extends the maximum REF_{IN} input rate. This function allows a 50% duty cycle signal to appear at the PFD input, which is necessary for cycle slip reduction.

10-Bit R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

Double Buffer

The DB14 bit enables or disables double buffering of Bits[DB23:DB21] in Register 4. The Program Modes section explains how double buffering works.

Charge Pump Current Setting

Bits[DB13:DB10] set the charge pump current. This value should be set to the charge pump current that the loop filter is designed with (see Figure 29).

Phase Detector Polarity

The DB7 bit sets the phase detector polarity. When a passive loop filter or a inverting active loop filter is used, this bit should be set to 0. If an active filter with an inverting characteristic is used, this bit should be set to 1.

Reference mode

The ADF4355-2 permits use of either differential or single-ended reference sources. For differential sources programming a '1' is required, and a '0' should be used if the REFIN is single-ended.

Level select

To assist with logic compatibility, MUXOUT can be programmed to two logic levels, a '0' to bit DB8 selects 1.8V logic, and a '1' selects 3.3V.

Power-Down

DB6 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. In software power-down mode, the part retains all information in its registers. The register contents are lost only if the supply voltages are removed.

When power-down is activated, the following events occur:

- Synthesizer counters are forced to their load state conditions.
- VCO is powered down.
- Charge pump is forced into three-state mode.
- Digital lock detect circuitry is reset.
- RF_{OUT} buffers are disabled.
- Input registers remain active and capable of loading and latching data.

Charge Pump Three-State

Setting the DB5 bit to 1 puts the charge pump into three-state mode. This bit should be set to 0 for normal operation.

Counter Reset

The DB4 bit is the reset bit for the R counter and the N counter of the ADF4355-2. When this bit is set to 1, the RF synthesizer N counter and R counter are held in reset. For normal operation, this bit should be set to 0.

REGISTER 5

Control Bits

With Bits[C4:C1] set to 0101, Register 5 is programmed. Figure 29 shows the input data format for programming this register.

Dither

Dither is a function which when enabled randomizes spurious energy into noise. It is recommended to use this mode by setting this bit DB24 to '1'. If unused, it can be set to '0'.

Anti-Backlash Pulsewidth setting

Setting this bit to a 1 sets a narrow pulsewidth suitable for integer-N applications. For fractional-N applications, the longer wider pulse width should be used by setting this bit to 0.

Cycle Slip Reduction

Setting the DB19 bit to 1 enables cycle slip reduction. CSR is a method for improving lock times, when the PLL low pass filter is less than 5% of the PFD. Note that the signal at the phase frequency detector (PFD) must have a 50% duty cycle for cycle slip reduction to work. The charge pump current setting

must also be set to the minimum value of 313 uA. See the cycle slip reduction section for more information.

Clock Divider Mode

Bits[DB17:DB16] must be set to 10 to activate phase resync. Setting Bits[DB16:DB15] to 00 disables the clock divider (see Figure 30).

12-Bit Clock Divider Value

The 12-bit clock divider value sets the timeout counter for activation of phase resync.

REGISTER 6

Control Bits

With Bits[C4:C1] set to 0110, Register 6 is programmed. Figure 30 shows the input data format for programming this register.

Negative Bleed

Use of constant negative bleed is recommended for most applications. This improves the linearity of the charge pump leading to lower noise and spurious than leaving it off. This is enabled by writing bit DB29 to '1', and disabled by writing a '0'.

VCO Low Dropout Regulator

If a very low noise, clean supply is available (such as the ADM7150 supplied with the evaluation board), then the internal LDO for the VCO can be powered down, and the VCO supplied with the voltage at V_{REGVCO}. This can be achieved by setting this bit to '1'. This requires the external voltage to be supplied to this pin. For noisier regulators it is better to use the internal LDO, set the bit to '0'.

Feedback Select

The DB24 bit selects the feedback from the VCO output to the N counter. When this bit is set to 1, the signal is taken directly from the VCO. When this bit is set to 0, the signal is taken from the output of the output dividers. The dividers enable coverage of the wide frequency band (35 MHz to 4.4 GHz). When the divider is enabled and the feedback signal is taken from the output, the RF output signals of two separately configured PLLs are in phase. This is useful in some applications where the positive interference of signals is required to increase the power.

Divider Select

Bits[DB23:DB21] select the value of the output divider (see Figure 31).

Bleed Currents

Bits[DB20:DB13] control the level of bleed current added to the charge pump output. This is used to optimize the spurious levels from the device. Experiment has shown that the ratio of bleed current / Charge pump current should equal 4/N. The optimum value can be improved by experiment.

Mute Till Lock Detect

When the DB11 bit is set to 1, the supply current to the RF output stage is shut down until the part achieves lock, as measured by the digital lock detect circuitry.

AUX Output Enable

The DB9 bit enables or disables the auxiliary RF output. If DB9 is set to 0, the auxiliary RF output is disabled; if DB9 is set to 1, the auxiliary RF output is enabled.

AUX Output Power

Bits[DB8:DB7] set the value of the auxiliary RF output power level (see Figure 30).

RF Output Enable

The DB6 bit enables or disables the primary RF output. If DB5 is set to 0, the primary RF output is disabled; if DB6 is set to 1, the primary RF output is enabled.

Output Power

Bits[DB5:DB4] set the value of the primary RF output power level (see Figure 30).

REGISTER 7

Control Bits

With Bits[C4:C1] set to 0111, Register 7 is programmed. Figure 31 shows the input data format for programming this register.

Fractional-N Lock Detect Count (LDP)

These bits set the number of consecutive cycles counted by the lock detect circuitry before asserting lock detect high. See Figure 32 for more details.

Loss of Lock Mode

This function should be used if the application is a fixed frequency application in which the reference (REFIN) is likely to be removed, like a clocking application. The standard lock detect circuit assumes that REFIN is always present. This functionality is enabled by setting DB7 to '1'.

Fractional-N Lock Detect Precision (LDP)

These bits set the precision of the lock detect circuitry in Fractional-N mode. Precision of 5, 6, 8 and 12 ns are available.

Lock Detect Mode (LDM)

If the DB3 bit is set to 0, each reference cycle is set by fractional-N lock detect precision as described above . If the DB3 bit is set to 1, each reference cycle is 2.4 ns long, which is more appropriate for integer-N applications.

REGISTERS 8 - 12

These registers are to be programmed with the assigned values as shown in the register maps, figures 32 - 36.

REGISTER INITIALIZATION SEQUENCE

At initial power-up, after the correct application of voltages to the supply pins, the ADF4355-2 registers should be started in the following sequence:

- Register 12
- Register 11
- Register 10
- Register 9
- Register 8
- Register 7
- Register 6
- Register 5
- Register 4
- Register 3
- Register 2
- Register 1
- Register 0

RF SYNTHESIZER—A WORKED EXAMPLE

The following equations are used to program the ADF5355 synthesizer:

$$RF_{OUT} = [INT + (FRAC1 + (FRAC2/MOD2)/MOD1)] \times [f_{PFD}]/RF\ divider \quad (3)$$

where:
RF_{OUT} is the RF frequency output.
INT is the integer division factor.
FRAC1 is the fractionality.
MOD1 is the fixed 24-bit modulus.

FRAC2 is the auxiliary modulus.

MOD2 is the auxiliary modulus.
RF divider is the output divider that divides down the VCO frequency.

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (4)$$

where:
REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.
T is the reference divide-by-2 bit (0 or 1).

For example, in a UMTS system where 2112.6 MHz RF frequency output (RF_{OUT}) is required, a 122.88 MHz reference frequency input (REF_{IN}) is available. Note that the ADF5355 operates in the frequency range of 3.5 GHz to 7.0 GHz. Therefore, the RF divider of 2 should be used (VCO frequency = 4225.2 MHz, RF_{OUT} = VCO frequency/RF divider = 4225.2 MHz/2 = 2112.6 MHz).

It is also important where the loop is closed. In this example, the loop is closed before the output divider (see Figure 37).

The max PFD should be used as much as possible, and with this reference 122.88 MHz can be selected.

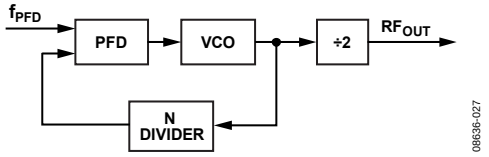


Figure 37 Loop Closed Before Output Divider

N = VCO frequency / PFD,

INT = INT(VCO frequency / PFD),

INT = 34. FRAC = 0.384765625

MOD1 = 15,777,216

FRAC1 = INT (MOD1 x FRAC) = 6070530

Remainder = 0.375 5/8.
MOD2 = 6144 , FRAC2 = 2304.

From Equation 4,

$$f_{PFD} = [122.88\ MHz \times (1 + 0)/2] = 61.44\ MHz \quad (5)$$

$$2112.6\ MHz = [61.44\ MHz \times [(INT + (FRAC1 + FRAC2/MOD2) / 2^{24}])/2 \quad (6)$$

where:
INT = 34.
FRAC = 6,070,530.

FRAC2 = 2304

MOD2 = 6144.

RF divider = 2

REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually improves noise performance by 3 dB. Note that the PFD cannot operate above 125 MHz due to a limitation in the speed of the Σ-Δ circuit of the N divider.

The reference divide-by-2 divides the reference signal by 2, resulting in a 50% duty cycle PFD frequency.

SPURIOUS OPTIMIZATION AND FAST LOCK

Narrow loop bandwidths can filter unwanted spurious signals, but these bandwidths usually have a long lock time. A wider loop bandwidth achieves faster lock times but may lead to increased spurious signals inside the loop bandwidth.

The fast-lock feature can achieve the same fast-lock time as the wider bandwidth but with the advantage of a narrow final loop bandwidth to keep spurs low.

SPUR MECHANISMS

This section describes the three different spur mechanisms that arise with a fractional-N synthesizer and how to minimize them in the ADF4355.

Integer Boundary Spurs

Another mechanism for fractional spur creation is the interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (the purpose of a fractional-N synthesizer), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency. These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth (hence the name integer boundary spurs).

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop may cause a problem. Feedthrough of low levels of on-chip reference switching noise, through the RF_{IN} pin back to the VCO, can result in reference spur levels as high as −90 dBc.

APPLICATIONS INFORMATION

DIRECT CONVERSION MODULATOR

Direct conversion architectures are increasingly being used to implement base station transmitters. Figure 38 shows how Analog Devices, Inc., parts can be used to implement such a system.

The circuit block diagram shows the AD9788 TxDAC® being used with the ADL5375. The use of dual integrated DACs, such as the AD9788 ensures minimum error contribution (over temperature) from this portion of the signal chain.

The local oscillator (LO) is implemented using the ADF4355-2. The low-pass filter was designed using ADIsimPLL™ for a channel spacing of 200 kHz and a closed-loop bandwidth of 20 kHz.

The LO ports of the ADL5375 can be driven differentially from the complementary $RF_{OUT}A$ and $RF_{OUT}B$ outputs of the ADF4355-2. This gives better performance than a single-ended LO driver and eliminates the use of a balun to convert from a single-ended LO input to the more desirable differential LO input for the ADL5375.

The ADL5375 accepts LO drive levels from −10 dBm to 0 dBm. The optimum LO power can be software programmed on the ADF4355-2, which allows levels from −4 dBm to +5 dBm from each output.

The RF output is designed to drive a 50 Ω load, but it must be ac-coupled, as shown in Figure. If the I and Q inputs are driven in quadrature by 2 V p-p signals, the resulting output power from the ADL5375 modulator is approximately 2 dBm.

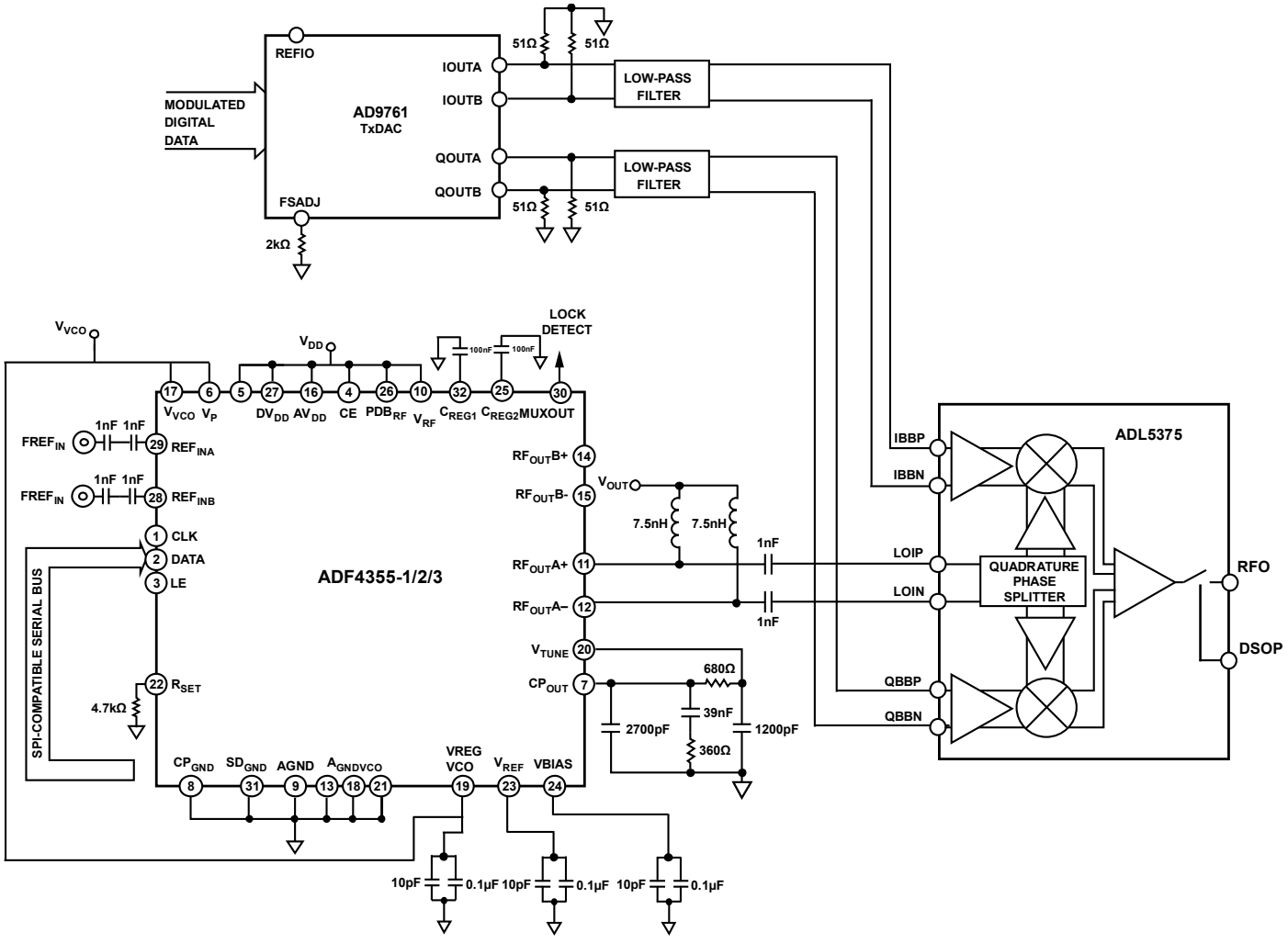


Figure 38. Direct Conversion Modulator

POWER SUPPLIES

The ADF5355 contains four multi-band VCO's which together cover an octave range of frequencies. To ensure best performance it is vital that a low noise regulator like the ADM7150 is connected to the V_{VCO} pin. Better VCO noise will result if this clean supply is connected to the V_{REGVCO} pin, and the internal LDO disabled in software. The same regulator can be connected to V_{VCO}, V_{REGVCO} and V_P.

For the 3.3V supply pins, one ADM7150 regulator can be used. The connections can be made as shown in figure 40 below.

.

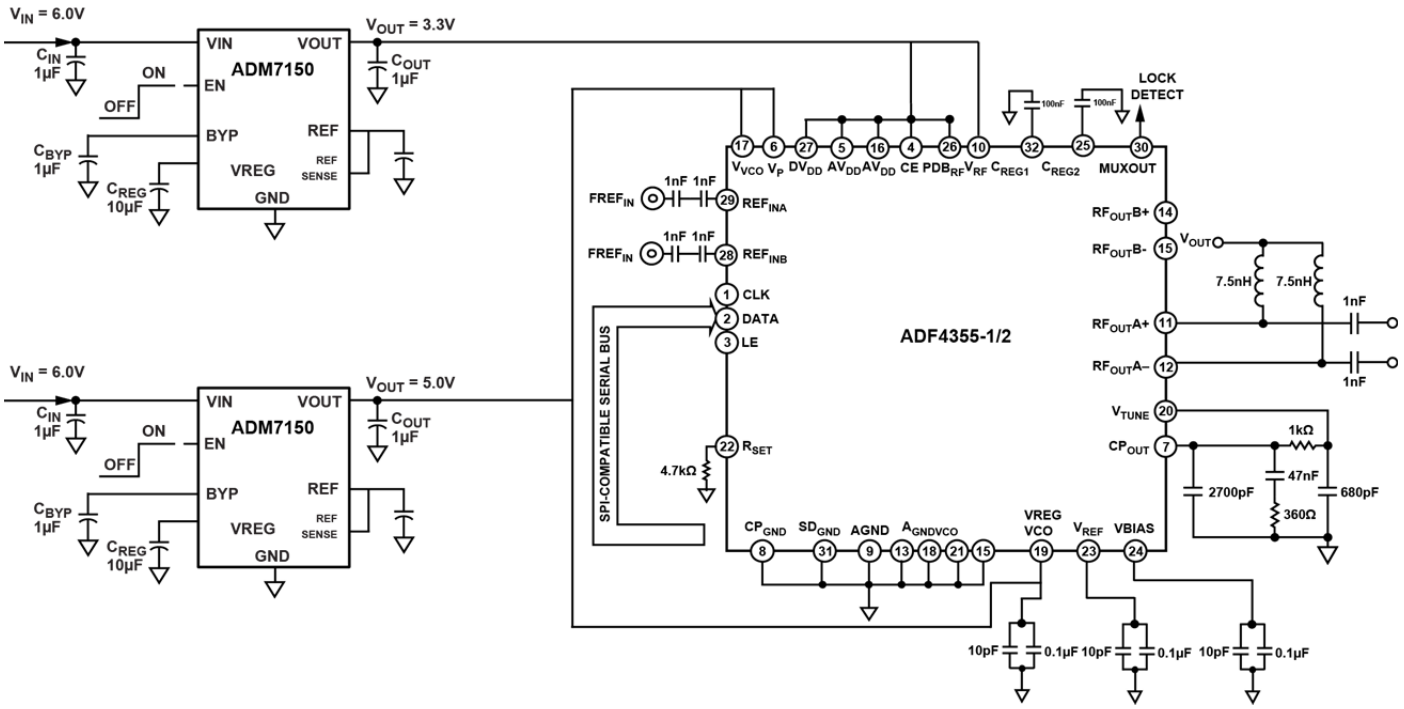


Figure 39. ADF5355 Power Supplies

PCB DESIGN GUIDELINES FOR A CHIP SCALE PACKAGE

The lands on the chip scale package (CP-32-2) are rectangular. The PCB pad for these lands must be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Each land must be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central exposed thermal pad. The thermal pad on the PCB must be at least as large as the exposed pad. On the PCB, there must be a minimum clearance of 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the PCB thermal pad to improve the thermal performance of the package. If vias are used, they must be incorporated into the thermal pad at 1.2 mm pitch grid. The via diameter must be between 0.3 mm and 0.33 mm, and the via barrel must be plated with 1 oz. of copper to plug the via.

The ADF4355 has internal matching which only requires an AC coupling capacitor on each output pin. Each differential pair should have equivalent terminations to each pin. Mismatched loads can cause a distorted output to appear.

For increased output power, a better solution is to use a shunt inductor (acting as an RF choke) to V_{VCO}. This gives a more output power.

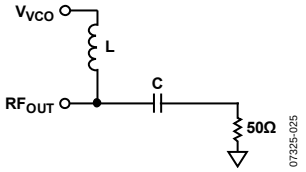


Figure 40. Optimum ADF4355-2 Output Stage

For lower frequencies it is better to use a larger inductor.

See Table 6 below:

Table 6. Matching Components

Frequency Range (MHz)	L (nH)	C (nF)
137.5 to 1000	120	1
1000 to 3000	7.5	1
3000 to 4400	4.7	1

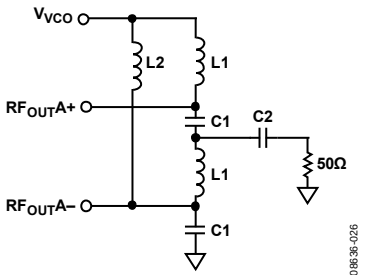


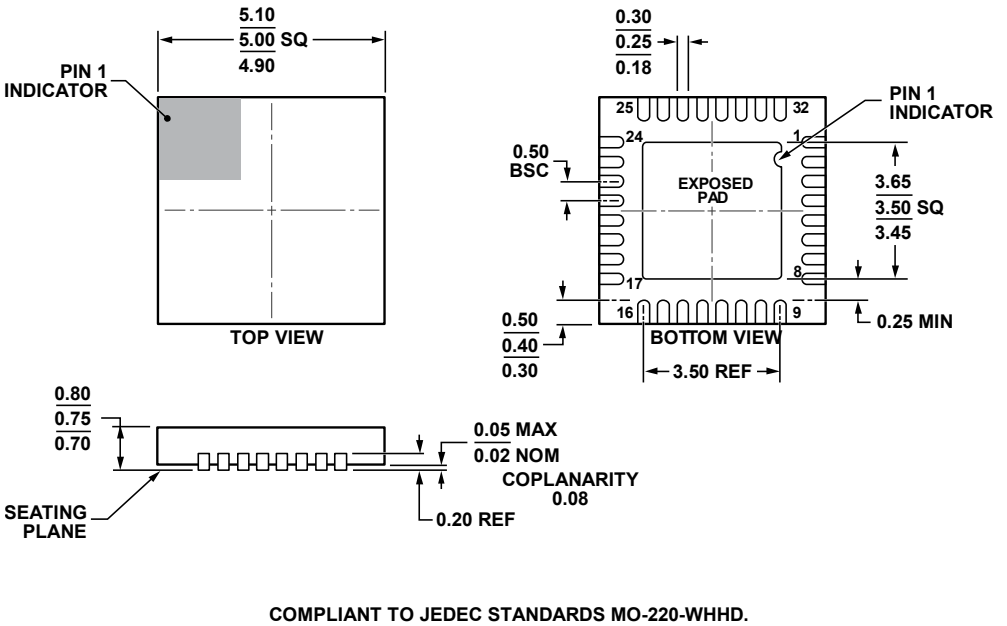
Figure 41. ADF4355-2 LC Balun

A balun using discrete inductors and capacitors can be implemented with the architecture shown in Figure . The LC balun comprises Component L1 and Component C1. L2 provides a dc path for $RF_{OUT}A-$, and Capacitor C2 is used for dc blocking.

Table 7. LC Balun Components

Frequency Range (MHz)	Inductor L1 (nH)	Capacitor C1 (pF)	RF Choke Inductor L2 (nH)	DC Blocking Capacitor C2 (pF)	Measured Output Power (dBm)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 44. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very, Very Thin Quad
(CP-32-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4355-2BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-11
ADF4355-2BCPZ-RL7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-11
EV-ADF4355-2SD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

PR12452-0-5/14(PrG)