LC²MOS
5 Ω R_{ON} SPST Switches

ADG451/ADG452/ADG453

FEATURES

- Low on resistance (4 Ω)
- On resistance flatness (0.2 Ω)
- 44 V supply maximum ratings
- ±15 V analog signal range
- Fully specified at ±5 V, +12 V, ±15 V
- Ultralow power dissipation (18 µW)
- ESD 2 kV
- Continuous current (100 mA)
- Fast switching times
  - t_{ON} 70 ns
  - t_{OFF} 60 ns
- TTL/CMOS-compatible
- Pin-compatible upgrade for ADG411/ADG412/ADG413 and ADG431/ADG432/ADG433

APPLICATIONS

- Relay replacement
- Audio and video switching
- Automatic test equipment
- Precision data acquisition
- Battery-powered systems
- Sample-and-hold systems
- Communication systems
- PBX, PABX systems
- Avionics

FUNCTIONAL BLOCK DIAGRAMS

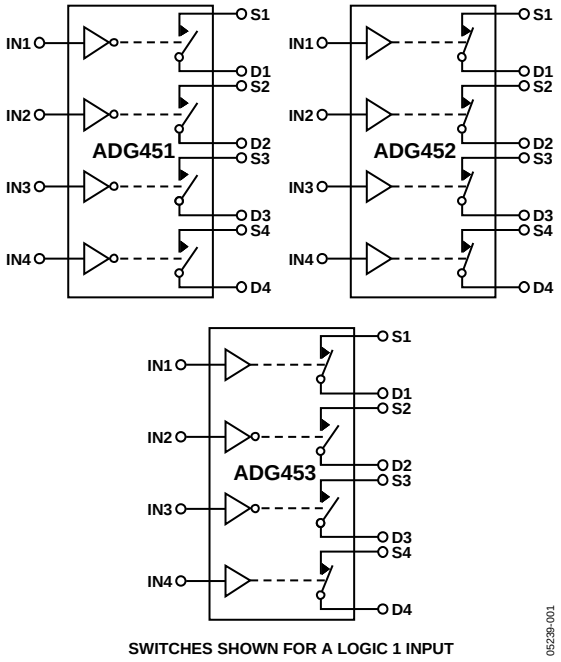

Figure 1.

GENERAL DESCRIPTION

The ADG451/ADG452/ADG453 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed, coupled with high signal bandwidth, makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG451/ADG452/ADG453 contain four independent single-pole/single-throw (SPST) switches. The ADG451 and ADG452 differ only in that the digital control logic is inverted. The ADG451 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG452. The ADG453 has two switches with digital control logic similar to that of the ADG451, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG453 exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

Rev. B

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REVISION HISTORY

12/04—Rev. A to Rev. B

Updated Format ..... Universal
Changes to Specifications Section 3
Changes to Absolute Maximum Ratings Section 8
Changes to Pin Configuration and Function Descriptions Section 9
Updated Outline Dimensions 16
Changes to Ordering Guide 17

2/98—Rev. 0 to Rev. A

10/97—Revision 0: Initial Version

PRODUCT HIGHLIGHTS

1. Low R_{ON} (5 Ω maximum)

2. Ultralow Power Dissipation

3. Extended Signal Range
   The ADG451/ADG452/ADG453 are fabricated on an enhanced LC²MOS process, giving an increased signal range that fully extends to the supply rails.

4. Break-Before-Make Switching
   This prevents channel shorting when the switches are configured as a multiplexer (ADG453 only.)

5. Single-Supply Operation
   For applications in which the analog signal is unipolar, the ADG451/ADG452/ADG453 can be operated from a single rail power supply. The parts are fully specified with a single 12 V power supply and remain functional with single supplies as low as 5.0 V.

6. Dual-Supply Operation
   For applications where the analog signal is bipolar, the ADG451/ADG452/ADG453 can be operated from a dual power supply ranging from ±4.5 V to ±20 V.

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V, V_{SS} = −15 V, V_L = +5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	B Version[1]			
Parameter	**25°C**	**T_{MIN} to T_{MAX}**	**Unit**	**Test Conditions/Comments**
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	4		Ω typ	V_D = −10 V to +10 V, I_S = −10 mA
	5	7	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_D = ±10 V, I_S = −10 mA
	0.5	0.5	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.2		Ω typ	V_D = −5 V, 0 V, +5 V, I_S = −10 mA
	0.5	0.5	Ω max	
LEAKAGE CURRENTS[2]				
Source Off Leakage, I_S (Off)	±0.02		nA typ	V_D = ±10 V, V_S = ±10 V; Figure 15
	±0.5	±2.5	nA max	
Drain Off Leakage, I_D (Off)	±0.02		nA typ	V_D = ±10 V, V_S = ±10 V; Figure 15
	±0.5	±2.5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04		nA typ	V_D = V_S = ±10 V; Figure 16
	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}; all others = 2.4 V or 0.8 V, respectively
		±0.5	μA max	
DYNAMIC CHARACTERISTICS[3]				
t_{ON}	70		ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = ±10 V; Figure 17
	180	220	ns max	
t_{OFF}	60		ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = ±10 V; Figure 17
	140	180	ns max	
Break-Before-Make Time Delay, t_D (ADG453 Only)	15		ns typ	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = +10 V; Figure 18
	5	5	ns min	
Charge Injection	20		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1.0 nF; Figure 19
	30		pC max	
Off Isolation	65		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 20
Channel-to-Channel Crosstalk	−90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 21
C_S (Off)	37		pF typ	f = 1 MHz
C_D (Off)	37		pF typ	f = 1 MHz
C_D, C_S (On)	140		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V; digital inputs = 0 V or 5 V
I_{DD}	0.0001		μA typ	
	0.5	5	μA max	

Parameter	B Version[1] 25°C	B Version[1] T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
I_{SS}	0.0001		µA typ	
	0.5	5	µA max	
I_L	0.0001		µA typ	
	0.5	5	µA max	
I_{GND}	0.0001		µA typ	
	0.5	5	µA max	

[1] Temperature range for B Version is −40°C to +85°C.
[2] T_{MAX} = 70°C.
[3] Guaranteed by design, not subject to production test.

V_{DD} = 12 V, V_{SS} = 0 V, V_L = 5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Version[1] 25°C	B Version[1] T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6		Ω typ	V_D = 0 V to +10 V, I_S = −10 mA
	8	10	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_D = +10 V, I_S = −10 mA
	0.5	0.5	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.0	1.0	Ω typ	V_D = 0 V, +5 V, I_S = −10 mA
LEAKAGE CURRENTS[2, 3]				
Source Off Leakage, I_S (Off)	±0.02		nA typ	V_D = 0 V, 10 V, V_S = 0 V, 10 V; Figure 15
	±0.5	±2.5	nA max	
Drain Off Leakage, I_D (Off)	±0.02		nA typ	V_D = 0 V, 10 V, V_S = 0 V, 10 V; Figure 15
	±0.5	±2.5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04		nA typ	V_D = V_S = 0 V, 10 V; Figure 16
	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	µA max	
DYNAMIC CHARACTERISTICS[4]				
t_{ON}	100		ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V; Figure 17
	220	260	ns max	
t_{OFF}	80		ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V; Figure 17
	160	200	ns max	
Break-Before-Make Time Delay, t_D (ADG453 Only)	15		ns typ	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 8 V; Figure 18
	10	10	ns min	
Charge Injection	10		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1.0 nF; Figure 19
Channel-to-Channel Crosstalk	−90		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 21
C_S (Off)	60		pF typ	f = 1 MHz
C_D (Off)	60		pF typ	f = 1 MHz
C_D, C_S (On)	100		pF typ	f = 1 MHz

Parameter	B Version[1] 25°C	B Version[1] T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = 13.2 V; digital inputs = 0 V or 5 V
I_{DD}	0.0001		µA typ	
	0.5	5	µA max	
I_L	0.0001		µA typ	
	0.5	5	µA max	V_L = 5.5 V
I_{GND}[4]	0.0001		µA typ	
	0.5	5	µA max	V_L = 5.5 V

[1] Temperature range for B Version is −40°C to +85°C.
[2] T_{MAX} = 70°C.
[3] Tested with dual supplies.
[4] Guaranteed by design, not subject to production test.

V_{DD} = +5 V, V_{SS} = −5 V, V_L = +5 V, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Version[1] 25°C	B Version[1] T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	7		Ω typ	V_D = −3.5 V to +3.5 V, I_S = −10 mA
	12	15	Ω max	
On Resistance Match Between Channels (ΔR_{ON})	0.3		Ω typ	V_D = 3.5 V, I_S = −10 mA
	0.5	0.5	Ω max	
LEAKAGE CURRENTS[2, 3]				
Source Off Leakage, I_S (Off)	±0.02		nA typ	V_D = ±4.5, V_S = ±4.5; Figure 15
	±0.5	±2.5	nA max	
Drain Off Leakage, I_D (Off)	±0.02		nA typ	V_D = 0 V, 5 V, V_S = 0 V, 5 V; Figure 15
	±0.5	±2.5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04		nA typ	V_D = V_S = 0 V, 5 V; Figure 16
	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5	µA max	
DYNAMIC CHARACTERISTICS[4]				
t_{ON}	160		ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V; Figure 17
	220	300	ns max	
t_{OFF}	60		ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 3 V; Figure 17
	140	180	ns max	
Break-Before-Make Time Delay, t_D (ADG453 Only)	50		ns typ	R_L = 300 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 3 V; Figure 18
	5	5	ns min	
Charge Injection	10		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1.0 nF; Figure 19
Off Isolation	65		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 20
Channel-to-Channel Crosstalk	−76		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 21
C_S (Off)	48		pF typ	f = 1 MHz
C_D (Off)	48		pF typ	f = 1 MHz
C_D, C_S (On)	148		pF typ	f = 1 MHz

Parameter	B Version[1] 25°C	B Version[1] T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
POWER REQUIREMENTS				V_{DD} = 5.5 V; digital inputs = 0 V or 5 V
I_{DD}	0.0001		µA typ	
	0.5	5	µA max	
I_{SS}	0.0001		µA typ	
	0.5	5	µA max	
I_L	0.0001		µA typ	
	0.5	5	µA max	V_L = 5.5 V
I_{GND}[4]	0.0001		µA typ	
	0.5	5	µA max	V_L = 5.5 V

[1] Temperature range for B Version is −40°C to +85°C.
[2] T_{MAX} = 70°C.
[3] Tested with dual supplies.
[4] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameters	Ratings
V_{DD} to V_{SS}	44 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[1]	V_{SS} −2 V to V_{DD} +2 V or 30 mA, whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D (pulsed at 1 ms, 10% duty cycle max)	300 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Plastic DIP Package, Power Dissipation	470 mW
θ_{JA} Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 s)	260°C
SOIC Package, Power Dissipation	600 mW
θ_{JA} Thermal Impedance	77°C/W
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	115°C/W
θ_{JC} Thermal Impedance	35°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C
ESD	2 kV

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Table 5. Truth Table (ADG451/ADG452)

ADG451 In	ADG452 In	Switch Condition
0	1	On
1	0	Off

Table 6. Truth Table (ADG453)

Logic	Switch 1, 4	Switch 2, 3
0	Off	On
1	On	Off

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

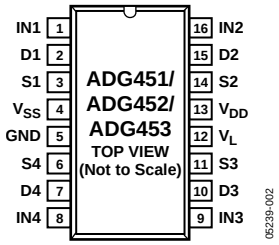


Figure 2. Pin Configuration (DIP, SOIC, TSSOP)

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	D1	Drain Terminal. Can be an input or an output.
3	S1	Source Terminal. Can be an input or an output.
4	V_{SS}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to GND.
5	GND	Ground (0 V) Reference.
6	S4	Source Terminal. Can be an input or an output.
7	D4	Drain Terminal. Can be an input or an output.
8	IN4	Logic Control Input.
9	IN3	Logic Control Input.
10	D3	Drain Terminal. Can be an input or an output.
11	S3	Source Terminal. Can be an input or an output.
12	V_L	Logic Power Supply (5 V).
13	V_{DD}	Most Positive Power Supply Potential.
14	S2	Source Terminal. Can be an input or an output.
15	D2	Drain Terminal. Can be an input or an output.
16	IN2	Logic Control Input.

TERMINOLOGY

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
On resistance match between any two channels, that is, R_{ON} maximum minus R_{ON} minimum.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)
Source leakage current with the switch off.

I_D(Off)
Drain leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_D (V_S)
Analog voltage on terminals D and S.

C_S (Off)
Off switch source capacitance.

C_D (Off)
Off switch drain capacitance.

C_D, C_S (On)
On switch capacitance.

t_{ON}
Delay between applying the digital control input and the output switching on. See Figure 17.

t_{OFF}
Delay between applying the digital control input and the output switching off.

t_D
Off time or on time measured between the 90% points of both switches, when switching from one address state to another. See Figure 18.

Crosstalk
A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

TYPICAL PERFORMANCE CHARACTERISTICS

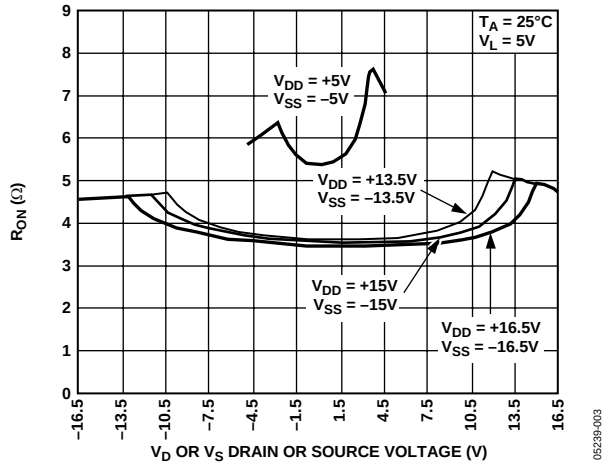


Figure 3. On Resistance as a Function of V_D (V_S) for Various Dual Supplies

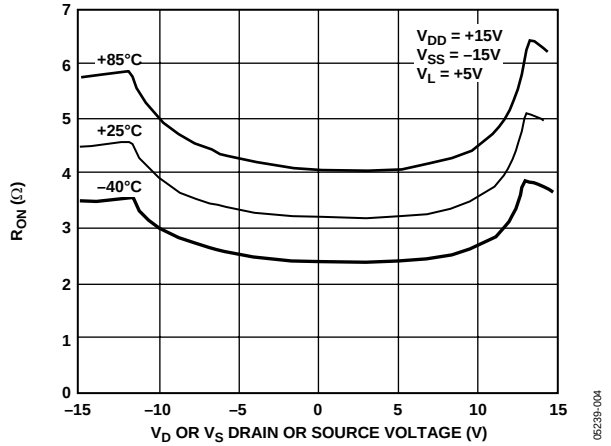


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures with Dual Supplies

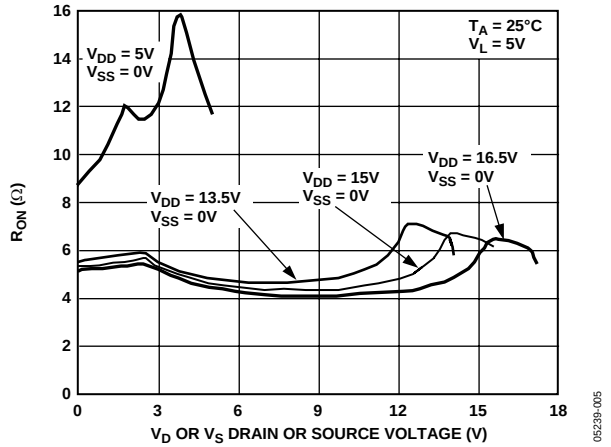


Figure 5. On Resistance as a Function of V_D (V_S) for Various Single Supplies

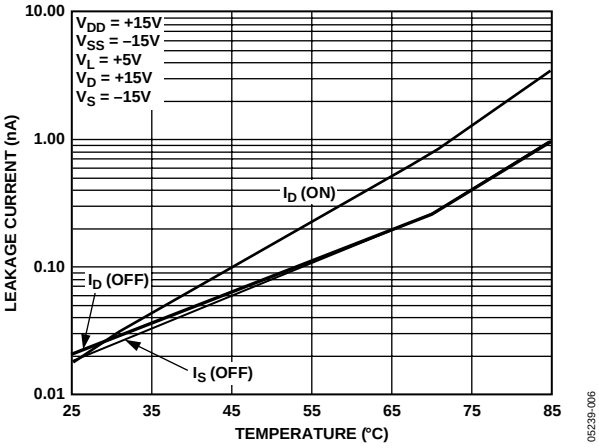


Figure 6. Leakage Currents as a Function of Temperature

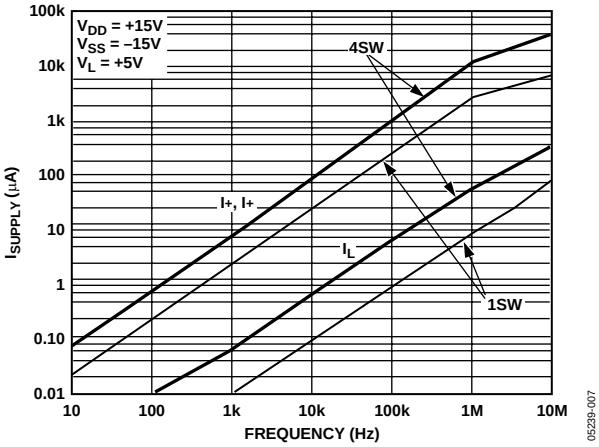


Figure 7. Supply Current vs. Input Switching Frequency

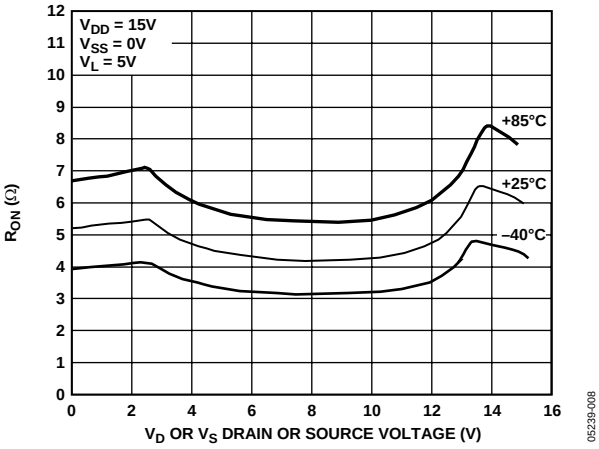


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures with Single Supplies

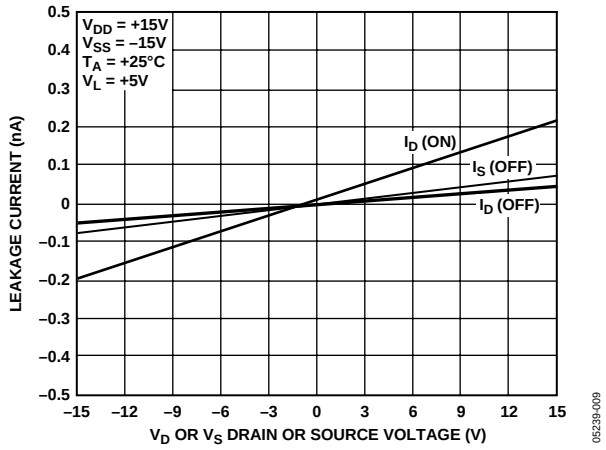


Figure 9. Leakage Currents as a Function of V_D (V_S)

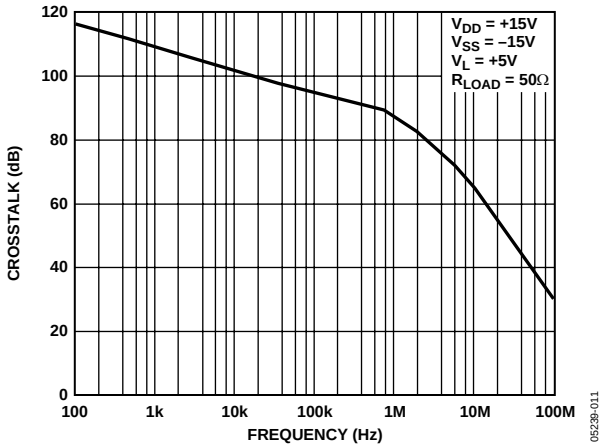


Figure 11. Crosstalk vs. Frequency

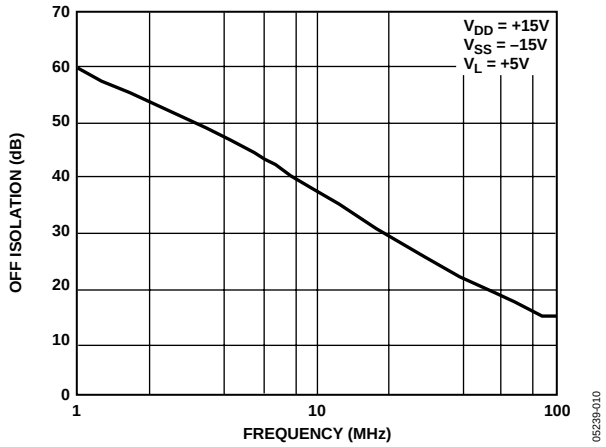


Figure 10. Off Isolation vs. Frequency

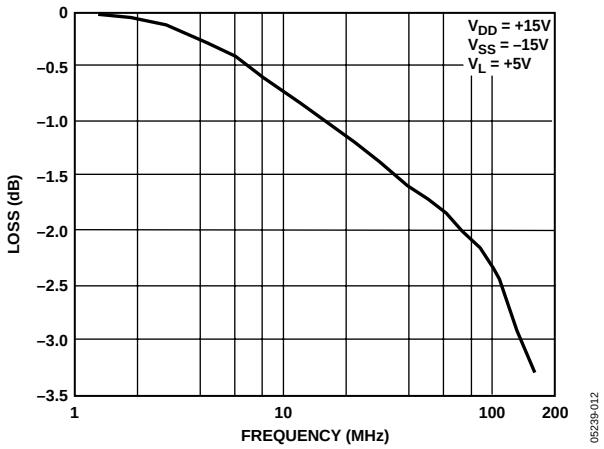


Figure 12. Frequency Response with Switch On

APPLICATIONS

Figure 13 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer, and the output operational amplifier is an AD711. During track mode, SW1 is closed and the output, V_{OUT}, follows the input signal, V_{IN}. In hold mode, SW1 is opened, and the signal is held by the hold capacitor, C_H.

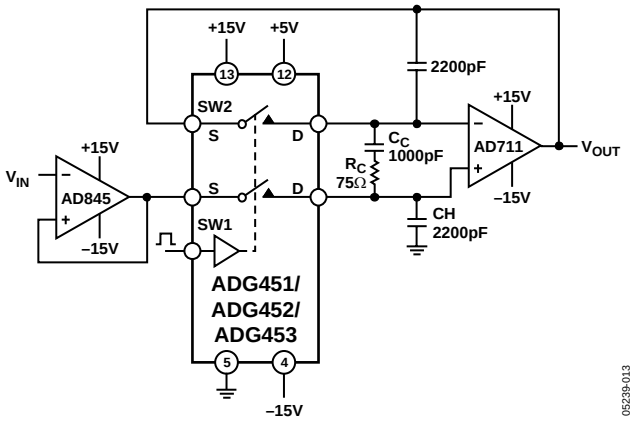


Figure 13. Fast, Accurate Sample-and-Hold Circuit

Due to switch and capacitor leakage, the voltage on the hold capacitor decreases with time. The ADG451/ADG452/ADG453 minimize this droop due to their low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 μV/μs.

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Because both switches are at the same potential, they have a differential effect on the op amp, AD711, which minimizes charge injection effects. Pedestal error is also reduced by the compensation network, R_C and C_C. This compensation network reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±10 V input range. Both the acquisition and settling times are 850 ns.

TEST CIRCUITS

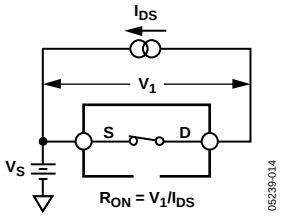


Figure 14. On Resistance

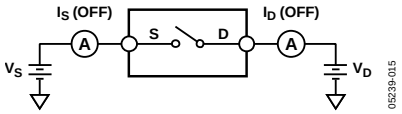


Figure 15. Off Leakage

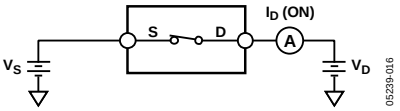


Figure 16. On Leakage

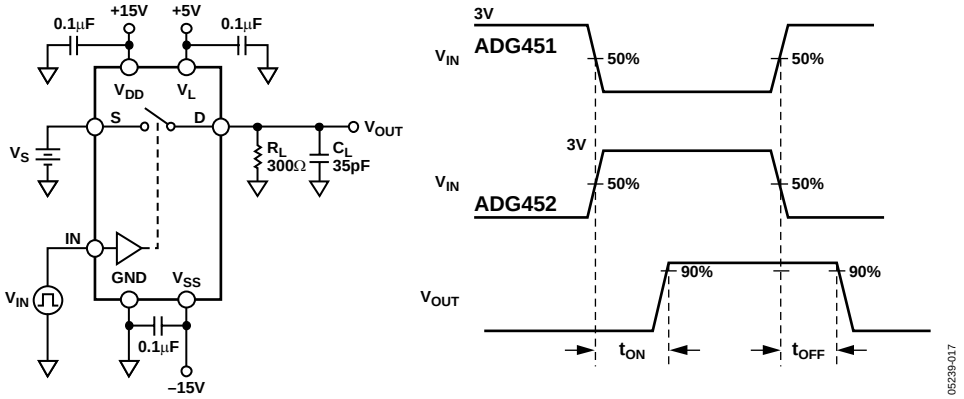


Figure 17. Switching Times

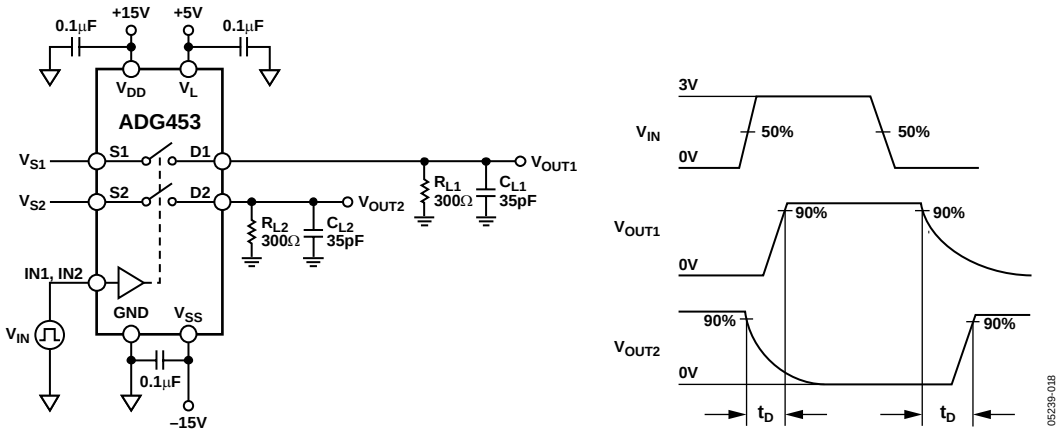


Figure 18. Break-Before-Make Time Delay

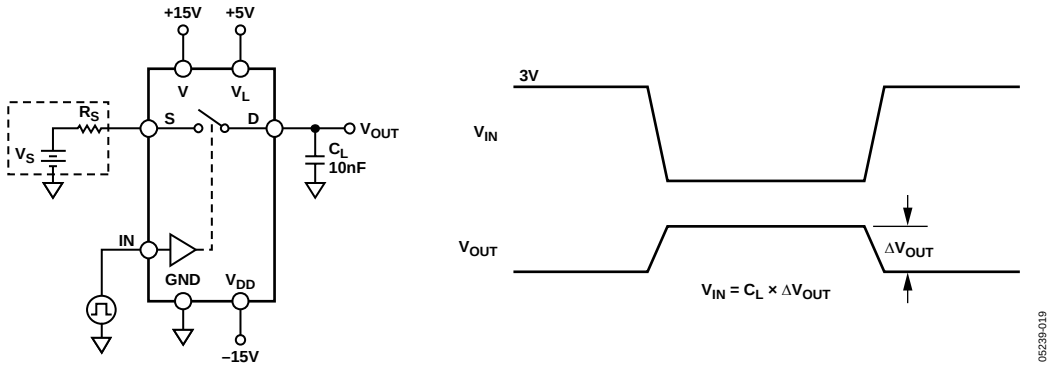


Figure 19. Charge Injection

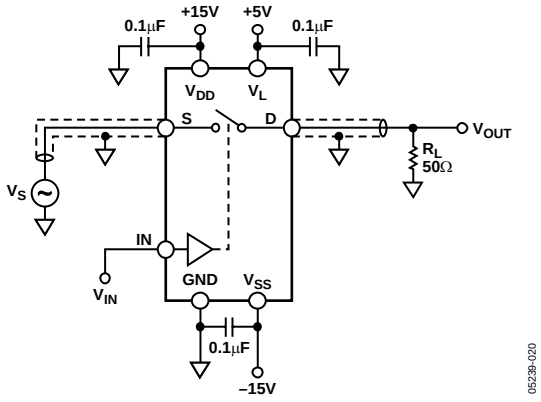
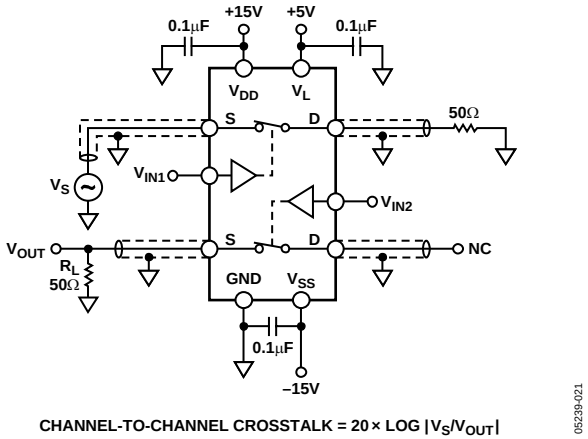


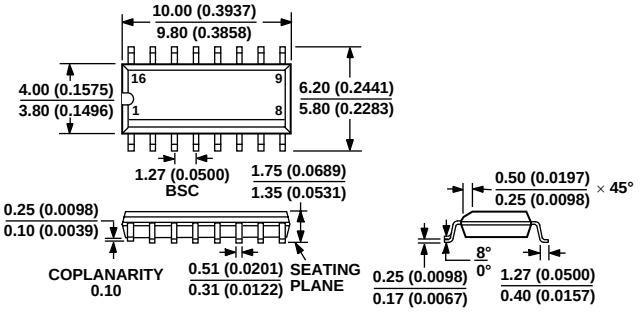
Figure 20. Off Isolation



CHANNEL-TO-CHANNEL CROSSTALK = 20 × LOG |V_S/V_{OUT}|

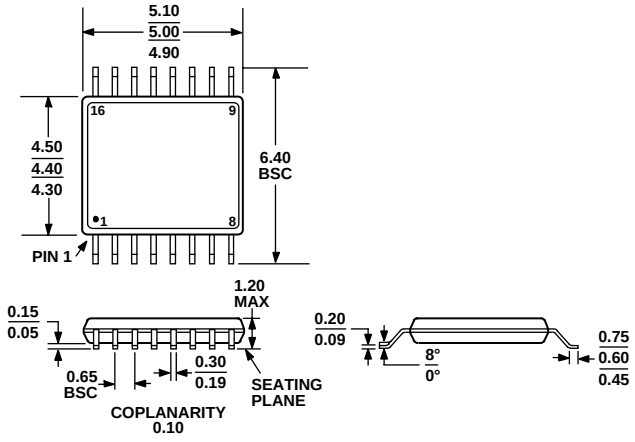
Figure 21. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS



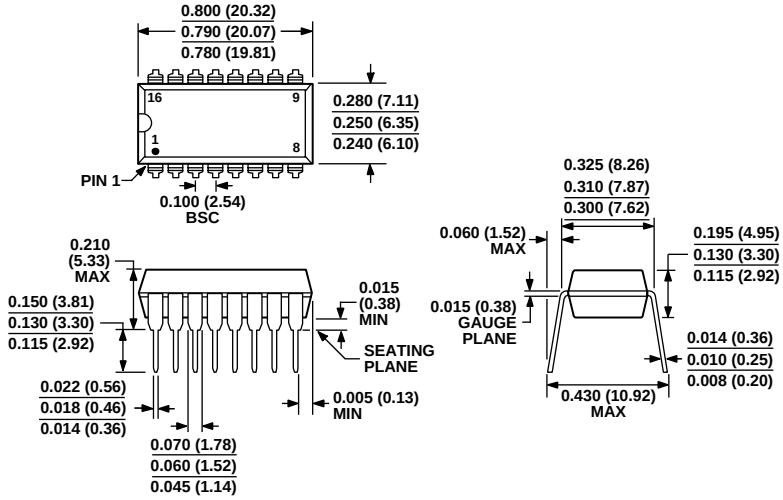
COMPLIANT TO JEDEC STANDARDS MS-012AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 22. 16-lead Small Outline Package [SOIC]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 23. 16-lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001-AB
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 24. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
ADG451BN	−40°C to +85°C	16-Lead Plastic DIP	N-16
ADG451BNZ[1]	−40°C to +85°C	16-Lead Plastic DIP	N-16
ADG451BR	−40°C to +85°C	16-lead SOIC	R-16
ADG451BR-REEL	−40°C to +85°C	16-lead SOIC	R-16
ADG451BR-REEL7	−40°C to +85°C	16-lead SOIC	R-16
ADG451BRZ[1]	−40°C to +85°C	16-lead SOIC	R-16
ADG451BRUZ[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG451BRUZ- REEL[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG451BRUZ- REEL7[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG451BCHIPS		DIE	
ADG452BN	−40°C to +85°C	16-Lead Plastic DIP	N-16
ADG452BR	−40°C to +85°C	16-lead SOIC	R-16
ADG452BR-REEL	−40°C to +85°C	16-lead SOIC	R-16
ADG452BR-REEL7	−40°C to +85°C	16-lead SOIC	R-16
ADG452BRZ[1]	−40°C to +85°C	16-lead SOIC	R-16
ADG452BRZ-REEL[1]	−40°C to +85°C	16-lead SOIC	R-16
ADG452BRZ-REEL7[1]	−40°C to +85°C	16-lead SOIC	R-16
ADG452BRUZ[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG452BRUZ-REEL[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG452BRUZ-REEL7[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG453BN	−40°C to +85°C	16-Lead Plastic DIP	N-16
ADG453BR	−40°C to +85°C	16-lead SOIC	R-16
ADG453BR-REEL	−40°C to +85°C	16-lead SOIC	R-16
ADG453BR-REEL7	−40°C to +85°C	16-lead SOIC	R-16
ADG453BRZ[1]	−40°C to +85°C	16-lead SOIC	R-16
ADG453BRUZ[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG453BRUZ-REEL[1]	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG453BRUZ-REEL7[1]	−40°C to +85°C	16-Lead TSSOP	RU-16

[1] Z = Pb-free part.

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