

FEATURES

Latch-up proof

Human body model (HBM) ESD rating: 8 kV

Low on resistance (13.5 Ω)

± 9 V to ± 22 V dual-supply operation

9 V to 40 V single-supply operation

48 V supply maximum ratings

Fully specified at ± 15 V, ± 20 V, $+12$ V, and $+36$ V

V_{SS} to V_{DD} analog signal range

APPLICATIONS

Relay replacement

Automatic test equipment

Data acquisition

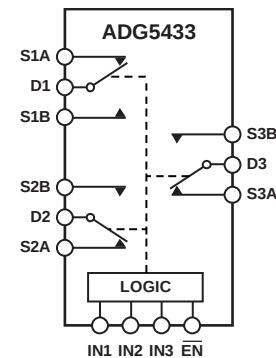
Instrumentation

Avionics

Audio and video switching

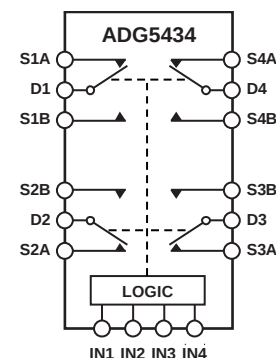
Communication systems

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR
A LOGIC 1 INPUT.

Figure 1. ADG5433 TSSOP and LFCSP_WQ



SWITCHES SHOWN FOR
A LOGIC 1 INPUT.

Figure 2. ADG5434 TSSOP

GENERAL DESCRIPTION

The ADG5433 and ADG5434 are monolithic industrial CMOS analog switches comprising three independently selectable single-pole, double-throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{\text{EN}}$ input on the ADG5433 (LFCSP and TSSOP packages) is used to enable or disable the device. When disabled, all channels are switched off.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} .
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG5433/ADG5434 can be operated from dual supplies up to ± 22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG5433/ADG5434 can be operated from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
6. No V_I logic power supply required.

Rev. B

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REVISION HISTORY

5/12—Rev. A to Rev. B

Removed Automotive Information (Throughout).....	1
Changes to Ordering Guide	22
Deleted Automotive Products Section.....	22

6/11—Rev. 0 to Rev. A

Change to Features Section	1
Change to I _{SS} Parameter, Table 2.....	5
Changes to Figure 4.....	10
Updated Outline Dimensions	21
Changes to Ordering Guide	22
Added Automotive Products Section.....	22

10/10—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance, R _{ON}	13.5 15	18	22	Ω typ Ω max	V _S = ±10 V, I _S = −10 mA; see Figure 26 V _{DD} = +13.5 V, V _{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR _{ON}	0.3			Ω typ	V _S = ±10 V, I _S = −10 mA
On-Resistance Flatness, R _{FLAT (ON)}	0.8	1.3	1.4	Ω max	V _S = ±10 V, I _S = −10 mA
	1.8			Ω typ	
	2.2	2.6	3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.05 ±0.25	±1	±7	nA typ nA max	V _{DD} = +16.5 V, V _{SS} = −16.5 V V _S = ±10 V, V _D = ∓10 V; see Figure 29
Drain Off Leakage, I _D (Off)	±0.1 ±0.4	±4	±30	nA typ nA max	V _S = ±10 V, V _D = ∓10 V; see Figure 29
Channel On Leakage, I _D (On), I _S (On)	±0.1 ±0.4	±4	±30	nA typ nA max	V _S = V _D = ±10 V; see Figure 25
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	V _{IN} = V _{GND} or V _{DD}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.002		±0.1	μA typ μA max	
Digital Input Capacitance, C _{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, t _{TRANSITION}	157 207	245	272	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 10 V
t _{ON} ($\overline{\text{EN}}$)	160			ns typ	R _L = 300 Ω, C _L = 35 pF
t _{OFF} ($\overline{\text{EN}}$)	196	241	274	ns max	V _S = 10 V; see Figure 34
	91			ns typ	R _L = 300 Ω, C _L = 35 pF
Break-Before-Make Time Delay, t _D	106	138	140	ns max	V _S = 10 V; see Figure 34
	45			ns typ	R _L = 300 Ω, C _L = 35 pF
			21	ns min	V _{S1} = V _{S2} = 10 V; see Figure 33
Charge Injection, Q _{INJ}	130			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 35
Off Isolation	−60			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 28
Channel-to-Channel Crosstalk	−60			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; Figure 27
Total Harmonic Distortion + Noise	0.01			% typ	R _L = 1 kΩ, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	145			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 31
Insertion Loss	−0.9			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 31
C _S (Off)	14			pF typ	V _S = 0 V, f = 1 MHz
C _D (Off)	24			pF typ	V _S = 0 V, f = 1 MHz
C _D (On), C _S (On)	53			pF typ	V _S = 0 V, f = 1 MHz

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
I_{DD}	45			$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
I_{SS}	55		70	$\mu\text{A max}$	
	0.001		1	$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
V_{DD}/V_{SS}			$\pm 9/\pm 22$	$\mu\text{A max}$	GND = 0 V
				V min/V max	

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	12.5			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$; see Figure 26
	14	17	21	Ω max	$V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	2.3			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
	2.7	3.1	3.5	Ω max	
LEAKAGE CURRENTS					$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 29
	± 0.25	± 1	± 7	nA max	
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 29
	± 0.4	± 4	± 30	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 15\text{ V}$; see Figure 25
	± 0.4	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	$\mu\text{A max}$	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, $t_{TRANSITION}$	150			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	199	230	253	ns max	$V_S = 10\text{ V}$
$t_{ON}(\overline{EN})$	152			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	186	223	253	ns max	$V_S = 10\text{ V}$; see Figure 34
$t_{OFF}(\overline{EN})$	90			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	104	118	130	ns max	$V_S = 10\text{ V}$; see Figure 34
Break-Before-Make Time Delay, t_D	36			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			17	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 33
Charge Injection, Q_{INJ}	176			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 35
Off Isolation	−60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
Channel-to-Channel Crosstalk	−60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion + Noise	0.012			% typ	$R_L = 1\text{ k}\Omega$, 20 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 30
−3 dB Bandwidth	140			MHz typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$; see Figure 31
Insertion Loss	−0.8			dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 31
C_S (Off)	15			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	23			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	52			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	50			μA typ	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$
	70		110	μA max	Digital inputs = 0 V or V_{DD}
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	26			Ω typ	$V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$; see Figure 26
	30	36	42	Ω max	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.3			Ω typ	$V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$
	1	1.5	1.6	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	5.5			Ω typ	$V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$
	6.5	8	12	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = 13.2\text{ V}$, $V_{SS} = 0\text{ V}$
	± 0.25	± 1	± 7	nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 29
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 29
	± 0.4	± 4	± 30	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = 1\text{ V}/10\text{ V}$; see Figure 25
	± 0.4	± 4	± 30	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, $t_{TRANSITION}$	220			ns typ	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$
	290	357	400	ns max	$V_S = 8\text{ V}$
$t_{ON}(\overline{EN})$	228			ns typ	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$
	289	370	426	ns max	$V_S = 8\text{ V}$; see Figure 34
$t_{OFF}(\overline{EN})$	90			ns typ	$R_L = 300\text{ }\Omega$, $C_L = 35\text{ pF}$
	115	131	151	ns max	$V_S = 8\text{ V}$; see Figure 34

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Break-Before-Make Time Delay, t_D	106		54	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ $V_{S1} = V_{S2} = 8\ \text{V}$; see Figure 33
Charge Injection, Q_{INJ}	60			pC typ	$V_S = 6\ \text{V}$, $R_S = 0\ \Omega$, $C_L = 1\ \text{nF}$; see Figure 35
Off Isolation	−60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 28
Channel-to-Channel Crosstalk	−60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.1			% typ	$R_L = 1\ \text{k}\Omega$, $6\ \text{V p-p}$, $f = 20\ \text{Hz}$ to $20\ \text{kHz}$; see Figure 30
−3 dB Bandwidth	150			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$; see Figure 31
Insertion Loss	−0.8			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 31
C_S (Off)	18			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (Off)	28			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (On), C_S (On)	54			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
POWER REQUIREMENTS					$V_{DD} = 13.2\ \text{V}$
I_{DD}	40 50		65 9/40	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = $0\ \text{V}$ or V_{DD}
V_{DD}				V min/V max	$\text{GND} = 0\ \text{V}$, $V_{SS} = 0\ \text{V}$

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36\ \text{V} \pm 10\%$, $V_{SS} = 0\ \text{V}$, $\text{GND} = 0\ \text{V}$, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$0\ \text{V}$ to V_{DD}	V	
On Resistance, R_{ON}	14.5			Ω typ	$V_S = 0\ \text{V}$ to $30\ \text{V}$, $I_S = -10\ \text{mA}$; see Figure 26
On-Resistance Match Between Channels, ΔR_{ON}	16 0.3	19	23	Ω max Ω typ	$V_{DD} = 32.4\ \text{V}$, $V_{SS} = 0\ \text{V}$ $V_S = 0\ \text{V}$ to $30\ \text{V}$, $I_S = -10\ \text{mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.8 3.5 4.3	1.3 5.5	1.4 6.5	Ω max Ω typ Ω max	$V_S = 0\ \text{V}$ to $30\ \text{V}$, $I_S = -10\ \text{mA}$
LEAKAGE CURRENTS					$V_{DD} = 39.6\ \text{V}$, $V_{SS} = 0\ \text{V}$
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$; see Figure 29
Drain Off Leakage, I_D (Off)	± 0.25 ± 0.1	± 1	± 7	nA max nA typ	$V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$; see Figure 29
Channel On Leakage, I_D (On), I_S (On)	± 0.4 ± 0.1 ± 0.4	± 4	± 30	nA max nA typ nA max	$V_S = V_D = 1\ \text{V}/30\ \text{V}$; see Figure 25
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002		± 0.1	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	6			pF typ	

Parameter	25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{\text{TRANSITION}}$	180			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
$t_{\text{ON}}(\overline{\text{EN}})$	262	274	289	ns max	$V_S = 18\ \text{V}$
	176			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
$t_{\text{OFF}}(\overline{\text{EN}})$	216	238	268	ns max	$V_S = 18\ \text{V}$; see Figure 34
	98			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
Break-Before-Make Time Delay, t_D	123	127	129	ns max	$V_S = 18\ \text{V}$; see Figure 34
	50			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
Charge Injection, Q_{INJ}			21	ns min	$V_{S1} = V_{S2} = 18\ \text{V}$; see Figure 33
	150			pC typ	$V_S = 18\ \text{V}$, $R_S = 0\ \Omega$, $C_L = 1\ \text{nF}$; see Figure 35
Off Isolation	–60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 28
Channel-to-Channel Crosstalk	–60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.4			% typ	$R_L = 1\ \text{k}\Omega$, 18 V p-p, $f = 20\ \text{Hz}$ to 20 kHz; see Figure 30
–3 dB Bandwidth	135			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$; see Figure 31
Insertion Loss	–1			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 31
C_S (Off)	18			pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
C_D (Off)	28			pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
C_D (On), C_S (On)	46			pF typ	$V_S = 18\ \text{V}$, $f = 1\ \text{MHz}$
POWER REQUIREMENTS					
I_{DD}	80			μA typ	$V_{\text{DD}} = 39.6\ \text{V}$
	100		130	μA max	Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	GND = 0 V, $V_{\text{SS}} = 0\ \text{V}$

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx**Table 5. ADG5433**

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	80	58	36	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	147	103	70	mA maximum
$V_{DD} = +20\text{ V}$, $V_{SS} = -20\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	85	63	39	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	156	109	74	mA maximum
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	63	45	28	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	116	84	53	mA maximum
$V_{DD} = 36\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	83	60	37	mA maximum
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	151	107	72	mA maximum

Table 6. ADG5434

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	70	51	31	mA maximum
$V_{DD} = +20\text{ V}$, $V_{SS} = -20\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	74	54	33	mA maximum
$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	54	39	23	mA maximum
$V_{DD} = 36\text{ V}$, $V_{SS} = 0\text{ V}$				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	73	53	32	mA maximum

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	
ADG5433	280 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5434	240 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx ²	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
20-Lead TSSOP (4-Layer Board)	143°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

¹ Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

² See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

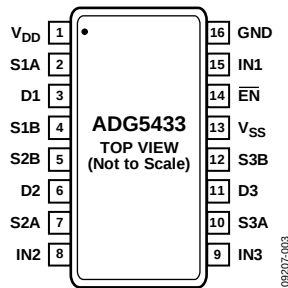
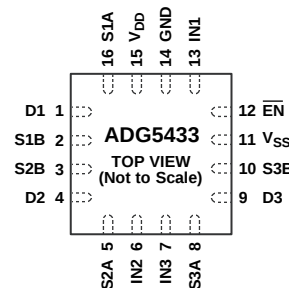


Figure 3. ADG5433 TSSOP Pin Configuration



NOTES
1. EXPOSED PAD IS TIED TO SUBSTRATE, V_{SS}.

Figure 4. ADG5433 LFCSP_WQ Pin Configuration

Table 8. ADG5433 Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP_WQ		
1	15	V _{DD}	Most Positive Power Supply Potential.
2	16	S1A	Source Terminal 1A. This pin can be an input or an output.
3	1	D1	Drain Terminal 1. This pin can be an input or an output.
4	2	S1B	Source Terminal 1B. This pin can be an input or an output.
5	3	S2B	Source Terminal 2B. This pin can be an input or an output.
6	4	D2	Drain Terminal 2. This pin can be an input or an output.
7	5	S2A	Source Terminal 2A. This pin can be an input or an output.
8	6	IN2	Logic Control Input 2.
9	7	IN3	Logic Control Input 3.
10	8	S3A	Source Terminal 3A. This pin can be an input or an output.
11	9	D3	Drain Terminal 3. This pin can be an input or an output.
12	10	S3B	Source Terminal 3B. This pin can be an input or an output.
13	11	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
14	12	$\overline{\text{EN}}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, IN _x logic inputs determine the on switches.
15	13	IN1	Logic Control Input 1.
16	14	GND	Ground (0 V) Reference.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

Table 9. ADG5433 Truth Table

EN	IN _x	S _x A	S _x B
1	X	Off	Off
0	0	Off	On
0	1	On	Off

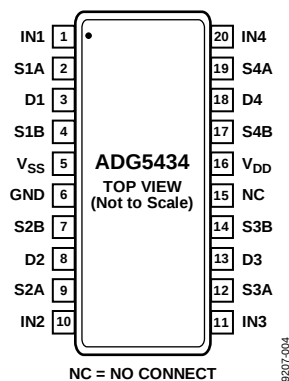


Figure 5. ADG5434 TSSOP Pin Configuration

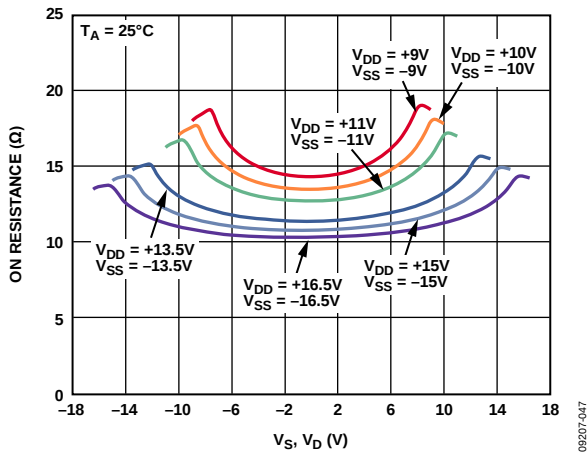
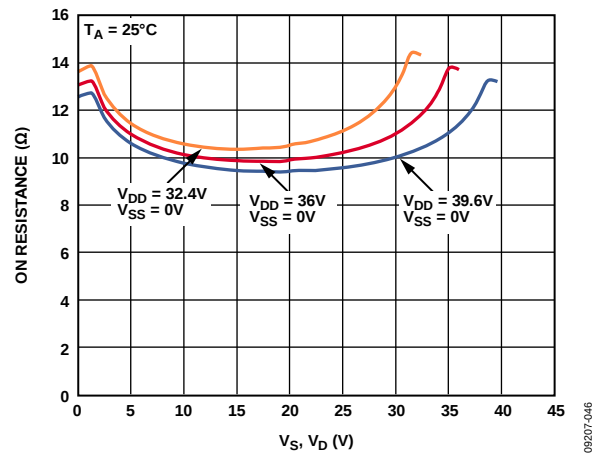
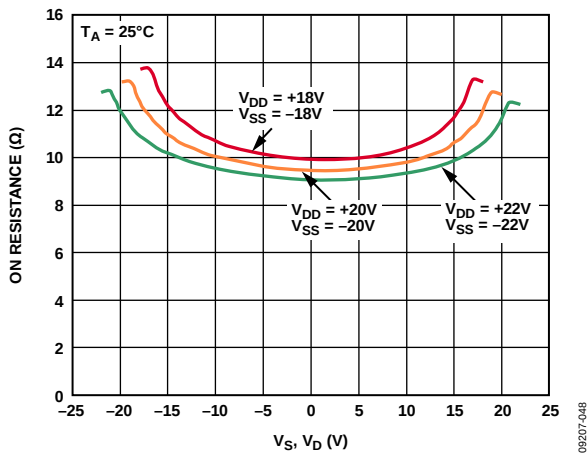
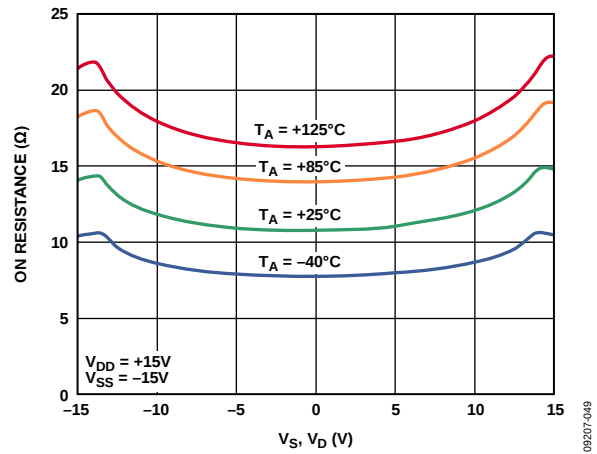
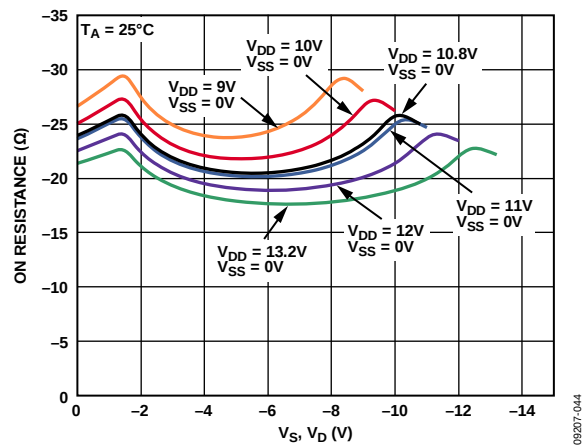
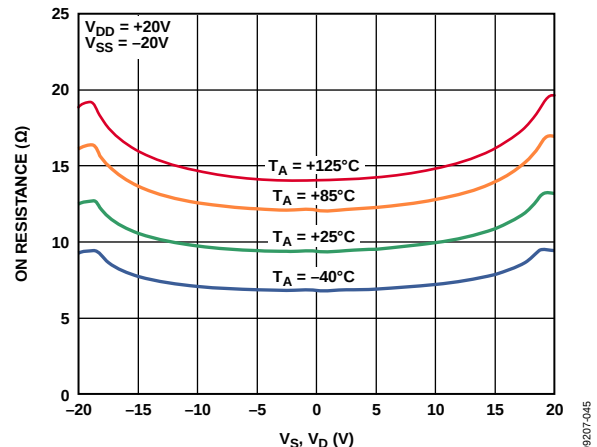
Table 10. ADG5434 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input 1.
2	S1A	Source Terminal 1A. This pin can be an input or an output.
3	D1	Drain Terminal 1. This pin can be an input or an output.
4	S1B	Source Terminal 1B. This pin can be an input or an output.
5	V _{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
6	GND	Ground (0 V) Reference.
7	S2B	Source Terminal 2B. This pin can be an input or an output.
8	D2	Drain Terminal 2. This pin can be an input or an output.
9	S2A	Source Terminal 2A. This pin can be an input or an output.
10	IN2	Logic Control Input 2.
11	IN3	Logic Control Input 3.
12	S3A	Source Terminal 3A. This pin can be an input or an output.
13	D3	Drain Terminal 3. This pin can be an input or an output.
14	S3B	Source Terminal 3B. This pin can be an input or an output.
15	NC	No Connect.
16	V _{DD}	Most Positive Power Supply Potential.
17	S4B	Source Terminal 4B. This pin can be an input or an output.
18	D4	Drain Terminal 4. This pin can be an input or an output.
19	S4A	Source Terminal 4A. This pin can be an input or an output.
20	IN4	Logic Control Input 4.

Table 11. ADG5434 Truth Table

IN _x	S _x A	S _x B
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 6. On Resistance as a Function of V_S, V_D (Dual Supply)Figure 9. On Resistance as a Function of V_S, V_D (Single Supply)Figure 7. On Resistance as a Function of V_S, V_D (Dual Supply)Figure 10. On Resistance as a Function of V_S (V_D) for Different Temperatures, $\pm 15\text{ V}$ Dual SupplyFigure 8. On Resistance as a Function of V_S, V_D (Single Supply)Figure 11. On Resistance as a Function of V_S (V_D) for Different Temperatures, $\pm 20\text{ V}$ Dual Supply

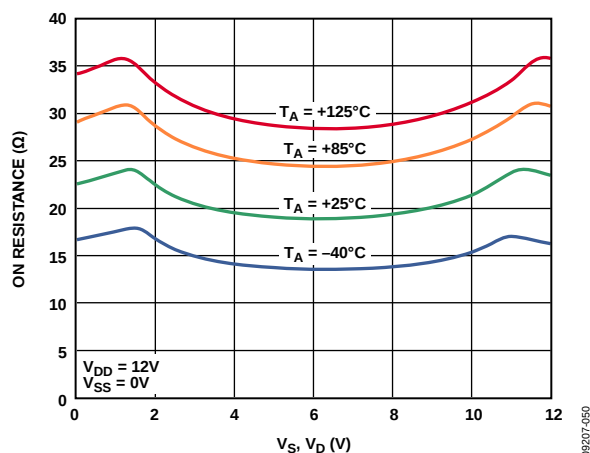


Figure 12. On Resistance as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

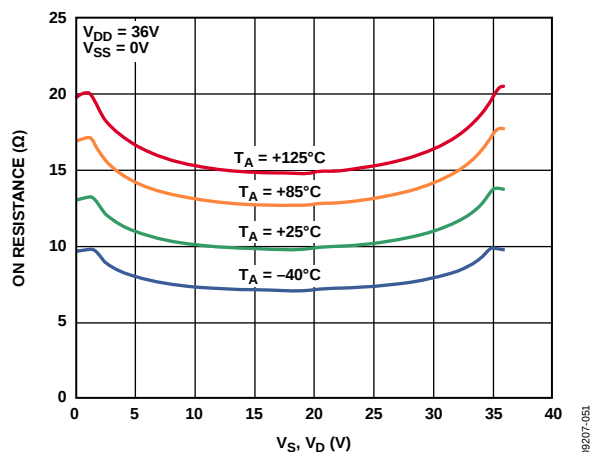


Figure 13. On Resistance as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

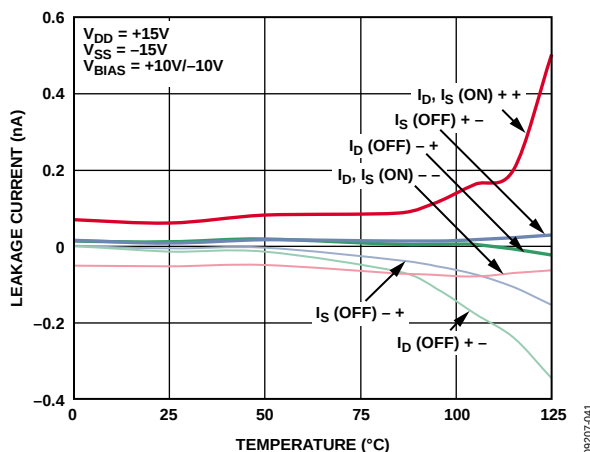


Figure 14. Leakage Currents as a Function of Temperature, ± 15 V Dual Supply

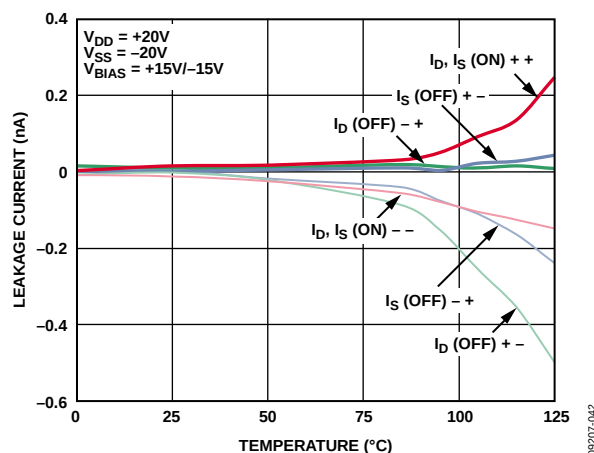


Figure 15. Leakage Currents as a Function of Temperature, ± 20 V Dual Supply

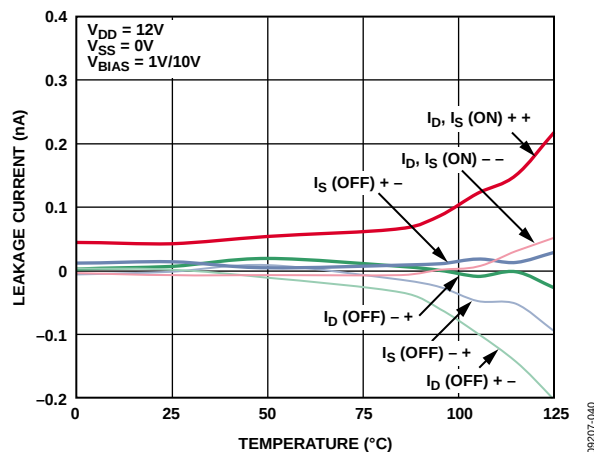


Figure 16. Leakage Currents as a Function of Temperature, 12 V Single Supply

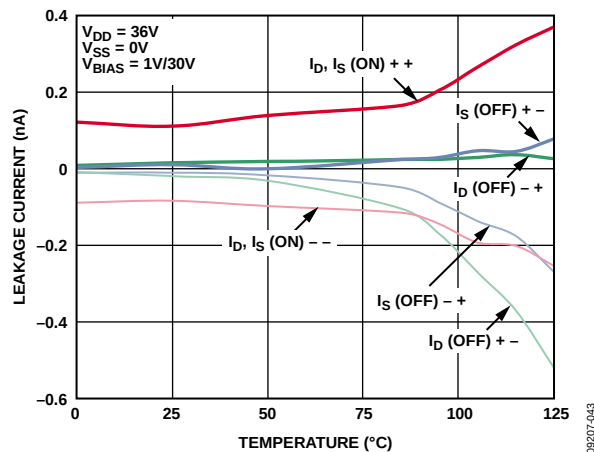


Figure 17. Leakage Currents as a Function of Temperature, 36 V Single Supply

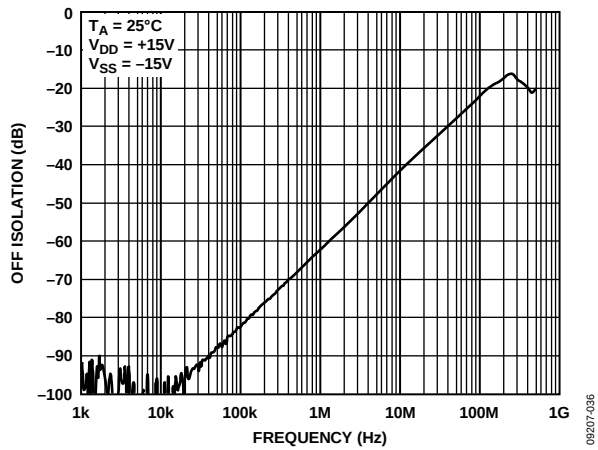


Figure 18. Off Isolation vs. Frequency

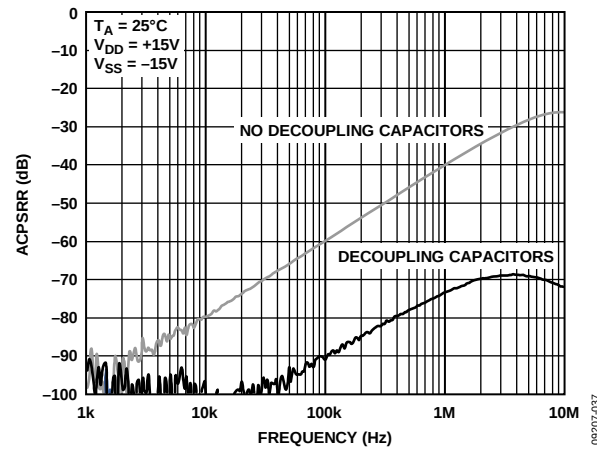


Figure 21. ACPSR vs. Frequency

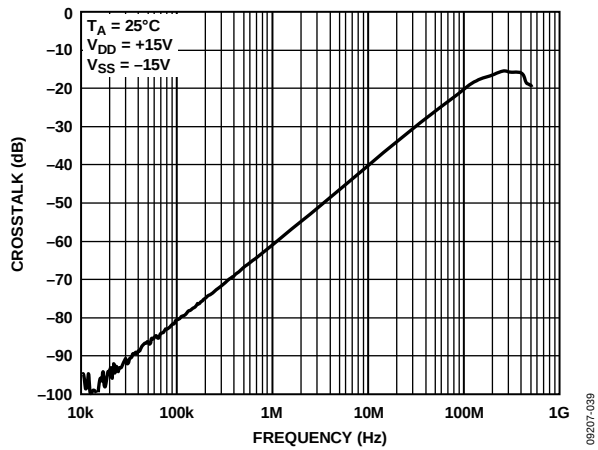


Figure 19. Crosstalk vs. Frequency

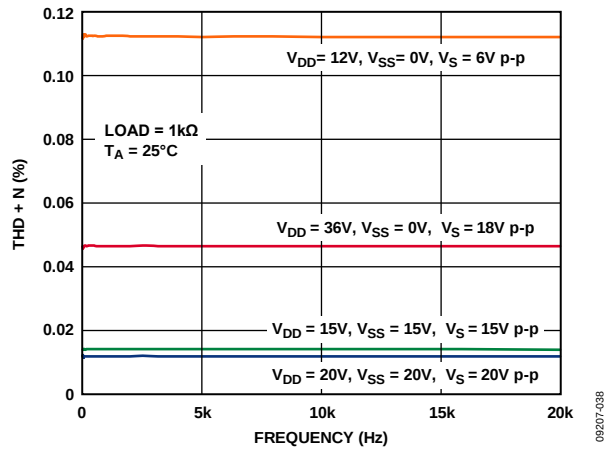


Figure 22. THD + N vs. Frequency

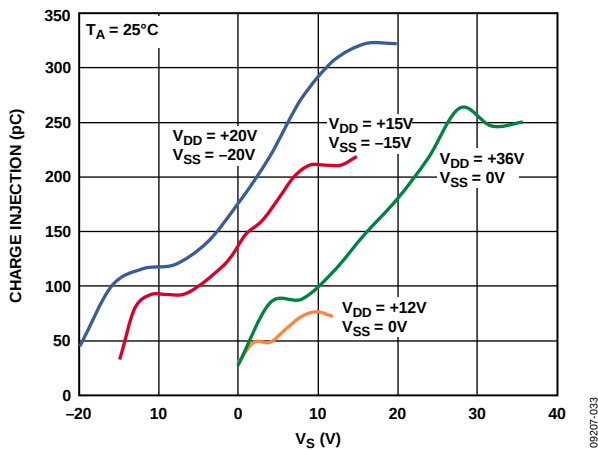


Figure 20. Charge Injection vs. Source Voltage

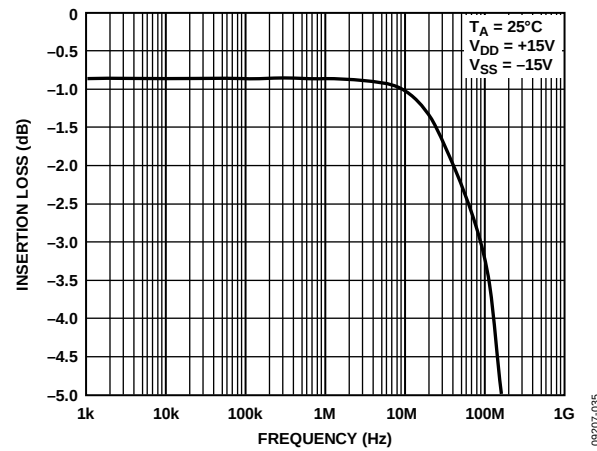


Figure 23. Bandwidth

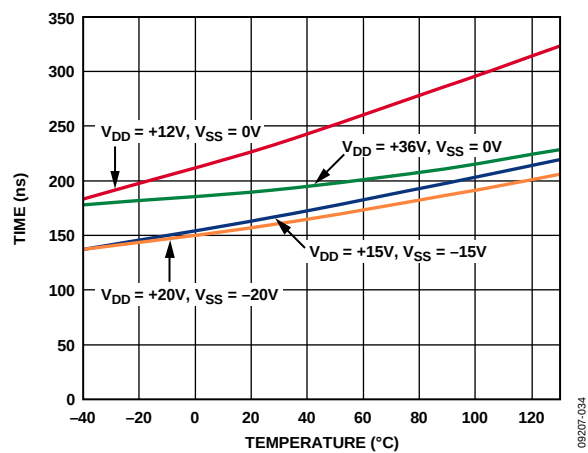


Figure 24. $t_{\text{TRANSITION}}$ Times vs. Temperature

TEST CIRCUITS

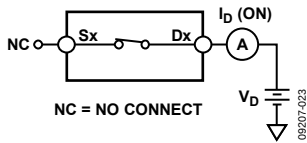


Figure 25. On Leakage

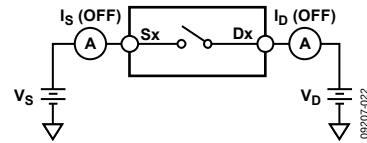


Figure 29. Off Leakage

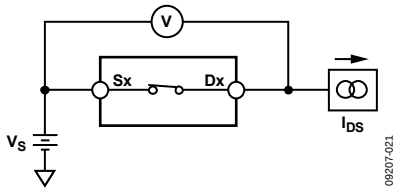


Figure 26. On Resistance

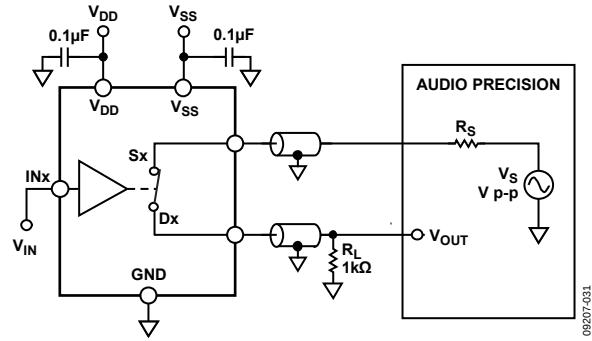


Figure 30. THD + Noise

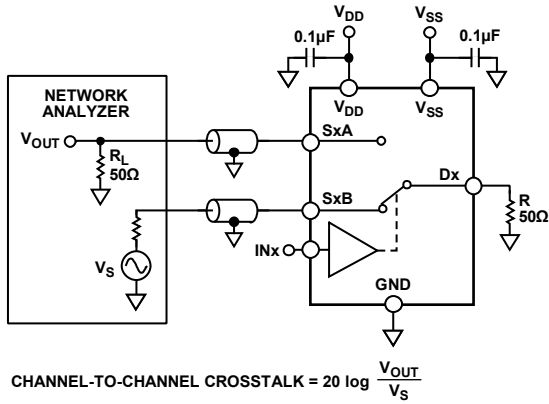


Figure 27. Channel-to-Channel Crosstalk

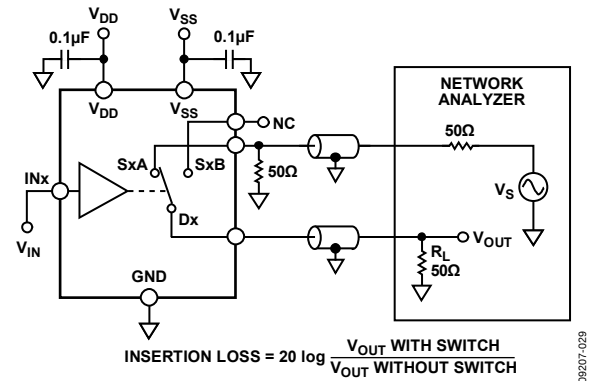


Figure 31. Bandwidth

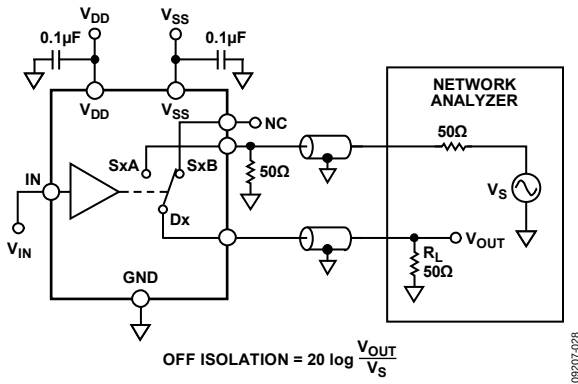


Figure 28. Off Isolation

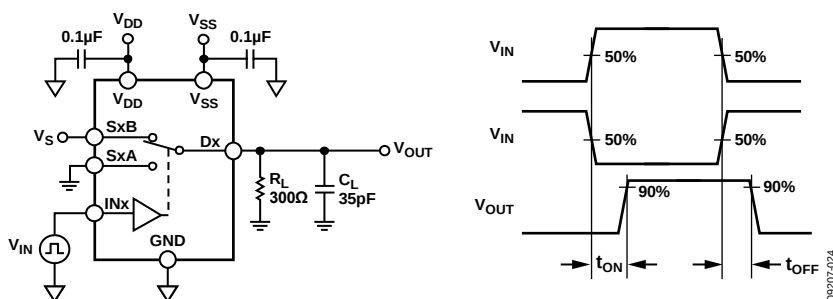


Figure 32. Switching Timing

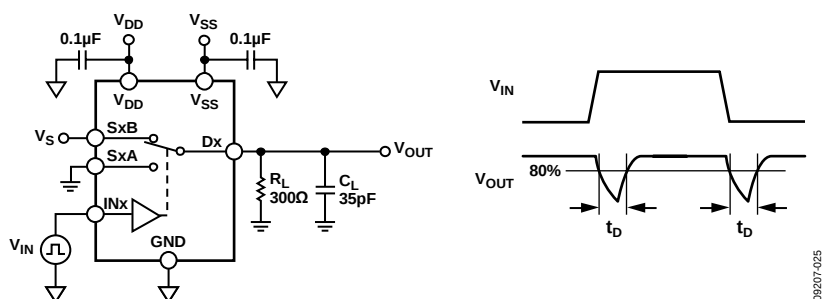
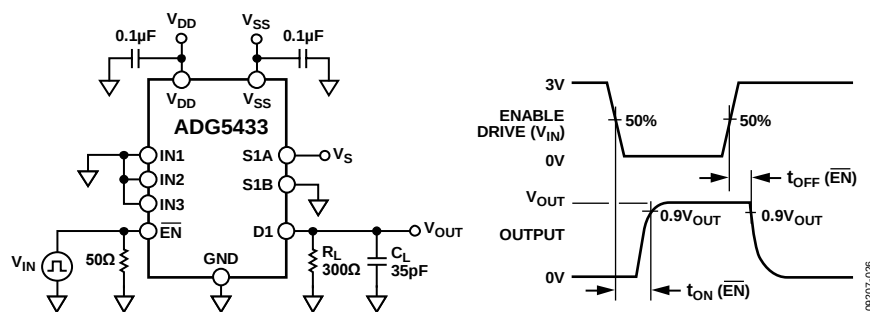
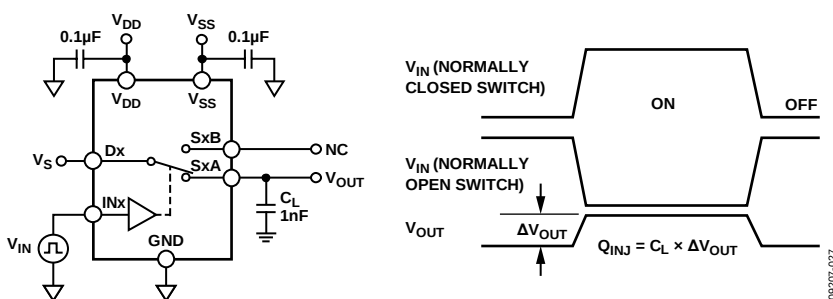
Figure 33. Break-Before-Make Delay, t_D Figure 34. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$ 

Figure 35. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance as measured over the specified analog signal range is represented by $R_{FLAT(ON)}$.

$I_S(Off)$

$I_S(Off)$ is the source leakage current with the switch off.

$I_D(Off)$

$I_D(Off)$ is the drain leakage current with the switch off.

$I_D(On), I_S(On)$

$I_D(On)$ and $I_S(On)$ represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

$C_D(Off)$

$C_D(Off)$ represents the off switch drain capacitance, which is measured with reference to ground.

$C_S(Off)$

$C_S(Off)$ represents the off switch source capacitance, which is measured with reference to ground.

$C_D(On), C_S(On)$

$C_D(On)$ and $C_S(On)$ represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} represents digital input capacitance.

$t_{ON}(\overline{EN})$

$t_{ON}(\overline{EN})$ represents the delay time between the 50% and 90% points of the digital input and switch on condition.

$t_{OFF}(\overline{EN})$

$t_{OFF}(\overline{EN})$ represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is a measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

TRENCH ISOLATION

In the ADG5433/ADG5434, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

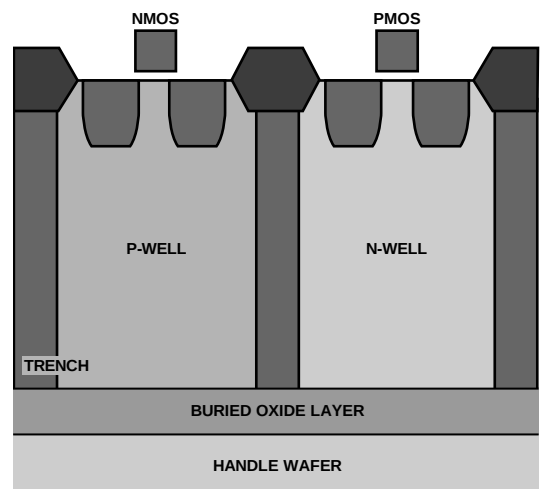


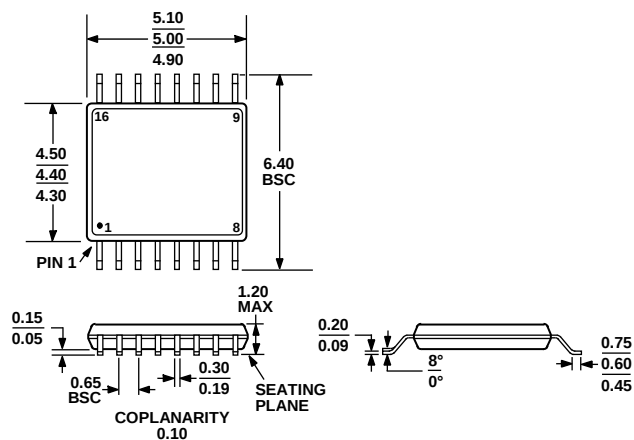
Figure 36. Trench Isolation

APPLICATIONS INFORMATION

The ADG54xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5433/ADG5434 high voltage switches allow single-supply

operation from 9 V to 40 V and dual supply operation from ± 9 V to ± 22 V. The ADG5433/ADG5434 (as well as other select devices within this family) achieve 8 kV human body model ESD ratings, which provide a robust solution eliminating the need for separate protect circuitry designs in some applications.

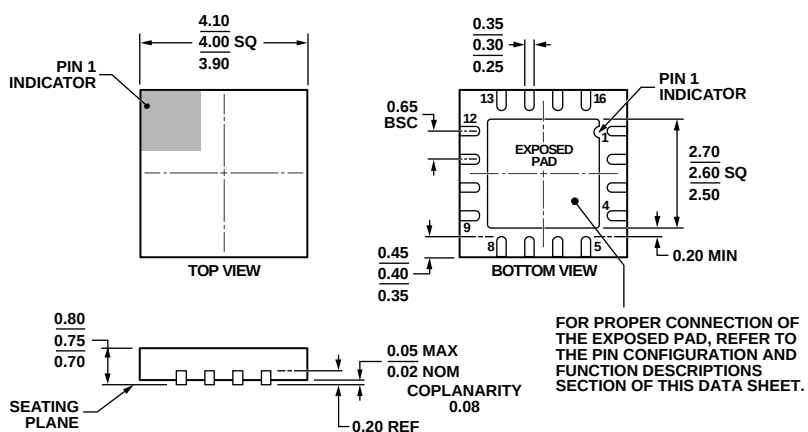
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 37. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm x 4 mm Body, Very Very Thin Quad
(CP-16-17)

Dimensions shown in millimeters

08-16-2010-C

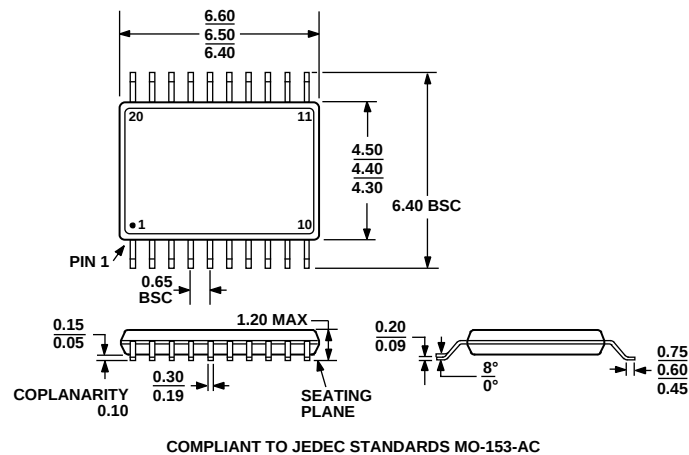


Figure 39. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Description	EN Pin	Package Option
ADG5433BRUZ	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG5433BRUZ-REEL7	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG5433BCPZ-REEL7	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	Yes	CP-16-17
ADG5434BRUZ	–40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG5434BRUZ-REEL7	–40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20

¹ Z = RoHS Compliant Part.

NOTES

NOTES