

FEATURES

- 1.8 V to 5.5 V operation
- Ultralow on resistance
 - 0.4 Ω typical
 - 0.6 Ω maximum at 5 V supply
- Excellent audio performance, ultralow distortion
 - 0.07 Ω typical
 - 0.14 Ω maximum R_{ON} flatness
- High current carrying capability
 - 400 mA continuous
 - 600 mA peak current at 5 V
- Automotive temperature range: -40°C to $+125^{\circ}\text{C}$
- Rail-to-rail switching operation
- Typical power consumption ($<0.1 \mu\text{W}$)

APPLICATIONS

- Cellular phones
- PDA's
- MP3 players
- Power routing
- Battery-powered systems
- PCMCIA cards
- Modems
- Audio and video signal routing
- Communication systems
- Data switching

GENERAL DESCRIPTION

The ADG888 is a low voltage, dual DPDT (double-pole, double-throw) CMOS device optimized for high performance audio switching. With its low power and small physical size, it is ideal for portable devices.

This device offers ultralow on resistance of less than 0.8Ω over the full temperature range, making it an ideal solution for applications requiring minimal distortion through the switch. The ADG888 also has the capability of carrying large amounts of current, typically 400 mA at 5 V operation.

When on, each switch conducts equally well in both directions and has an input signal range that extends to the supplies. The ADG888 exhibits break-before-make switching action.

FUNCTIONAL BLOCK DIAGRAM

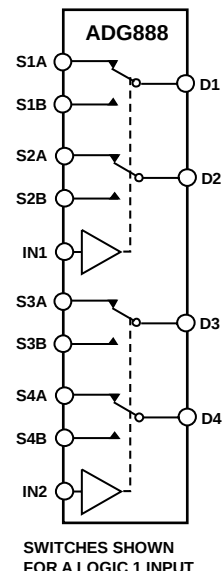


Figure 1.

The ADG888 is available in a 16-ball WLCSP, 16-lead LFCSP, and a 16-lead TSSOP. These packages make the ADG888 the ideal solution for space-constrained applications.

PRODUCT HIGHLIGHTS

1. $<0.6 \Omega$ over full temperature range of -40°C to $+125^{\circ}\text{C}$.
2. High current handling capability (400 mA continuous current at 5 V).
3. Low THD + N (0.008% typical).
4. Tiny 16-ball WLCSP, 16-lead LFCSP, and 16-lead TSSOP.

Rev. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	ESD Caution.....	5
Applications.....	1	Pin Configurations and Function Descriptions	6
Functional Block Diagram	1	Typical Performance Characteristics	7
General Description	1	Test Circuits.....	9
Product Highlights	1	Terminology	11
Revision History	2	Outline Dimensions	12
Specifications.....	3	Ordering Guide	13
Absolute Maximum Ratings.....	5		

REVISION HISTORY

12/06—Rev. 0 to Rev. A	
Updated Format.....	Universal
Changes to Table 2.....	4
Changes to Table 3.....	5
Changes to Ordering Guide	13
7/05—Revision 0: Initial Version	

SPECIFICATIONS

$V_{DD} = 4.2\text{ V to }5.5\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	+25°C	B Version ¹	Y Version ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V _{DD}	V	V _{DD} = 4.2 V, V _S = 0 V to V _{DD} , I _{DS} = 100 mA See Figure 16
On Resistance (R _{ON})	0.4	0.55	0.6	Ω typ	
	0.48			Ω max	
On Resistance Match Between Channels (ΔR _{ON})	0.04			Ω typ	V _{DD} = 4.2 V, V _S = 2.2 V, I _{DS} = 100 mA
On Resistance Flatness (R _{FLAT (ON)})	0.06	0.07	0.075	Ω max	V _{DD} = 4.2 V, V _S = 0 V to V _{DD} I _{DS} = 100 mA
	0.07			Ω typ	
		0.11	0.13	0.14	
LEAKAGE CURRENTS					
Source Off Leakage I _S (Off)	±0.2			nA typ	V _{DD} = 5.5 V V _S = 1 V/4.5 V, V _D = 4.5 V/1 V; see Figure 17
Channel On Leakage I _D , I _S (On)	±0.2			nA typ	V _S = V _D = 1 V or 4.5 V; see Figure 18
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	V _{IN} = V _{INL} or V _{INH}
Input Low Voltage, V _{INL}			0.8	V max	
Input Current					
I _{INL} or I _{INH}	0.005			μA typ	
			±0.1	μA max	
C _{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS ²					
t _{ON}	22			ns typ	R _L = 50 Ω, C _L = 35 pF
	30	33	35	ns max	V _S = 3 V/0 V; see Figure 19
t _{OFF}	13			ns typ	R _L = 50 Ω, C _L = 35 pF
	17	18	19	ns max	V _S = 3 V/0 V; see Figure 19
Break-Before-Make Time Delay (t _{BBM})	9			ns typ	R _L = 50 Ω, C _L = 35 pF
			5	ns min	V _{S1} = V _{S2} = 3 V; see Figure 20
Charge Injection	70			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 21
Off Isolation	−67			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 22
Channel-to-Channel Crosstalk	−99			dB typ	Adjacent channel; R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 25
	−67			dB typ	Adjacent switch; R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 23
Total Harmonic Distortion (THD + N)	0.008			%	R _L = 32 Ω, f = 20 Hz to 20 kHz, V _S = 3 V p-p
Insertion Loss	−0.03			dB typ	R _L = 50 Ω, C _L = 5 pF; see Figure 24
−3 dB Bandwidth	29			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 24
C _S (Off)	58			pF typ	
C _D , C _S (On)	110			pF typ	
POWER REQUIREMENTS					
I _{DD}	0.003			μA typ	V _{DD} = 5.5 V Digital inputs = 0 V or 5.5 V
		1	4	μA max	

¹ Temperature range for the Y version is -40°C to +125°C for the TSSOP and LFCSP; temperature range for the B version is -40°C to +85°C for the WLCSP.

² Guaranteed by design, not production tested.

ADG888

$V_{DD} = 2.7 \text{ V}$ to 3.6 V , $GND = 0 \text{ V}$, unless otherwise noted.

Table 2.

Parameter	+25°C	B Version ¹	Y Version ¹	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	0.5			Ω typ	$V_{DD} = 2.7 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD}
	0.7	0.75	0.8	Ω max	$I_S = 100 \text{ mA}$; see Figure 16
On Resistance Match Between Channels (ΔR_{ON})	0.045			Ω typ	$V_{DD} = 2.7 \text{ V}$, $V_S = 1 \text{ V}$
	0.072	0.077	0.083	Ω max	$I_S = 100 \text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	0.16			Ω typ	$V_{DD} = 2.7 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD}
			0.262	Ω max	$I_S = 100 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage I_S (Off)	± 0.2			nA typ	$V_{DD} = 3.6 \text{ V}$
Channel On Leakage I_D , I_S (On)	± 0.2			nA typ	$V_S = 1 \text{ V}/2.6 \text{ V}$, $V_D = 2.6 \text{ V}/1 \text{ V}$; see Figure 17
					$V_S = V_D = 1 \text{ V}$ or 2.6 V ; see Figure 18
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.3	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
C_{IN} , Digital Input Capacitance	2			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	28			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$; see Figure 19
	43	47	50	ns max	$V_S = 1.5 \text{ V}/0 \text{ V}$
t_{OFF}	13			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$; see Figure 19
	20	21	22	ns max	$V_S = 1.5 \text{ V}/0 \text{ V}$
Break-Before-Make Time Delay (t_{BBM})	14			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$; see Figure 20
Charge Injection	50			pC typ	$V_S = 0 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 21
Off Isolation	-67			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 22
Channel-to-Channel Crosstalk	-99			dB typ	Adjacent channel; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 25
	-67			dB typ	Adjacent switch; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; see Figure 23
Total Harmonic Distortion (THD + N)	0.01			%	$R_L = 32 \Omega$, $f = 20 \text{ Hz}$ to 20 kHz , $V_S = 1 \text{ V p-p}$
Insertion Loss	-0.04			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 24
-3 dB Bandwidth	29			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 24
C_S (Off)	60			pF typ	
C_D , C_S (On)	115			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003			μA typ	$V_{DD} = 3.6 \text{ V}$
		1	2	μA max	Digital inputs = 0 V or 3.6 V

¹ Temperature range for the Y version is -40°C to $+125^\circ\text{C}$ for the TSSOP and LFCSP; temperature range for the B version is -40°C to $+85^\circ\text{C}$ for the WLCSP.

² Guaranteed by design, not production tested.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	–0.3 V to +6 V
Analog Inputs, Digital Inputs ¹	–0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Peak Current, S or D 5 V operation	600 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D 5 V operation	400 mA
Operating Temperature Range Automotive (Y Version) TSSOP and LFCSP packages Industrial (B version) WLCSP package	–40°C to +125°C
Storage Temperature Range	–40°C to +85°C
Junction Temperature	–65°C to +150°C
16-Lead TSSOP Package θ_{JA} Thermal Impedance (4-Layer Board) θ_{JC} Thermal Impedance	112°C/W 27.6°C/W
16-Lead WLCSP Package θ_{JA} Thermal Impedance (4-Layer Board)	130°C/W
16-Lead LFCSP Package θ_{JA} Thermal Impedance (4-Layer Board)	30.4°C/W
Reflow Soldering (Pb-Free) Peak Temperature Time at Peak Temperature	260(+0/–5)°C 10 sec to 40 sec

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Limit current to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

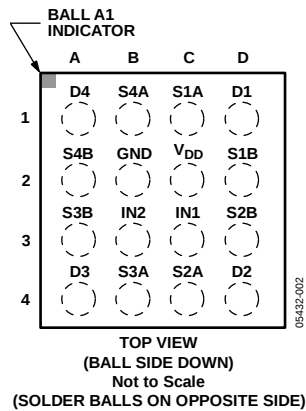


Figure 2. 16-Ball WLCSP Pin Configuration

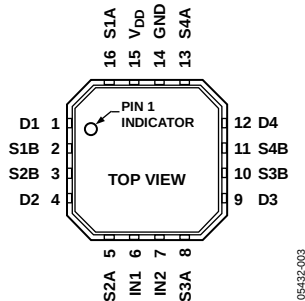


Figure 3. 16-Lead LFCSP Pin Configuration

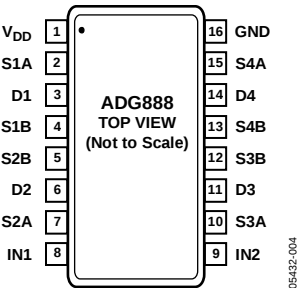


Figure 4. 16-Lead TSSOP Pin Configuration

Table 4. Pin Function Descriptions

WLCSP Ball No.	LFCSP Pin No.	TSSOP Pin No.	Mnemonic	Description
2C	15	1	V _{DD}	Most Positive Power Supply Potential.
2B	14	16	GND	Ground (0 V) Reference.
1B, 1C, 2A, 2D, 3A, 3D, 4B, 4C	2, 3, 5, 8, 10, 11, 13, 16	2, 4, 5, 7, 10, 12, 13, 15	S	Source Terminal. Can be an input or output.
1A, 1D, 4A, 4D	1, 4, 9, 12	3, 6, 11, 14	D	Drain Terminal. Can be an input or output.
3B, 3C	6, 7	8, 9	IN	Logic Control Input.

Table 5. Truth Table

Logic (IN1/IN2)	Switch 1A/2A/3A/4A	Switch 1B/2B/3B/4B
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

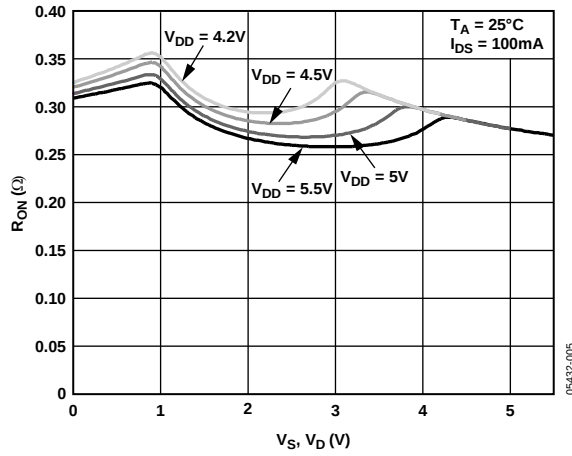


Figure 5. On Resistance vs. V_D (V_S), $V_{DD} = 4.2$ V to 5.5 V

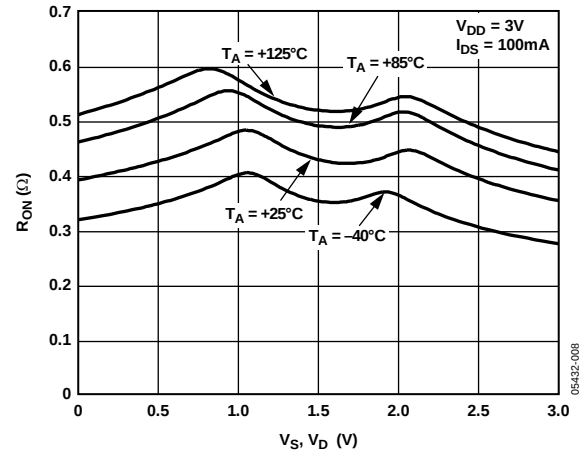


Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3$ V

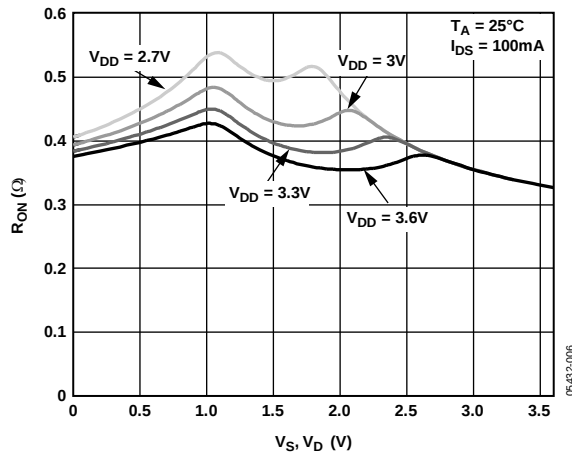


Figure 6. On Resistance vs. V_D (V_S), $V_{DD} = 2.7$ V to 3.6 V

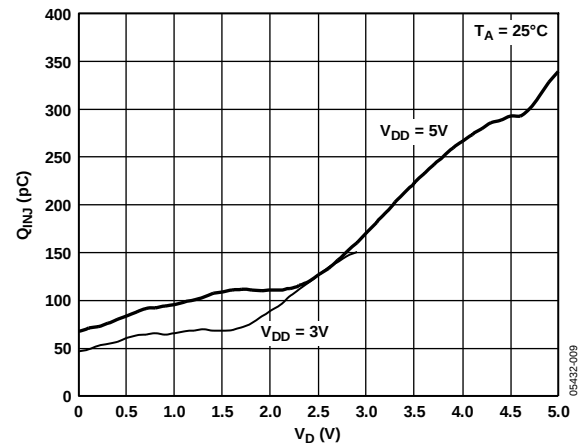


Figure 9. Charge Injection vs. Source Voltage

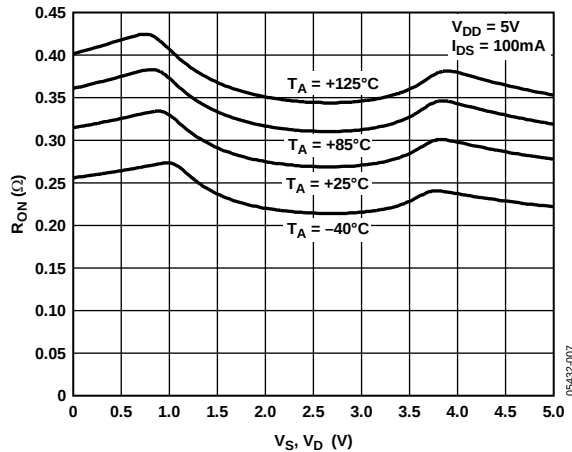


Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 5$ V

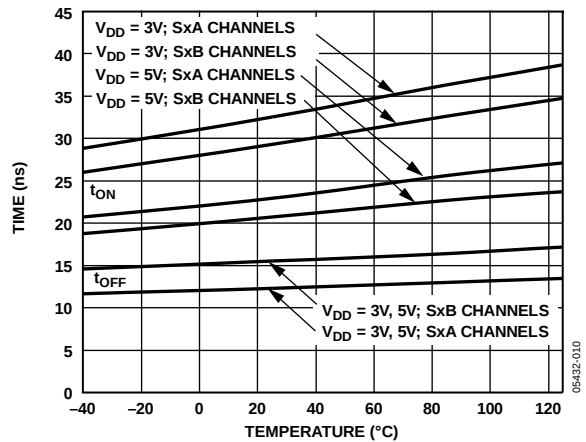


Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

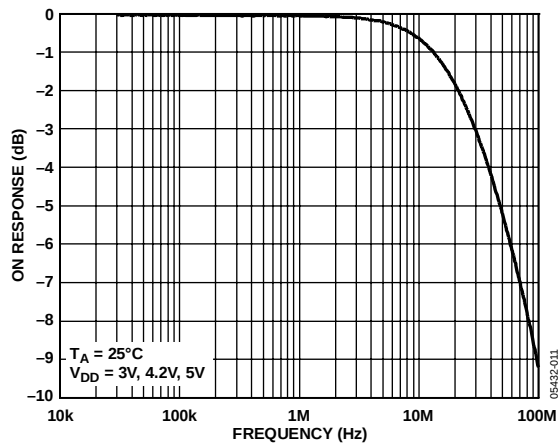


Figure 11. Bandwidth

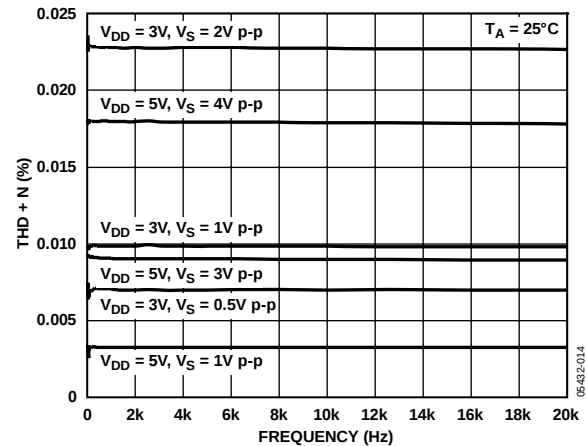


Figure 14. Total Harmonic Distortion + Noise (THD + N)

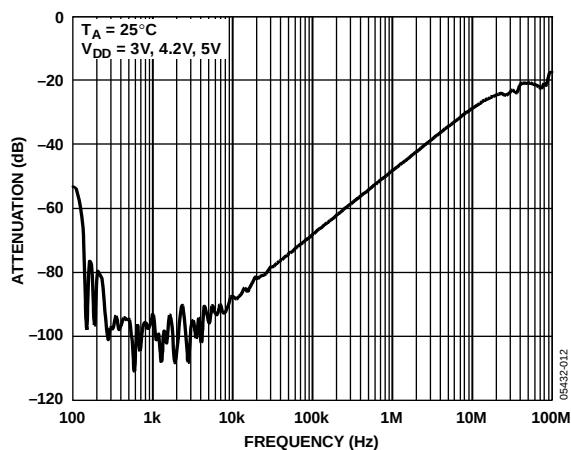


Figure 12. Off Isolation vs. Frequency

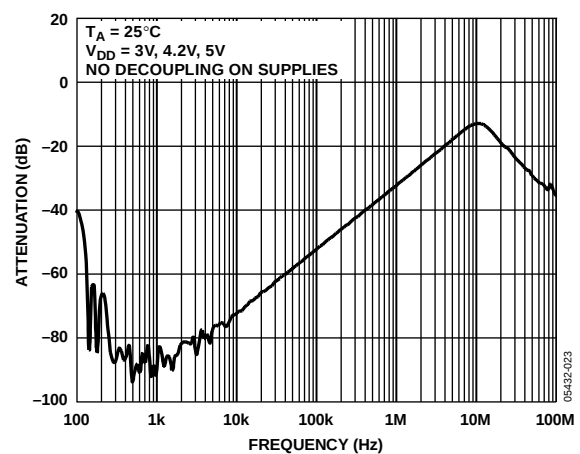


Figure 15. AC PSRR

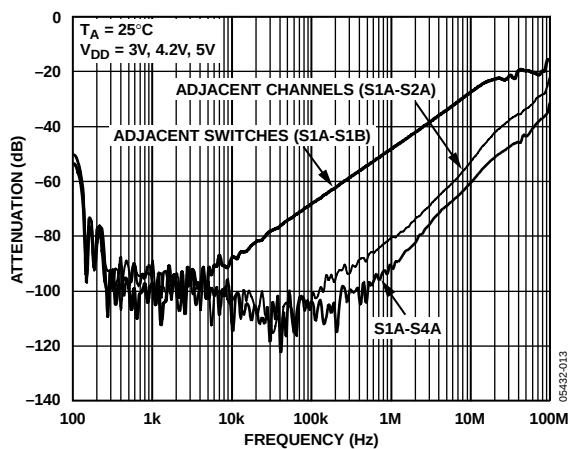


Figure 13. Crosstalk vs. Frequency

TEST CIRCUITS

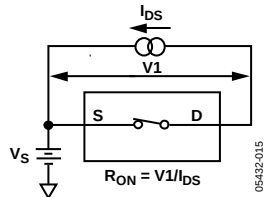


Figure 16. On Resistance

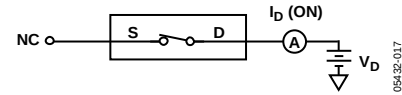


Figure 18. On Leakage

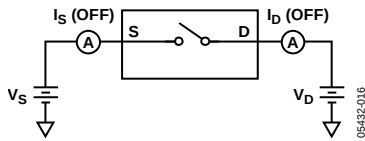


Figure 17. Off Leakage

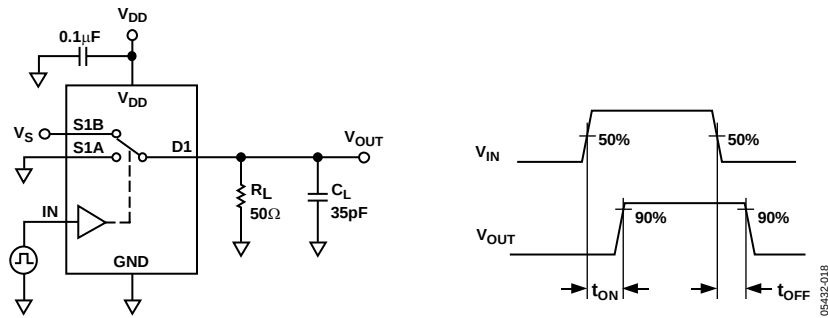


Figure 19. Switching Times, t_{ON} , t_{OFF}

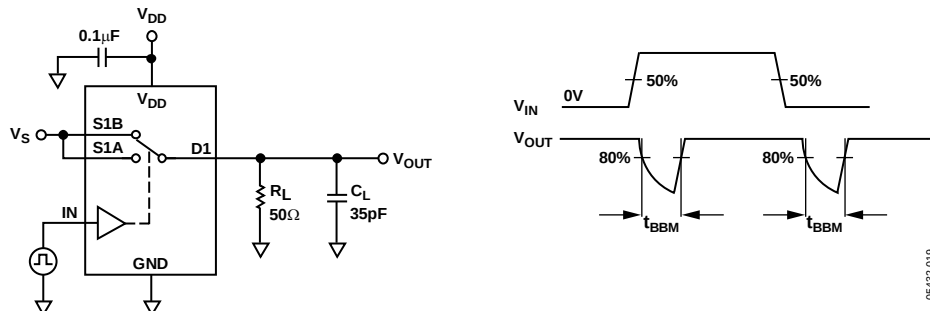


Figure 20. Break-Before-Make Time Delay, t_{BBM}

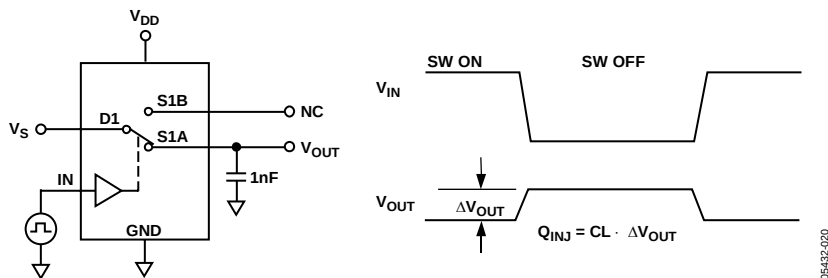
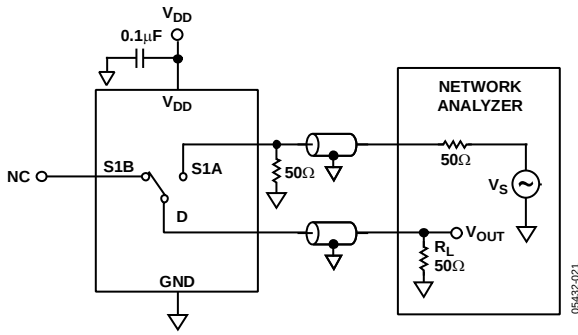
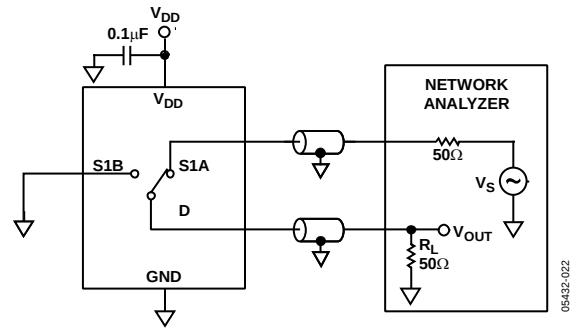


Figure 21. Charge Injection



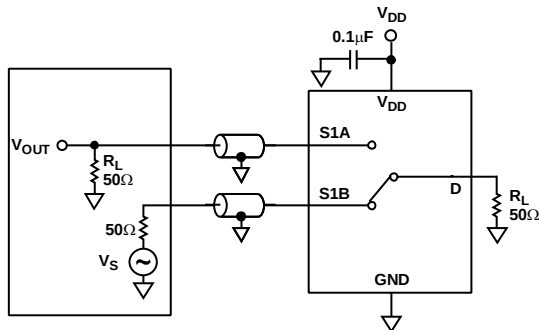
$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 22. Off Isolation



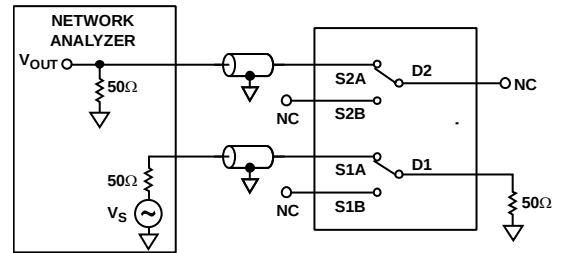
$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Figure 24. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 23. Channel-to-Channel Crosstalk (S1A to S1B)



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_S}$$

Figure 25. Channel-to-Channel Crosstalk (S1A to S2A)

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_S)

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

R_{FLAT (ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}

On resistance match between any two channels.

I_S (OFF)

Source leakage current with the switch off.

I_D, I_S (ON)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (OFF)

Off switch source capacitance. Measured with reference to ground.

C_D, C_S (ON)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. This is specified for two conditions:

- Adjacent channel, that is, S1A to S2A, S1B to S2B, S3A to S4A, or S3B to S4B.
- Adjacent switch, that is, S1A to S1B, S2A to S2B, S3A to S3B, or S4A to S4B.

–3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitudes plus signal noise to the fundamental.

OUTLINE DIMENSIONS

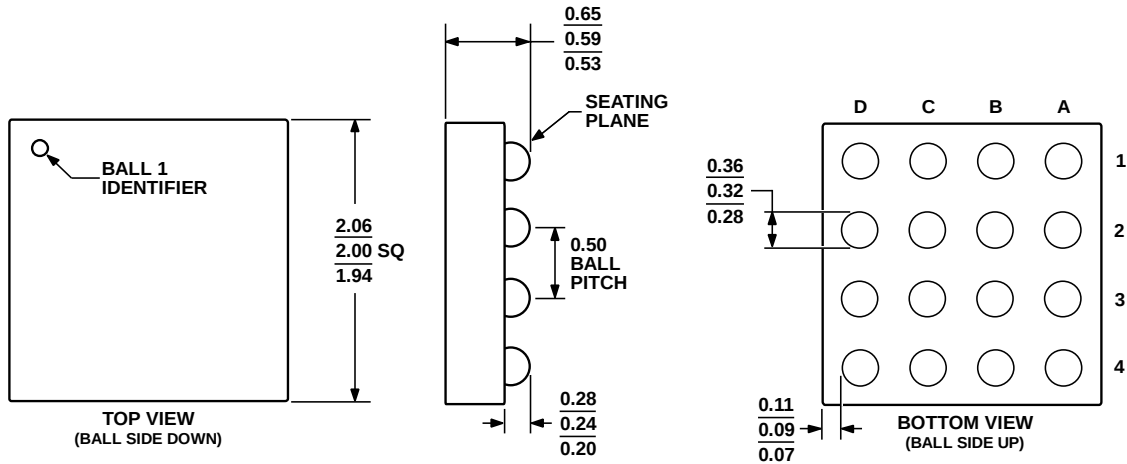
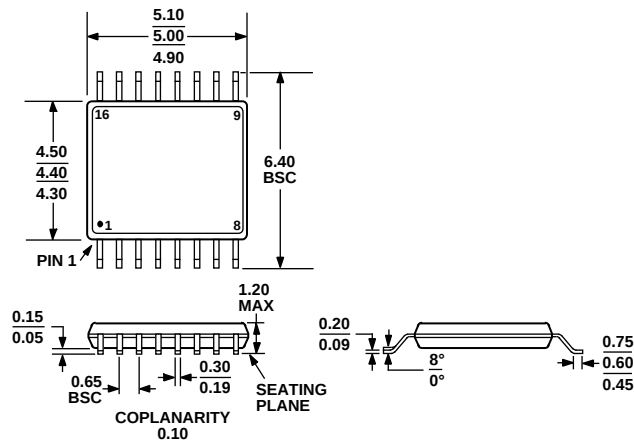


Figure 26. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16)

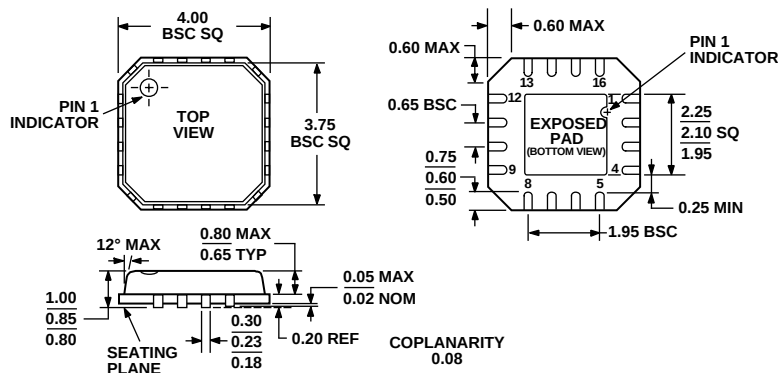
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 27. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 28. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding ¹
ADG888YRUZ ²	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG888YRUZ-REEL ²	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG888YRUZ-REEL7 ²	–40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16	
ADG888YCPZ-REEL ²	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	S0D
ADG888YCPZ-REEL7 ²	–40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-16-4	S0D
ADG888BCBZ-REEL ²	–40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16	S02
ADG888BCBZ-REEL7 ²	–40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16	S02
EVAL-ADG888EB		Evaluation Board		

¹ Branding on these packages is limited to three characters due to space constraints.

² Z = Pb-free part.

ADG888

NOTES

NOTES

ADG888

NOTES