ANALOG DEVICES

Ultralow Power Energy Harvester PMU with MPPT and Charge Management

Preliminary Technical Data

ADP5091/ADP5092

FEATURES

Boost regulator with maximum power point tracking (MPPT) with dynamic sensing or none-sensing mode
Hysteresis mode for best ultra light load efficiency
450 nA ultralow quiescent current (CBP ≥ MINOP)
360 nA ultralow quiescent current (CBP < MINOP)
Input voltage operation range from 80 mV to 3.3 V
Fast cold start from 380 mV (typical) with charge pump
Programmable shutdown point on MINOP pin based on input open circuit voltage (OCV)
150mA regulated output from 1.5V to 3.6V
Programmable voltage monitor (2 V to 5.2 V) to support charging storage elements
Optional BACK_UP power path management
RF transmission friendly to shut down switcher temporarily via micro-controller (MCU) communication

APPLICATIONS

Photovoltaic (PV) cell energy harvesting
TEG energy harvesting
Industrial monitoring
Self-powered wireless sensor devices
Portable and wearable devices with energy harvesting

TYPICAL APPLICATION CIRCUIT

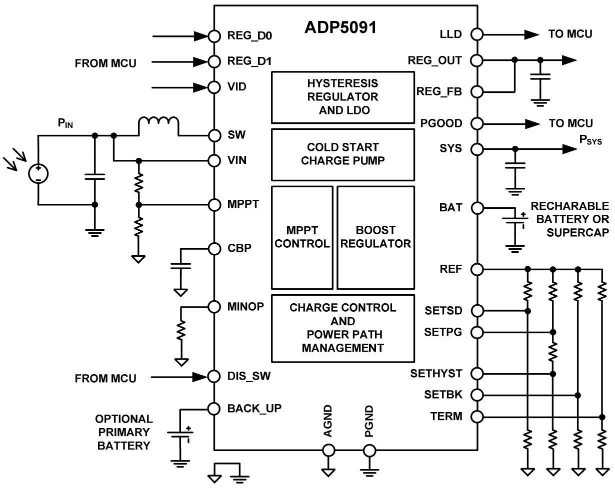

Figure 1.

GENERAL DESCRIPTION

The ADP5091/92 is an intelligent integrated energy harvesting nano-powered management solution that converts dc power from PV cells or thermoelectric generators (TEGs).The device charges storage elements such as rechargeable Li-Ion batteries, thin film batteries, super capacitors, or conventional capacitors, and powers up small electronic devices and battery-free systems.

The ADP5091/92 provides efficient conversion of the harvested limited power from a 16 µW to 600 mW range with sub-µW operation losses. With the internal cold-start circuit, the regulator can start operating at an input voltage as low as 380 mV. After cold startup, the regulator is functional at an input voltage range of 80 mV to 3.3 V. An additional 150mA regulated output can be programmed by an external resistor divide or VID pin.

By sensing the input voltage, the control loop keeps the input voltage ripple in a fixed range to maintain stable dc-to-dc boost conversion. The OCV dynamic sensing mode and none-sensing mode both programming regulation points of the input voltage allow extraction of the highest possible energy from the harvester. A programmable minimum operation threshold (MINOP) enables boost shutdown during a low light condition. As a low light indicator for microprocessor, the LLD is the MIONP comparator output. In addition, the DIS_SW pin can temporarily shut down the boost regulator and is RF transmission friendly.

The charging control function of ADP5091/92 protects rechargeable energy storage, which is achieved by monitoring the battery voltage with programmable charging termination voltage and shutdown discharging voltage. In addition, a programmable PGOOD flag with programmable hysteresis monitors the SYS voltage.

An optional primary cell battery can be connected and managed by an integrated power path management control block that is programmable to switch the power source from the energy harvester, rechargeable battery, and primary cell battery.

The ADP5091/92 is available in a 24-lead LFCSP and is rated for a −40°C to +125°C junction temperature range.

Rev. PrA Document Feedback

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Technical Support
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SPECIFICATIONS

V_{IN} = 1.2 V, V_{SYS} =V_{BAT} = 3V, T_J = -40°C to 125°C for minimum/maximum specifications and T_A =25°C for typical specifications, unless otherwise noted. External components L = 22 µH, C_{IN} = 4.7 µF, C_{SYS}= 4.7 µF.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Operating Quiescent Current of SYS Pin ($V_{IN} > V_{CBP} \geq V_{MINOP}$)	I_{Q_SYS}	REG_D0=low, REG_D1=low		450		nA
		REG_D0=high, REG_D1= low		488		nA
		REG_D0= low, REG_D1= high		520		nA
		REG_D0= high, REG_D1= high		500		nA
Sleeping Quiescent Current of SYS Pin ($V_{CBP} < V_{MINOP}$)	$I_{IQ\_SLEEP\_SYS}$	REG_D0= low, REG_D1= low		360		nA
COLD-START CIRCUIT						
Minimum Input Voltage for Cold-Start	V_{IN_COLD}	V_{SYS} = 0 V, 0°C < T_A < 85°C		380	440	mV
Minimum Input Power for Cold-Start	P_{IN_COLD}			16		µW
End of Cold-Start Operation Threshold	V_{SYS_TH}		1.8	1.93	2.03	V
End of Cold-Start Operation Hysteresis	V_{SYS_HYS}			125		mV
BOOST REGULATOR						
Input Voltage Operation Range	V_{IN}	Cold-start completed	0.1		3.3	V
Input Power Operation Range	P_{IN}	Cold-start completed, V_{IN} = 3 V			600	mW
SYS Threshold of Starting Charging BAT	V_{SYS_CHG}			2.1		V
SYS Hysteresis of Stopping Charging BAT	$V_{SYS\_CHG\_HYS}$			150		mV
Input Peak Current	I_{IN_PEAK}	Factory trim, 1 bit (200mA, 300mA)		200	300	mA
				300	400	mA
Low-Side Switch on Resistance	$R_{LS\_DS\_ON}$	Pin-to-pin measurement		0.5	TBD	Ω
High-Side Switch on Resistance	$R_{HS\_DS\_ON}$	Pin-to-pin measurement		1	TBD	Ω
SYS Switch on Resistance	$R_{SYS\_DS\_ON}$			0.48	0.70	Ω
DIS_SW High Voltage	DIS_SW_{HIGH}		1			V
DIS_SW Low Voltage	DIS_SW_{LOW}				0.5	V
DIS_SW Delay	t_{DIS_DELAY}			1		µs
VIN CONTROL AND MINOP						
VIN Open Circuit Voltage Sampling Cycle	T_{VOC_CYCLE}	Factory trim, 2 bit (4 s , 8 s, 16 s, 32 s)		16		s
VIN Open Circuit Voltage Sampling Time	T_{VOC_SAMPL}			256		ms
MINOP Bias Current	I_{MINOP}		1.45	2	2.55	µA
MINOP Operation Voltage Range of Dynamic MPPT sensing Mode	V_{MINOP_DSM}				1.5	V
MINOP Threshold of MPPT None-sensing Mode	V_{MINOP_NSM}			1.8		V
MPPT Bias Current of MPPT None-sensing Mode	I_{MPPT}		1.45	2	2.55	µA
LLD Pull High Resistor (ADP5091/92 Only)				11.4		kΩ
LLD Pull Low Resistor (ADP5091/92 Only)				11.4		kΩ
LLD High Voltage	V_{LLD_IH}				REG_OUT	
Leakage Current at CBP Pin	I_{CBP_LEAK}			10	100	pA
ENERGY STORAGE MANAGEMENT						
Internal Voltage of Charging BAT	V_{CHR}			2.2		V
Internal Reference Voltage	V_{REF}		0.98	1	1.02	V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Battery Stop Discharging Threshold	V_{BAT_SD}		2.0		V_{BAT_TERM}	V
Battery Stop Discharging Hysteresis Resistor	$R_{BAT\_SD\_HYS}$		65	103.5	150	kΩ
Battery Terminal Charging Threshold	V_{BAT_TERM}		2.2		5.2	V
Battery Terminal Charging Hysteresis	$V_{BAT\_TERM\_HYS}$			3	3.7	%
PGOOD Rising Threshold at SYS Pin	V_{SYS_PG}		V_{BAT_SD}		V_{BAT_TERM}	V
PGOOD Pull High Resistor				11.4		kΩ
PGOOD Pull Low Resistor				11.4		kΩ
PGOOD High Voltage	V_{PGOOD_IH}				SYS	V
Battery Switches on Resistance	$R_{BAT\_SW\_ON}$	Pin-to-pin measurement	TBD	0.6	TBD	Ω
Battery Source Current	I_{BAT}				1	A
Leakage Current at BAT Pin	I_{BAT_LEAK}	$V_{BAT} = 2$ V, $V_{BAT\_SD} = 2.2$ V, $V_{SYS} = 2$ V		15	50	nA
		$V_{BAT} = 3.3$ V, $V_{BAT\_SD} = 2.2$ V, $V_{SYS} = 0$ V		0.5	20	nA
BACKUP POWER PATH						
Turning off BACK_UP Switch Threshold	V_{BK_TF}		2.0		V_{BAT_TERM}	V
Turning off BACK_UP Switch Hysteresis Resistor	$R_{BK\_TF\_HYS}$		65	103.5	150	kΩ
BACK_UP and BAT Comparator Offset	V_{BKP_OFFSET}	$V_{SYS} \geq V_{SYS\_TH}$	135	185	250	mV
BACK_UP and BAT Comparator Hysteresis	V_{BAT_HYS}	$V_{SYS} \geq V_{SYS\_TH}$	55	75	100	mV
BACK_UP Current Capability	I_{BKP}	$V_{SYS} \geq V_{SYS\_TH}$		400	520	mA
Leakage Current at BACK_UP Pin	I_{BKP_LEAK}	$V_{BACK\_UP} = V_{SYS} = V_{BAT} = 3$ V		6	18	nA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}	$V_{SYS} \geq V_{SYS\_TH}$		135		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

REGULATED OUTPUT SPECIFICATIONS

$V_{IN} = 1.2$ V, $V_{SYS} = V_{BAT} = 3$ V, $V_{REG_OUT} = 2$V, L = 22 µH, $C_{IN} = 4.7$ µF, $C_{SYS} = 4.7$ uF, $C_{REG\_OUT} = 4.7$ uF; $T_J = -40$°C to 125°C for minimum/maximum specifications and $T_A = 25$°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
REGULATED OUTPUT						
Output Options by VID Control	V_{REG_OUT}		1.5		3.6	V
REG_OUT OF BOOST MODE						
REG_OUT Wake Threshold	V_{REG_WAKE}		1.005	1.020	1.036	V
REG_OUT Sleep Threshold	V_{REG_SLEEP}		1.015	1.030	1.046	V
High-Side Switches on Resistance	$R_{BST\_DS\_ON}$			1	TBD	Ω
Current Limit Threshold of Boost Mode	$V_{REG\_BST\_LIM}$			100	TBD	mA
REG_OUT OF LDO MODE						
REG_OUT Accuracy	V_{REG_LDO}	$I_{OUT} = 10$ mA	-1		1	%
		0 µA < I_{OUT} < 150 mA, $V_{SYS} = (V_{REG\_OUT} + 0.5$ V)	-3.5		3.5	%
Adjustable REG_OUT Accuracy	$V_{REG\_LDO\_ADJ}$	$I_{OUT} = 10$ mA	0.99	1	1.01	V
		0 µA < I_{OUT} < 150 mA, $V_{SYS} = (V_{REG\_OUT} + 0.5$ V)	0.97	1	1.03	V
REG_OUT Dropout	V_{REG_DROP}	$I_{OUT} = 150$ mA		100		mV
Current Limit Threshold of LDO Mode	I_{REG_LIM}	$V_{SYS} \geq V_{SYS\_TH}$	220	320		mA
Output Noise	OUT_{NOISE}	10Hz to 100kHz		100		uV rms
Power Supply Rejection Ratio	PSRR	100Hz		65		dB
		1kHz		50		dB
REG_D0 and REG_D1						
Input Logic High	$V_{REG\_DX\_IH}$		1.2			V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Logic Low	$V_{REG\_DX\_IL}$				0.4	V
Input Leakage Current	$I_{REG\_DX\_LEAK}$			20		nA
REG_GOOD (ADP5092 Only)						
REG_GOOD Rising Threshold	V_{REG_GOOD}			90		%
REG_GOOD Hysteresis	$V_{REG\_GOOD\_HYS}$			5		%
REG_GOOD Pull High Resistor				11.4		kΩ
REG_GOOD Pull Low Resistor				11.4		kΩ
REG_GOOD High Voltage	$V_{REG\_GOOD\_IH}$				REG_OUT	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN, MPPT, CBP, MINOP	−0.3 V to +3.6 V
DIS_SW, TERM, SETPG,SETSD, SETBK, PGOOD, PG_HYS, REF, REG_D0, VID, REG_D1, LLD to AGND	−0.3 V to +6.0 V
SW, SYS, BAT, BACK_UP, REG_OUT, REG_FB to PGND	
PGND to AGND	−0.3 V to +0.3 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP Package	TBD	TBD	

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

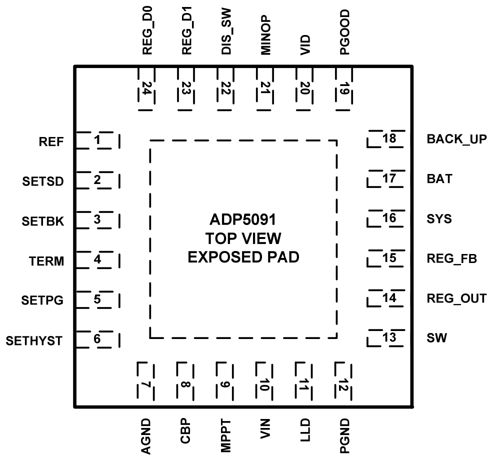

Figure 2. ADP5091 LFCSP Package Pin Configuration

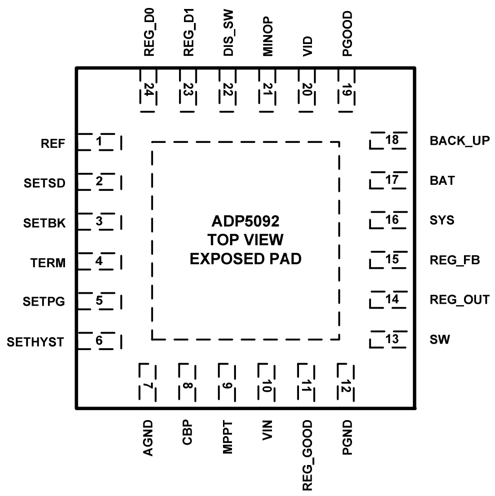

Figure 3. ADP5092 LFCSP Package Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REF	Provides Voltage Reference for the SETSD, SETPG, SETBK and TERM Pins.
2	SETSD	Shutdown Setting. This pin sets the shutdown discharging voltage based on the BAT node voltage level.
3	SETBK	Sets BACK_UP disabled threshold monitoring BAT voltage. Connect this pin to AGND without BACK_UP storage element.
4	TERM	Termination Charging Voltage. This pin sets the termination charging voltage based on the BAT node voltage level.
5	SETPG	Sets Power Good Voltage Based on SYS Node Voltage Level.
6	SETHYST	Sets PGOOD Falling Hysteresis. Resistor divider input for PGOOD Falling Hysteresis.
7	AGND	Analog Ground.
8	CBP	Capacitor bypass. Samples and Holds the Maximum Power Point Level. Connect a 10 nF capacitor from this pin to AGND. When MPPT is disabled, tie CBP to an external reference that is lower than VIN. Analog Ground.
9	MPPT	Maximum Power Point Tracking. This pin sets the maximum power point tracking level for different energy harvesters. Place a resistor through AGND to set MPPT voltage at MINOP voltage higher than the threshold of MPPT None-sensing Mode.
10	VIN	Input Supply from Energy Harvester Source. Connect at least a 4.7 μF capacitor as close as possible between this pin and PGND.
11	LLD	Low light density indicator to MCU. LLD pulls high at the MINOP voltage higher than CBP voltage. ADP5091 only.
	REG_GOOD	Regulated Output Power Good. ADP5092 only.
12	PGND	Power Ground.
13	SW	Switching Node for Inductive Boost Regulator with Connection to External Inductor. Connect a 22 μH inductor between this pin and VIN.
14	BAT	Places Rechargeable Battery or Super Cap as a Storage for SYS Output Supply.
15	REG_FB	Regulated Output Feedback Voltage Sense Input. Connect to a resistor divider from REG_OUT.
16	SYS	Output Supply to System Load. Connect at least a 4.7 μF capacitor as close as possible between this pin and PGND.
17	REG_OUT	Regulated output. Connect at least a 1 μF capacitor as close as possible between this pin and PGND.
18	BACK_UP	Optional Input Supply from the Backup Primary Battery Cell.
19	PGOOD	Output Supply to MCU. Maintains a pulled high signal when SYS is higher than SETPG threshold.
20	VID	Voltage Configuration Pin of REG_OUT. Set up to 8 different REG_OUT tied low through a resistor to AGND.
21	MINOP	Minimum Operating Power. Place a resistor on this pin to set the minimum operating input voltage level. The boost regulator starts switching when the CBP voltage exceeds the MINOP voltage. When MINOP voltage is above the threshold of MPPT None-sensing Mode, IC operates at a fixed MPPT ratio. Connect this pin through AGND to disable MINOP function.

Pin No.	Mnemonic	Description
22	DIS_SW	Control Signal from MCU or RF Transceiver to Stop Switching Boost Charger.
23	REG_D1	Regulated output working mode set.
24	REG_D0	Regulated output working mode set.
	EPAD	Exposed Pad. The exposed pad must be connected to AGND.

DETAILED FUNCTIONAL BLOCK DIAGRAM

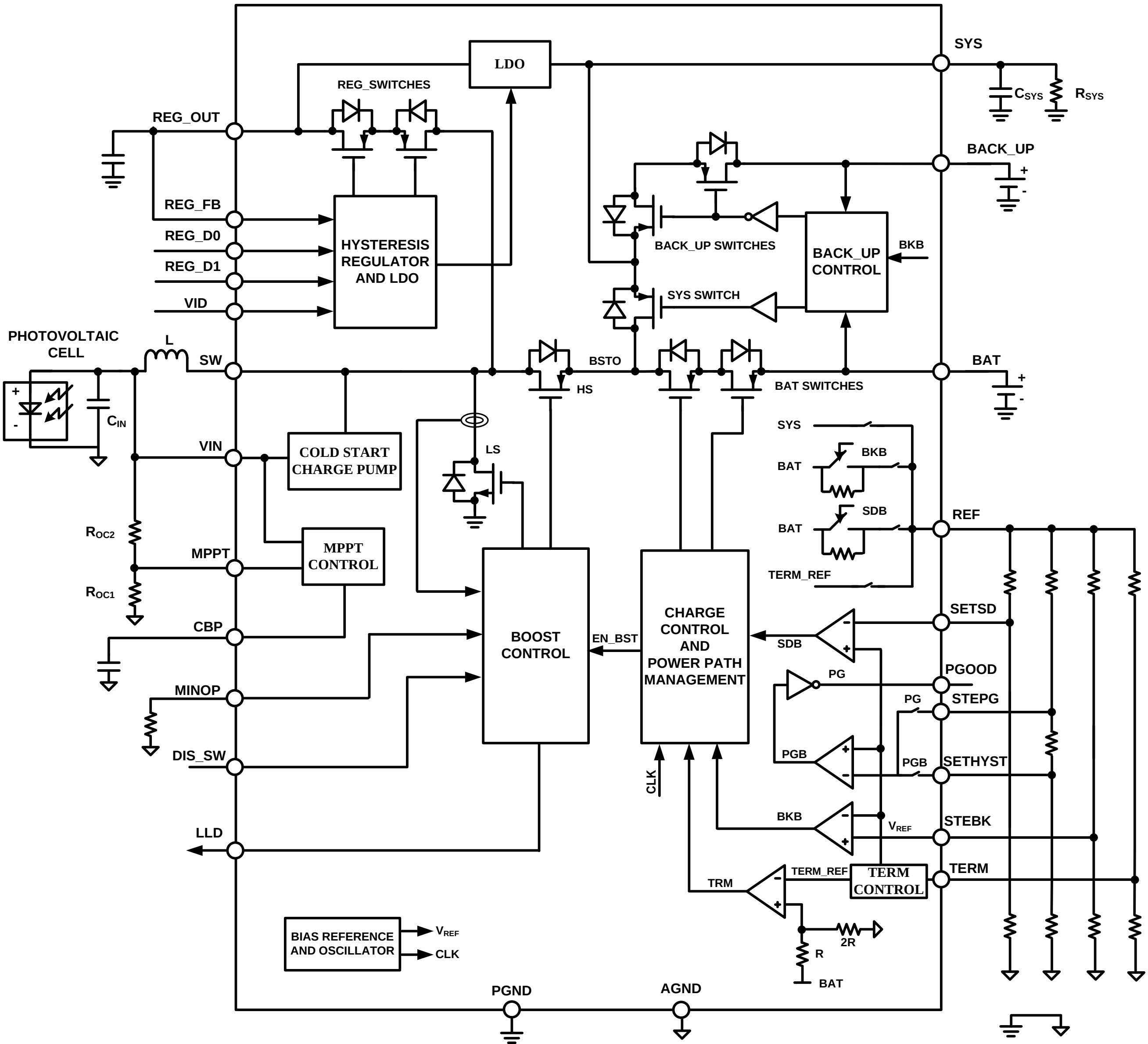

Figure 4. Detailed Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

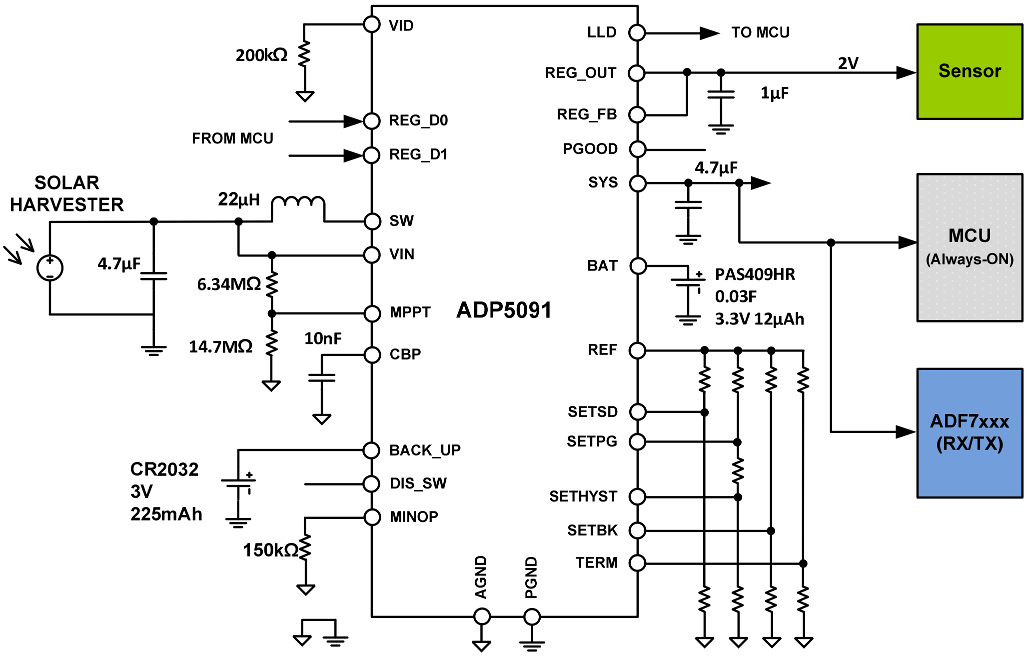

Figure 5. The ADP5091/92-Based Energy Harvester Wireless Sensor Application with Solarprint 0.5 V 450 µa PV-Cell as the Harvesting Energy Source, Shoei Electronics Polyacene Coin Type Capacitor PAS409HR as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell CR2032 as the Backup Battery.

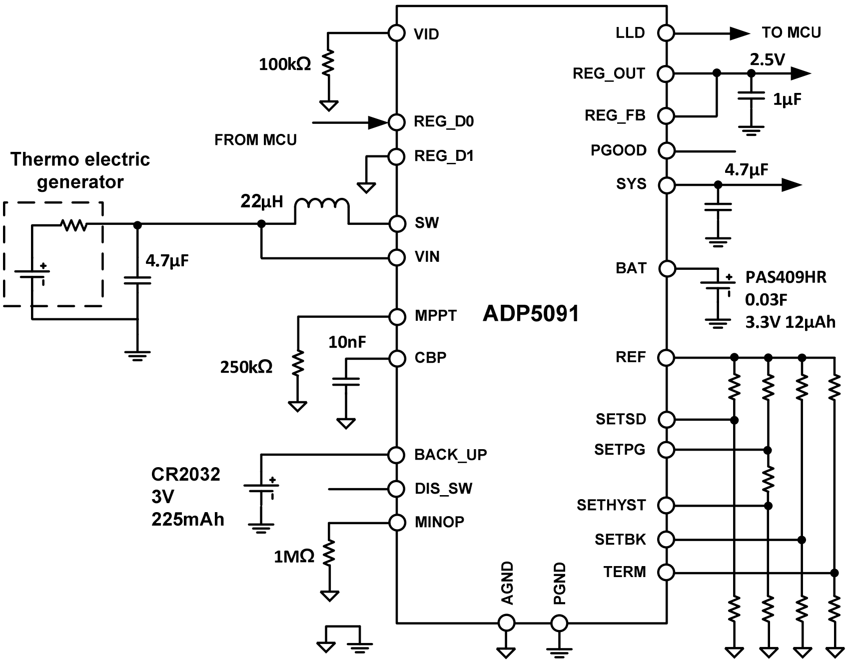

Figure 6. The ADP5091/92-Based Energy Harvester Circuit with a Thermo Electric Generator as the Harvesting Energy Source, Shoei Electronics Polyacene Coin Type Capacitor Pas409hr as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell Cr2032 as the Backup Battery.

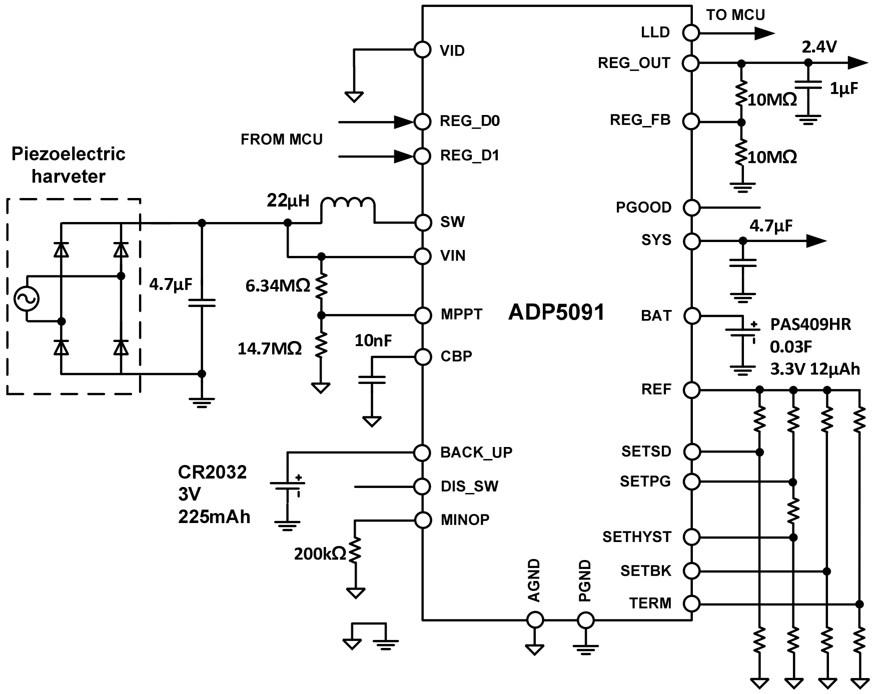

Figure 7. The ADP5091/92-Based Energy Harvester Circuit with a Piezoelectric Generator as the Harvesting Energy Source, Shoei Electronics Polyacene Coin Type Capacitor Pas409hr as the Harvested Energy Storage, and Panasonic Primary Li-Ion Coin Cell Cr2032 as the Backup Battery.

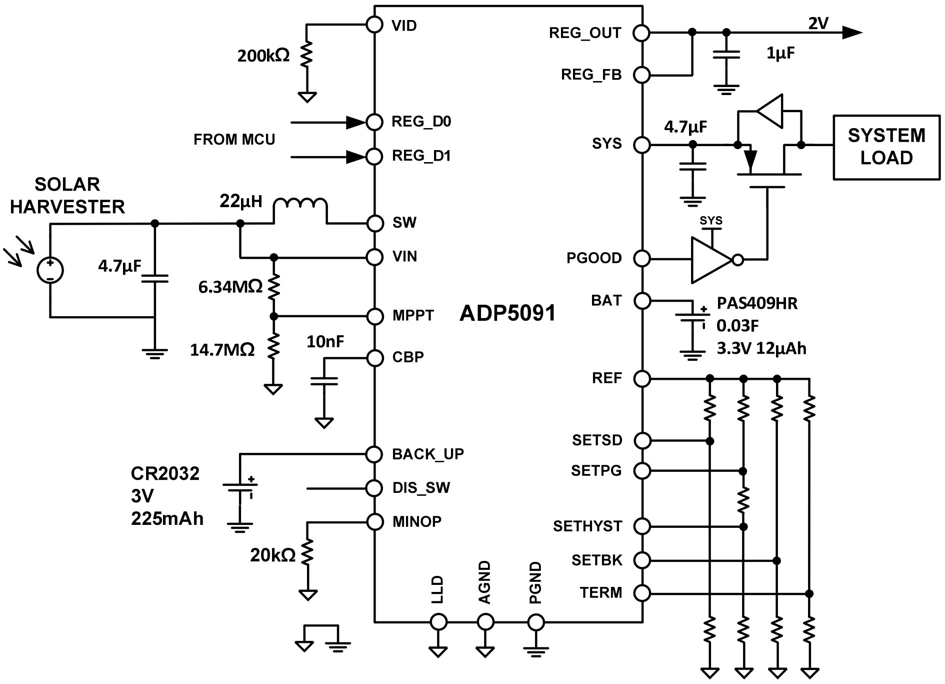

Figure 8. PGOOD Function Determines the Time to Enable the System Load

FACTORY PROGRAMMABLE OPTIONS

To order a device with options other than the default options, contact your local Analog Devices sales or distribution representative.

Table 6. Input Current Limit Options

Option	Description
Option 0	200 mA **(default)**
Option 1	300 mA

Table 7. VIN Open Circuit Voltage Sampling Cycle Options

Option	Description
Option 0	4 s **(default)**
Option 1	8 s
Option 2	16 s
Option 3	32 s

OUTLINE DIMENSIONS

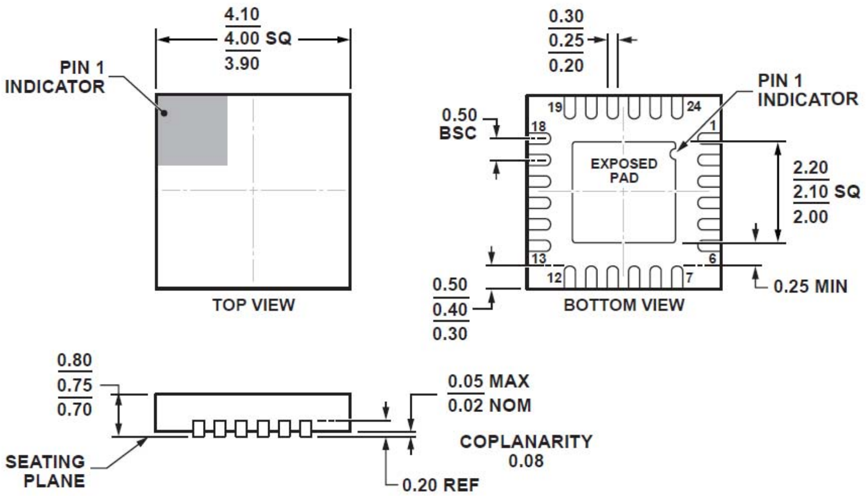

Figure 9. 24-Lead Lead Frame Chip Scale Package [LFCSP-WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE TBD

Model[1]	Temperature Range	Package Description	Package Option
ADP5091ACPZ-R7	−40°C to + 125°C	24-Lead LFCSP_WQ	CP-24-10
ADP5092ACPZ-R7	−40°C to + 125°C	24-Lead LFCSP_WQ	CP-24-10
ADP5091-EVALZ		Evaluation Board	
ADP5092-EVALZ		Evaluation Board	

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[1] Z = RoHS Compliant Part.