ANALOG DEVICES

700 MHz to 2700 MHz RX Mixer with Integrated IF Amplifier, Fractional-N PLL and VCO

Preliminary Technical Data

ADRF6620

FEATURES

Integrated fractional-N PLL
RF input frequency range: 700 MHz to 2700 MHz
Internal LO frequency range: 350 MHz to 2850 MHz
Input P1dB: 17 dBm
Input IP3: 40 dBm
4PST RF input switch
RF digital switch attenuator range 0 to 15 dB
Integrated RF tunable balun allowing single-ended 50Ω input
Multi-core integrated VCO
Integrated IF variable gain amplifier
IF 1 dB bandwidth : 500 MHz.
Balanced 150 Ω IF output impedance
Programmable via 3-wire SPI interface
Single 5V supply

APPLICATIONS

Cellular base stations

FUNCTIONAL BLOCK DIAGRAM

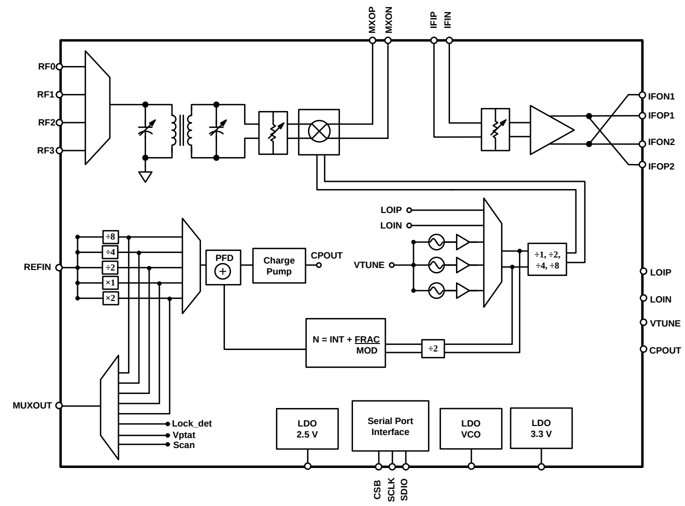

Figure 1.

GENERAL DESCRIPTION

The ADRF6620 is a highly integrated active mixer and synthesizer ideally suited for next generation communication systems. The feature rich device consists of a high linearity broadband active mixer, an integrated fractional-N phase-locked loop (PLL), low phase noise multi-core voltage controlled oscillator (VCO), and IF variable gain amplifier (VGA). In addition, the ADRF6620 also integrates a 4:1 RF switch, an on-chip tunable RF balun, programmable RF attenuator, and LDO. This highly integrated device fits within a small 7mm x 7mm footprint.

The high isolation 4:1 RF switch and on-chip tunable RF balun enable the ADRF6620 to support 4 single ended 50 Ohm terminated RF inputs. A programmable attenuator ensures an optimal differential RF input level to the high linearity mixer core. The integrated attenuator offers an attenuation range of 0 to 15 dB with resolution step size of 1 dB.

The ADRF6620 offers two alternatives for generating the differential LO input signal: externally via a high frequency low phase noise LO signal or internally via the on-chip Fractional-N synthesizer. The integrated synthesizer enables continuous LO coverage from 350 to 2850 MHz. The PLL reference input can support a wide frequency range since the divide or multiplication blocks can be used to increase or decrease the reference frequency to the desired value before it is passed to the phase frequency detector (PFD).

The integrated high linearity VGA provides additional gain range from 0 dB to 12 dB in 0.5 dB steps for maximum flexibility in driving an ADC.

The ADRF6620 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 48 pin, RoHS-compliant, 7 mm x 7 mm LFCSP package with an exposed paddle. Performance is specified over the -40°C to +85°C temperature range.

Rev. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LO INPUT					
LO Internal Frequency		350		2850	MHz
External LO Frequency		350		6000	MHz
LO Input Level					dBm
LO Input Impedance			50		Ω
RF INPUT					
RF Frequency		700		2700	MHz
Return Loss			12		dB
Input Impedance			50		Ω
Input Power				TBD	dBm
RF DIGITAL SWITCH ATTENUATOR					
Attenuation Range	Step size: 1dB	0		15	dB
SUPPLY VOLTAGE		4.7	5.0	5.25	V
External LO + IF Amp			1.3		W
Internal LO + IF Amp			1.7		W
IF Amp			0.5		W

SYSTEM SPECIFICATIONS: RF INPUT TO IF AMPLIFIER OUTPUT

VCC = 5 V, ambient temperature (T_A) = 25°C, high side LO injection, f_{IF} = 200 MHz, internal LO mode, IF amp output load = 150 Ω, 2 V p-p differential output

Table 2. RF Switch + Balun + RF Attenuator+ Mixer + IF Amp

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE AT RF = 900 MHz	IF = 200 MHz				
Conversion Gain			11.5		dB
Output P1dB			18		dBm
OIP3	−1 V p-p each output tone, 1MHz tone spacing		45		dBm
OIP2	−1 V p-p each output tone, 1MHz tone spacing		78		dBm
Noise Figure					
DYNAMIC PERFORMANCE AT RF = 1900 MHz	IF = 200 MHz				
Conversion Gain			10.5		dB
Output P1dB			18		dBm
OIP3	−1 V p-p each output tone, 1MHz tone spacing		44		dBm
OIP2	−1 V p-p each output tone, 1MHz tone spacing		68		dBm
Noise Figure					
DYNAMIC PERFORMANCE AT RF = 2100 MHz	IF = 200 MHz				dB
Conversion Gain			10		dBm
Output P1dB			18		dBm
OIP3	−1 V p-p each output tone, 1MHz tone spacing		44		dBm
OIP2	−1 V p-p each output tone, 1MHz tone spacing		64		dBm
Noise Figure					
DYNAMIC PERFORMANCE AT RF = 2700 MHz	IF = 200 MHz				
Conversion Gain			9		dB
Output P1dB			18		dBm
OIP3	−1 V p-p each output tone, 1MHz tone spacing		44		dBm
OIP2	−1 V p-p each output tone, 1MHz tone spacing		74		dBm
Noise Figure					

SYNTHESIZER/PLL SPECIFICATIONS

VCC = 5 V, ambient temperature (T_A) = 25°C, f_{REF} = 153.6 MHz, f_{REF} power = 4 dBm, f_{PFD} = 38.4 MHz, loop filter bandwidth = 100 kHz

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
PLL Reference Frequency		12		464	MHz
PLL Reference Amplitude		TBD	4	14	dBm
PFD Frequency		24		58	MHz
Internal VCO Range		2800		5700	MHz
Open Loop SSB Phase Noise	VTUNE = 2 V				
$f_{LO} = f_{VCO}/2$ = 1.7 GHz, f_{VCO} = 3.4 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−81		dBc/Hz
	100 kHz offset		−103		dBc/Hz
	800 kHz offset		−123		dBc/Hz
	1 MHz offset		−125		dBc/Hz
	6 MHz offset		−143		dBc/Hz
	10 MHz offset		−147		dBc/Hz
	40 MHz offset		−155		dBc/Hz
$f_{LO} = f_{VCO}/2$ = 2.3 GHz, f_{VCO} = 4.6 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−74		dBc/Hz
	100 kHz offset		−101		dBc/Hz
	800 kHz offset		−123		dBc/Hz
	1 MHz offset		−125		dBc/Hz
	6 MHz offset		−143		dBc/Hz
	10 MHz offset		−147		dBc/Hz
	40 MHz offset		−156		dBc/Hz
$f_{LO} = f_{VCO}/2$ = 2.75 GHz, f_{VCO} = 5.5 GHz	1 kHz offset		−39		dBc/Hz
	10 kHz offset		−69		dBc/Hz
	100 kHz offset		−99		dBc/Hz
	800 kHz offset		−121		dBc/Hz
	1 MHz offset		−124		dBc/Hz
	6 MHz offset		−142		dBc/Hz
	10 MHz offset		−146		dBc/Hz
	40 MHz offset		−155		dBc/Hz
REFERENCE SPURS	f_{REF} = 153.6 MHz, f_{PFD} = 38.4 MHz,				
	$f_{PFD}/2$				dBc
	$f_{PFD} \times 1$		−82		dBc
	$f_{PFD} \times 2$				dBc
	$f_{PFD} \times 3$				dBc
CLOSED LOOP PERFORMANCE	f_{REF} = 153.6 MHz, f_{PFD} = 38.4 MHz, 120 kHz loop filter				
$f_{LO} = f_{VCO}/2$ = 1.7 GHz, f_{VCO} = 3.4 GHz	1 kHz offset		−93		dBc/Hz
	10 kHz offset		−104		dBc/Hz
	100 kHz offset		−99		dBc/Hz
	800 kHz offset		−120		dBc/Hz
	1 MHz offset		−123		dBc/Hz
	6 MHz offset		−137		dBc/Hz
	10 MHz offset		−144		dBc/Hz
	40 MHz offset		−158		dBc/Hz
	Integrated phase noise (1 kHz to 40 MHz)		0.21		° rms
	Figure of merit[1]		−222		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Lock Time			TBD	µS
$f_{LO} = f_{VCO}/2 = 2.3$ GHz, $f_{VCO} = 4.6$ GHz	1 kHz offset		−90		dBc/Hz
	10 kHz offset		−100		dBc/Hz
	100 kHz offset		−97		dBc/Hz
	800 kHz offset		−116		dBc/Hz
	1 MHz offset		−121		dBc/Hz
	6 MHz offset		−138		dBc/Hz
	10 MHz offset		−145		dBc/Hz
	40 MHz offset		−156		dBc/Hz
	Integrated phase noise (1 kHz to 40 MHz)		0.3		° rms
	Figure of merit[1]		−222		dBc/Hz
	Lock Time			TBD	µS
$f_{LO} = f_{VCO}/2 = 2.75$ GHz, $f_{VCO} = 5.5$ GHz	1 kHz offset		−88		dBc/Hz
	10 kHz offset		−96		dBc/Hz
	100 kHz offset		−95		dBc/Hz
	800 kHz offset		−120		dBc/Hz
	1 MHz offset		−122		dBc/Hz
	6 MHz offset		−138		dBc/Hz
	10 MHz offset		−145		dBc/Hz
	40 MHz offset		−157		dBc/Hz
	Integrated phase noise (1 kHz to 40 MHz)		0.38		° rms
	Figure of merit[1]		−222		dBc/Hz
	Lock Time			TBD	µS

[1] The figure of merit (FOM) is computed as phase noise (dBc/Hz)-10Log10(f_{PFD}) – 20Log10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 160 MHz, f_{REF} power = 4 dBm with a 40 MHz f_{PFD}. The FOM was computed at 50 kHz offset.

RF INPUT TO MIXER OUTPUT SPECIFICATIONS

VCC = 5 V, ambient temperature (T_A) = 25°C, high side LO injection, f_{IF} = 200 MHz, external LO mode, RF attenuation = 0 dB

Table 4. RF Switch + Balun + RF Attenuator+ Mixer

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER GAIN	Differential 255 Ω load		−4		dB
MIXER LOAD IMPEDANCE	Differential		255		Ω
GAIN FLATNESS				1	dB
DYNAMIC PERFORMANCE @ RF = 900 MHz					
Conversion Gain	C_{IN} = 6, C_{OUT} = 8, IF = 200 MHz		−2		dB
Input P1dB			17		dBm
IIP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
IIP2	−5 dBm each input tone, 1 MHz tone spacing		65		dBm
Noise Figure			15		dB
LO to RF Leakage			−70		dBm
RF to LO Leakage			−60		dBc
LO to IF Leakage			−32		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−45		dBc
Isolation[1]	Isolation between RFIN0 to RFIN3		−52		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE @ RF = 1900 MHz					
Conversion Gain	C_{IN} = 0, C_{OUT} = 2, IF = 200 MHz		−3		dB
Input P1dB			17		dBm
IIP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
IIP2	−5 dBm each input tone, 1 MHz tone spacing		62		dBm
Noise Figure			17		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−50		dBc
LO to IF Leakage			−35		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−43		dBc
Isolation	Isolation between RFIN0 to RFIN3		−47		dBc
DYNAMIC PERFORMANCE @ RF = 2100 MHz					
Conversion Gain	C_{IN} =2, C_{OUT} = 2, IF = 200 MHz		−3.5		dB
Input P1dB			18		dBm
IIP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
IIP2	−5 dBm each input tone, 1 MHz tone spacing		54.5		dBm
Noise Figure			18		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−40		dBc
LO to IF Leakage			−35		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−40		dBc
Isolation	Isolation between RFIN0 to RFIN3		−45		dBc
DYNAMIC PERFORMANCE @ RF = 2700 MHz					
Conversion Gain	C_{IN} = 2, C_{OUT} = 0, IF = 200 MHz		−4.7		dB
Input P1dB			19		dBm
IIP3	−5 dBm each input tone, 1 MHz tone spacing		40		dBm
IIP2	−5 dBm each input tone, 1 MHz tone spacing		56		dBm
Noise Figure			21		dB
LO to RF Leakage			−60		dBm
RF to LO Leakage			−45		dBc
LO to IF Leakage			−40		dBm
RF to IF Leakage	With respect to 0 dBm RF input power		−42		dBc
Isolation	Isolation between RFIN0 to RFIN3		−41		dBc

[1] Isolation between RF inputs. An input signal was applied to RFIN0 while RFIN1-RFIN3 were terminated with 50Ω. The IF signal amplitude was measured at the mixer output. Next, the internal switch was configured for RFIN3 and the feed thru was measured as a delta from the fundamental. This difference is recorded as isolation between RFIN0 and RFIN3.

VARIABLE GAIN IF AMPLIFIER SPECIFICATIONS

VCC = 5 V, ambient temperature (T_A) = 25°C, R_s = R_L = 150 Ω, f_{IF} = 200 MHz.

Table 5. Variable Gain IF Amplifier

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
−1 dB BANDWIDTH			600		MHz
SLEW RATE					V/ns
INPUT STAGE					
Maximum Input Swing			10.8		V p-p
Input Impedance	Differential		150		Ω
Common Mode Input Voltage			1.5		V
CMRR			50		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN					
Voltage Gain	Step size 0.5 dB, Differential 150Ω load	3		15	dB
Gain Flatness	For 20 MHz		0.2	1.0	dB
Gain Accuracy		0.25			dB
Gain Temperature Sensitivity					
Gain Step Response					
OUTPUT STAGE					
Output Voltage Swing					
Output Impedance	Differential		150		Ω
NOISE/HARMONIC PERFORMANCE @ 200 MHZ					
Output P1dB					
OIP3	Differential 150 Ω load		TBD		dBm
OIP2	Differential 150 Ω load		TBD		dBm
HD2	Differential 150 Ω load		TBD		dBc
HD3	Differential 150Ω load		TBD		dBc
Noise Figure	Differential 150Ω load		TBD		dB
POWER					
Power Up Current					mA
Power Down Current			6		mA

DIGITAL LOGIC SPECIFICATIONS

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{IH} (Input Voltage High)		1.4			V
V_{IL} (Input Voltage Low)				0.70	V
V_{OH} (Output Voltage High)	I_{OH} = −100 µA	2.3			V
V_{OL} (Output Voltage Low)	I_{OL} = 100 µA	0.2			V
Serial Clock Period	t_{CLK}	38			ns
Setup Time Between Data and Rising Edge of SCLK	t_{DS}	8			ns
Hold Time Between Data and Rising Edge of SCLK	t_{DH}	8			ns
Setup Time Between Falling Edge of CSB and SCLK	t_S	10			ns
Hold Time Between Rising Edge of CSB and SCLK	t_H	10			ns
Minimum Period that SCLK Should Be in a Logic High State	t_{HI}	10			ns
Minimum Period that SCLK Should Be in a Logic Low State	t_{LO}	10			ns
Maximum Time Delay Between Falling Edge of SCLK and Output Data Valid for a Read Operation	t_{ACCESS}			231	ns
Maximum Time Delay Between CSB Deactivation and SDIO Bus Return to High Impedance	t_z			5	ns

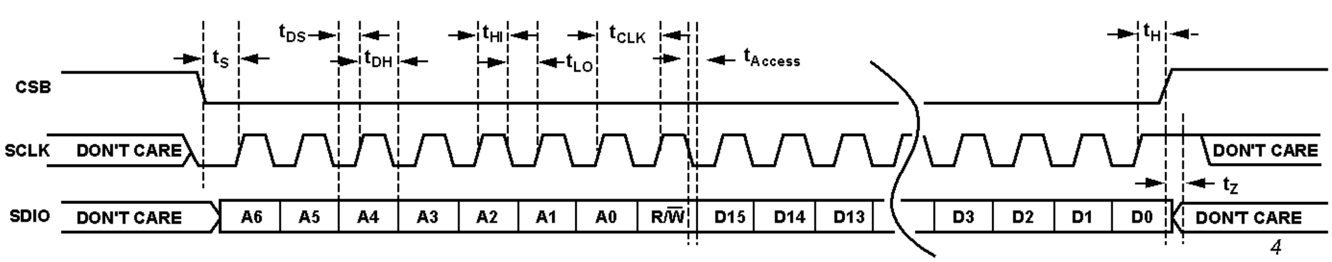

Figure 2. Setup and Hold Timing Measurements

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
VCC	−0.5 V to +5.5 V
RFSW0, RFSW1	−0.3 V to +3.6 V
RFIN0 to RFIN3	2.5 V peak ac-coupled
LOIN, LOIP	16 dBm
REFIN	−0.3 V to +3.6 V
IFIN, IFIP	−1.2 V to +3.6 V
SEN, SCLK, SDATA	−0.3 V to +3.6 V
VTUNE	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

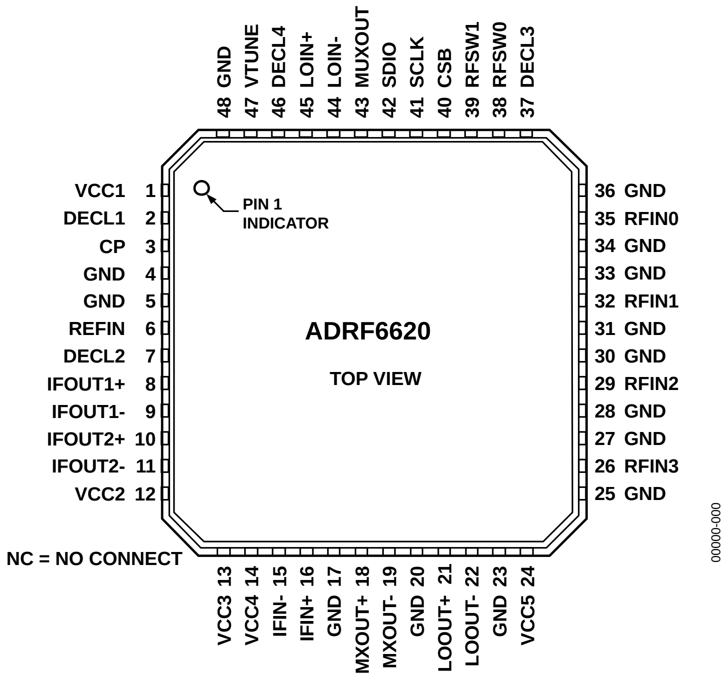

Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC1	5 V Power Supply. Connect a 100 pF and 0.1 µF capacitors between this pin and ground and locate them close to the pin.
2	DECL1	3.3 V LDO Decoupling. Connect a 100 pF and 0.1 µF capacitors between this pin and ground and locate them close to the pin.
3	CP	Charge Pump Output. Connect to VTUNE pin through the loop filter
4, 5	GND	Ground
6	REFIN	PLL Reference Clock Input. Nominal input level is 1Vppk. Input range is 10MHz to 320 MHz. Pin is internally biased and should be AC coupled.
7	DECL2	2.5V LDO Decoupling. Connect a 100 pF and 0.1 µF capacitors between this pin and ground and locate them close to the pin.
8, 9, 10, 11	IFOUT1+, IFOUT1-, IFOUT2+, IFOUT2-	The IF amplifier outputs on the ADRF6620 have two output pins for each polarity and they are oriented in an alternating fashion, IFOUT1+ (pin 8), IFOUT1- (pin 9), IFOUT2+ (pin 10) and IFOUT2- (pin11). The positive pins should be connected where IFOUT1+ and IFOUT2+ are tied together. Similarly, the negative pins should be connected where IFOUT1- and IFOUT2- are tied together. The output stage of the IF amp is an open collector configuration which requires a DC bias of +5V nominal. Bias choke inductors can be used to achieve this configuration. The bias choke inductors should be carefully chosen to be able to handle a maximum current of 50 mA on each side.
12	VCC2	5 V Power Supply. Connect a 100 pF and 0.1 µF capacitors between this pin and ground and locate them close to the pin.
13, 14	VCC3, VCC4	Factory Calibration Pins. Connect to 5V power supply.
15, 16	IFIN-, IFIN+	Differential IF Amp Inputs.
17	GND	Ground.
18,19	MXOUT+, MXOUT-	Differential Mixer Outputs. The output stage of the mixer is an open collector configuration which requires a DC bias of +5V nominal. Bias choke inductors can be used to achieve this configuration. The bias choke inductors should be carefully chosen to be able to handle a maximum current of 50 mA on each side.
20	GND	Ground.
21, 22	LOOUT+, LOOUT-	Differential LO Outputs. The differential output impedance is 50 Ω
23	GND	Ground

Pin No.	Mnemonic	Description
24	VCC5	5 V Power Supply. Connect a 100 pF and 0.1 μF capacitors between this pin and ground and locate them close to the pin.
25, 27, 28, 30, 31, 33, 34, 36	GND	Ground.
26, 29, 32, 35	RFIN3 – RFIN0	RF Inputs. Terminate unused RF inputs with a DC blocking cap to GND. The single-ended RF inputs have a 50 Ω input impedance.
37	DECL3	3.3V LDO Decoupling. Connect a 100 pF and 0.1 μF capacitors between this pin and ground and locate them close to the pin.
38, 39	RFSW0, RFSW1	Refer to Table 10. For a logic high, connect this pin to 2.5 V logic.
40	CSB	SPI Chip Select, Active Low. 3.3 V tolerant logic levels.
41	SCLK	SPI Clock. 3.3 V tolerant logic levels.
42	SDIO	SPI Data Input and Output. 3.3 V tolerant logic levels.
43	MUXOUT	Multiplex Output. Output pin providing the PLL reference signal or the PLL lock detect.
44, 45	LOIN-, LOIN+	Differential Local Oscillator Inputs. Differential input impedance of 50 Ω.
46	DECL4	VCO LDO Decoupling. Connect a 100 pF and 0.1 μF capacitors between this pin and ground and locate them close to the pin.
47	VTUNE	VCO Tuning Voltage. This pin is driven by the output of the loop filter and the nominal input voltage range is 1.5 V to 2.5 V.
48	GND	Ground.
49 (EPAD)	Exposed pad (EPAD)	Ground. Pin 49 is the exposed thermal pad on the bottom of the package. The exposed pad must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

SYSTEM PERFORMANCE: RF INPUT TO IF AMP OUTPUT

VCC = 5 V, T = 25°C, RFDSA @ minimum attenuation, IFAMP @ max gain, third-order, low-pass filter between the mixer output and IF amp input, high side LO, internal LO, IF frequency = 200 MHz

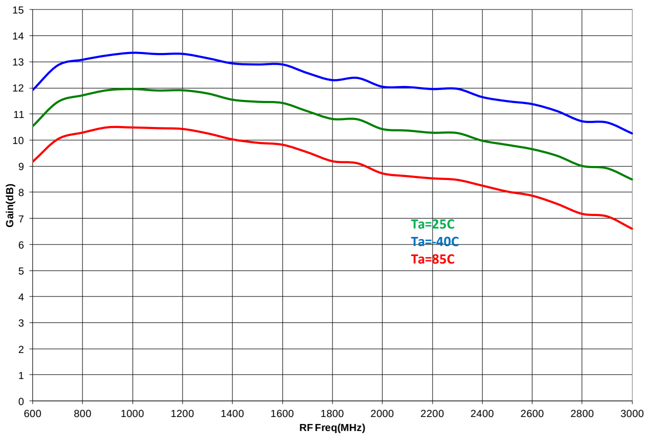

Figure 4. Gain vs. RF Frequency, IF Freq=200 MHz

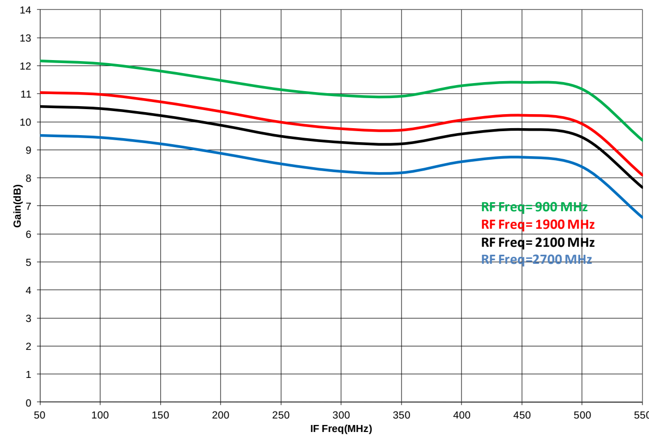

Figure 7. Gain vs. IF Frequency, LO Sweep with Fixed RF, IF Roll off

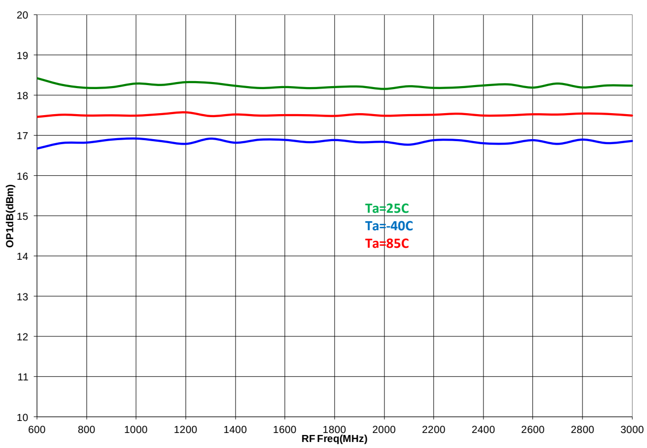

Figure 5. OP1dB vs. RF Frequency

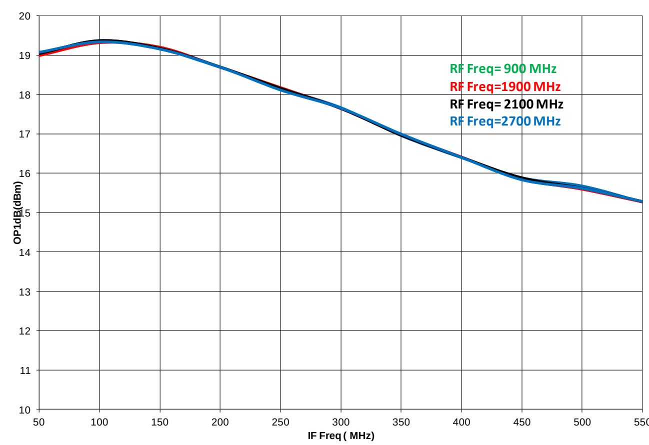

Figure 8. OP1dB vs. IF Frequency, LO Sweep with Fixed RF, IF Roll off

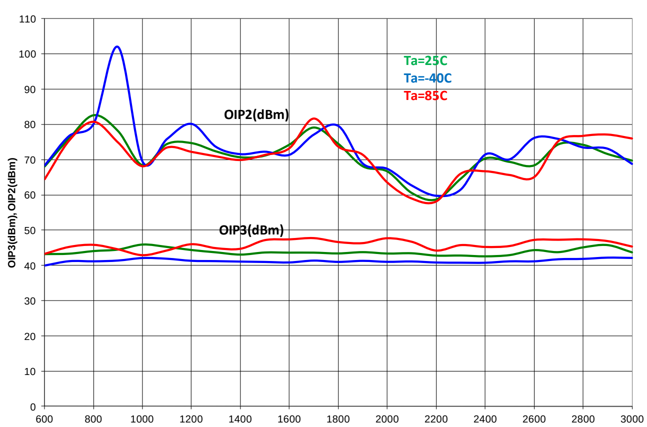

Figure 6. OIP2 / OIP3 vs. RF Frequency, Measured on 1 Vpp on each tone

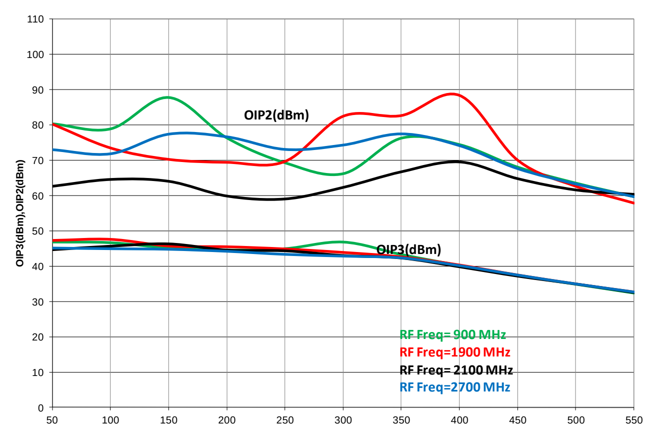

Figure 9. OIP2 / OIP3 vs. . IF Frequency, LO Sweep with Fixed RF, IF Roll off

PHASED-LOCKED LOOP

VCC = +5 V, T = 25°C

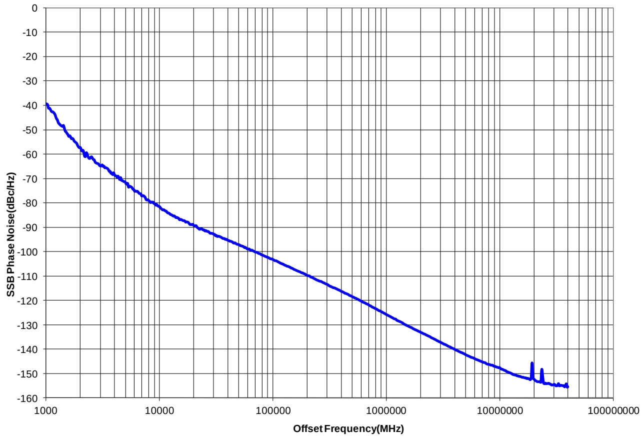

Figure 10. Open Loop VCO Phase Noise, F_{VCO} = 3.4 GHz, LODIVA=0, VTUNE=2V

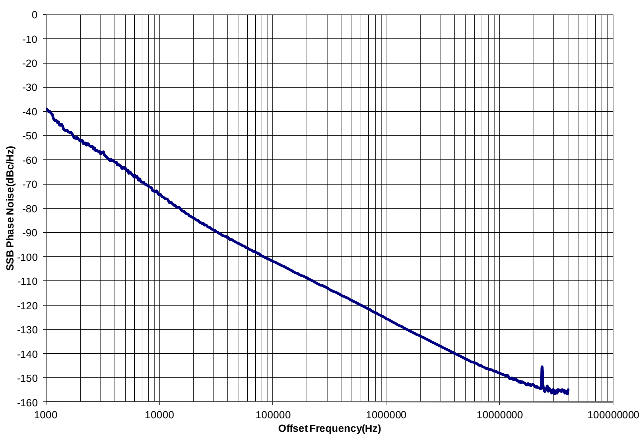

Figure 11. Open Loop Phase Noise, F_{VCO} = 4.6 GHz, LODIVA=0, VTUNE=2V

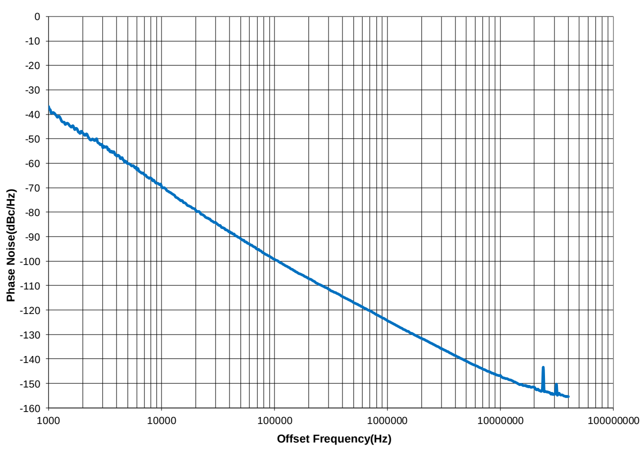

Figure 12. Open Loop Phase Noise, F_{VCO} = 5.5 GHz, LODIVA=0, VTUNE=2V

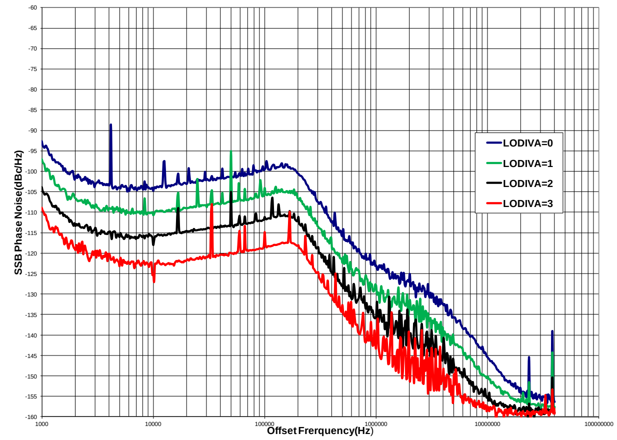

Figure 13. Closed Loop Phase Noise for Various LO_DIV_A dividers, F_{VCO} = 3.4 GHz, 120 KHz Loop Filter, REF Freq=153.6 MHz, REF Pin = +4 dBm, PFD=38.4 MHz

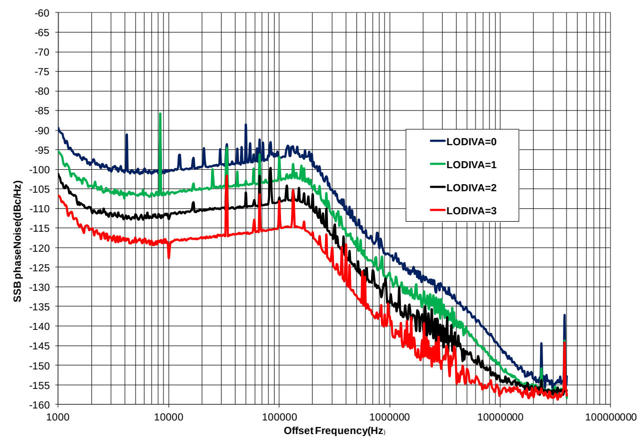

Figure 14. Closed Loop Phase Noise for Various LO_DIV_A dividers, F_{VCO} = 4.6 GHz, 120 KHz Loop Filter, REF Freq=153.6 MHz, REF Pin = +4 dBm, PFD=38.4 MHz

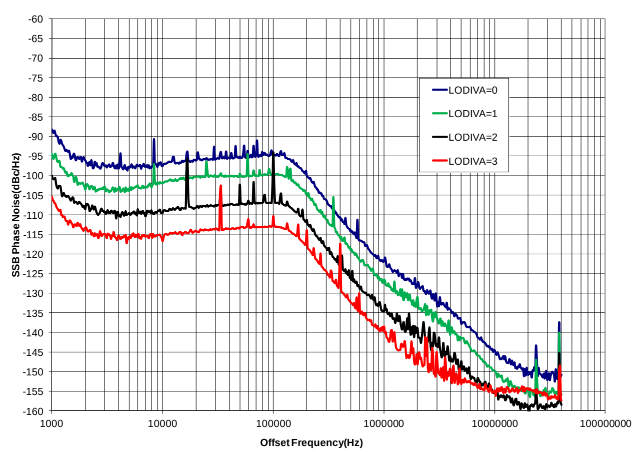

Figure 15. Closed Loop Phase Noise for Various LO_DIV_A dividers, F_{VCO} = 5.532 GHz, 120 KHz Loop Filter, REF Freq=153.6 MHz, REF Pin = +4 dBm, PFD=38.4 MHz

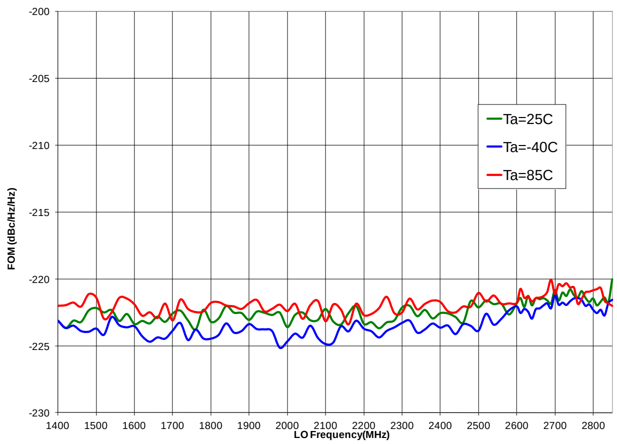

Figure 16. PLL Figure of Merit

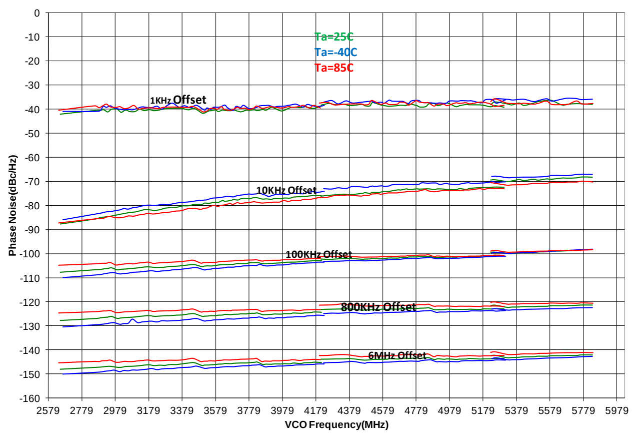

Figure 17. Open Loop Phase Noise vs. VCO Frequency LODIVA=0

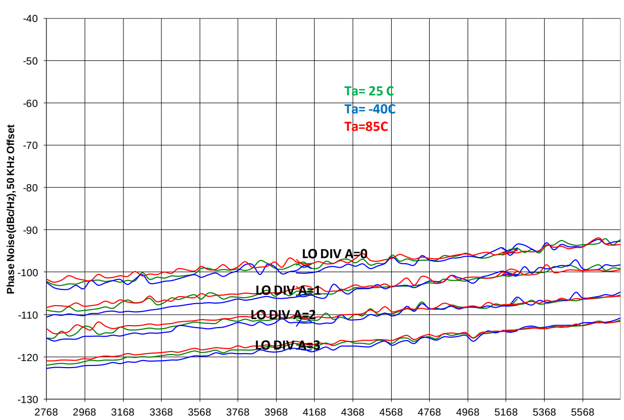

Figure 18. 120 KHz BW Loop Phase Noise 50 KHz Offset, LODIVA=1

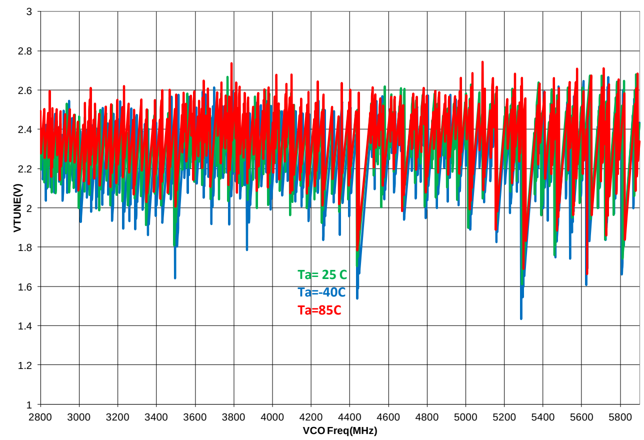

Figure 19. VTUNE vs VCO Frequency

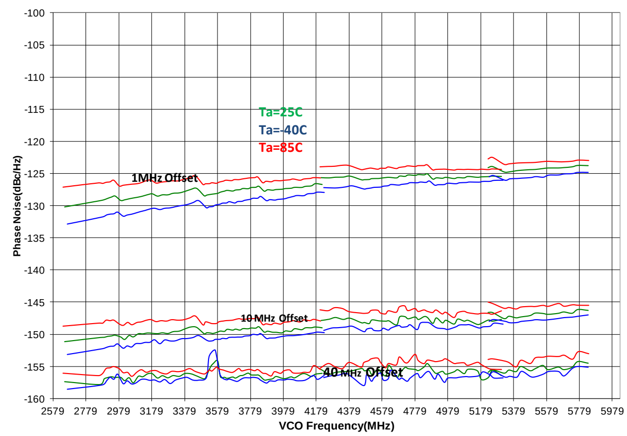

Figure 20. Open Loop Phase Noise vs. VCO Frequency LODIVA=0

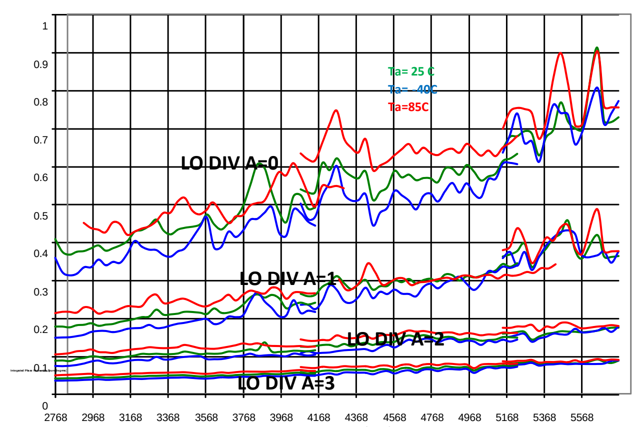

Figure 21. Integrated Phase Noise with spurs , LODIVA=0,1,2,3

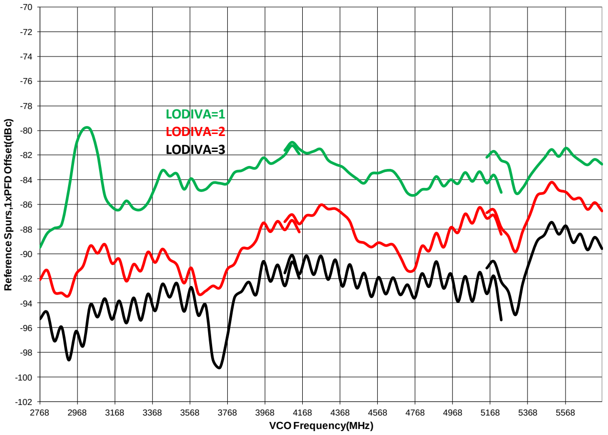

Figure 22. Reference Spurs, LODVA=1,2,3 ,1xPFD Offset, measured on LO Output

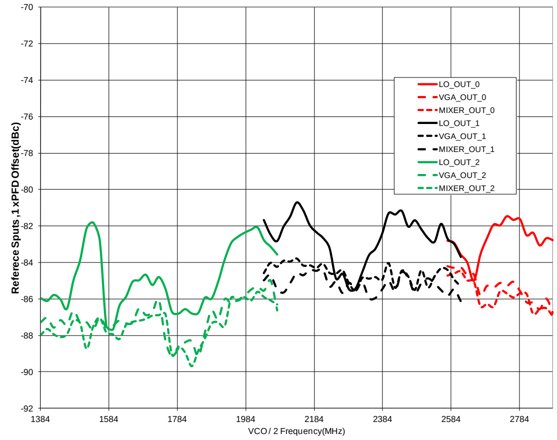

Figure 23. Reference Spurs, LODVA=1 ,1xPFD Offset, measured on LO Output, Mixer Output and VGA Output

VARIABLE GAIN IF AMPLIFIER

VCC = +5 V, T = 25°C, R_S = R_L = 150 Ω, IF = 200 MHz, 2 Vppk differential output unless otherwise noted

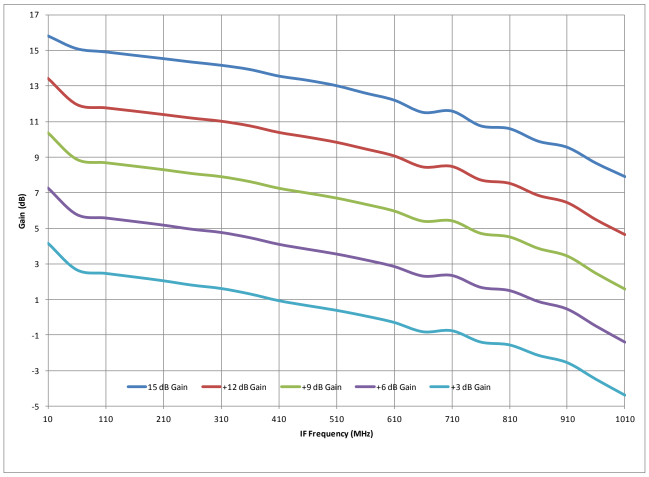

Figure 24. Gain vs. Frequency

TBD

Figure 27. Gain vs. Gain Code

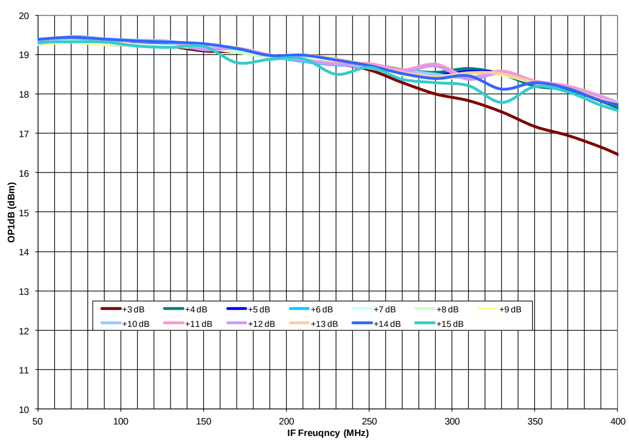

Figure 25. OP1 dB vs. IF Frequency

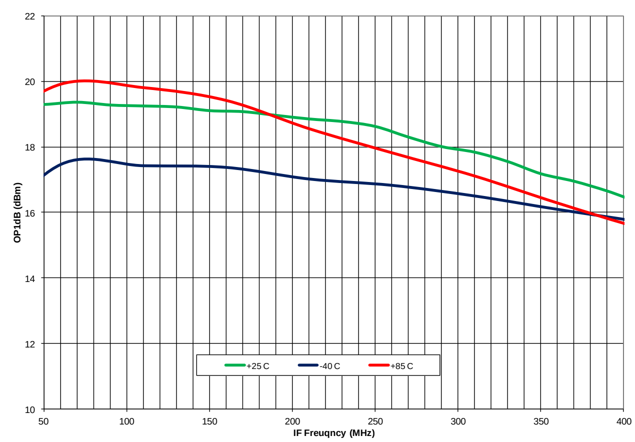

Figure 28. OP1 dB vs. IF Frequency, Temp Sweep, +15 dB Gain

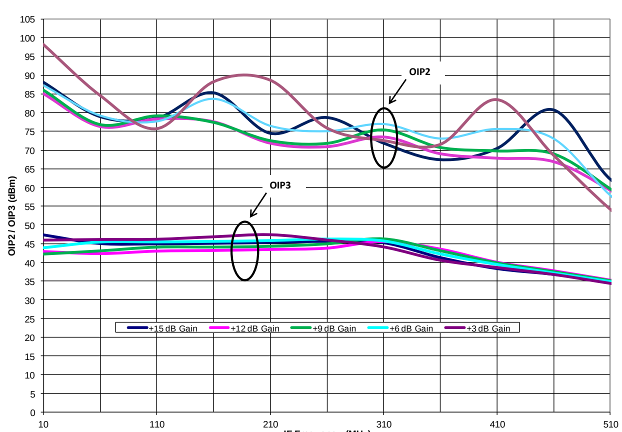

Figure 26. OIP3 vs. IF Frequency

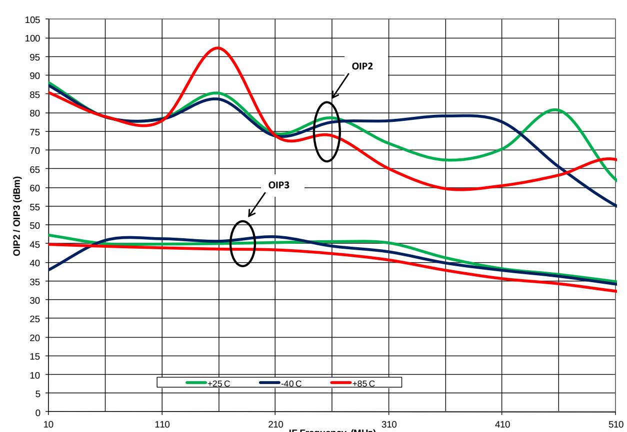

Figure 29. OIP2/OIP3 vs. IF Frequency, Temp Sweep, +15 dB Gain

RF INPUT TO MIXER OUTPUT PERFORMANCE

VCC = 5 V, T = 25°C, R_L = 250 Ω, f_{LO} = external, P_{LO} = 0 dBm, RFDSA = 0dB, RFSWSEL = 0

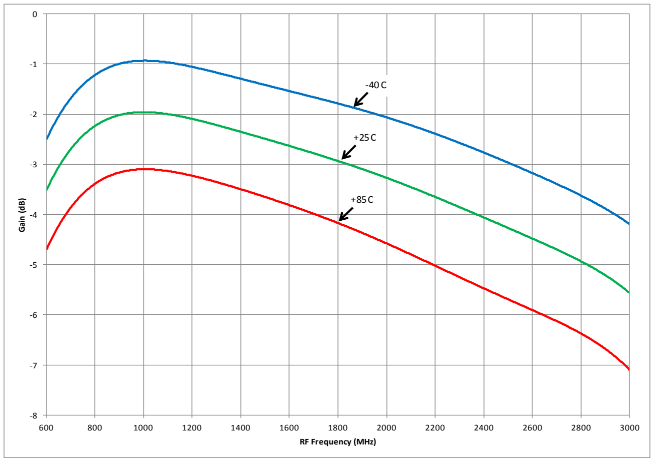

Figure 30. Gain vs. RF Frequency, Cin and Cout Optimized

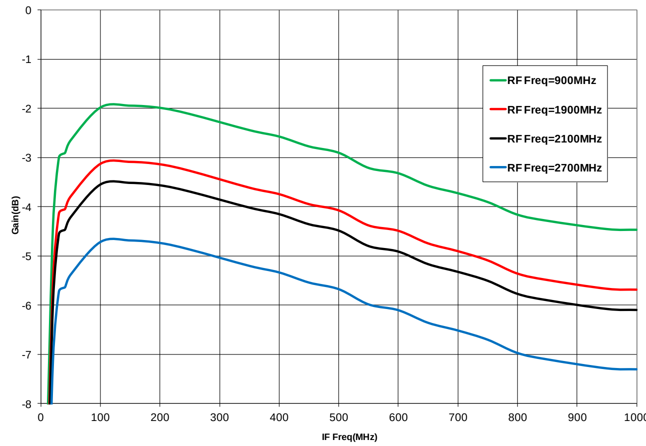

Figure 33. Gain vs. IF FrequencyLO Sweep with Fixed RF, IF Roll off

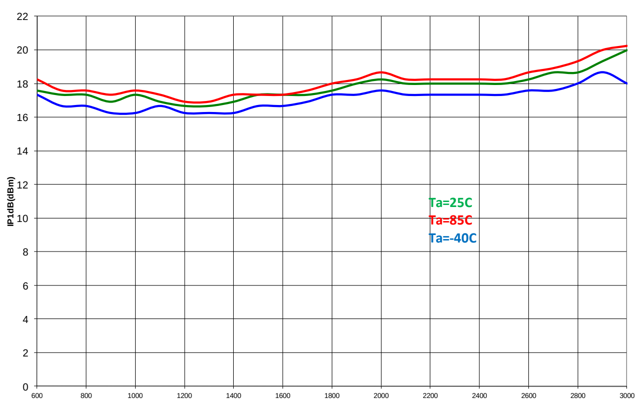

Figure 31. P1dB vs. RF Frequency

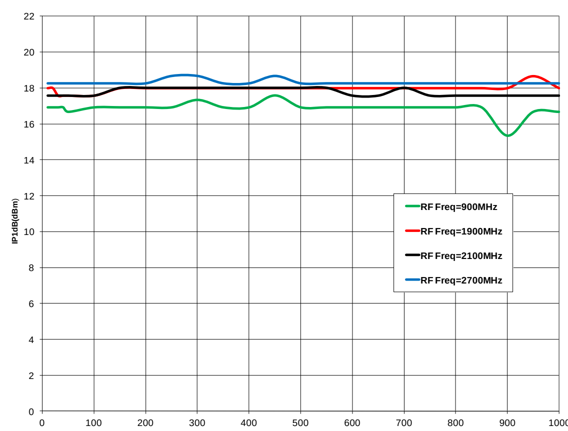

Figure 34. P1dB vs. IF Frequency LO Sweep with Fixed RF, IF Roll off

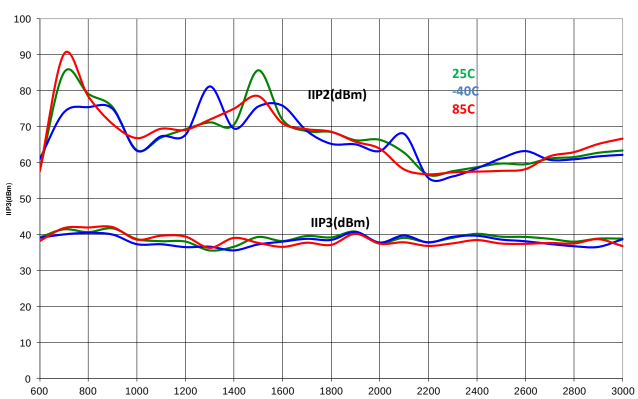

Figure 32. IP2/IP3 vs. RF Frequency, Pin =-5dBm /tone, 1MHz spacing

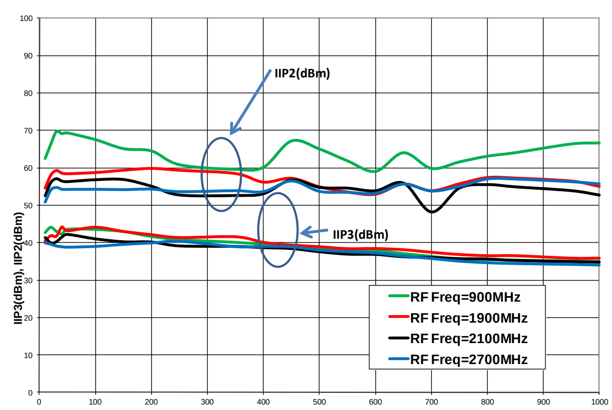

Figure 35. IP2/IP3 vs. IF Frequency, Pin =-5dBm /tone, 1MHz spacing LO Sweep with Fixed RF, IF Roll off

THEORY OF OPERATION

The ADRF6620 integrates the essential building blocks to offer the most complete receiver solution, especially for the feedback down converter path for digital pre-distortion in cellular base stations. The main features that make the ADRF6620 an attractive solution include a SP4T RF input switch with variable attenuation, a tunable balun, a wideband active mixer, and an IF variable gain amplifier. Additionally, the ADRF6620 integrates a local oscillator (LO) generation block consisting of a synthesizer and a multi-core VCO with an octavee range and low phase noise. The synthesizer uses a Fractional-N PLL to enable continuous LO coverage from 700 MHz to 2850 MHz.

Putting all the building blocks of the ADRF6620 together, the signal path through the device starts at the RF input where one of four single-ended RF inputs is selected by the input mux and converted to a differential signal via a tunable balun. The differential RF signal is attenuated to an optimal input level via the digital step attenuator with 15 dB of attenuation range in 1dB steps. The RF signal is then mixed via a Gilbert cell mixer with the LO signal down to an IF frequency. The 255 Ω terminated differential output of the mixer is brought off chip to a pair of inductors and passed through an IF filter. The output of such filter is AC coupled off chip and fed to an on chip digital attenuator and IF amplifier. The output of the IF amplifier is then passed to an off chip ADC.

INPUT SWITCHES

The ADRF6620 integrates a single pole four through (SP4T) switch where 1 of 4 RF inputs is selected. Control of the desired RF input can be achieved externally via pin control or serially via register writes to the SPI. Pin control allows faster control over the switch as compared to the serial write approach. Using the pins the RF switches can switch at speeds up to 100 ns. When using the serial port control the switch time would be 100 ns plus the latency of the SPI programming.

Register 0x23[11], RFSW_MUX, selects whether the RF input switch is controlled via the pins or serially. By default at power up the device is configured for serial control. Writing to bits 9 and 10 in register 0x23, RFSW_SEL, allows selection of one of the four RF inputs. Alternatively, by making the RFSW_MUX bit high, pins 38 and 39 can be used to control the RF input. **Table 10** summarizes the different control options for the RF inputs.

Table 10. RF Input Selection Table

RFSW_MUX	SPI Control Reg 0x23		Pin Control		
Reg 0x23[11]	[10]	[9]	Pin 39	Pin 38	RF Input
0	0	0	X	X	RFIN0
0	0	1	X	X	RFIN1
0	1	0	X	X	RFIN2
0	1	1	X	X	RFIN3
1	X	X	0	0	RFIN0
1	X	X	0	1	RFIN1
1	X	X	1	0	RFIN2
1	X	X	1	1	RFIN3

RFIN ports that are not used should be properly terminated to improve on isolation. The RFIN ports are internally terminated with 50 Ω and the DC level resides at 2.5V. In order not to disrupt the DC level, the recommended termination is a DC blocking cap to GND.

TUNABLE BALUN

The ADRF6620 integrates a programmable balun operating over a frequency range of 700 MHz to 2700 MHz. The tunable balun offers the benefit of ease of drivability with single-ended 50Ω RF inputs and the single-ended to differential conversion of the balun optimizes common mode rejection.

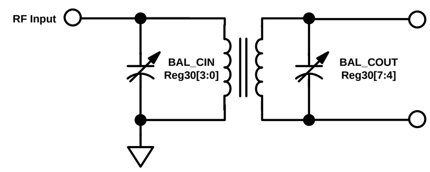

Figure 36. Integrated Tunable Balun

The RF balun tuning is accomplished by switching parallel capacitances on the primary and secondary sides of the balun by writing to register 0x30. The added capacitance in parallel with the inductive windings of the balun changes the resonant frequency of the LC tank. Therefore, selecting the proper combination of BAL_CIN and BAL_COUT will set the desired frequency and optimize gain. Under most circumstances, the input and output can be tuned together, though sometimes it may be advantageous for matching reasons to tune them separately. Refer to the application section titled "RF Input Balun Optimization for Gain" for recommended BAL_CIN and BAL_COUT settings.

RF ATTENUATOR

Following the tunable balun is the digital step attenuator (DSA). The attenuation range is 0 to 15 dB with a step size of 1dB. The control for the DSA can be found in register 0x23[8:5], RFDSA_SEL.

ACTIVE MIXER

The ADRF6620 has a double balanced mixer that uses high performance SiGe NPN transistors. This mixer is based on the Gilbert cell design of four cross-connected transistors.

The mixer output load provides a 255 Ω differential output resistance. The mixer output should be pulled to the positive supply externally using a pair of RF chokes or using an output transformer with the center tap connected to the positive supply.

VARIABLE GAIN IF AMPLIFIER

The ADRF6620 integrates a differential variable gain amplifier (VGA) consisting of a 150Ω digitally controlled passive attenuator followed by a highly linear transconductance amplifier with feedback. The attenuation range is 12 dB controlled through the serial interface registers and the transconductor amplifier has a fixed gain of 15 dB. Therefore, at minimum attenuation the gain of the IF amplifier is +15 dB and at max attenuation, the gain is +3 dB. The attenuation is controlled by addressing register 0x23[4:0], IF_ATTN. The attenuation step size is 0.5 dB.

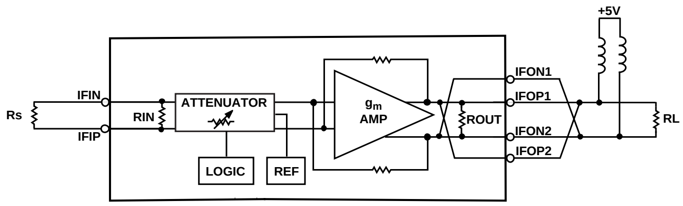

Figure 37. Simplified IF Amplifier Schematic

An independent internal voltage reference circuit sets the DC voltage level at the input of the amplifier to approximately 1.5 V. The reference is not accessible and cannot be adjusted.

The amplifier consumes 35 mA through the VCC pin and 75mA through the two choke inductors combined in its active state. The IF amplifier can be powered down by disabling register 0x01[11], IF_AMP_EN. In its power down state the IF amplifier current reduces to 6 mA. The DC level at the input remains at approximately 1.5 V regardless if the IF amplifier is enabled.

At minimum attenuation the gain of the IF amplifier is 15 dB when driving a 150 Ω load. The input and output resistance of the amplifier is set to 150 Ω in matched condition. If the load or the source resistance is not equal to 150 Ω, the following equations can be used to determine the resulting gain and input/output resistances.

$$Voltage\ Gain = A_V = 0.044 \times (1000||R_L)$$

$$R_{IN} = (1000 + R_L)/(1 + 0.044 \times R_L)$$

$$S21(Gain) = 2 \times R_{IN}/(R_{IN} + R_S) \times A_V$$

$$R_{OUT} = (1000 + R_S)/(1 + 0.044 \times R_S)$$

Note that at the maximum attenuation setting, R_s, as seen by the amplifier is the output resistance of the attenuator which is 150 Ω. However, at the minimum attenuation setting, R_s is the source resistance that is connected to the input of the part.

The DC current to the outputs of each amplifier is supplied through two external chokes. The inductance of the chokes and the resistance of the load in parallel with the output resistance of the device add a low frequency pole to the response. The parasitic capacitance of the chokes add to the output capacitance of the part. This total capacitance in parallel with the load and output resistance sets the high frequency pole of the device. Generally, the larger the inductance of the choke, the higher its parasitic capacitance. Therefore, this trade-off must be considered when the value and type of the choke are selected.

The amplifier has two output pins for each polarity and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. Refer to the Application section for the recommended PCB layout.

LO GENERATION BLOCK

The ADRF6620 offers two modes of sourcing the LO signal to the mixer. The first mode uses the on-chip phase locked loop (PLL) and voltage controlled oscillator (VCO) to generate the LO signal. This mode of operation provides a high quality LO that meets the performance requirements of most applications. Using the on-chip synthesizer and VCO removes the burden of generating and distributing a high-frequency LO signal. The second mode bypasses the integrated LO generation block and allows the LO to be supplied externally. This mode enables the user to provide a very high quality signal directly to the mixer core. Sourcing the LO signal externally may be necessary in demanding applications that require the lowest possible phase noise performance.

External LO Mode

The control to select either external or internal LO mode can be found in register 0x22[2:0], VCO_SEL. To configure for external LO mode, write 0x22[2:0] = 3 decimal and apply the differential LO signals to pin 44 (LOIN) and pin 45 (LOIP). The external LO frequency range is 350 MHz to 6 GHz. Only a 1X LO signal is required for the active mixer. However, the ADRF6620 offers the flexibility of using a higher frequency signal and dividing it down before it reaches the mixer. The LO divider can be found in register 0x22[4:3], LO_DIV_A, where the options are ÷1, ÷2, ÷4, ÷8.

The external LO input pins present a broadband differential 50 Ω input impedance. The LOIP and LOIN input pins must be AC coupled. When not in use these pins can be left unconnected.

Internal LO Mode

For internal LO mode, the ADRF6620 includes an on-chip VCO and PLL for LO synthesis. The PLL, illustrated in Figure 63, consists of a reference path, phase and frequency detector (PFD), charge pump, and a programmable integer divider with prescaler. The reference path takes in a reference clock and divides it down by a factor of 1, 2, 4, or 8 or multiplies it by a factor of 2 and then passes it to the PFD. The PFD compares this signal to the divided down signal from the VCO. Depending on the PFD polarity selected, the PFD sends an up/down signal to the charge pump if the VCO signal is slow/fast compared to the reference frequency. The charge pump sends a current pulse to the off chip loop filter to increase or decrease the tuning voltage, VTUNE.

The ADRF6620 integrates three VCO cores covering an octave range of 2.8 GHz to 5.7 GHz. Table 11, summarizes the frequency range for each VCO. The desired VCO can be selected by addressing register 0x22[2:0], VCO_SEL.

Table 11. VCO Range

VCO_SEL: 0x22[2:0]	Frequency Range
0	5.2 GHz to 5.7 GHz
1	4.1 GHz to 5.2 GHz
2	2.8 GHz to 4.1 GHz

The N-divider divides down the differential VCO signal to the PFD frequency. The N-divider can be configured for fractional or integer mode by addressing register 0x02[11], DIV_MODE. The default configuration is set for fractional mode. The following equations can be used to determine the N value and PLL frequency.

$$f_{PFD} = \frac{f_{VCO}}{2 \times N}$$

$$N = INT + \frac{FRAC}{MOD}$$

$$f_{LO} = \frac{f_{PFD} \times 2 \times N}{LO\_Divider}$$

f_{PFD} is the phase frequency detector frequency

f_{VCO} is the VCO frequency

INT is the integer divide ratio programmed in register 0x02

$FRAC$ is the fractional divider programmed in register 0x03

MOD is the modulus divide ratio programmed in register 0x04

f_{LO} is the LO frequency going to the mixer core when the loop is locked.

$LO\_Divider$ is the final divider block that divides the VCO frequency down by 1, 2, 4,or 8 before it reaches the mixer. This control is located in register 0x22[4:3]. Refer to Table 12.

Table 12. LO Divider

LO_DIV_A: 0x22[4:3]	LO_Divider
00	1
01	2
10	4
11	8

The lock detect signal is available as one of the selectable outputs through the MUXOUT pin, with a logic high signifying that the loop is locked. The control for the MUXOUT pin is located in register 0x21[6:4] and the default configuration is for PLL lock detect.

To ensure that the PLL locks to the desired frequency it is important to follow a proper write sequence of the PLL registers. The PLL registers should be configured accordingly to achieve the desired frequency and the last writes should be to registers 0x02 (INT), 0x03 (FRAC), or 0x04 (MOD). When registers 0x02, 0x03, and 0x04 are programmed, an internal VCO calibration is initiated and this is the last step to locking the PLL.

Additional LO Controls

The ADRF6620 offers additional configurability of the LO signal to make the device more versatile for different application cases. The LO output drive level can be controlled by accessing register 0x22[8:7]. This offers increased drive strengths of the LO signal. Table 13, shows the available drive levels.

Table 13. LO Drive Level

LO_DRV_LVL: 0x22[8:7]	Amplitude
00	-5 dBm
01	-1 dBm
10	1.5 dBm
11	3 dBm

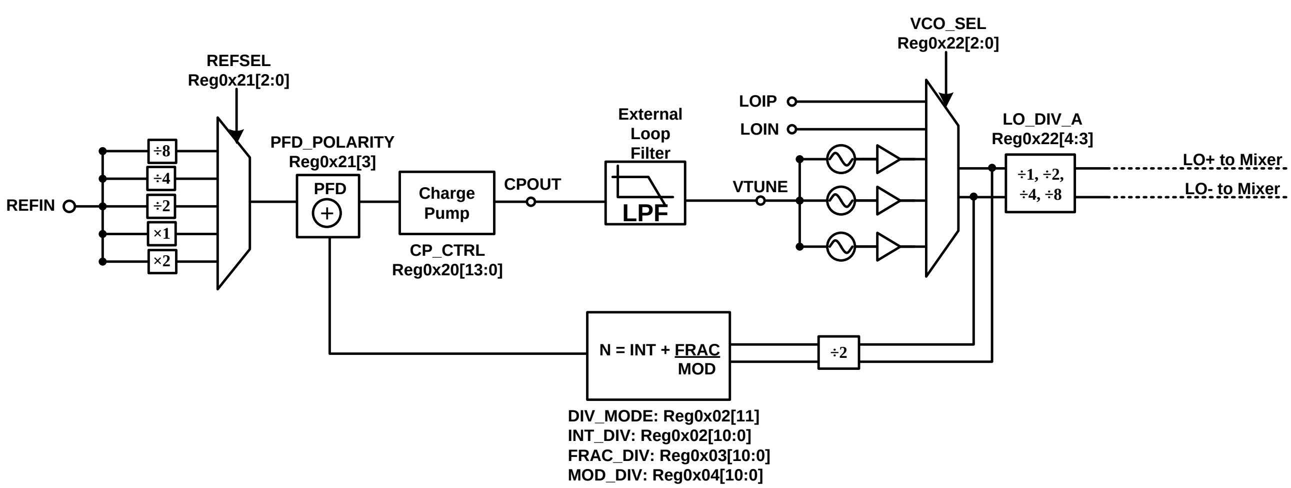

Figure 38. LO Generation Block Diagram

Additionally, the LO signal going to the mixer core is accessible through the LOIP and LOIN pins (pin 21 and 22) by enabling the LO_DRV_EN bit in register 0x01[7]. This flexibility offers direct monitoring of the LO signal to the mixer for debug purposes or the LO signal can be used to daisy chain many devices synchronously. One ADRF6620 can serve as the master where the LO signal is sourced and the subsequent slave devices share the same LO output signal from the master. This will substantially ease the LO requirements of a system requiring multiple LO's.

SERIAL PORT INTERFACE (SPI)

The ADRF6620 serial port interface (SPI) allows the user to configure the device for specific functions or operations through a structured register space provided inside the chip. This provides the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the serial port.

The serial port interface consists of three control lines SCLK, SDIO, and CSB. SCLK (serial clock) is the serial shift clock. SCLK synchronizes serial interface reads and writes. SDIO (serial data input/output) is an input and output depending on the instruction being sent and the relative position in the timing frame. CSB (chip select bar) is an active low control that gates the read and write cycles. The falling edge of CSB in conjunction with the rising edge of SCLK determines the start of the frame. All SCLK and SDIO activity is ignored when CSB is high. Figure 2and Table 6provide the serial timing and its definitions. Figure 2 is repeated below in Figure 39 as a quick reference.

The ADRF6620 protocol consists of 7 register address bits, followed by a Read/$\overline{\text{Write}}$, and 16 data bits. Both the address and data fields are organized MSB to LSB.

On a write cycle, up to 16 bits of serial write data is shifted in, MSB to LSB. If the rising edge of CSB occurs before the LSB of the serial data is latched only the bits that were latched will be written to the device. If more than 16 data bits are shifted in, the 16 most recent bits will be written to the device. The ADRF6620 input logic level for the write cycle supports an interface as low as 1.8V.

On a read cycle, up to 16 bits of serial read data is shifted out, MSB to LSB. Data shifted out beyond 16 bits will be undefined. Read back content at a given register address does not necessarily need to correspond with the write data of the same address. The output logic levels for a read cycle is 2.5V.

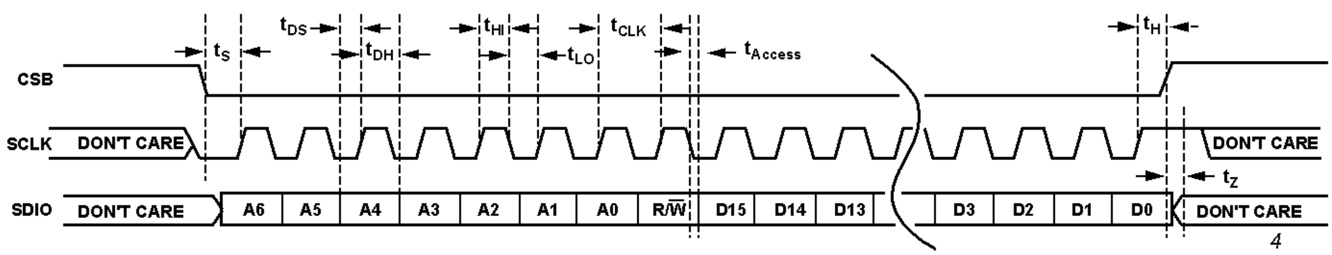

Figure 39. Serial Port Interface

APPLICATION INFORMATION

RF INPUT BALUN OPTIMIZATION FOR GAIN

The ADRF6620's gain was measured for every combination of CIN and COUT and the data is presented in plots shown in Figure 40 to Figure 43. As can be seen from the plots a range of CIN and COUT values can be used to optimize the ADRF6620's gain. Additionally, the optimized CIN and COUT values do not change over temperature. Once the values are chosen, the gain will change over temperature however, the signature of the CIN and COUT values will be fixed.

For low input frequencies, more capacitance will need to be switched in and this is achieved by programming higher codes into CIN and COUT, register0x30. On the contrary, at high frequencies minimal capacitance is required and therefore lower CIN and COUT codes are programmed.

These plots should only be used as guides and should not be interpreted in the absolute sense. Since every customer's application and PCB design are different, a recommended CIN and COUT value may fit one application but not another. Therefore, the plots should be used as reference guides to approximate the CIN and COUT values and further fine-tuning may be necessary to achieve max gain.

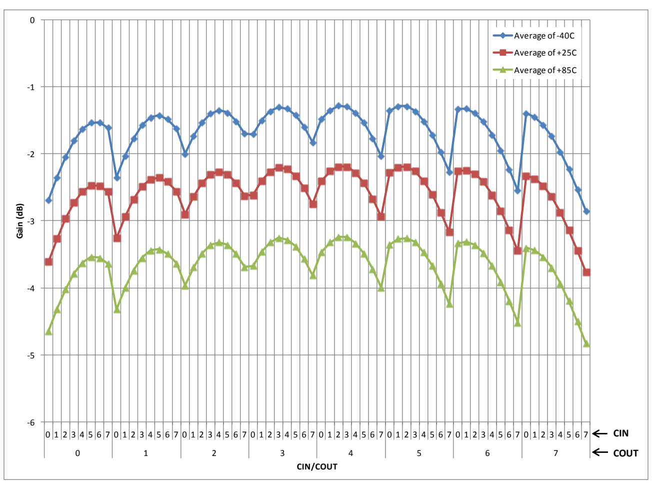

Figure 40. Gain vs. CIN and COUT at RF = 900 MHz

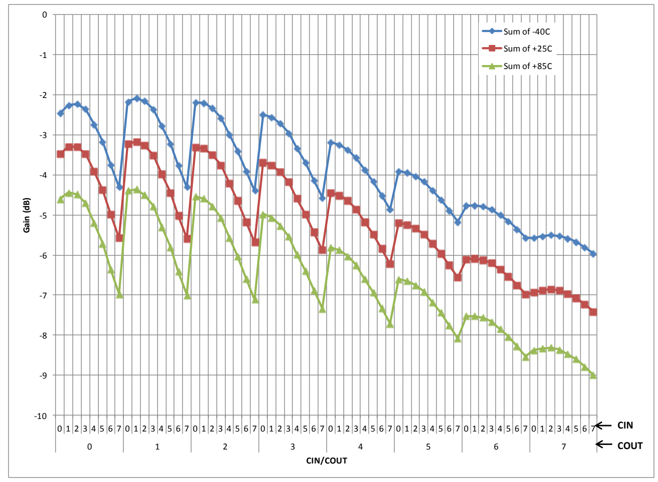

Figure 41. Gain vs. CIN and COUT at RF = 1900 MHz

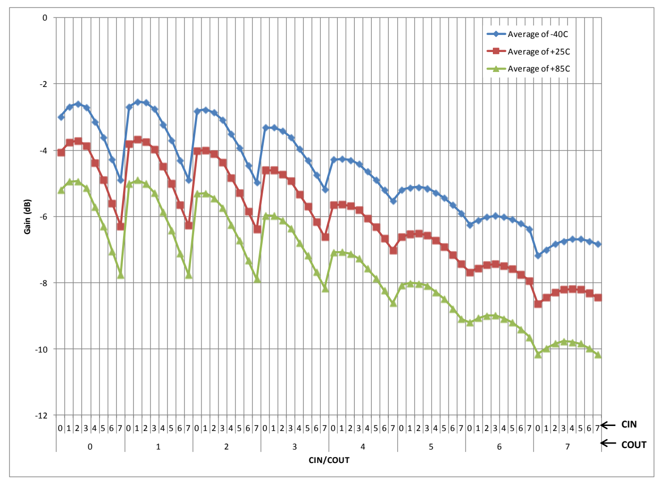

Figure 42. Gain vs. CIN and COUT at RF = 2100 MHz

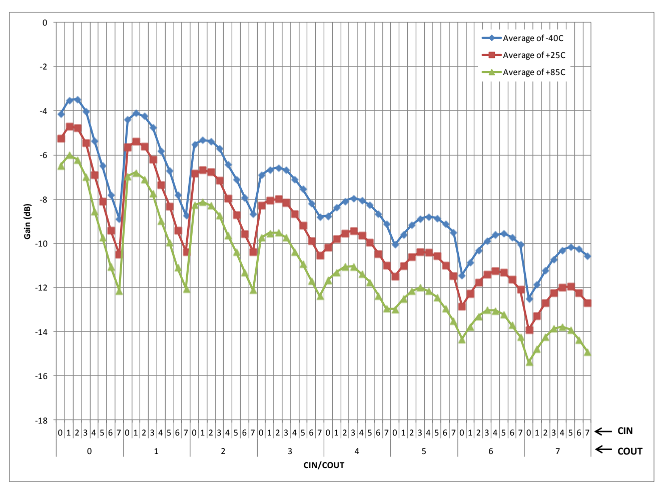

Figure 43. Gain vs. CIN and COUT at RF = 2700 MHz

Table 14.

			Optimized IIP3			IIP3 and NF Balance			Optimized NF		
RF Freq (MHz)	CIN	COUT	CDAC	RDAC	BIAS	CDAC	RDAC	BIAS	CDAC	RDAC	BIAS
600	14	14	10	6	4	15	4	2	15	4	0
700	14	14	14	5	4	15	4	2	15	4	0
800	10	10	13	5	4	14	3	2	15	2	0
900	6	8	12	5	4	13	3	2	14	2	0
940	6	6	12	5	4	11	5	2	13	2	0
1000	4	6	11	5	4	10	4	2	11	3	0
1100	2	4	10	5	4	10	3	1	11	2	0
1200	2	4	9	5	4	9	3	1	10	2	0
1300	0	4	8	8	4	9	3	1	10	2	0
1400	0	4	7	6	4	8	4	1	9	2	0
1500	0	4	7	6	4	7	5	2	8	3	0
1600	0	4	7	8	4	7	5	2	8	2	0
1700	0	2	6	6	4	6	5	2	7	4	0
1800	0	2	6	9	4	6	5	2	7	4	0
1840	0	2	6	9	5	6	5	2	7	3	0
1900	0	2	6	9	5	5	6	2	7	3	0
2000	0	2	5	7	5	6	3	0	6	3	0
2100	2	2	5	9	5	5	5	1	6	3	0
2140	2	2	5	9	4	5	5	1	6	3	0
2200	4	0	4	7	4	5	5	1	6	3	0
2300	4	0	4	7	4	5	5	1	6	3	0
2400	2	0	4	7	4	5	5	1	6	3	0
2500	2	0	4	7	4	5	5	1	6	3	0
2600	2	0	4	7	4	5	5	1	6	3	0
2700	2	0	4	7	4	5	5	1	6	3	0
2800	2	0	4	7	4	15	4	2	15	4	0
2900	2	0	4	7	4	15	4	2	15	4	0
3000	0	0	4	7	4	14	3	2	15	2	0

OUTLINE DIMENSIONS

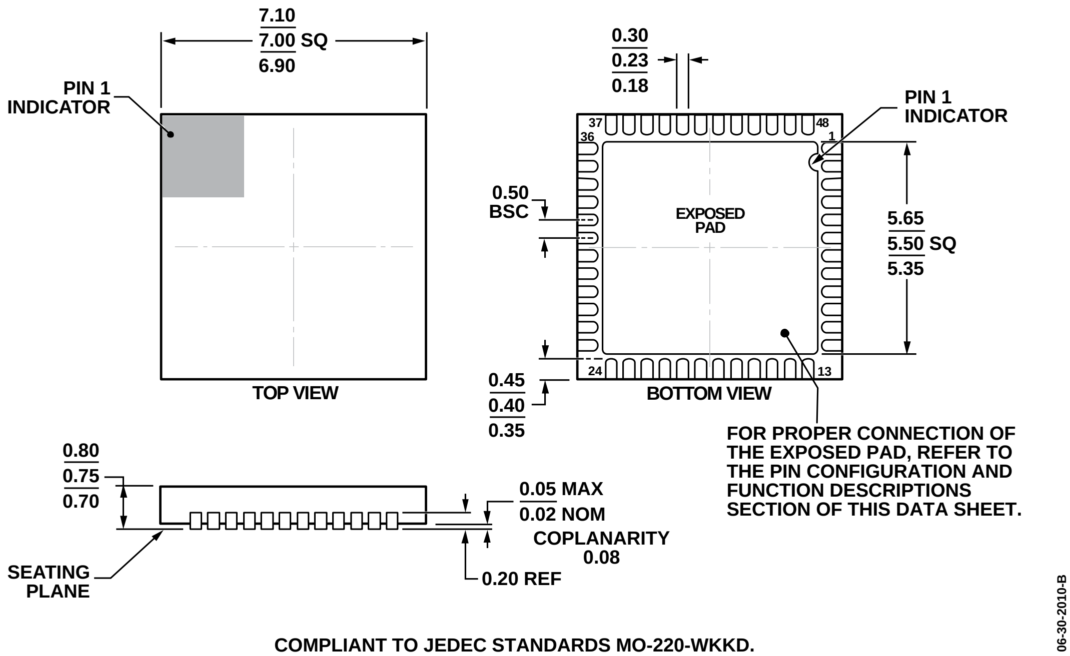

Figure 44.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option