DSP Microcomputer

ADSP-2186L

FEATURES

Performance

25 ns Instruction Cycle Time 40 MIPS Sustained Performance
Single-Cycle Instruction Execution
Single-Cycle Context Switch
3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
Multifunction Instructions
Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 400 Cycle Recovery from Power-Down Condition
Low Power Dissipation in Idle Mode

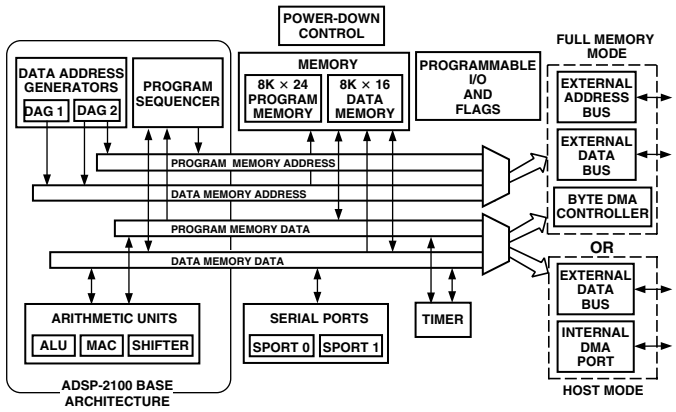
Integration

ADSP-2100 Family Code Compatible, with Instruction Set Extensions
40K Bytes of On-Chip RAM, Configured as 8K Words On-Chip Program Memory RAM and 8K Words On-Chip Data Memory RAM
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator and Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution
Programmable 16-Bit Interval Timer with Prescaler
100-Lead LQFP and 144-Ball Mini-BGA

System Interface

16-Bit Internal DMA Port for High Speed Access to On-Chip Memory (Mode Selectable)
4 MByte Byte Memory Interface for Storage of Data Tables and Program Overlays
8-Bit DMA to Byte Memory for Transparent Program and Data Memory Transfers (Mode Selectable)
I/O Memory Interface with 2048 Locations Supports Parallel Peripherals (Mode Selectable)
Programmable Memory Strobe and Separate I/O Memory Space Permits "Glueless" System Design (Mode Selectable)
Programmable Wait State Generation
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Internal DMA Port
Six External Interrupts

FUNCTIONAL BLOCK DIAGRAM



13 Programmable Flag Pins Provide Flexible System Signaling
UART Emulation through Software SPORT Reconfiguration
ICE-Port™ Emulator Interface Supports Debugging in Final Systems

GENERAL DESCRIPTION

The ADSP-2186L is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The ADSP-2186L combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities and on-chip program and data memory.

The ADSP-2186L integrates 40K bytes of on-chip memory configured as 8K words (24-bit) of program RAM and 8K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2186L is available in a 100-lead LQFP and 144-ball mini-BGA packages.

In addition, the ADSP-2186L supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers and global interrupt masking for increased flexibility.

Fabricated in a high speed, double metal, low power, CMOS process, the ADSP-2186L operates with a 25 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-21xx family DSPs contain a shadow bank register that is useful for single cycle context switching of the processor.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

Pin Terminations (Continued)

Pin Name	I/O 3-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2:0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15:13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL1}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL0}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQE}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	O		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	O		High or Low
DT1/FO	O	O		Float
EE	I	I		
$\overline{EBR}$	I	I		
$\overline{EBG}$	O	O		
$\overline{ERESET}$	I	I		
$\overline{EMS}$	O	O		
$\overline{EINT}$	I	I		
ECLK	I	I		
ELIN	I	I		
ELOUT	O	O		

NOTES
*Hi-Z = High Impedance.
1. If the CLKOUT pin is not used, turn it OFF, using CLKODIS in Sport0 autobuffer control register.
2. If the Interrupt/Programmable Flag pins are not used, there are two options:
   Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive).
   Option 2: Program the unused pins as OUTPUTS, set them to 1, and let them float.
3. All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, $\overline{RESET}$, and PF3:0 are not included in the table because these pins must be used.

Setting Memory Mode

Memory Mode selection for the ADSP-2186L is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are passive and active.

Passive configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 100 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Active configuration involves the use of a three-stateable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{RESET}$ signal such that it only drives the PF2 pin when $\overline{RESET}$ is active (low). After $\overline{RESET}$ is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output.

To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level and not oscillate should the three-state driver's level hover around the logic switching point.

Interrupts

The interrupt controller allows the processor to respond to the thirteen possible interrupts (eleven of which can be enabled at any one time), and $\overline{RESET}$ with minimum overhead. The ADSP-2186L provides four dedicated external interrupt input pins, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$ and $\overline{IRQE}$ (shared with the PF7:4 pins). In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FI and FO, for a total of six external interrupts. The ADSP-2186L also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and $\overline{RESET}$). The $\overline{IRQ2}$, $\overline{IRQ0}$ and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and IRQE is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
$\overline{RESET}$ (or Power-Up with PUCR = 1)	0000 (Highest Priority)
Power-Down (Nonmaskable)	002C
$\overline{IRQ2}$	0004
$\overline{IRQL1}$	0008
$\overline{IRQL0}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{IRQE}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{IRQ1}$	0020
SPORT1 Receive or $\overline{IRQ0}$	0024
Timer	0028 (Lowest Priority)

Interrupt routines can either be nested, with higher priority interrupts taking precedence, or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2186L masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ pins are external level-sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts.

On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop and subroutine nesting.

The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;

DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The ADSP-2186L has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-2186L processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 400 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 400 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 400 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge (PWDACK) pin indicates when the processor has entered power-down.

Idle

When the ADSP-2186L is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on the ADSP-2186L to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction. The format of the instruction is:

IDLE (n)

where n = 16, 32, 64 or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals such as SCLK, CLKOUT and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-2186L will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64 or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-2186L, two serial devices, a byte-wide EPROM and optional external program and data overlay memories (mode selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSP-2186L also provides four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Additional system peripherals can be added in this mode through the use of external hardware to generate and latch address signals.

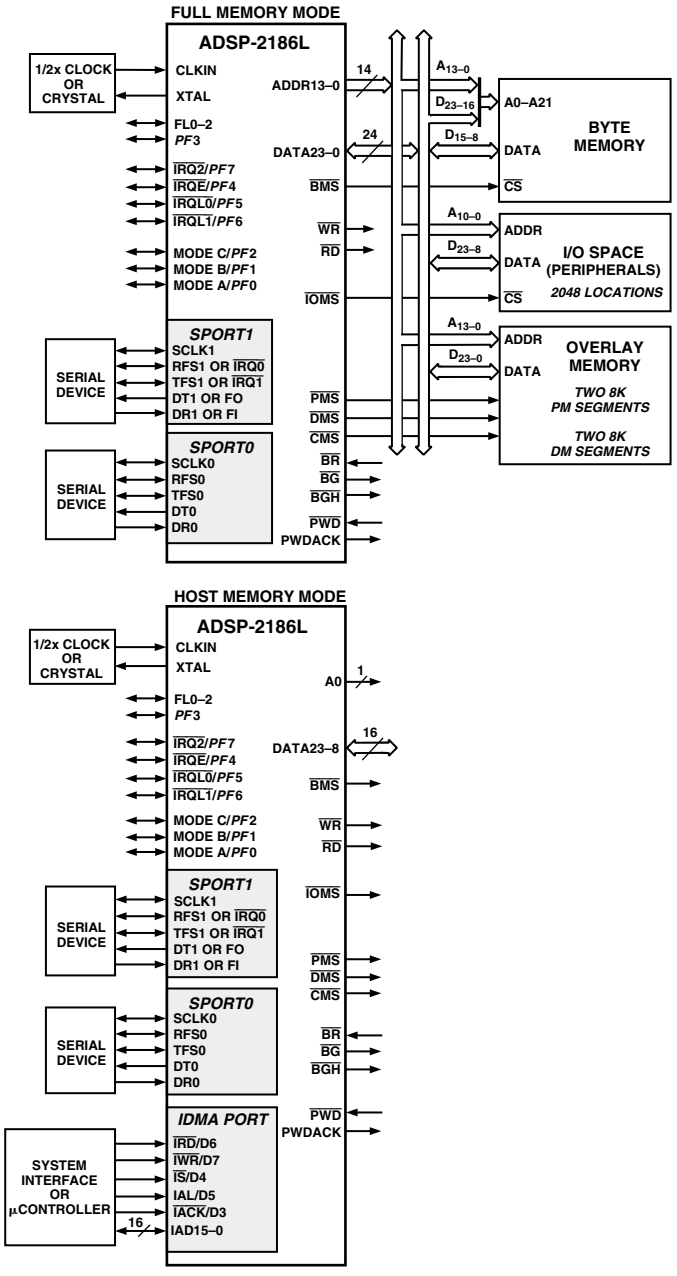


Figure 2. Basic System Configuration

Clock Signals

The ADSP-2186L can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information on the power-down feature, refer to the *ADSP-218x DSP Hardware Reference.*

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

The ADSP-2186L uses an input clock with a frequency equal to half the instruction rate; a 0.20 MHz input clock yields a 25 ns processor cycle (which is equivalent to 40 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2186L includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

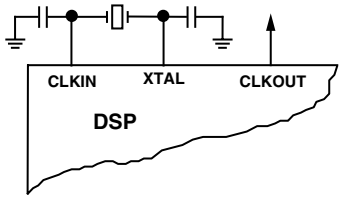


Figure 3. External Crystal Connections

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2186L. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulsewidth specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, an external Schmidt trigger is recommended.

ADSP-2186L Mini-BGA (CA) Package Pinout
Bottom View

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	VDD	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	VDD	$\overline{\text{PWD}}$	A7/IAD6	A5/IAD4	$\overline{\text{RD}}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{\text{BGH}}$	NC	$\overline{\text{WR}}$	NC	D
D10	GND	VDD	GND	GND	PF3	FL2	PF0 [MODE A]	FL0	A8/IAD7	VDD	VDD	E
D9	NC	D8	D11	D7/$\overline{\text{IWR}}$	NC	NC	FL1	A11/ IAD10	A12/ IAD11	NC	A13/ IAD12	F
D4/$\overline{\text{IS}}$	NC	NC	D5/IAL	D6/$\overline{\text{IRD}}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{\text{IACK}}$	D2/IAD15	TFS0	DT0	VDD	GND	GND	GND	CLKIN	H
VDD	VDD	D1/IAD14	$\overline{\text{BG}}$	RFS1/ $\overline{\text{IRQ0}}$	D0/IAD13	SCLK0	VDD	VDD	NC	VDD	CLKOUT	J
$\overline{\text{EBG}}$	$\overline{\text{BR}}$	$\overline{\text{EBR}}$	$\overline{\text{ERESET}}$	SCLK1	TFS1/ $\overline{\text{IRQ1}}$	RFS0	$\overline{\text{DMS}}$	$\overline{\text{BMS}}$	NC	NC	NC	K
$\overline{\text{EINT}}$	ELOUT	ELIN	$\overline{\text{RESET}}$	GND	DR0	$\overline{\text{PMS}}$	GND	$\overline{\text{IOMS}}$	$\overline{\text{IRQL1}}$ +PF6	NC	$\overline{\text{IRQE}}$ +PF4	L
ECLK	EE	$\overline{\text{EMS}}$	NC	GND	DR1/ FI	DT1/ FO	GND	$\overline{\text{CMS}}$	NC	$\overline{\text{IRQ2}}$ +PF7	$\overline{\text{IRQL0}}$ +PF5	M

The ADSP-2186L Mini-BGA package pinout is shown in the table below. Pin names in **bold** text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$.

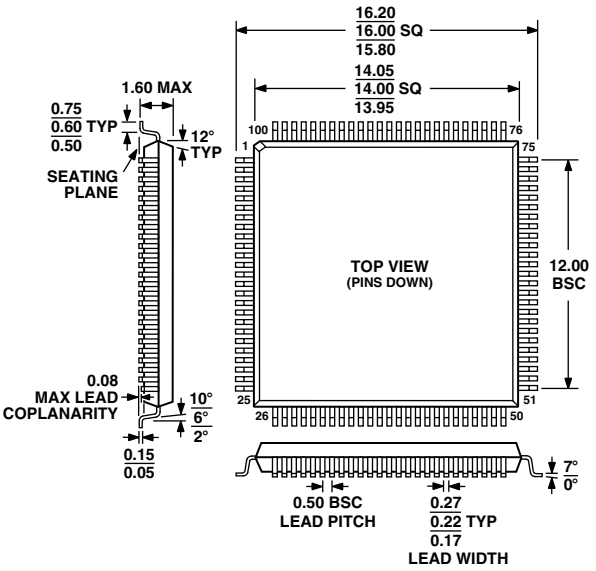
Mini-BGA Package Pinout

Ball #	Name	Ball #	Name	Ball #	Name	Ball #	Name
A01	A2/**IAD1**	D01	N/C	G01	XTAL	K01	N/C
A02	A1/**IAD0**	D02	$\overline{\text{WR}}$	G02	N/C	K02	N/C
A03	GND	D03	N/C	G03	GND	K03	N/C
A04	A0	D04	$\overline{\text{BGH}}$	G04	A10/**IAD9**	K04	$\overline{\text{BMS}}$
A05	N/C	D05	A9/**IAD8**	G05	N/C	K05	$\overline{\text{DMS}}$
A06	GND	D06	PF1[MODE B]	G06	N/C	K06	RFS0
A07	N/C	D07	PF2[MODE C]	G07	N/C	K07	TFS1/$\overline{\text{IRQ1}}$
A08	N/C	D08	N/C	G08	D6/$\overline{\textbf{IRD}}$	K08	SCLK1
A09	N/C	D09	D13	G09	D5/**IAL**	K09	$\overline{\text{ERESET}}$
A10	D22	D10	D12	G10	N/C	K10	$\overline{\text{EBR}}$
A11	GND	D11	N/C	G11	N/C	K11	$\overline{\text{BR}}$
A12	GND	D12	GND	G12	D4/$\overline{\textbf{IS}}$	K12	$\overline{\text{EBG}}$
B01	A4/**IAD3**	E01	VDD	H01	CLKIN	L01	$\overline{\text{IRQE}}$+PF4
B02	A3/**IAD2**	E02	VDD	H02	GND	L02	N/C
B03	GND	E03	A8/**IAD7**	H03	GND	L03	$\overline{\text{IRQL1}}$+PF6
B04	N/C	E04	FL0	H04	GND	L04	$\overline{\text{IOMS}}$
B05	N/C	E05	PF0[MODE A]	H05	VDD	L05	GND
B06	GND	E06	FL2	H06	DT0	L06	$\overline{\text{PMS}}$
B07	VDD	E07	PF3	H07	TFS0	L07	DR0
B08	D23	E08	GND	H08	D2/**IAD15**	L08	GND
B09	D20	E09	GND	H09	D3/$\overline{\textbf{IACK}}$	L09	$\overline{\text{RESET}}$
B10	D18	E10	VDD	H10	GND	L10	ELIN
B11	D17	E11	GND	H11	N/C	L11	ELOUT
B12	D16	E12	D10	H12	GND	L12	$\overline{\text{EINT}}$
C01	PWDACK	F01	A13/**IAD12**	J01	CLKOUT	M01	$\overline{\text{IRQL0}}$+PF5
C02	A6/**IAD5**	F02	N/C	J02	VDD	M02	$\overline{\text{IRQ2}}$+PF7
C03	$\overline{\text{RD}}$	F03	A12/**IAD11**	J03	N/C	M03	N/C
C04	A5/**IAD4**	F04	A11/**IAD10**	J04	VDD	M04	$\overline{\text{CMS}}$
C05	A7/**IAD6**	F05	FL1	J05	VDD	M05	GND
C06	$\overline{\text{PWD}}$	F06	N/C	J06	SCLK0	M06	DT1/FO
C07	VDD	F07	N/C	J07	D0/**IAD13**	M07	DR1/FI
C08	D21	F08	D7/$\overline{\textbf{IWR}}$	J08	RFS1/$\overline{\text{IRQ0}}$	M08	GND
C09	D19	F09	D11	J09	$\overline{\text{BG}}$	M09	N/C
C10	D15	F10	D8	J10	D1/**IAD14**	M10	$\overline{\text{EMS}}$
C11	N/C	F11	N/C	J11	VDD	M11	EE
C12	D14	F12	D9	J12	VDD	M12	ECLK

OUTLINE DIMENSIONS

Dimensions shown in millimeters.

100-Lead Metric Thin Plastic Quad Flatpack (LQFP)
(ST-100)

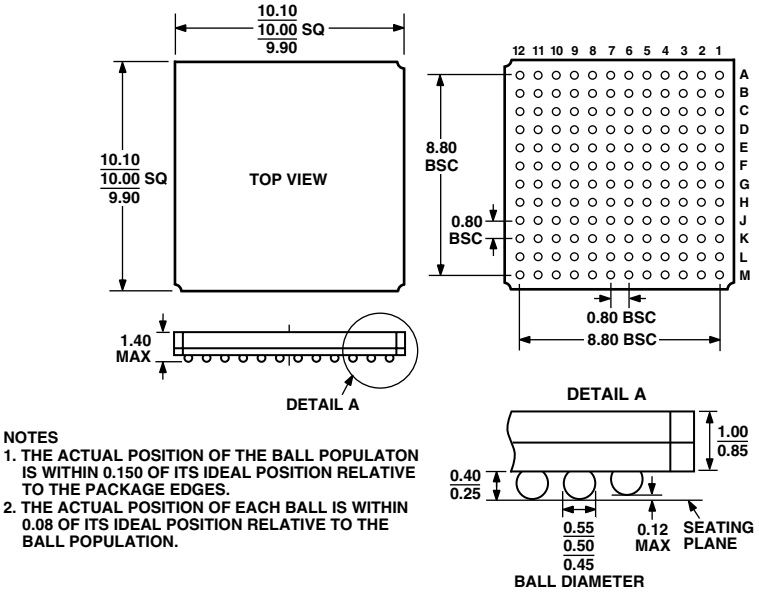


NOTE
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.

OUTLINE DIMENSIONS

Dimensions shown in millimeters.

144-Ball Metric Mini-BGA (CA-144)



NOTES
1. THE ACTUAL POSITION OF THE BALL POPULATON IS WITHIN 0.150 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.08 OF ITS IDEAL POSITION RELATIVE TO THE BALL POPULATION.

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option*
ADSP-2186LKST-115	0°C to +70°C	28.8	100-Lead LQFP	ST-100
ADSP-2186LBST-115	–40°C to +85°C	28.8	100-Lead LQFP	ST-100
ADSP-2186LKST-133	0°C to +70°C	33.3	100-Lead LQFP	ST-100
ADSP-2186LBST-133	–40°C to +85°C	33.3	100-Lead LQFP	ST-100
ADSP-2186LKST-160	0°C to +70°C	40.0	100-Lead LQFP	ST-100
ADSP-2186LBST-160	–40°C to +85°C	40.0	100-Lead LQFP	ST-100
ADSP-2186LBCA-160	–40°C to +85°C	40.0	144-Ball Mini-BGA	CA-144

*ST = Plastic Thin Quad Flatpack (LQFP); CA = Mini-BGA.