Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management

Preliminary Technical Data

ADuCM4050

FEATURES

EEMBC ULPMark™-CP Score (3 V): 203
Ultra low power active and hibernate modes
- **Active <40 µA/MHz (typical)**
- **Flexi <100 µA (typical)**
- **Hibernate <680 nA (typical)**
- **Shutdown <50 nA (typical)**
- **Shutdown (Fast wake-up) <200 nA (typical)**

ARM Cortex-M4F processor at 52 MHz with FPU, MPU, ITM with SWD interface
Power management
- **Single-supply operation (VBAT): 1.74 V to 3.6 V**
- **Optional buck converter for improved efficiency**

Memory options
- **512 KB of embedded flash memory with ECC**
- **4 KB of cache memory to reduce active power**
- **128 KB of configurable system SRAM with parity**

Safety
- **Watchdog with dedicated on-chip oscillator**
- **Hardware CRC with programmable polynomial**
- **Multiparity bit protected SRAM**
- **ECC protected embedded flash**

Security
- **Hardware cryptographic accelerator supporting AES-128, AES-256, and SHA-256**
- **Protected key storage in flash, SHA-256 based keyed HMAC and key wrap and unwrap**
- **User code protection**
- **TRNG**

DIGITAL PERIPHERALS

3 SPI interfaces to enable glueless interface to sensors, radios, and converters
1 I^2C and 2 UART peripheral interfaces
SPORT for natively interfacing with converters and radios
Programmable GPIOs (44 in LFCSP and 51 in WLCSP)
3 general-purpose timers with PWM support
RGB timer for driving RGB LED
RTC and FLEX_RTC with SensorStrobe and time stamping
Programmable beeper
27-channel DMA controller

CLOCKING FEATURES

26 MHz clock: on-chip oscillator, external crystal oscillator, SYS_CLKIN for external clock, and integrated PLL
32 kHz clock: on-chip oscillator and low power crystal oscillator
Clock fail detection for external crystals

ANALOG PERIPHERALS

12-bit SAR ADC, 1.8 MSPS, 8 channels, and digital comparator

APPLICATIONS

Internet of Things (IoT)
- **Smart agriculture, smart building, smart metering, smart city, smart machine, and sensor network**

Wearables
- **Fitness and clinical**
- **Machine learning and neural networks**

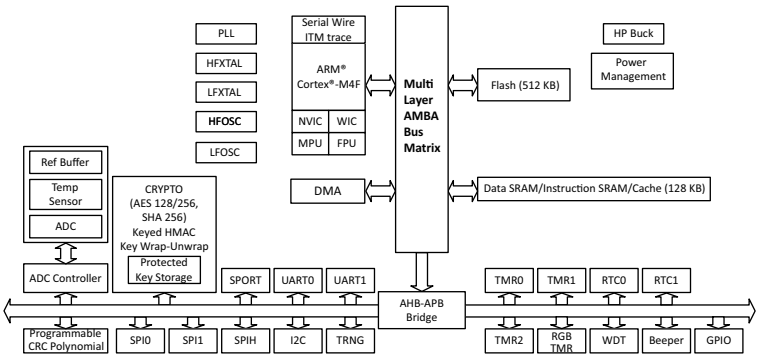

Figure 1. Functional Block Diagram

Rev. PrE **Document Feedback**

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GENERAL DESCRIPTION

The ADuCM4050 microcontroller unit (MCU) is an ultra low power integrated microcontroller system with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM® Cortex®-M4F processor. The MCU also has a collection of digital peripherals, embedded SRAM and flash memory, and an analog subsystem which provides clocking, reset, and power management capability in addition to an analog-to-digital converter (ADC) subsystem.

The system features include the following:

- Up to 52 MHz ARM Cortex-M4F processor
- 512 KB of embedded flash memory with error correction code (ECC)
- Optional 4 KB cache for lower active power
- 128 KB system SRAM with parity
- Power management unit (PMU)
- Multilayer advanced microcontroller bus architecture (AMBA) bus matrix
- Central direct memory access (DMA) controller
- Beeper interface
- Cryptographic hardware supporting advanced encryption standard (AES) -128, AES-256 along with various modes (electronic code book (ECB), cipher block chaining (CBC), counter (CTR), cipher block chaining-message authentication code (CCM/CCM*) modes) and secure hash algorithm (SHA)-256

  Protected key storage with key wrap-unwrap

  Keyed hashed message authentication code (HMAC) with key unwrap
- Serial port (SPORT), serial peripheral interface (SPI), inter integrated (I^2C), and universal asynchronous receiver/transmitter (UART) peripheral interfaces
- Real-time clock (RTC)
- General-purpose and watchdog timers
- Programmable general-purpose input/output (GPIO) pins
- Hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial
- Power on reset (POR) and power supply monitor (PSM)
- 12-bit successive approximation register (SAR) ADC
- RGB timer for driving RGB LED
- True random number generator (TRNG)

To support low dynamic and hibernate power management, the ADuCM4050 MCU provides a collection of power modes and features such as dynamic- and software-controlled clock gating and power gating.

For full details on the ADuCM4050 MCU, refer to the *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference.*

HIGHLIGHTS

The following are the key features of the ADuCM4050 MCU:

- Industry leading ultralow power consumption.
- Robust operation.
  - Full voltage monitoring in deep sleep modes.
  - ECC support on flash.
  - Parity error detection on SRAM memory.
  - Leading edge security.
  - Fast encryption provides read protection to customer algorithms.
  - Write protection prevents device reprogramming by unauthorized code.
- Failure detection of 32 kHz LFXTAL via interrupt.
- SensorStrobe™ for precise time synchronized sampling of external sensors.
  - Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the ADXL363 accelerometer.
  - Software intervention is not required after setup.
  - No pulse drift due to software execution.

ARM CORTEX-M4F PROCESSOR

The ARM Cortex-M4F core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 bits or 32 bits.

The processor has the following features:

- Cortex-M4F architecture
  - Thumb-2 instruction set architecture (ISA) technology
  - Three-stage pipeline with branch speculation
  - Low latency interrupt processing with tail chaining
  - Single-cycle multiply
  - Hardware divide instructions
  - Nested vectored interrupt controller (NVIC) (72 interrupts and 8 priorities)
  - Six hardware breakpoints and one watchpoint (unlimited software breakpoints using Segger JLink)
  - Bit banding support
  - Trace support—instruction trace macrocell (ITM), trace port interface unit (TPIU), and data watchpoint and trace (DWT) triggers and counters

- Memory protection unit (MPU)
  - Eight-region MPU with subregions and background region
  - Programmable clock generator unit
- Configurable for ultralow power operation
  - Deep sleep modes, dynamic power management
  - Programmable clock generator unit
- Floating point unit (FPU)
  - Supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations
  - Provides conversions between fixed point and floating point data formats, and floating point constant instructions

ARM Cortex-M4F Subsystem

The memory map of the ADuCM4050 MCU is based on the ARM Cortex-M4F model. By retaining the standardized memory mapping, it is easier to port applications across Cortex-M4F platforms. The ADuCM4050 application development is based on memory blocks across code/SRAM regions. Sufficient internal memory is available via internal SRAM and internal flash.

Code Region

Accesses in this region (0x0000_0000 to 0x0007_FFFF, except 0x0007_F000 to 0x0007_FFFF that is meant for protected key storage) are performed by the core and target the memory and cache resources.

SRAM Region

Accesses in this region (0x1000_0000 to 0x2005_7FFF) are performed by the ARM Cortex-M4F core. The SRAM region of the core can otherwise act as a data region for an application.

- **Internal SRAM Data Region.** This space can contain read/write data. Internal SRAM can be partitioned between code and data (SRAM region in M4F space) in 32 KB blocks. Access to this region occurs at core clock speed with no wait states. It also supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system devices.
- **System MMRs.** Various system memory mapped registers (MMRs) reside in this region.

System Region

Accesses in this region (0xE000 0000 to 0xFFFF FFFF) are performed by the ARM Cortex-M4F core, and are handled within the Cortex-M4F platform.

- **CoreSight™ ROM**. The read only memory (ROM) table entries point to the debug components of the processor.
- **ARM APB Peripheral**. This space is defined by ARM and occupies the bottom 256 KB of the system (SYS) region (0xE000 0000 to 0xE004 0000). The space supports read/write access by the M4F core to the internal peripherals of the ARM core (NVIC, system control space (SCS), wake-up interrupt controller (WIC)) and CoreSight ROM. It is not accessible by system DMA.
- **Platform Control Register**. This space has registers within the Cortex-M4F platform component that control the ARM core, its memory, and the code cache. It is accessible by the Cortex-M4F core (but not accessible by system DMA).

MEMORY ARCHITECTURE

The internal memory of the ADuCM4050 MCU is shown in Figure 2. It incorporates 512 KB of embedded flash memory for program code and nonvolatile data storage, 96 KB of data SRAM, and 32 KB of SRAM (configured as instruction space or data space).

SRAM Region

This memory space contains the application instructions and literal (constant) data which must be accessed in real-time. It supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system peripherals. Byte, half-word and word accesses are supported.

SRAM is divided into 96 KB data SRAM and 32 KB instruction SRAM. If instruction SRAM is not enabled, then the associated 32 KB can be mapped as data SRAM, resulting in 128 KB of data SRAM.

When the cache controller is enabled, 4 KB of the instruction SRAM is reserved as cache memory.

Parity bit error detection (optional) is available on all SRAM memories. Multiple parity bits are associated with each 32-bit word.

In hibernate mode, up to 124 KB of SRAM can be retained in the following ways:

- 124 KB of data SRAM.
- 96 KB of data SRAM and 28 KB of instruction SRAM.

MMRs (Peripheral Control and Status)

For the address space containing MMRs, refer to Figure 2. These registers provide control and status for on-chip peripherals of the ADuCM4050 MCU.

For more information about the MMRs, refer to the *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference*.

Flash Memory

The ADuCM4050 MCU includes 512 KB of embedded flash memory, which is accessed using a flash controller. The flash controller is coupled with a cache controller. A prefetch mechanism is implemented in the flash controller to optimize code performance.

Flash writes are supported by a key hole mechanism via advanced peripheral bus (APB) writes to MMRs. The flash controller provides support for DMA based key hole writes.

With respect to flash integrity, the device supports the following:

- A fixed user key required for running protected commands, including mass erase and page erase.
- An optional and user definable user failure analysis key (FAA key). Analog Devices personnel need this key while performing failure analysis.
- An optional and user definable write protection for user-accessible memory.
- An optional 8-bit ECC. It is enabled by default. It is recommended not to disable ECC.

Cache Controller

The ADuCM4050 MCU has an optional 4 KB instruction cache. In certain applications, enabling the cache and executing the code can result in lower power consumption rather than operating directly from flash. When enabling the cache controller, 4 KB of instruction SRAM is reserved as cache memory. In hibernate mode, the cache memory is not retained.

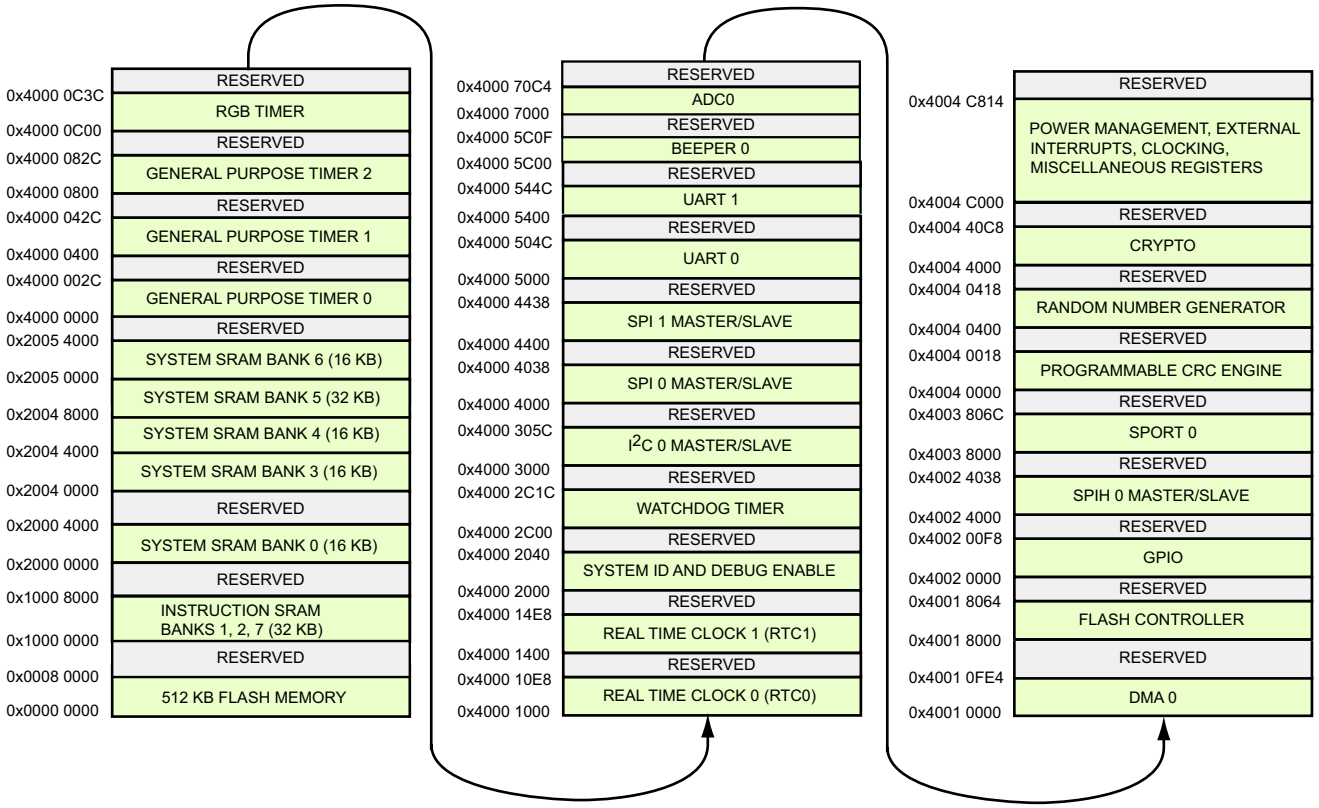


Figure 2. ADuCM4050 Memory Map—SRAM Mode 0

SYSTEM AND INTEGRATION FEATURES

The ADuCM4050 MCU provides several features that ease system integration.

Reset

There are four kinds of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the ARM Cortex-M4F core.

The $\overline{\text{SYS\_HWRST}}$ pin is toggled to perform a hardware reset.

Booting

The ADuCM4050 MCU supports two boot modes: booting from internal flash and upgrading software through UART download. If the GPIO17 pin (SYS_BMODE0) is pulled low during power-up or a hard reset, the MCU enters into serial download mode. In this mode, an on-chip loader routine is initiated in the kernel, which configures the UART port and communicates with the host to manage the firmware upgrade via a specific serial download protocol.

Table 1. Boot Modes

Boot Mode	Description
0	UART download mode.
1	Flash boot. Boot from integrated flash memory.

Power Management

The ADuCM4050 MCU has an integrated power management system that optimizes performance and extend battery life of the device.

The power management system consists of the following:

- Integrated 1.2 V low dropout regulator (LDO) and optional capacitive buck regulator
- Integrated power switches for low standby current in hibernate and shutdown modes

Additional power management features include the following:

- Customized clock gating for active modes
- Power gating to reduce leakage in hibernate/shutdown modes
- Flexible sleep modes
- Shutdown mode with no retention
- Optional high efficiency buck converter to reduce power
- Integrated low power oscillators

Power Modes

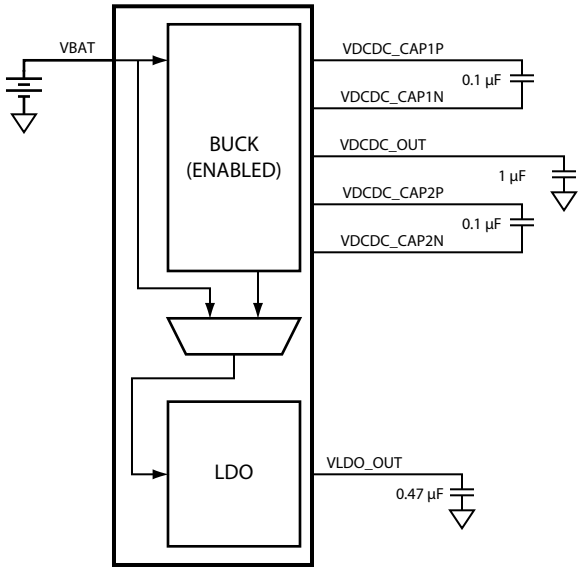
The PMU provides control of the ADuCM4050 MCU power modes and allows the ARM Cortex-M4F to control the clocks and power gating to reduce the power consumption. Several power modes are available. Each mode provides an additional low power benefit with a corresponding reduction in functionality.

- Active mode. All peripherals can be enabled. Active power is managed by optimized clock management. See Table 3 for details on active mode current consumption.
- Flexi™ mode. The ARM Cortex-M4F core is clock gated, but the remainder of the system is active. No instructions can be executed in this mode, but DMA transfers can continue between peripherals as well as memory to memory. See Table 4 for details on Flexi mode current consumption.
- Hibernate mode. This mode provides state retention, configurable SRAM and port pin retention, a limited number of wake-up interrupts (SYS_WAKEn, UART0_RX, and optionally, two RTCs—RTC0 and RTC1 (FLEX_RTC).
- Shutdown mode. This mode is the deepest sleep mode, in which all the digital and analog circuits are powered down with an option to wake from four possible wake-up sources. The RTC0 can be (optionally) enabled in this mode, and the device can be periodically woken up by the RTC0 interrupt. Wake-up time is approximately 76 ms.
- Shutdown mode—fast wake-up. This mode has a faster wake-up time than shutdown mode at the expense of higher power consumption. Wake-up time <1.5 ms.

  See Table 5 for deep sleep (hibernate, shutdown, and fast shutdown) modes specifications.

The following features are available for power management and control:

- Voltage range of 1.74 V to 3.6 V using a single supply (such as the CR2032 coin cell battery).
- GPIOs are driven directly from the battery. The pin state is retained in hibernate and shutdown modes. The GPIO configuration is only retained in hibernate mode.
- Wake-up from external interrupts (via GPIOs), UART0_RX interrupt, and RTCs for hibernate mode.
- Wake-up from external interrupts (via GPIOs) and RTC0 for shutdown mode.
- Optional high power buck converter for 1.2 V full on support (MCU use only). See Figure 3 for suggested external circuitry.



Note: For designs in which the optional buck is not used, the following pins must be left unconnected—VDCDC_CAP1P, VDCDC_CAP1N, VDCDC_OUT, VDCDC_CAP2P, and VDCDC_CAP2N.

Figure 3. Buck Enabled Design

Security Features

The ADuCM4050 MCU provides a combination of hardware and software protection mechanisms that lock out access to the device in secure mode, but grant access in open mode. These mechanisms include password protected slave boot modes (UART), as well as password protected serial wire debug (SWD) interfaces.

Mechanisms are provided to protect the device contents (flash, SRAM, CPU registers, and peripheral registers) from being read through an external interface by an unauthorized user. This is referred to as read protection.

It is possible to protect the device from being reprogrammed in circuit with unauthorized code. This is referred to as in circuit write protection.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

The device can be configured with no protection, read protection, or read and in circuit write protection. It is not necessary to provide in circuit write protection without read protection.

Cryptographic Accelerator

The cryptographic accelerator is a 32-bit APB DMA capable peripheral. There are two 128-bit buffers provided for data input/output operations. These buffers read in or read out 128 bits in four data accesses. Big endian and little endian data formats are supported, as are the following modes:

- ECB mode—AES mode
- CTR mode
- CBC mode
- Message authentication code (MAC) mode
- CCM/CCM* mode
- SHA-256 modes
- Protected key storage with key wrap and unwrap—HMAC signature generation

True Random Number Generator (TRNG)

The TRNG is used during operations where nondeterministic values are required. This can include generating challenges for secure communication or keys used for an encrypted communication channel. The generator can run multiple times to generate a sufficient number of bits for the strength of the intended operation. The true random number generator can seed a deterministic random bit generator.

Reliability and Robustness Features

The ADuCM4050 MCU provides several features that can enhance or help achieve certain levels of system safety and reliability. While the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness:

- ECC enabled flash memory. The entire flash array can be protected to either correct single-bit errors or detect two-bit errors per 64-bit flash data (enabled by default).
- Multiparity bit protected SRAM. Each word of the SRAM and cache memory is protected by multiple parity bits to allow detection of random soft errors.
- Software watchdog. The on-chip watchdog timer can provide software-based supervision of the ADuCM4050 core.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator computes the CRC for a block of memory locations. The exact memory location can be in the SRAM, flash, or any combination of MMRs. The CRC accelerator generates a checksum that can be compared with an expected signature.

The main features of the CRC include the following:

- Generates a CRC signature for a block of data.
- Supports programmable polynomial length of up to 32 bits.
- Operates on 32 bits of data at a time, and generates CRC for any data length.

- Supports MSB first and LSB first CRC implementations.
- Various data mirroring capabilities.
- Initial seed to be programmed by user.
- DMA controller (memory to memory transfer) used for data transfer to offload the MCU.

Programmable GPIOs

The ADuCM4050 MCU has 44 and 51 GPIO pins in the LFCSP and WLCSP packages, respectively, with multiple, configurable functions defined by user code. They can be configured as input/output pins and have programmable pull-up resistors. All GPIO pins are functional over the full supply range.

In deep sleep modes, GPIO pins retain their state. On reset, they tristate.

Timers

The ADuCM4050 MCU contains three general-purpose timers, a watchdog timer, and an RGB timer.

All timers support event capture feature, where they can take 40 different interrupts.

General-Purpose Timers

The ADuCM4050 MCU has three identical general-purpose timers, each with a 16-bit up/down counter. The up/down counter can be clocked from one of four user-selectable clock sources. Any selected clock source can be scaled down using a prescaler of 1, 16, 64, or 256.

Watchdog Timer (WDT)

The WDT is a 16-bit count down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, or 256. The WDT is clocked by the 32 kHz on-chip oscillator (LFOSC) and used to recover from an illegal software state. The WDT requires periodic servicing to prevent it from forcing a reset or interrupt to the MCU.

RGB Timer

The ADuCM4050 MCU has an RGB timer that supports a common anode RGB LED. It has a timer counter and three compare registers. It can generate three distinct PWM waveforms on three ports/pins simultaneously so that different colors can be realized on the common anode RGB LED.

When RGB timer is in operation, the other three timers are available for user software.

Analog-to-Digital Converter (ADC) Subsystem

The ADuCM4050 MCU integrates a 12-bit SAR ADC with up to eight external channels. Conversions can be performed in single or autocycle mode. In single mode, the ADC can be configured to convert on a particular channel by selecting one of the channels. Autocycle mode is provided to convert over multiple channels with reduced MCU overhead of sampling and reading individual channel registers. The ADC can also be used for temperature sensing and measuring battery voltage using dedicated channels.

Temperature sensing and battery monitoring cannot be included in autocycle mode.

A digital comparator allows an interrupt to be triggered if ADC input is above or below a programmable threshold. Use the ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 pins with the digital comparator.

Use the ADC in DMA mode to reduce MCU overhead by moving ADC results directly into SRAM with a single interrupt asserted when the required number of ADC conversions has been completely logged to memory.

The main features of the ADC subsystem include the following:

- 12-bit resolution.
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS.
- Integrated input mux that supports up to eight channels.
- Temperature sensing support.
- Battery monitoring support.
- Software selectable on-chip reference voltage generation—1.25 V and 2.5 V.
- Software-selectable internal or external reference.
- Autocycle mode—ability to automatically select a sequence of input channels for conversion.
- Multiple conversions over a single channel or multiple channels can be performed without core interruption.
- Averaging function—converted data on single or multiple channels can be averaged up to 256 samples.
- Alert function—internal digital comparator for the ADC_VIN0, ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold. In addition, up to eight cycles of hysteresis are built in.
- Dedicated DMA channel support.
- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result.

Clocking

The ADuCM4050 MCU has the following clocking options:

- High frequency clocks
  - Internal oscillator—HFOSC (26 MHz)
  - External crystal oscillator—HFXTAL (26 MHz or 16 MHz)
  - GPIO clock in—SYS_CLKIN
  - Phase-locked loop (PLL)
- Low frequency clocks (32 kHz)
  - Internal oscillator—LFOSC
  - External crystal oscillator—LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled when using an internal buck regulator.
- LFOSC cannot be disabled even if using LFXTAL.

Clock sources with a frequency greater than 26 MHz can be achieved by using a PLL. The maximum frequency sourced from the PLL is 52 MHz.

When core frequency is greater than 26 MHz, flash wait states must be programmed to 1.

As PLL is disabled and relock is transparent to user software, hibernate mode can enter and exit seamlessly when the system frequency is sourced from PLL.

Clock Fail Detection

The LFOSC clock continuously monitors LFXTAL in hibernate, active, and Flexi power modes. If LFXTAL stops running, there is an option to detect and generate an interrupt and/or automatically switch to LFOSC without software intervention.

The HFOSC clock monitors HFXTAL, GPIO clock, and the PLL clock. If any of these clocks are used as the system clock, and fail to toggle, it can be detected through an interrupt. There is an option to automatically switch to HFOSC.

Real-Time Clock (RTC)

The ADuCM4050 MCU has two RTC blocks—RTC0 and RTC1 (FLEX_RTC). The clock blocks share a low power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

The FLEX_RTC supports four SensorStrobe outputs. Using this mechanism, the ADuCM4050 MCU can be used as a programmable clock generator in all power modes, except shutdown mode. In this way, the external sensors can have their timing domains mastered by the ADuCM4050 MCU, as the SensorStrobe output is a programmable divider from the FLEX_RTC, which can operate up to a resolution of 30.7 µs. The sensors and MCU are in sync, which removes the need for additional resampling of data to time align it.

In the absence of this mechanism,

- The external sensor uses an RC oscillator (~±30% typical variation). The MCU must sample the data and resample it on the time domain of the MCU before using it.

Or

- The MCU remains in a higher power state and drives each data conversion on the sensor side.

This mechanism allows the ADuCM4050 MCU to be in a lower power state for a long duration and avoids unnecessary data processing, extending the battery life of the end product. The key differences between RTC0 and RTC1 are shown in Table 2.

Table 2. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of Time Base (Prescaling)	Counts time at 1 Hz in units of seconds. Operationally, always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds.	Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16,384, or 32,768.
Source Clock	LFXTAL.	Depending on the low frequency multiplexer (LFMUX) configuration, the RTC is clocked by the LFXTAL or the LFOSC.
Wake-Up Timer	Wake-up time is specified in units of seconds.	Supports alarm times down to a resolution of 30.7 µs, that is, where the time is specified down to a specific 32 kHz clock cycle.
Number of Alarms	One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
SensorStrobe Mechanism	Not available.	Four independent channels with fine control on duty cycle and frequency (0.5 Hz to 16 kHz). SensorStrobe is an alarm function in the RTC that sends an output pulse via GPIOs to an external device to instruct that device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, Flexi, and hibernate modes.
Input Capture	Not available.	Input capture takes a snapshot of the RTC real-time count when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM4050 MCU. Typically, an input capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM4050 MCU that the RTC must take a snapshot of time corresponding to the event. Taking this snapshot can wake up the ADuCM4050 MCU and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred.
Input Sampling	Not available.	Each SensorStrobe channel has up to three separate GPIO inputs from an external device, which can be sampled based on the output pulse sent to the external device. Each channel can be configured to interrupt the ADuCM4050 MCU when any activity happens on these GPIO inputs from the external device. These inputs can broadcast sensor states such as FIFO full, switch open, and threshold crossed. This feature allows the ADuCM4050 MCU to remain in a low power state and wakeup to process the data only when a specific programmed sequence from an external device is detected.

Beeper Driver

The ADuCM4050 MCU has an integrated audio driver for a beeper.

The beeper driver module in the ADuCM4050 MCU generates a differential square wave of programmable frequency. It drives an external piezoelectric sound component with two terminals that connect to the differential square wave output.

The beeper driver consists of a module that can deliver frequencies ranging from 8 kHz to ~0.25 kHz. It operates on a fixed independent 32 kHz clock source that is unaffected by changes in system clocks.

It allows programmable tone durations from 4 ms to 1.02 sec in 4 ms increments. Pulse (single-tone) and sequence (multitone) modes provide versatile playback options.

In sequence mode, the beeper can be programmed to play any number of tone pairs from 1 to 254 (2 to 508 tones) or be programmed to play forever (until stopped by the user). Interrupts are available to indicate the start or end of any beep, the end of a sequence, or when the sequence is nearing completion.

Debug Capability

The ADuCM4050 MCU supports a 2-wire SWD interface and trace feature via a single-wire viewer port.

ON-CHIP PERIPHERAL FEATURES

The ADuCM4050 MCU contains a rich set of peripherals connected to the core via several concurrent high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1).

The ADuCM4050 MCU contains high speed serial ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the MCU and system to many application scenarios.

Serial Ports (SPORT)

The ADuCM4050 MCU provides two single direction half SPORTs or one bidirectional full SPORT. The synchronous serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices audio codecs, ADCs, and DACs. The serial ports contain two data lines, a clock, and a frame sync. The data lines can be programmed to either transmit or receive, and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory or external memory via dedicated DMA channels. The frame sync and clock can be shared. Some of the ADCs/DACs require two control signals for their conversion process. To interface with such devices, SPT0_ACNV and SPT0_BCNV signals are provided. To use these signals, enable the timer enable mode. In this mode, a PWM timer inside the module generates the programmable SPT0_ACNV and SPT0_BCNV signals.

Serial ports operate in two modes:

- Standard digital signal processor (DSP) serial mode
- Timer enable mode

Serial Peripheral Interface (SPI) Ports

The ADuCM4050 MCU provides three SPIs. SPI is an industry standard, full-duplex, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received. Each SPI incorporates two DMA channels that interface with the DMA controller. One DMA channel transmits and the other receives. The SPI on the MCU eases interfacing to external serial flash devices.

The SPI features include the following:

- Serial clock phase mode and serial clock polarity mode
- Loopback mode
- Continuous transfer mode
- Wired OR output mode
- Read command mode for half-duplex operation (transmit followed by receive)
- Flow control support
- Multiple $\overline{CS}$ line support
- $\overline{CS}$ software override support
- Support for 3-pin SPI

UART Ports

The ADuCM4050 MCU provides two full-duplex UART ports that are fully compatible with PC standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. The UART port includes support for five to eight data bits, and none, even, or odd parity. A frame is terminated by one, one and a half, or two stop bits.

I^2C

The ADuCM4050 MCU provides an I^2C bus peripheral that has two pins for data transfer. SCL is a serial clock pin and SDA is a serial data pin. The pins are configured in a wired AND format that allows arbitration in a multimaster system. A master device can be configured to generate the serial clock. The frequency is programmed by the user in the serial clock divisor register. The master channel can operate in fast mode (400 kHz) or standard mode (100 kHz).

DEVELOPMENT SUPPORT

Development support for the ADuCM4050 MCU includes documentation, evaluation hardware, and development software tools.

Documentation

The *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference* details the functionality of each block on the ADuCM4050 MCU. It includes power management, clocking, memories, and peripherals.

Hardware

The ADZS-U4050LF-EZKIT® (for 64-lead LFCSP) and ADZS-U4050WL-EZKIT® (for 72-ball WLCSP) are available to prototype sensor configuration with the ADuCM4050 MCU.

Software

The ADZS-U4050LF-EZKIT and ADZS-U4050WL-EZKIT include a complete development and debug environment for the ADuCM4050 MCU. The board support package (BSP) for the ADuCM4050 MCU is provided for the IAR Embedded Workbench for ARM, Keil™, and CrossCore® embedded studio (CCES) environments.

The BSP also includes operating system (OS) aware drivers and example code for all the peripherals on the device.

ADDITIONAL INFORMATION

The following documentation that describe the ADuCM4050 MCU can be ordered from any Analog Devices sales office or accessed electronically on the Analog Devices website:

- *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference*
- *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Anomaly List*

This data sheet describes the ARM Cortex-M4F core and memory architecture used on the ADuCM4050 MCU. It does not provide detailed programming information about the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M4F processor include the following:

- *ARM Cortex-M4F Devices Generic User Guide*
- *ARM Cortex-M4F Technical Reference Manual*

REFERENCE DESIGNS

The Circuits from the Lab® web page provides the following for the ADuCM4050 reference design:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Condition	Min	Typ	Max	Unit
V_{BAT}[1, 2]	External Battery Supply Voltage		1.74	3.0	3.6	V
V_{IH}	High Level Input Voltage	V_{BAT} = 3.6 V	2.5			V
V_{IL}	Low Level Input Voltage	V_{BAT} = 1.74 V			0.45	V
V_{BAT_ADC}	ADC Supply Voltage		1.74	3.0	3.6	V
T_J	Junction Temperature	$T_{AMBIENT}$ = −40°C to +85°C	−40		+85	°C

[1] Must remain powered (even if the associated function is not used).
[2] Value applies to VBAT_ANA1,VBAT_ANA2,VBAT_DIG1, and VBAT_DIG2 pins.

ELECTRICAL CHARACTERISTICS

Parameter		Condition	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	V_{BAT} = minimum V, I_{OH} = −1.0 mA	1.4			V
V_{OL}[1]	Low Level Output Voltage	V_{BAT} = minimum V, I_{OL} = 1.0 mA			0.4	V
I_{IHPU}[2]	High Level Input Current Pull-Up	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}		0.01	1	µA
I_{ILPU}[2]	Low Level Input Current Pull-Up	V_{BAT} = maximum V, V_{IN} = 0 V			100	µA
I_{OZH}[3]	Three-State Leakage Current	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}		0.01	1	µA
I_{OZL}[3]	Three-State Leakage Current	V_{BAT} = maximum V, V_{IN} = 0 V		0.01	1	µA
I_{OZLPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = maximum V, V_{IN} = 0 V			100	µA
I_{OZHPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}			1	µA
I_{OZLPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = maximum V, V_{IN} = 0 V			1	µA
I_{OZHPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}			100	µA
C_{IN}	Input Capacitance	T_J = 25°C		10		pF

[1] Applies to the output and bidirectional pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_01, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P0_06, P0_07, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, P2_12, P2_13, P2_14, P2_15, P0_09, P3_00, P3_01, P3_02, and P3_03.
[2] Applies to the input pin with pull-up: $\overline{\text{SYS\_HWRST}}$.
[3] Applies to the three-state pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, P0_09, P2_12, P2_13, P2_14, P2_15, P0_09, P3_00, P3_01, P3_02, and P3_03.
[4] Applies to the three-state pins with pull-ups: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, P0_09, P0_07, P1_01, P2_12, P2_13, P2_14, P2_15, P0_09, P3_00, P3_01, P3_02, and P3_03.
[5] Applies to the three-state pin with pull-down: P0_06.

Power Supply Current

Table 3. Active Mode—Current Consumption When V_{BAT} = 3.0 V

Conditions[1]	Buck	Typ[2]	Max[3]	Unit
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[4]	Disabled	3.38	4.78	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[4]	Disabled	3.65	5.04	mA
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[4]	Enabled	1.83	2.71	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[4]	Enabled	1.97	2.84	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[4]	Disabled	2.34	5.82	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[4]	Disabled	2.60	6.09	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[4]	Enabled	1.27	3.28	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[4]	Enabled	1.40	3.41	mA
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz[5]	Disabled	5.61	6.90	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz[5]	Disabled	6.14	7.42	mA
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz[5]	Enabled	2.94	3.78	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz[5]	Enabled	3.21	4.04	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz[5]	Disabled	4.46	8.05	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz[5]	Disabled	4.98	8.58	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz[5]	Enabled	2.33	4.39	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz[5]	Enabled	2.59	4.65	mA
Code executing from SRAM, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[4]	Disabled	2.66	5.10	mA
Code executing from SRAM, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[4]	Disabled	2.92	5.36	mA
Code executing from SRAM, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[4]	Enabled	1.43	2.87	mA
Code executing from SRAM, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[4]	Enabled	1.56	3.00	mA
Code executing from SRAM, peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz[5]	Disabled	5.08	7.52	mA
Code executing from SRAM, peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz[5]	Disabled	5.60	8.04	mA
Code executing from SRAM, peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz[5]	Enabled	2.64	4.09	mA
Code executing from SRAM, peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz[5]	Enabled	2.90	4.35	mA

[1] The code being executed is a prime number generation in a continuous loop, with HFOSC as the system clock source.
[2] Junction temperature (T_J) = 25°C.
[3] Junction temperature (T_J) = 85°C.
[4] Zero wait states and low HP Buck load.
[5] One wait state and high HP Buck load.

Table 4. Flexi™ Mode—Current Consumption When V_{BAT} = 3.0 V

Conditions	Buck	Typ[1]	Max[2]	Unit
Peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz	Disabled	0.62	3.06	mA
Peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz	Disabled	0.88	3.32	mA
Peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz	Enabled	0.40	1.85	mA
Peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz	Enabled	0.54	1.98	mA
Peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz	Disabled	1.04	3.48	mA
Peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz	Disabled	1.57	4.01	mA
Peripheral clocks off, PCLK = 52 MHz, HCLK = 52 MHz	Enabled	0.62	2.06	mA
Peripheral clocks on, PCLK = 52 MHz, HCLK = 52 MHz	Enabled	0.88	2.33	mA

[1] Junction temperature (T_J) = 25°C.
[2] Junction temperature (T_J) = 85°C.

Table 5. Deep Sleep Modes[1]—Current Consumption

Mode	Conditions	V_{BAT} = 1.8 V Typ[2]	V_{BAT} = 3.0 V Typ[2]	V_{BAT} = 3.6 V Typ[2]	V_{BAT} = 1.8 V Typ[3]	V_{BAT} = 3.0 V Typ[3]	V_{BAT} = 3.6 V Typ[3]	Unit
HIBERNATE	RTC1 and RTC0 disabled, 16 KB SRAM retained, LFXTAL off	0.88	0.69	0.68	3.35	2.46	2.35	µA
	RTC1 and RTC0 disabled, 28 KB SRAM retained, LFXTAL off	1.0	0.77	0.75	4.23	2.94	2.83	µA
	RTC1 and RTC0 disabled, 48 KB SRAM retained, LFXTAL off	1.08	0.83	0.80	5.84	3.82	3.49	µA
	RTC1 and RTC0 disabled, 60 KB SRAM retained, LFXTAL off	1.19	0.90	0.86	6.80	4.48	3.98	µA
	RTC1 and RTC0 disabled, 80 KB SRAM retained, LFXTAL off	1.47	1.10	1.05	7.75	5.12	4.77	µA
	RTC1 and RTC0 disabled, 92 KB SRAM retained, LFXTAL off	1.55	1.15	1.10	8.57	5.55	5.21	µA
	RTC1 and RTC0 disabled, 112 KB SRAM retained, LFXTAL off	1.62	1.21	1.15	10.11	6.82	5.84	µA
	RTC1 and RTC0 disabled, 124 KB SRAM retained, LFXTAL off	1.72	1.26	1.20	11.22	7.31	6.67	µA
	RTC1 enabled, 16 KB SRAM retained, LFOSC as source for RTC1	0.95	0.74	0.71	3.43	2.52	2.41	µA
	RTC1 enabled, 124 KB SRAM retained, LFOSC as source for RTC1	1.78	1.32	1.25	11.32	7.39	6.74	µA
SHUTDOWN	RTC0 disabled	0.03	0.05	0.07	0.32	0.43	0.55	µA
FAST SHUTDOWN	RTC0 disabled	0.18	0.20	0.22	0.48	0.60	0.72	µA

[1] Buck enable/disable selection does not affect power consumption.
[2] Junction temperature (T_J) = 25°C.
[3] Junction temperature (T_J) = 85°C.

Table 6. Wake-Up Time

Mode	VTOR	Root Clock	HCLK/PCLK (MHZ)	Wake-up Time	Unit
FLEXI	Flash	HFOSC	26	1.605	µs
HIBERNATE	Flash	HFOSC	26	10.356	µs
	SRAM	HFOSC	26	4.984	µs
	Flash	HFXTAL	26	686.452	µs
	Flash	PLL_HFOSC	26	14.487	µs
	Flash	PLL_HFXTAL	26	742.668	µs
	Flash	PLL_HFOSC	52	15.730	µs
	Flash	PLL_HFXTAL	52	726.101	µs
SHUTDOWN	Flash	HFOSC	26	68.144	ms
FAST SHUTDOWN	Flash	HFOSC	26	1.220	ms

SYSTEM CLOCKS/TIMERS SPECIFICATIONS

Table 7 and Table 8 show the system clock specifications for the ADuCM4050 MCU.

Platform External Crystal Oscillator

Table 7. Platform External Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL)					
$C_{EXT1} = C_{EXT2}$	6		10	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for $C_L \leq 5$ pF (maximum) and ESR = 30 kΩ (maximum). C_{EXT1}, C_{EXT2} must be selected considering the printed circuit board (PCB) trace capacitance due to routing.
Frequency		32,768		Hz	
HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL)					
$C_{EXT1} = C_{EXT2}$			20	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for C_L = 10 pF (maximum) and ESR = 50 Ω (maximum). C_{EXT1}, C_{EXT2} must be selected considering the PCB trace capacitance due to routing.
Frequency		26		MHz	

On-Chip RC Oscillator

Table 8. On-Chip RC Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
HIGH FREQUENCY RC OSCILLATOR (HFOSC)					
Frequency	25.03	26	27.04	MHz	
LOW FREQUENCY RC OSCILLATOR (LFOSC)					
Frequency	30,800	32,768	35,062	Hz	

ADC SPECIFICATIONS

Parameter[1, 2]	VBAT/VREF (V)	Package	Typ[3]	Unit	Conditions
NO MISSING CODE	1.8/1.25 (internal/external)	64-lead LFCSP	12	Bits	F_{in} = 1068 Hz, F_s = 100 KSPS, internal reference in low power mode, 400,000 samples end point method used
	1.8/1.25 (internal/external)	72-ball WLCSP	12	Bits	
	3.0/2.5 (internal/external)	64-lead LFCSP	12	Bits	
INTEGRAL NONLINEARITY ERROR	1.8/1.25 (internal/external)	64-lead LFCSP	±1.6	LSB	
	1.8/1.25 (internal/external)	72-ball WLCSP	±1.4	LSB	
	3.0/2.5 (internal/external)	64-lead LFCSP	−1.7, +1.3	LSB	
DIFFERENTIAL NONLINEARITY ERROR	1.8/1.25 (internal/external)	64-lead LFCSP	−0.7, +1.15	LSB	
	1.8/1.25 (internal/external)	72-ball WLCSP	−0.75, +1.0	LSB	
	3.0/2.5 (internal/external)	64-lead LFCSP	−0.7, +1.1	LSB	
OFFSET ERROR	1.8/1.25 (external)	64-lead LFCSP	±0.5	LSB	
	1.8/1.25 (external)	72-ball WLCSP	±0.5	LSB	
	3.0/2.5 (external)	64-lead LFCSP	±0.5	LSB	
GAIN ERROR	1.8/1.25 (external)	64-lead LFCSP	±2.5	LSB	
	1.8/1.25 (external)	72-ball WLCSP	±3.0	LSB	
	3.0/2.5 (external)	64-lead LFCSP	±0.5	LSB	
I_{VBAT_ADC}[4]	1.8/1.25 (internal)	64-lead LFCSP	129	µA	F_{in} = 1068 Hz, F_s = 100 KSPS, internal reference in low power mode
	1.8/1.25 (internal)	72-ball WLCSP	124	µA	
	3.0/2.5 (internal)	64-lead LFCSP	157	µA	

[1] The ADC is characterized in standalone mode without core activity and minimal or no switching on the adjacent ADC channels and digital inputs/outputs.
[2] The specifications are characterized after performing internal ADC offset calibration.
[3] T_J = 25°C.
[4] Current consumption from VBAT_ADC supply when ADC is performing the conversion.

FLASH SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Conditions
FLASH					
Endurance	10,000			Cycles	
Data Retention		10		Years	

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 9 may cause permanent damage to the product. This is a stress rating only. The functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Absolute Maximum Ratings

Parameter	Rating	Unit
SUPPLY		
VBAT_ANA1	−0.3 to +3.6	V
VBAT_ANA2		
VBAT_ADC		
VBAT_DIG1		
VBAT_DIG2		
VREF_ADC		
ANALOG		
VDCDC_CAP1N	−0.3 to +3.6	V
VDCDC_CAP1P		
VDCDC_OUT		
VDCDC_CAP2N		
VDCDC_CAP2P		
VLDO_OUT	−0.3 to +1.32	V
SYS_HFXTAL_IN		
SYS_HFXTAL_OUT		
SYS_LFXTAL_IN		
SYS_LFXTAL_OUT		
DIGITAL INPUT/OUTPUT		
P0.X	−0.3 to +3.6	V
P1.X		
P2.X		
P3.X		
$\overline{\text{SYS\_HWRST}}$		

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

Figure 4 and Table 10 provide details about package branding. For a complete listing of product availability, see the Future (Planned) Products section.

Figure 4. Product Information on Package[1]

[1] Exact brand can differ depending on package type.

Table 10. Package Brand Information

Brand Key	Field Description
ADuCM4050	Product model
t	Temperature range
pp	Package type
Z	RoHS compliant designation
cc	See Future (Planned) Products section
vvvvvv.x	Assembly lot code
n.n	Silicon revision
yyww	Date code

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Reset Timing

Table 11 and Figure 5 describe reset operation.

Table 11. Reset Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{WRST}	$\overline{SYS\_HWRST}$ Asserted Pulse Width Low[1]	4		µs

[1] Applies after power-up sequence is complete.

Figure 5. Reset Timing

System Clock and PLL

Table 12 describes system clock and PLL specifications.

Table 12. System Clock and PLL

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CK}	PLL Input CLKIN Period[1]	38.5	62.5	ns
f_{PLL}	PLL Output Frequency[2, 3]	16	60	MHz
t_{PCLK}	System Peripheral Clock Period	38.5	154	ns
t_{HCLK}	Advanced High Performance Bus (AHB) Subsystem Clock Period	38.5	154	ns

[1] The input to the PLL can come from either the high frequency external crystal or from the high frequency internal RC oscillator.

[2] For the minimum value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 16, PLL_DIV2 = 1 for PLL input clock = 26 MHz; and PLL_MSEL = 13, PLL_NSEL = 26, PLL_DIV2 = 1 for PLL input clock = 16 MHz.

[3] For the maximum value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 30, PLL_DIV2 = 0 for PLL input clock = 26 MHz; and PLL_MSEL = 8, PLL_NSEL = 30, PLL_DIV2 = 0 for 16 MHz.

Serial Ports

To determine whether communication is possible between two devices at a particular clock speed, confirm the following specifications:

- Frame sync delay, frame sync setup, and hold
- Data delay, data setup, and hold
- Serial clock (SPT_CLK) width

In Figure 6, the rising edge or falling edge of SPT_CLK (external or internal) can be used as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$.

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency is set by the following equation:

$$f_{SPTCLKPROG} = \frac{f_{PCLK}}{2 \times (CLKDIV + 1)}$$

where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535.

Table 13. Serial Ports—External Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	5		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	8		ns
t_{SCLKW}	SPT_CLK Width[2]	38.5		ns
t_{SPTCLK}	SPT_CLK Period[2]	77		ns
SWITCHING CHARACTERISTICS				
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]		20	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		20	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	1		ns

[1] This specification is referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK.
[3] This specification is referenced to the drive edge.

Table 14. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	25		ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	0		ns
SWITCHING CHARACTERISTICS				
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]		20	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	-8		ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]		20	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	-7		ns
t_{SCLKIW}	SPT_CLK Width	$t_{PCLK} - 1.5$		ns
t_{SPTCLK}	SPT_CLK Period	$(2 \times t_{PLCK}) - 1$		ns

[1] This specification is referenced to the sample edge.
[2] This specification is referenced to the drive edge.

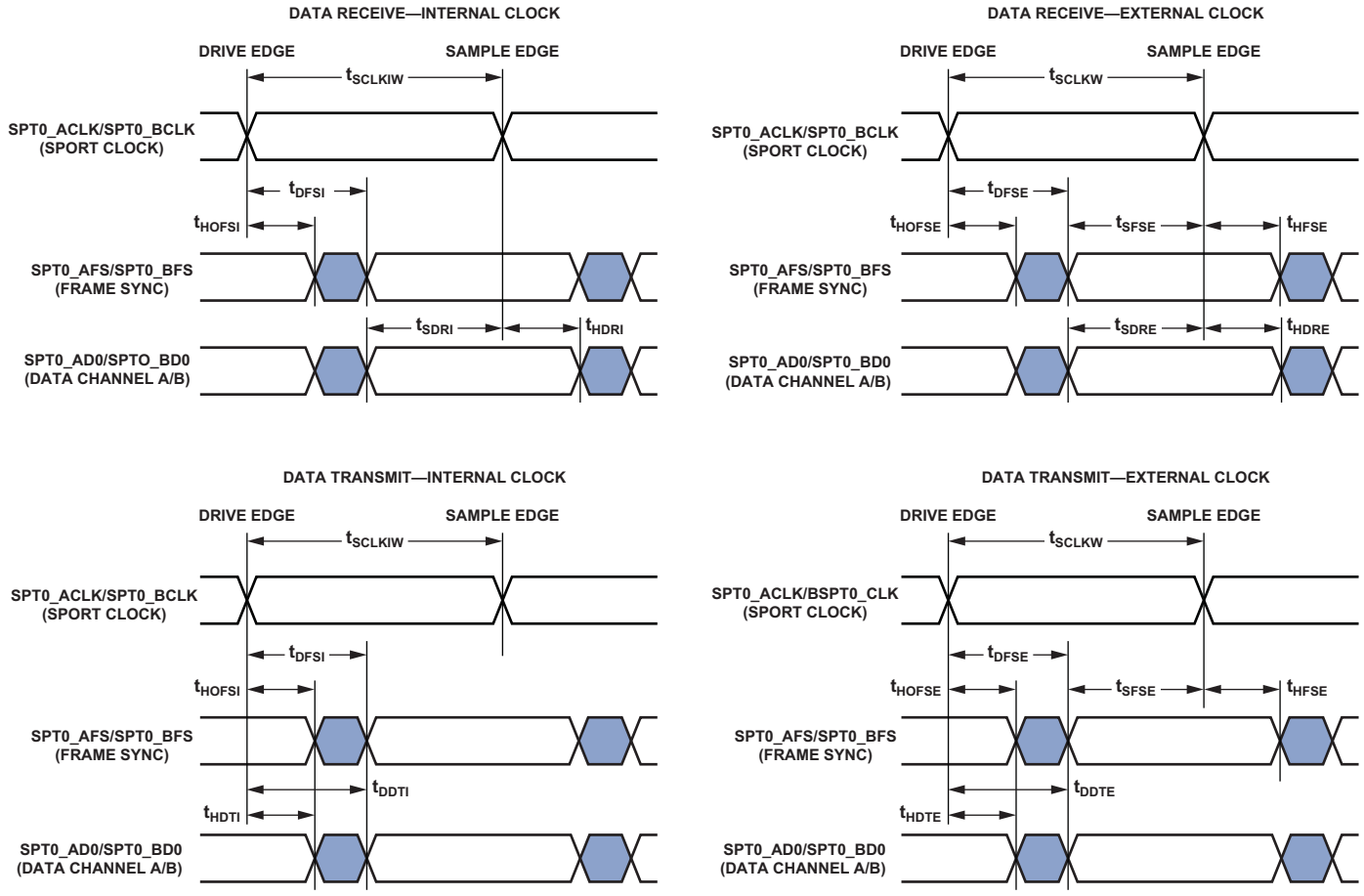


Figure 6. Serial Ports

Table 15. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	5		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		160	ns

[1] Referenced to the drive edge.

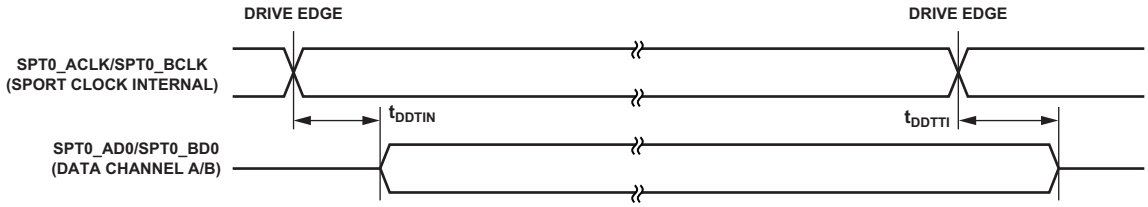


Figure 7. Serial Ports—Enable and Three-State

SPI Timing

Table 16. SPI Master Mode Timing[1]

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	$(2 \times t_{PCLK}) - 6.5$		ns
t_{SL}	SCLK Low Pulse Width	$t_{PCLK} - 3.5$		ns
t_{SH}	SCLK High Pulse Width	$t_{PCLK} - 3.5$		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	5		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	20		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge		25	ns
t_{DOSU}	Data Output Setup Before SCLK Edge	$t_{PCLK} - 2.2$		ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	$t_{PCLK} + 2$		ns

[1] This specification is characterized with respect to double drive strength.

Table 17. SPIH Master Mode Timing[1]

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	$(2 \times t_{PCLK}) - 6.5$		ns
t_{SL}	SCLK Low Pulse Width	$t_{PCLK} - 2$		ns
t_{SH}	SCLK High Pulse Width	$t_{PCLK} - 2$		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	3.5		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	12		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge		12.5	ns
t_{DOSU}	Data Output Setup Before SCLK Edge	$t_{PCLK} - 2.2$		ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	$t_{PCLK} + 2$		ns

[1] This specification is characterized with respect to double drive strength.

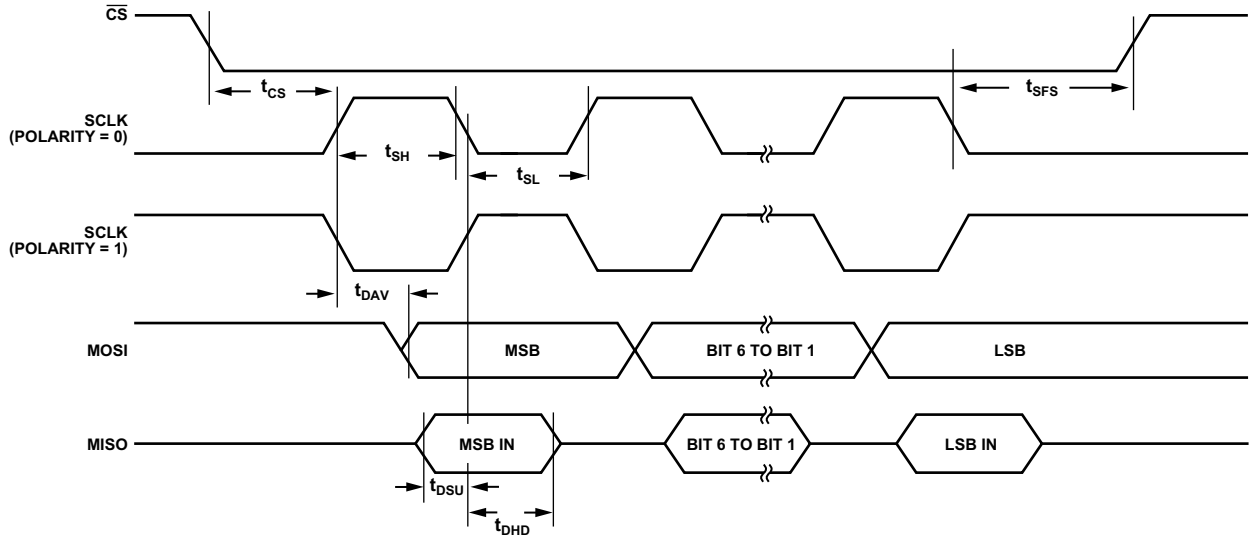


Figure 8. SPI Master Mode Timing (Phase Mode = 1)

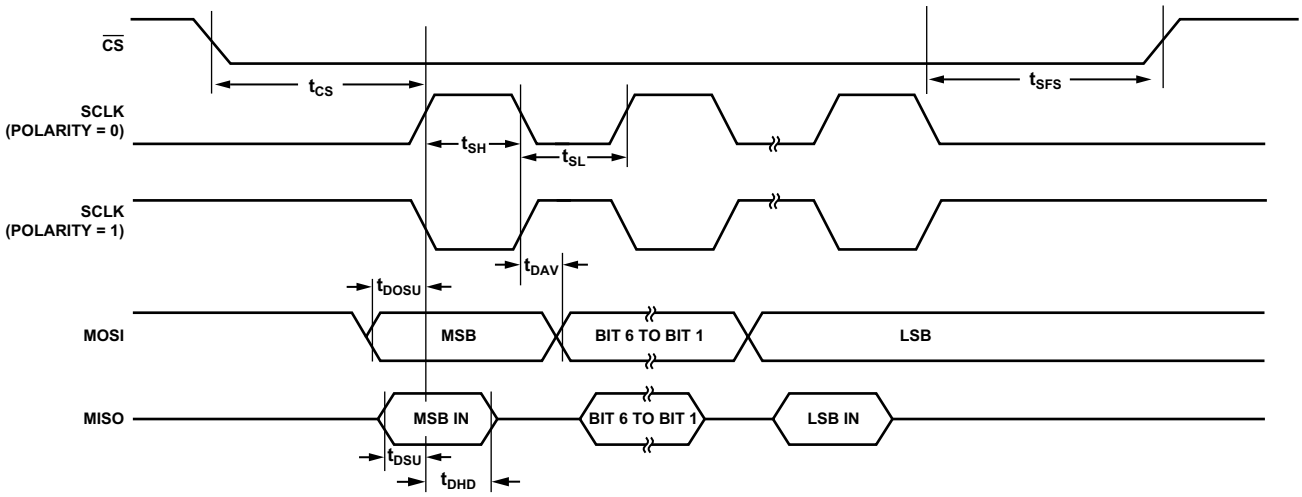


Figure 9. SPI Master Mode Timing (Phase Mode = 0)

Table 18. SPI Slave Mode Timing[1]

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	38.5		ns
t_{SL}	SCLK Low Pulse Width	38.5		ns
t_{SH}	SCLK High Pulse Width	38.5		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	6		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	8		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge		20	ns
t_{DOCS}	Data Output Valid After $\overline{CS}$ Edge		20	ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	38.5		ns

[1] This specification is characterized with respect to double drive strength.

Table 19. SPIH Slave Mode Timing[1]

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	19.23		ns
t_{SL}	SCLK Low Pulse Width	19.23		ns
t_{SH}	SCLK High Pulse Width	19.23		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	1		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	1		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge		15	ns
t_{DOCS}	Data Output Valid After $\overline{CS}$ Edge		15	ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	19.23		ns

[1] This specification is characterized with respect to double drive strength.

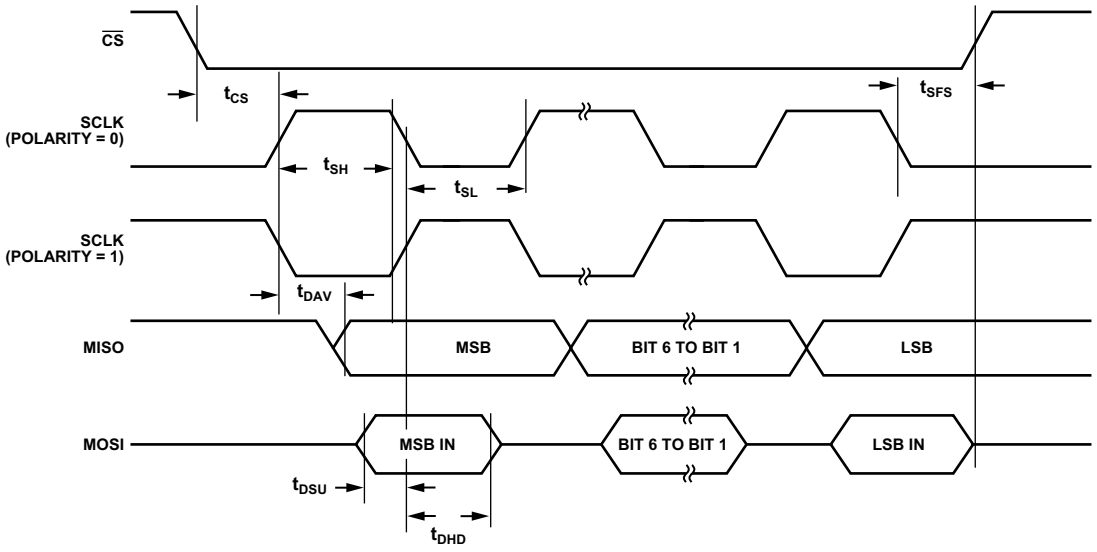


Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

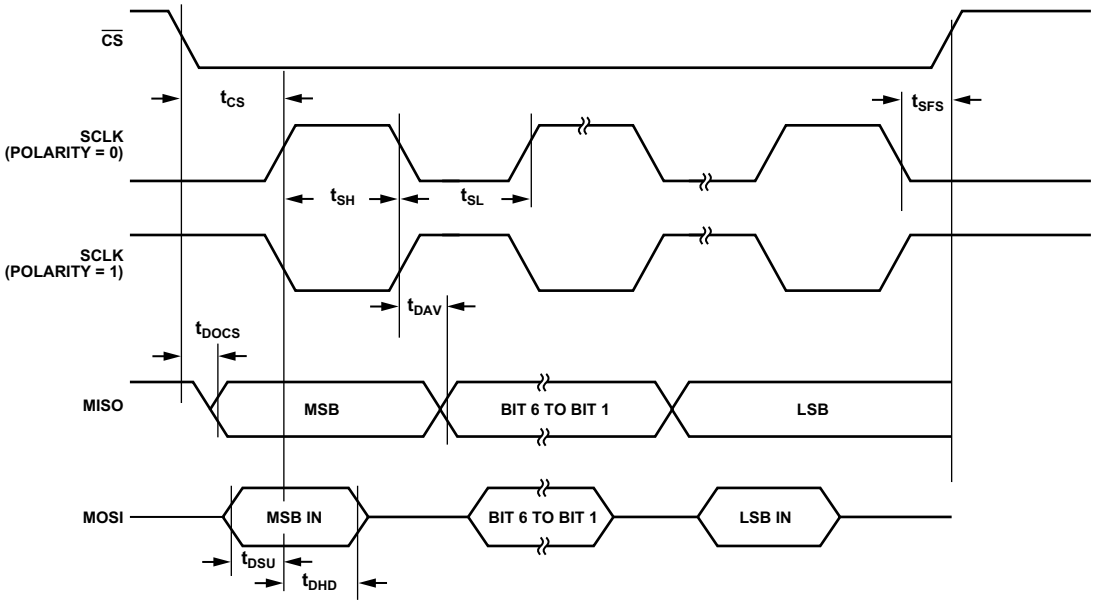


Figure 11. SPI Slave Mode Timing (Phase Mode = 0)

General-Purpose Port Timing

Table 20 and Figure 12 describe general-purpose port operations.

Table 20. General-Purpose Port Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$4 \times t_{PCLK}$		ns

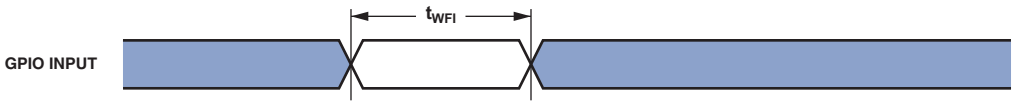


Figure 12. General-Purpose Port Timing

Timer PWM_OUT Cycle Timing

Table 21 and Figure 13 describe timer PWM_OUT cycle timing.

Table 21. Timer PWM_OUT Cycle Timing

Parameter		Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{PWMO}	Timer Pulse Width Output	$(4 \times t_{PCLK}) - 6$	$256 \times (2^{16} - 1)$	ns

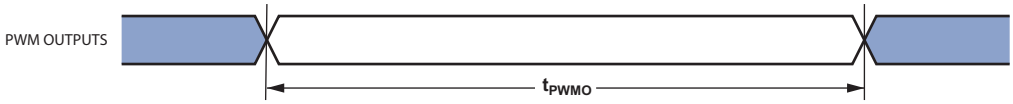


Figure 13. Timer PWM_OUT Cycle Timing

MCU TEST CONDITIONS

The ac signal specifications (timing parameters) appearing in this data sheet include output disable time, output enable time, and others. Timing is measured on signals when they cross the V_{MEAS} level as described in Figure 14. All delays (in nano seconds or micro seconds) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS}. The value of V_{MEAS} is set to $V_{BAT}/2$.

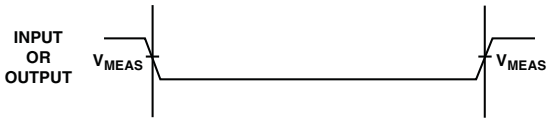
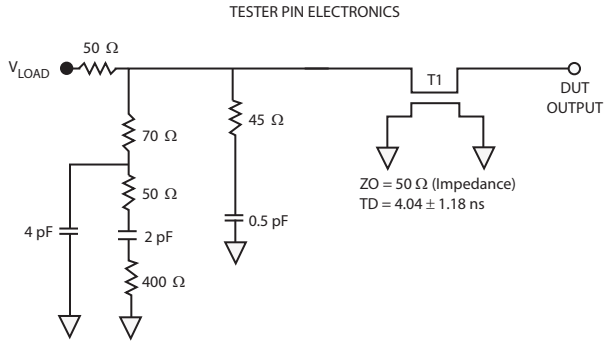


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 15. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

DRIVER TYPES

Table 22 shows driver types.

Table 22. Driver Types

Driver Type[1, 2, 3]	Associated Pins
Type A	P1_10, P0_10, P0_11,P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_01, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07,P1_08, P1_09, P0_07, P0_00, P0_01, P0_02, P0_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P2_11, P2_12, P2_13, P2_14, P3_00, P3_01, P3_02, P3_03, $\overline{\text{SYS\_HWRST}}$
Type B	P0_08, P0_09, P0_14, P1_11, P1_12, P1_13, P1_14, P2_02
Type C	P0_04, P0_05
Type D	P0_06

[1] In single drive mode, the maximum source/sink capacity is 2 mA.
[2] In double drive mode, the maximum source/sink capacity is 4 mA.
[3] At maximum drive capacity, only 16 GPIOs are allowed to switch at any given point of time.

Figure 16 through Figure 21 show the typical current voltage characteristics for the output drivers of the MCU.

The curves represent the current drive capability of the output drivers as a function of output voltage.

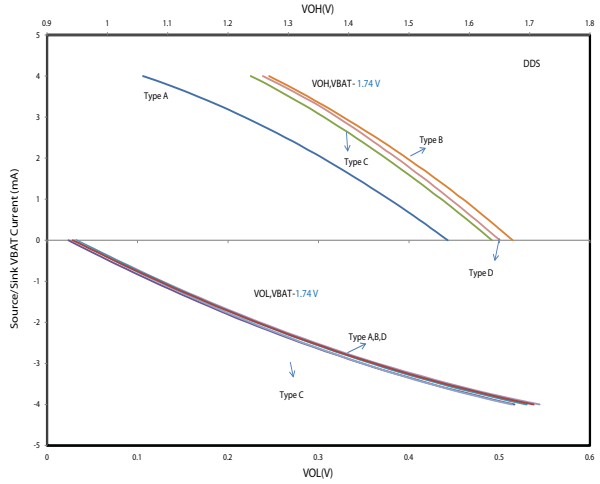


Figure 16. Output Double Drive Strength Characteristics (VBAT = 1.74 V)

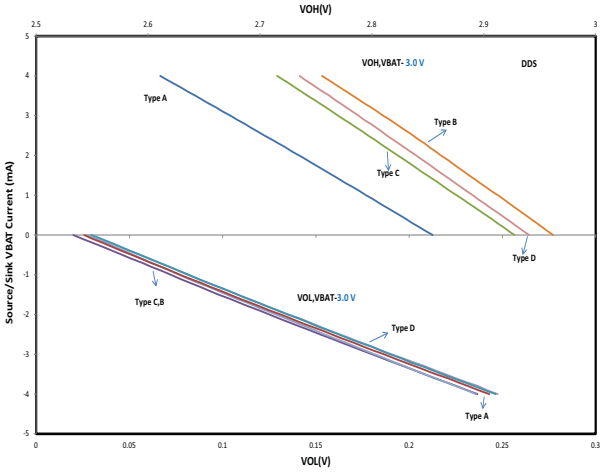


Figure 18. Output Double Drive Strength Characteristics (VBAT = 3.0 V)

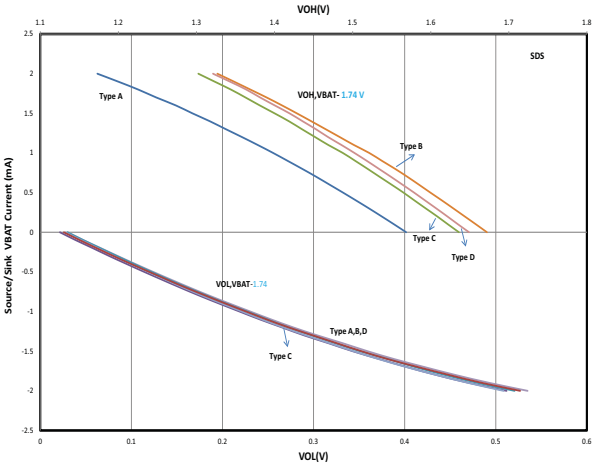


Figure 17. Output Single Drive Strength Characteristics (VBAT = 1.74 V)

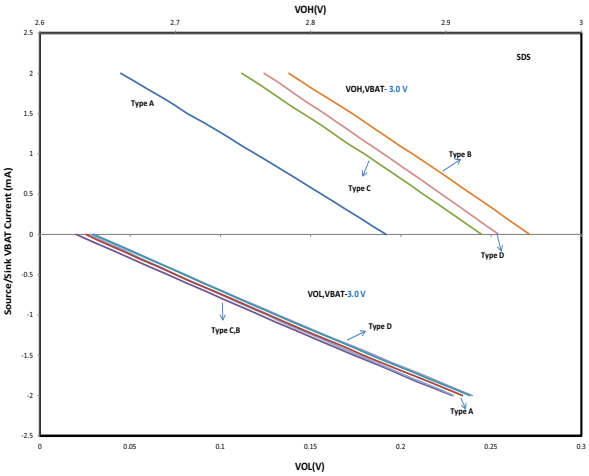


Figure 19. Output Single Drive Strength Characteristics (VBAT = 3.0 V)

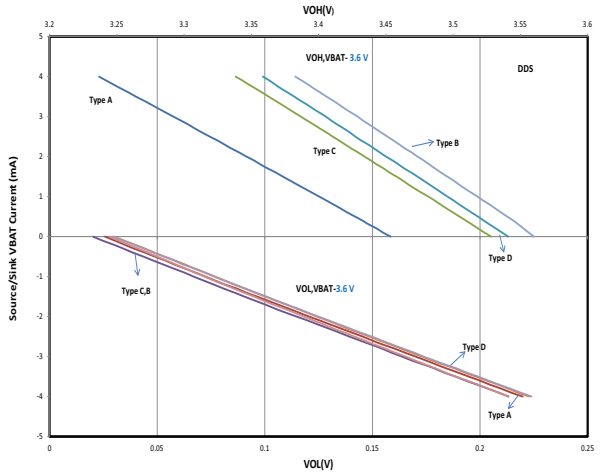


Figure 20. Output Double Drive Strength Characteristics (VBAT = 3.6 V)

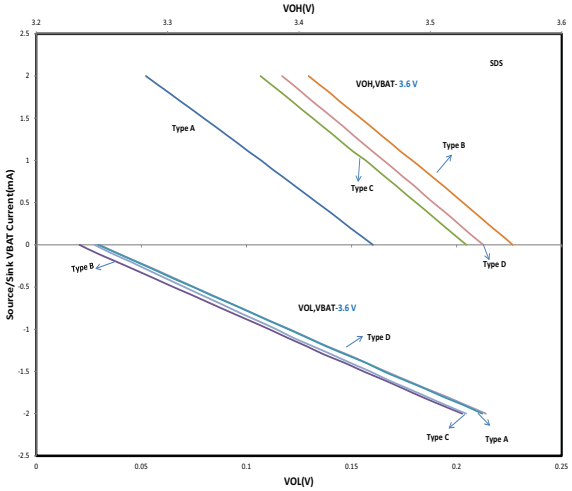


Figure 21. Output Single Drive Strength Characteristics (VBAT = 3.6 V)

ENVIRONMENTAL CONDITIONS

Table 23. Thermal Characteristics (64-Lead LFCSP)

Parameter	Typ	Unit
θ_{JA}	26.3	°C/W
θ_{JC}	1.0	°C/W

Values of θ_{JA} are provided for package comparison and printed circuit board (PCB) design considerations.
θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A is ambient temperature (°C).
T_J is junction temperature (°C).
P_D is power dissipation (to calculate P_D, see the Power Supply Current section.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Figure 22 shows an overview of signal placement on the 72-Ball WLCSP.

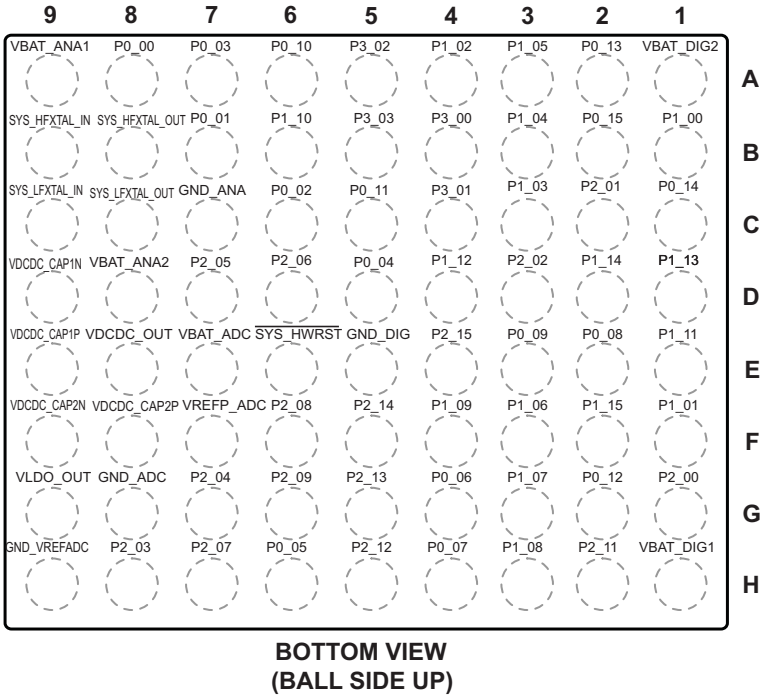


Figure 22. 72-Ball WLCSP Configuration

Table 24 lists the 72-Ball WLCSP package by ball number for the ADuCM4050 MCU.

Table 24. 72-Ball WLCSP Assignment (Numerical by Ball Number)

Ball No.	Signal	GPIO Pull	Ball No.	Signal	GPIO Pull	Ball No.	Signal	GPIO Pull
A1	VBAT_DIG2	Not applicable	C7	GND_ANA	Not applicable	F4	P1_09	Pull-up
A2	P0_13	Pull-up	C8	SYS_LFXTAL_OUT	Not applicable	F5	P2_14	Pull-up
A3	P1_05	Pull-up	C9	SYS_LFXTAL_IN	Not applicable	F6	P2_08	Pull-up
A4	P1_02	Pull-up	D1	P1_13	Pull-up	F7	VREFP_ADC	Not applicable
A5	P3_02	Pull-up	D2	P1_14	Pull-up	F8	VDCDC_CAP2P	Not applicable
A6	P0_10	Pull-up	D3	P2_02	Pull-up	F9	VDCDC_CAP2N	Not applicable
A7	P0_03	Pull-up	D4	P1_12	Pull-up	G1	P2_00	Pull-up
A8	P0_00	Pull-up	D5	P0_04	Pull-up	G2	P0_12	Pull-up
A9	VBAT_ANA1	Not applicable	D6	P2_06	Pull-up	G3	P1_07	Pull-up
B1	P1_00	Pull-up	D7	P2_05	Pull-up	G4	P0_06	Pull-down
B2	P0_15	Pull-up	D8	VBAT_ANA2	Not applicable	G5	P2_13	Pull-up
B3	P1_04	Pull-up	D9	VDCDC_CAP1N	Not applicable	G6	P2_09	Pull-up
B4	P3_00	Pull-up	E1	P1_11	Pull-up	G7	P2_04	Pull-up
B5	P3_03	Pull-up	E2	P0_08	Pull-up	G8	GND_ADC	Not applicable
B6	P1_10	Pull-up	E3	P0_09	Pull-up	G9	VLDO_OUT	Not applicable
B7	P0_01	Pull-up	E4	P2_15	Pull-up	H1	VBAT_DIG1	Not applicable
B8	SYS_HFXTAL_OUT	Not applicable	E5	GND_DIG	Not applicable	H2	P2_11	Pull-up
B9	SYS_HFXTAL_IN	Not applicable	E6	$\overline{\text{SYS\_HWRST}}$	Not applicable	H3	P1_08	Pull-up
C1	P0_14	Pull-up	E7	VBAT_ADC	Not applicable	H4	P0_07	Pull-up
C2	P2_01	Pull-up	E8	VDCDC_OUT	Not applicable	H5	P2_12	Pull-up
C3	P1_03	Pull-up	E9	VDCDC_CAP1P	Not applicable	H6	P0_05	Pull-up
C4	P3_01	Pull-up	F1	P1_01	Pull-up	H7	P2_07	Pull-up
C5	P0_11	Pull-up	F2	P1_15	Pull-up	H8	P2_03	Pull-up
C6	P0_02	Pull-up	F3	P1_06	Pull-up	H9	GND_VREFADC	Not applicable

Figure 23 shows an overview of signal placement on the 64-Lead LFCSP_WQ.

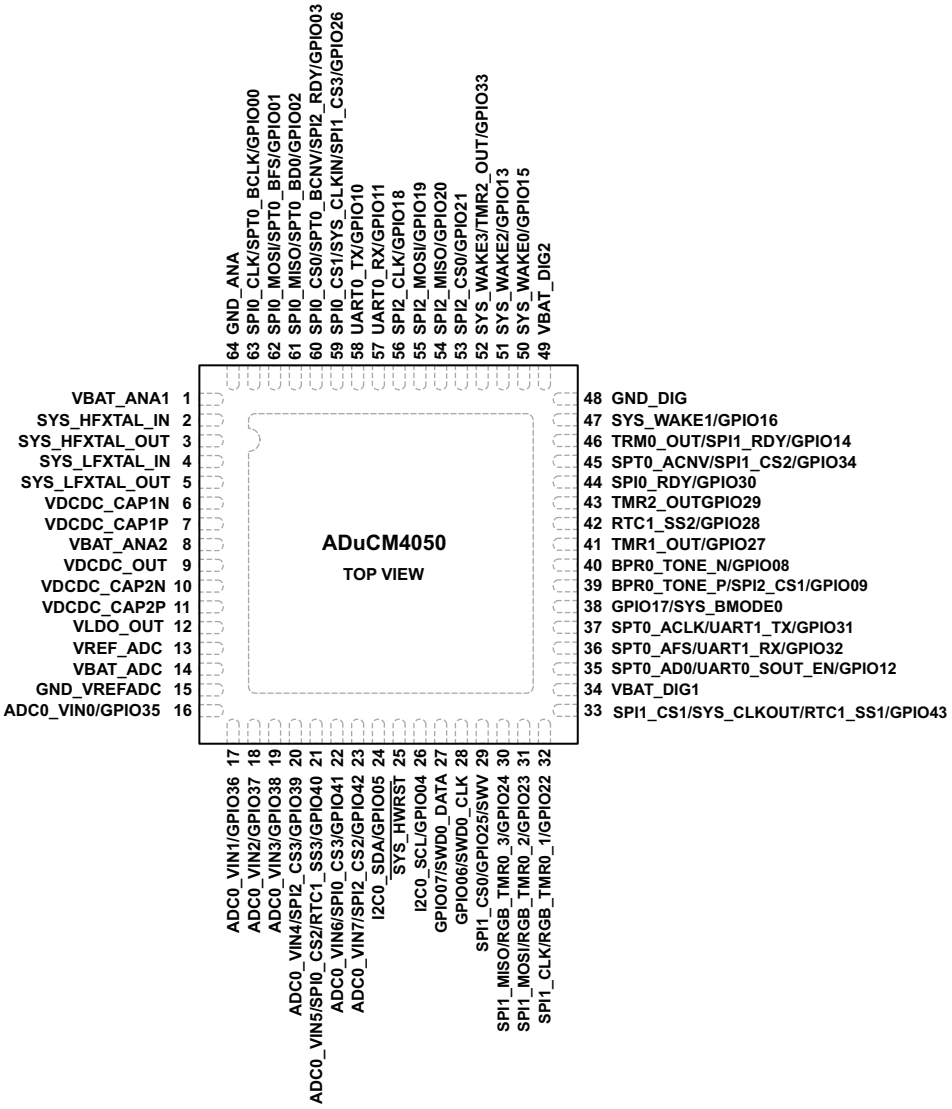


Figure 23. 64-Lead LFCSP Configuration

Table 25 lists the 64-Lead LFCSP package by lead number for the ADuCM4050 MCU.

Table 25. 64-Lead LFCSP Assignment (Numerical by Lead Number)

Lead No.	Signal	GPIO Pull	Lead No.	Signal	GPIO Pull	Lead No.	Signal	GPIO Pull
1	VBAT_ANA1	Not available	23	P2_10	Pull-up	45	P2_02	Pull-up
2	SYS_HFXTAL_IN	Not available	24	P0_05	Pull-up	46	P0_14	Pull-up
3	SYS_HFXTAL_OUT	Not available	25	$\overline{\text{SYS\_HWRST}}$	Not available	47	P1_00	Pull-up
4	SYS_LFXTAL_IN	Not available	26	P0_04	Pull-up	48	GND_DIG	Not available
5	SYS_LFXTAL_OUT	Not available	27	P0_07	Pull-up	49	VBAT_DIG2	Not available
6	VDCDC_CAP1N	Not available	28	P0_06	Pull-down	50	P0_15	Pull-up
7	VDCDC_CAP1P	Not available	29	P1_09	Pull-up	51	P0_13	Pull-up
8	VBAT_ANA2	Not available	30	P1_08	Pull-up	52	P2_01	Pull-up
9	VDCDC_OUT	Not available	31	P1_07	Pull-up	53	P1_05	Pull-up
10	VDCDC_CAP2N	Not available	32	P1_06	Pull-up	54	P1_04	Pull-up
11	VDCDC_CAP2P	Not available	33	P2_11	Pull-up	55	P1_03	Pull-up
12	VLDO_OUT	Not available	34	VBAT_DIG1	Not available	56	P1_02	Pull-up
13	VREFP_ADC	Not available	35	P0_12	Pull-up	57	P0_11	Pull-up
14	VBAT_ADC	Not available	36	P2_00	Pull-up	58	P0_10	Pull-up
15	GND_VREFADC	Not available	37	P1_15	Pull-up	59	P1_10	Pull-up
16	P2_03	Pull-up	38	P1_01	Pull-up	60	P0_03	Pull-up
17	P2_04	Pull-up	39	P0_09	Pull-up	61	P0_02	Pull-up
18	P2_05	Pull-up	40	P0_08	Pull-up	62	P0_01	Pull-up
19	P2_06	Pull-up	41	P1_11	Pull-up	63	P0_00	Pull-up
20	P2_07	Pull-up	42	P1_12	Pull-up	64	GND_ANA	Not available
21	P2_08	Pull-up	43	P1_13	Pull-up	Exposed Pad	GND	Not available
22	P2_09	Pull-up	44	P1_14	Pull-up			

Table 26 lists the signal descriptions of the ADuCM4050 MCU.

Table 26. Signal Functional Descriptions

GPIO Signal Name	Description
SPIn_CLK	SPI Clock. n= 0, 1, 2.
SPIn_MOSI	SPI Master Out Slave In. n= 0, 1, 2.
SPIn_MISO	SPI Master In Slave Out. n= 0, 1, 2.
SPIn_RDY	SPI Ready Signal. n= 0, 1, 2.
SPIn_CSm	SPI Chip Select Signal. n= 0, 1, 2 and m= 0, 1, 2, 3.
SPT0_ACLK	SPORT A Clock Signal.
SPT0_AFS	SPORT A Frame Sync.
SPT0_AD0	SPORT A Data Pin 0.
SPT0_ACNV	SPORT A Converter Signal for Interface with ADC.
SPT0_BCLK	SPORT B Clock Signal.
SPT0_BFS	SPORT B Frame Sync.
SPT0_BD0	SPORT B Data Pin 0.
SPT0_BCNV	SPORT B Converter Signal for Interface with ADC.
I2C0_SCL	I^2C Clock.
I2C0_SDA	I^2C Data.
SWD0_CLK	Serial Wire Debug Clock.
SWD0_DATA	Serial Wire Debug Data.
BPR0_TONE_N	Beeper Tone Negative Pin.
BPR0_TONE_P	Beeper Tone Positive Pin.
UARTn_TX	UART Transmit Pin. n= 0, 1.
UARTn_RX	UART Receive Pin. n= 0, 1.
UART0_SOUT_EN	UART Serial Data Out Pin.
SYS_WAKEn	System Wake-Up Pin. Wake Up from Flexi/Hibernate/Shutdown Modes[1]. n= 0, 1, 2, 3.
TMRn_OUT	Timer Output Pin. n= 0, 1, 2.
RGB_TMR0_n	RGB Timer Pin. n= 1, 2, 3.
SYS_BMODE0	Boot Mode Pin.
SYS_CLKIN	External Clock In Pin.
SYS_CLKOUT	External Clock Out Pin.
SWV	Serial Wire Viewer.
RTC1_SSn	RTC1 SensorStrobe Pin. n= 1, 2, 3, 4.
ADC0_VINn	ADC Voltage Input Pin. n= 0, 1, 2, 3, 4, 5, 6, 7.

[1] For shutdown, SYS_WAKE3 is not capable of waking the device from shutdown mode.

GPIO MULTIPLEXING

Table 27. Signal Multiplexing for PORT 0

Signal	Availability		Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
	WLCSP	LFCSP				
P0_00	Yes	Yes	GPIO00	SPI0_CLK	SPT0_BCLK	Not applicable
P0_01	Yes	Yes	GPIO01	SPI0_MOSI	SPT0_BFS	Not applicable
P0_02	Yes	Yes	GPIO02	SPI0_MISO	SPT0_BD0	Not applicable
P0_03	Yes	Yes	GPIO03	SPI0_CS0	SPT0_BCNV	SPI2_RDY
P0_04	Yes	Yes	GPIO04	I2C0_SCL	Not applicable	Not applicable
P0_05	Yes	Yes	GPIO05	I2C0_SDA	Not applicable	Not applicable
P0_06	Yes	Yes	SWD0_CLK	GPIO06	Not applicable	Not applicable
P0_07	Yes	Yes	SWD0_DATA	GPIO07	Not applicable	Not applicable
P0_08	Yes	Yes	GPIO08	BPR0_TONE_N	Not applicable	Not applicable
P0_09	Yes	Yes	GPIO09	BPR0_TONE_P	SPI2_CS1	Not applicable
P0_10	Yes	Yes	GPIO10	UART0_TX	Not applicable	Not applicable
P0_11	Yes	Yes	GPIO11	UART0_RX	Not applicable	Not applicable
P0_12	Yes	Yes	GPIO12	SPT0_AD0	Not applicable	UART0_SOUT_EN
P0_13	Yes	Yes	GPIO13	SYS_WAKE2	Not applicable	Not applicable
P0_14	Yes	Yes	GPIO14	TMR0_OUT	SPI1_RDY	Not applicable
P0_15	Yes	Yes	GPIO15	SYS_WAKE0	Not applicable	Not applicable

Table 28. Signal Multiplexing for PORT 1

Signal	Availability		Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
	WLCSP	LFCSP				
P1_00	Yes	Yes	GPIO16	SYS_WAKE1	Not applicable	Not applicable
P1_01	Yes	Yes	SYS_BMODE0	GPIO17	Not applicable	Not applicable
P1_02	Yes	Yes	GPIO18	SPI2_CLK	Not applicable	Not applicable
P1_03	Yes	Yes	GPIO19	SPI2_MOSI	Not applicable	Not applicable
P1_04	Yes	Yes	GPIO20	SPI2_MISO	Not applicable	Not applicable
P1_05	Yes	Yes	GPIO21	SPI2_CS0	Not applicable	Not applicable
P1_06	Yes	Yes	GPIO22	SPI1_CLK	Not applicable	RGB_TMR0_1
P1_07	Yes	Yes	GPIO23	SPI1_MOSI	Not applicable	RGB_TMR0_2
P1_08	Yes	Yes	GPIO24	SPI1_MISO	Not applicable	RGB_TMR0_3
P1_09	Yes	Yes	GPIO25	SPI1_CS0	Not applicable	SWV
P1_10	Yes	Yes	GPIO26	SPI0_CS1	SYS_CLKIN	SPI1_CS3
P1_11	Yes	Yes	GPIO27	Not applicable	TMR1_OUT	Not applicable
P1_12	Yes	Yes	GPIO28	Not applicable	RTC1_SS2	Not applicable
P1_13	Yes	Yes	GPIO29	TMR2_OUT	Not applicable	Not applicable
P1_14	Yes	Yes	GPIO30	Not applicable	SPI0_RDY	Not applicable
P1_15	Yes	Yes	GPIO31	SPT0_ACLK	UART1_TX	Not applicable

Table 29. Signal Multiplexing for PORT 2

Signal	Availability		Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
	WLCSP	LFCSP				
P2_00	Yes	Yes	GPIO32	SPT0_AFS	UART1_RX	Not applicable
P2_01	Yes	Yes	GPIO33	SYS_WAKE3	TMR2_OUT	Not applicable
P2_02	Yes	Yes	GPIO34	SPT0_ACNV	SPI1_CS2	Not applicable
P2_03	Yes	Yes	GPIO35	ADC0_VIN0	Not applicable	Not applicable
P2_04	Yes	Yes	GPIO36	ADC0_VIN1	Not applicable	Not applicable
P2_05	Yes	Yes	GPIO37	ADC0_VIN2	Not applicable	Not applicable
P2_06	Yes	Yes	GPIO38	ADC0_VIN3	Not applicable	Not applicable
P2_07	Yes	Yes	GPIO39	ADC0_VIN4	SPI2_CS3	Not applicable
P2_08	Yes	Yes	GPIO40	ADC0_VIN5	SPI0_CS2	RTC1_SS3
P2_09	Yes	Yes	GPIO41	ADC0_VIN6	SPI0_CS3	Not applicable
P2_10	No	Yes	GPIO42	ADC0_VIN7	SPI2_CS2	Not applicable
P2_11	Yes	Yes	GPIO43	SPI1_CS1	SYS_CLKOUT	RTC1_SS1
P2_12	Yes	No	GPIO44	UART1_TX	SPI2_CS3	Not applicable
P2_13	Yes	No	GPIO45	UART1_RX	SPI0_CS2	Not applicable
P2_14	Yes	No	GPIO46	SPI0_CS3	Not applicable	Not applicable
P2_15	Yes	No	GPIO47	SPI2_CS2	SPI1_CS3	SPI0_CS1

Table 30. Signal Multiplexing for PORT 3

Signal	Availability		Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
	WLCSP	LFCSP				
P3_00	Yes	No	GPIO48	RGB_TMR0_1	SPT0_ACLK	Not applicable
P3_01	Yes	No	GPIO49	RGB_TMR0_2	SPT0_AFS	Not applicable
P3_02	Yes	No	GPIO50	RGB_TMR0_3	SPT0_AD0	Not applicable
P3_03	Yes	No	GPIO51	RTC1_SS4	SPT0_ACNV	Not applicable

OUTLINE DIMENSIONS

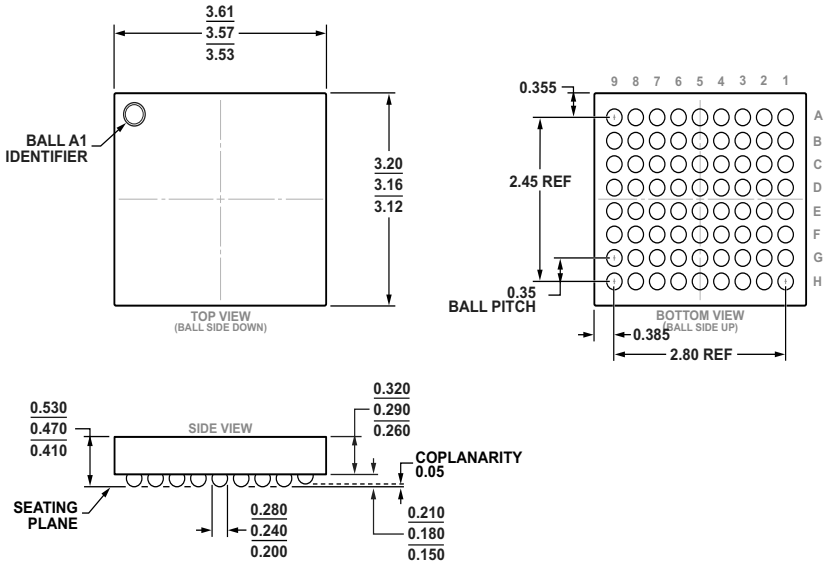


Figure 24. 72-Ball Wafer Level Chip Scale Package (WLCSP)
(CB-72-3)
Dimensions shown in mm

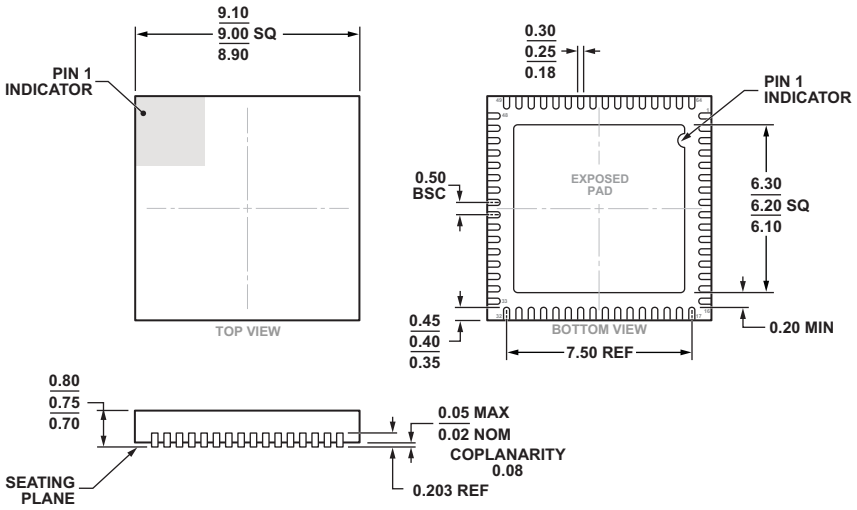


Figure 25. 64-Lead Frame Chip Scale Package (LFCSP)
9 mm x 9 mm Body, Very Thin Quad
(CP-64-17)
Dimensions shown in mm
Note: Exposed pad must be grounded

FUTURE (PLANNED) PRODUCTS

Model[1]	Description	Temperature[2, 3]	Package Description	Package Option
ADuCM4050BCPZ-U1	ULP ARM Cortex-M4F with 512 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP	CP-64-17
ADuCM4050BCBZ-U1	ULP ARM Cortex-M4F with 512 KB Embedded Flash	−40°C to +85°C	72-Ball WLCSP	CB-72-3
ADZS-U4050LF-EZKIT	ADuCM4050 LFCSP Evaluation Kit	−40°C to +85°C	64-Lead LFCSP	CP-64-17
ADZS-U4050WL-EZKIT	ADuCM4050 WLCSP Evaluation Kit	−40°C to +85°C	72-Ball WLCSP	CB-72-3

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See the Absolute Maximum Ratings section for T_J (junction temperature) specification which is the only temperature specification.
[3] These are preproduction devices. See U1-Grade agreement for details.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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